Lab5 Bonus Bubble Sort

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一、 目標

用演算法 bubble sort 的原理對 data 進行排序，須注意的有下列 3 點：

i. 由小排到大。

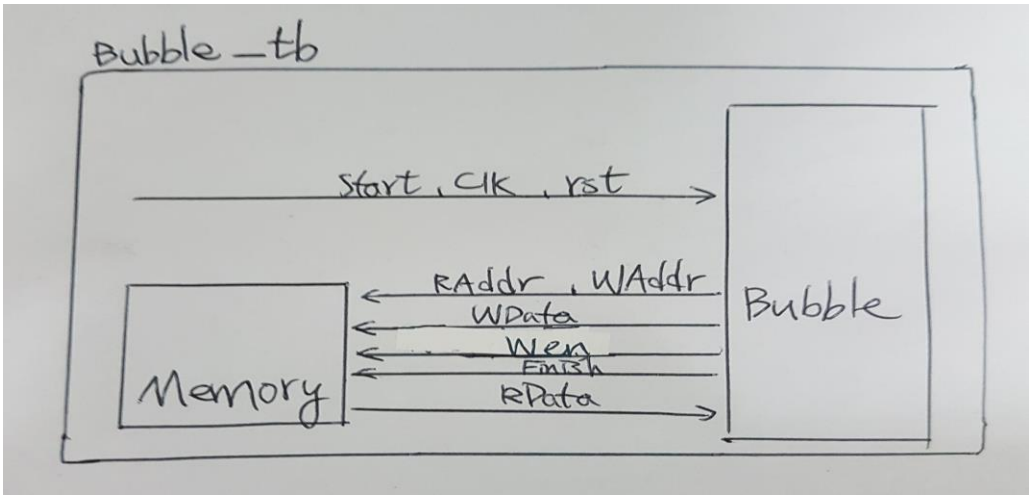
ii. 每完成一個循環，最後一個 data 都會固定下來，不必再考慮。

iii. 若已經排好了可以提前結束。

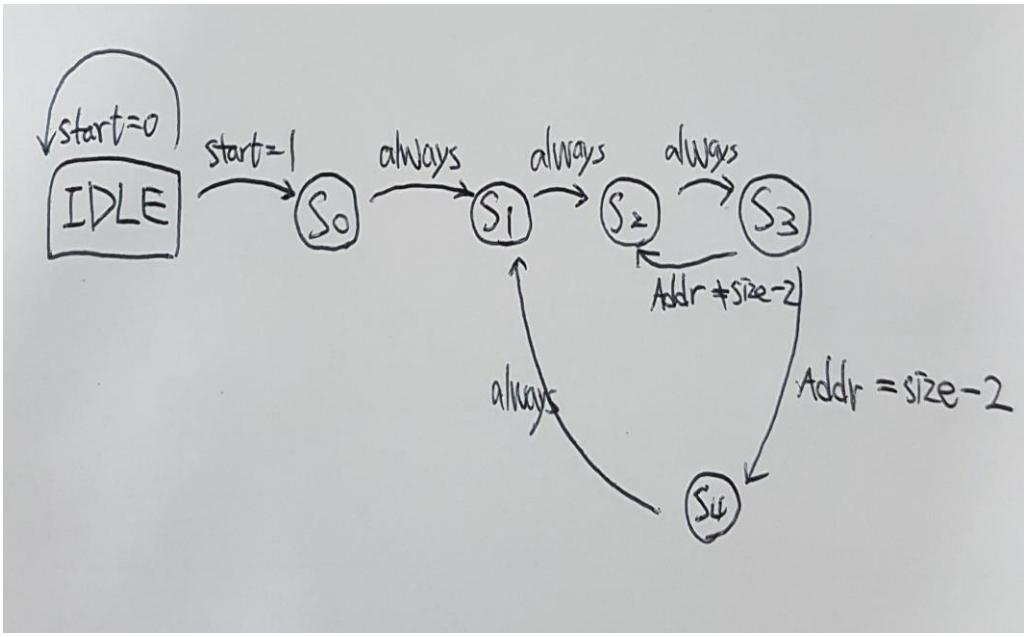
有了以上的觀念，設計出來的 Bubble Sort 我覺得蠻有效率的。

二、 設計

Bubble sort 電路、Testbench、Memory(RAM)的關係如下：



State Transition Graph:

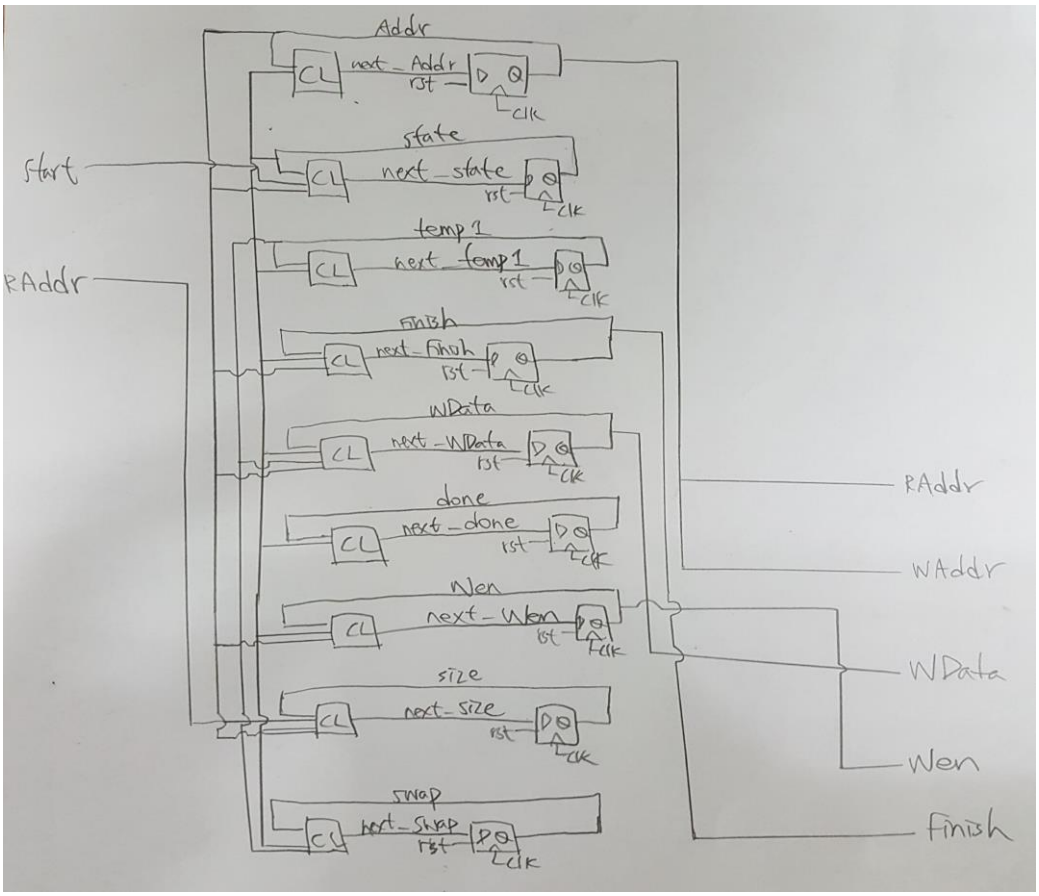


註解：

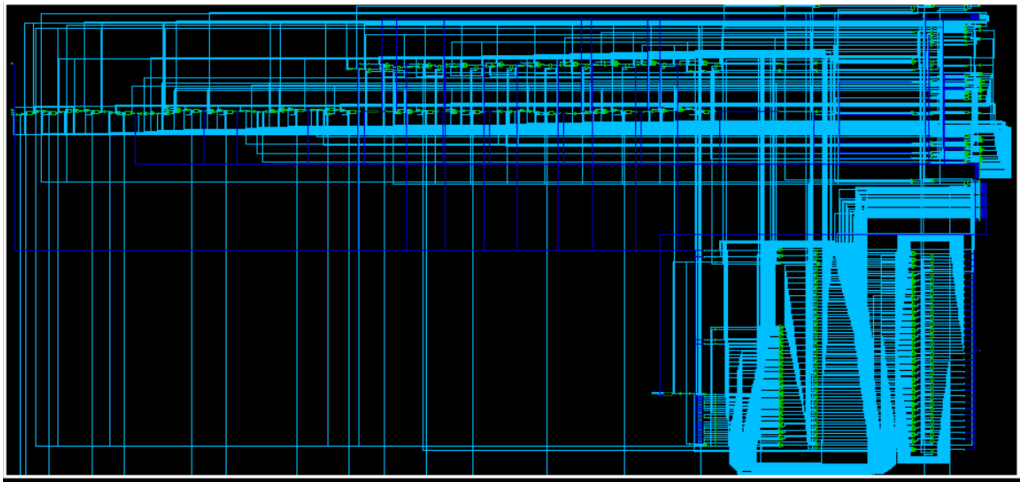
s0、s1 為準備階段，主要處理 s2 時所要用到的其中一個值 temp1，接著在 s2 可以得到兩個值(temp1、temp2)，並比大小。

s3 是寫值的階段，寫完繼續回去 s2 比大小；若是一個循環的最後，則進入 s4 寫入最後一個 data，接著回到 s1 開始新的循環。

Block Diagram:



Dv 模擬電路：



Make sim1: (結果為 Congratulations All PASS !!!)

```
[dld0026@ic26 ~/temp]$ make sim1
rm -rf *.log INCA_libs
ncverilog header.v Bubble.v Bubble_tb.v +define+TEST1 +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
file: header.v
file: Bubble.v
        module worklib.Bubble:v
                errors: 0, warnings: 0
file: Bubble_tb.v
        module worklib.Bubble_tb:v
                errors: 0, warnings: 0
        module worklib.SRAM:v
                errors: 0, warnings: 0
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Building instance overlay tables: ..................... Done
        Generating native compiled code:
                worklib.Bubble:v <0x2e6db472>
                        streams:   5, words:  6230
                worklib.Bubble_tb:v <0x340cd727>
                        streams:   6, words:  5779
                worklib.SRAM:v <0x1da8622b>
                        streams:   4, words:  1155
        Building instance specific data structures.
        Loading native compiled code:     ..................... Done
        Design hierarchy summary:
                                Instances  Unique
                Modules:                3       3
                Registers:             31      31
                Scalar wires:           6       -
                Vectored wires:         4       -
                Always blocks:          6       6
                Initial blocks:         5       5
                Pseudo assignments:     1       1
                Simulation timescale:  100ps
        Writing initial simulation snapshot: worklib.Bubble_tb:v
Loading snapshot worklib.Bubble_tb:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may
crash the programs that are using this file.
*Verdi3* : Create FSDB file 'Bubble.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.

Congratulations All PASS !!!


Simulation complete via $finish(1) at time 756 NS + 3
./Bubble_tb.v:123               $finish;
ncsim> exit
```

Make sim2: (結果為 Congratulations All PASS !!!)

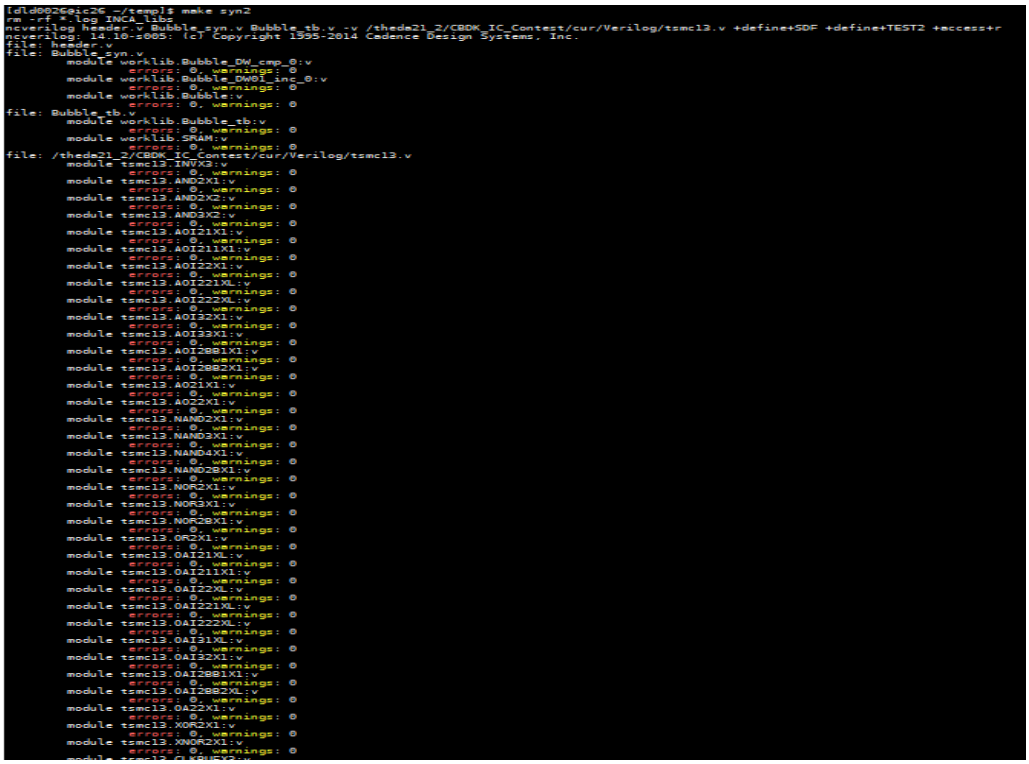
```
[dld0026@ic26 ~/temp]$ make sim2
rm -rf *.log INCA_libs
ncverilog header.v Bubble.v Bubble_tb.v +define+TEST2 +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
file: header.v
file: Bubble.v
        module worklib.Bubble:v
                errors: 0, warnings: 0
file: Bubble_tb.v
        module worklib.Bubble_tb:v
                errors: 0, warnings: 0
        module worklib.SRAM:v
                errors: 0, warnings: 0
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
        Building instance overlay tables: ..................... Done
        Generating native compiled code:
                worklib.Bubble:v <0x2e6db472>
                        streams:   5, words:  6230
                worklib.Bubble_tb:v <0x340cd727>
                        streams:   6, words:  5779
                worklib.SRAM:v <0x1da8622b>
                        streams:   4, words:  1155
        Building instance specific data structures.
        Loading native compiled code:     ..................... Done
        Design hierarchy summary:
                                Instances  Unique
                Modules:                3       3
                Registers:             31      31
                Scalar wires:           6       -
                Vectored wires:         4       -
                Always blocks:          6       6
                Initial blocks:         5       5
                Pseudo assignments:     1       1
                Simulation timescale:  100ps
        Writing initial simulation snapshot: worklib.Bubble_tb:v
Loading snapshot worklib.Bubble_tb:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi3* : Create FSDB file 'Bubble.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.

Congratulations All PASS !!!


Simulation complete via $finish(1) at time 3348 NS + 3
./Bubble_tb.v:123               $finish;
ncsim> exit
```

Make syn1: (結果為 Congratulations All PASS !!!)

```
Simulation complete via $finish(1) at time 3348 NS + 3
./Bubble_tb.v:123              $finish;
ncsim> exit
[dld0026@ic26 ~/temp]$ make syn1
rm -rf *.log INCA_libs
ncverilog header.v Bubble_syn.v Bubble_tb.v -v /theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v +define+SDF +define+TEST1 +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
file: header.v
file: Bubble_syn.v
        module worklib.Bubble_DW_cmp_0:v
                errors: 0, warnings: 0
        module worklib.Bubble_DW01_inc_0:v
                errors: 0, warnings: 0
        module worklib.Bubble:v
                errors: 0, warnings: 0
file: Bubble_tb.v
        module worklib.Bubble_tb:v
                errors: 0, warnings: 0
        module worklib.SRAM:v
                errors: 0, warnings: 0
file: /theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v
        module tsmc13.INVX3:v
                errors: 0, warnings: 0
        module tsmc13.AND2X1:v
                errors: 0, warnings: 0
        module tsmc13.AND2X2:v
                errors: 0, warnings: 0
        module tsmc13.AND3X2:v
                errors: 0, warnings: 0
        module tsmc13.AOI21X1:v
                errors: 0, warnings: 0
        module tsmc13.AOI211X1:v
                errors: 0, warnings: 0
        module tsmc13.AOI22X1:v
                errors: 0, warnings: 0
        module tsmc13.AOI221XL:v
                errors: 0, warnings: 0
        module tsmc13.AOI222XL:v
                errors: 0, warnings: 0
        module tsmc13.AOI32X1:v
                errors: 0, warnings: 0
        module tsmc13.AOI33X1:v
                errors: 0, warnings: 0
        module tsmc13.AOI2BB1X1:v
                errors: 0, warnings: 0
        module tsmc13.AOI2BB2X1:v
                errors: 0, warnings: 0
        module tsmc13.AO21X1:v
                errors: 0, warnings: 0
        module tsmc13.AO22X1:v
                errors: 0, warnings: 0
        module tsmc13.NAND2X1:v
                errors: 0, warnings: 0
        module tsmc13.NAND3X1:v
                errors: 0, warnings: 0
        module tsmc13.NAND4X1:v
                errors: 0, warnings: 0
        module tsmc13.NAND2BX1:v
                errors: 0, warnings: 0
        module tsmc13.NOR2X1:v
                errors: 0, warnings: 0
        module tsmc13.NOR3X1:v
                errors: 0, warnings: 0
```

```
                errors: 0, warnings: 0
        module tsmc13.XNOR2X1:v
                errors: 0, warnings: 0
        module tsmc13.CLKBUFX3:v
                errors: 0, warnings: 0
        module tsmc13.CLKINVX1:v
                errors: 0, warnings: 0
        module tsmc13.ADDHXL:v
                errors: 0, warnings: 0
        module tsmc13.DFFRX1:v
                errors: 0, warnings: 0
        module tsmc13.DFFNSRX1:v
                errors: 0, warnings: 0
        primitive tsmc13.udp_dff:v
                errors: 0, warnings: 0
                Caching library 'tsmc13' ....... Done
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
 Bubble_DW_cmp_0 P338 (  .A(temp1), .B(RData), .TC(1'b1), .GE_LT(1'b0),
                         |
ncelab: *W,CUVWSP (./Bubble_syn.v,223|21): 1 output port was not connected:
ncelab: (./Bubble_syn.v,8): EQ_NE

  DFFNSRX1 \state_reg[1]  (  .D(next_state[1]), .CKN(clk), .SN(1'b1), .RN(n397),
                             |
ncelab: *W,CUVWSP (./Bubble_syn.v,391|24): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,19089): QN

        Reading SDF file from location "./Bubble.sdf"
        Annotating SDF timing data:
                Compiled SDF file:     Bubble.sdf.X
                Log file:
                Backannotation scope:  Bubble_tb.bubble
                Configuration file:
                MTM control:
                Scale factors:
                Scale type:
        Annotation completed successfully...
        SDF statistics: No. of Pathdelays = 1680  Annotated = 100.00% -- No. of Tchecks = 875  Annotated = 94.06%
                                        Total       Annotated      Percentage
                 Path Delays             1680            1680          100.00
                      $hold                26               0            0.00
                      $width              283             283          100.00
                   $setuphold             566             540           95.41
        Building instance overlay tables: ..................... Done
        Generating native compiled code:
                tsmc13.ADDHXL:v <0x0b9e90ed>
                        streams:   4, words:   284
                tsmc13.DFFNSRX1:v <0x3cb6d561>
                        streams:   2, words:   106
                tsmc13.DFFRX1:v <0x5dd5b074>
                        streams:   2, words:   106
                tsmc13.XNOR2X1:v <0x2c701b77>
                        streams:   4, words:   284
                tsmc13.XOR2X1:v <0x7c0db446>
                        streams:   4, words:   284
                worklib.Bubble:v <0x490b4eee>
                        streams:   1, words:   186
                worklib.Bubble_tb:v <0x025459b3d>
                        streams:   6, words:  5853
                worklib.SRAM:v <0x5ed76762>
                        streams:   4, words:  1345
        Building instance specific data structures.
        Loading native compiled code:     ..................... Done
        Design hierarchy summary:
                                 Instances  Unique
                Modules:               566      45
                UDPs:                   90       1
                Primitives:           1226       8
                Timing outputs:        599      19
                Registers:             100      13
                Scalar wires:          724       -
                Expanded wires:         32       1
                Always blocks:           3       3
                Initial blocks:          5       5
                Cont. assignments:       1      11
                Pseudo assignments:      1       1
                Timing checks:         875     104
                Interconnect:         1434       -
                Delayed tcheck signals:  283      85
                Simulation timescale:    1ps
        Writing initial simulation snapshot: worklib.Bubble_tb:v
Loading snapshot worklib.Bubble_tb:v ..................... Done
Verdi3* Loading libsscore_ius141.so
Verdi3* : Enable Parallel Dumping ...
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
Verdi3* : Create FSDB file 'Bubble_syn.fsdb'
Verdi3* : Begin traversing the scopes, layer (0).
Verdi3* : End of traversing.

Congratulations All PASS !!!

Simulation complete via $finish(1) at time 756598 PS + 0
./Bubble_tb.v:123              $finish;
ncsim> exit
```

Make syn2: (結果為 Congratulations All PASS !!!)



```
[dld0026pic26 ~/temp]$ make syn2
rm -rf *.log INCA_libs
ncverilog header.v Bubble_syn.v Bubble_tb.v -v /theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v +define+SDF +define+TEST2 +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
file: header.v
file: Bubble_syn.v
        module worklib.Bubble_DW_cmp_0:v
                errors: 0, warnings: 0
        module worklib.Bubble_DW01_inc_0:v
                errors: 0, warnings: 0
        module worklib.Bubble:v
                errors: 0, warnings: 0
file: Bubble_tb.v
        module worklib.Bubble_tb:v
                errors: 0, warnings: 0
        module worklib.SRAM:v
                errors: 0, warnings: 0
file: /theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v
        module tsmc13.INVX3:v
                errors: 0, warnings: 0
        module tsmc13.AND2X1:v
                errors: 0, warnings: 0
        module tsmc13.AND2X2:v
                errors: 0, warnings: 0
        module tsmc13.AND3X2:v
                errors: 0, warnings: 0
        module tsmc13.AOI21X1:v
                errors: 0, warnings: 0
        module tsmc13.AOI211X1:v
                errors: 0, warnings: 0
        module tsmc13.AOI22X1:v
                errors: 0, warnings: 0
        module tsmc13.AOI221XL:v
                errors: 0, warnings: 0
        module tsmc13.AOI222XL:v
                errors: 0, warnings: 0
        module tsmc13.AOI32X1:v
                errors: 0, warnings: 0
        module tsmc13.AOI33X1:v
                errors: 0, warnings: 0
        module tsmc13.AOI2BB1X1:v
                errors: 0, warnings: 0
        module tsmc13.AOI2BB2X1:v
                errors: 0, warnings: 0
        module tsmc13.AO21X1:v
                errors: 0, warnings: 0
        module tsmc13.AO22X1:v
                errors: 0, warnings: 0
        module tsmc13.NAND2X1:v
                errors: 0, warnings: 0
        module tsmc13.NAND3X1:v
                errors: 0, warnings: 0
        module tsmc13.NAND4X1:v
                errors: 0, warnings: 0
        module tsmc13.NAND2BX1:v
                errors: 0, warnings: 0
        module tsmc13.NOR2X1:v
                errors: 0, warnings: 0
        module tsmc13.NOR3X1:v
                errors: 0, warnings: 0
        module tsmc13.NOR2BX1:v
                errors: 0, warnings: 0
        module tsmc13.OR2X1:v
                errors: 0, warnings: 0
        module tsmc13.OAI21XL:v
                errors: 0, warnings: 0
        module tsmc13.OAI211X1:v
                errors: 0, warnings: 0
        module tsmc13.OAI22XL:v
                errors: 0, warnings: 0
        module tsmc13.OAI221XL:v
                errors: 0, warnings: 0
        module tsmc13.OAI222XL:v
                errors: 0, warnings: 0
        module tsmc13.OAI31XL:v
                errors: 0, warnings: 0
        module tsmc13.OAI32X1:v
                errors: 0, warnings: 0
        module tsmc13.OAI2BB1X1:v
                errors: 0, warnings: 0
        module tsmc13.OAI2BB2XL:v
                errors: 0, warnings: 0
        module tsmc13.OA22X1:v
                errors: 0, warnings: 0
        module tsmc13.XOR2X1:v
                errors: 0, warnings: 0
        module tsmc13.XNOR2X1:v
                errors: 0, warnings: 0
        module tsmc13.CLKBUFX3:v
                errors: 0, warnings: 0
        module tsmc13.CLKINVX1:v
                errors: 0, warnings: 0
        module tsmc13.ADDHXL:v
                errors: 0, warnings: 0
        module tsmc13.DFFRX1:v
                errors: 0, warnings: 0
        module tsmc13.DFFNSRX1:v
                errors: 0, warnings: 0
        primitive tsmc13.udp_dff:v
                errors: 0, warnings: 0
                Caching library 'tsmc13' ....... Done
                Caching library 'worklib' ....... Done
        Elaborating the design hierarchy:
  Bubble_DW_cmp_0 r338 ( .A(temp1), .B(RData), .TC(1'b1), .GE_LT(1'b0),
                         |
ncelab: *W,CUVWSP (./Bubble_syn.v,223|21): 1 output port was not connected:
ncelab: (./Bubble_syn.v,8): EQ_NE

  DFFNSRX1 \state_reg[1]  ( .D(next_state[1]), .CKN(clk), .SN(1'b1), .RN(n397),
                            |
ncelab: *W,CUVWSP (./Bubble_syn.v,391|24): 1 output port was not connected:
ncelab: (/theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v,19089): QN

        Reading SDF file from location "./Bubble.sdf"
        Annotating SDF timing data:
                Compiled SDF file:      Bubble.sdf.X
                Log file:
                Backannotation scope:   Bubble_tb.bubble
                Configuration file:
                MTM control:
                Scale factors:
                Scale type:
        Annotation completed successfully...
        SDF statistics: No. of Pathdelays = 1680  Annotated = 100.00% -- No. of Tchecks = 875  Annotated = 94.06%
                                        Total       Annotated      Percentage
                 Path Delays             1680            1680          100.00
                    $hold                  26               0            0.00
                  $width                  283             283          100.00
                $setuphold                566             540           95.41
        Building instance overlay tables: ..................... Done
        Generating native compiled code:
                tsmc13.ADDHXL:v <0x0b9e90ed>
                        streams:   4, words:   284
                tsmc13.DFFNSRX1:v <0x3cb6d561>
                        streams:   2, words:   106
                tsmc13.DFFRX1:v <0x5dd5b074>
                        streams:   2, words:   106
                tsmc13.XNOR2X1:v <0x2c701b77>
                        streams:   4, words:   284
                tsmc13.XOR2X1:v <0x7c0db446>
                        streams:   4, words:   284
                worklib.Bubble:v <0x490b4eae>
                        streams:   1, words:   186
                worklib.Bubble_tb:v <0x025459b3d>
                        streams:   6, words:  5853
                worklib.SRAM:v <0x5ed76762>
                        streams:   4, words:  1345
        Building instance specific data structures.
        Loading native compiled code:     ..................... Done
        Design hierarchy summary:
                                 Instances  Unique
                Modules:               506      45
                UDPs:                   90       1
                Primitives:           1226       8
                Timing outputs:        599      19
                Registers:             100      13
                Scalar wires:          724       -
                Expanded wires:         32       1
                Always blocks:           3       3
                Initial blocks:          5       5
                Cont. assignments:       1      11
                Pseudo assignments:      1       1
                Timing checks:         875     104
                Interconnect:         1434       -
                Delayed check signals:  283      85
                Simulation timescale:   1ps
        Writing initial simulation snapshot: worklib.Bubble_tb:v
Loading snapshot worklib.Bubble_tb:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP2, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi3* : Create FSDB file 'Bubble_syn.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.

Congratulations All PASS !!!


Simulation complete via $finish(1) at time 3348598 PS + 0
./Bubble_tb.v:123               $finish;
ncsim> exit
```

三、 問題與討論

1. 終於到最後一個 Lab 了，感謝助教一直以來的 carry，也感謝我的肝不離不棄。

2. Lab5 Bonus 的 RAM 是可以同時讀跟寫的嗎？還有它是給 Address 馬上可以讀寫嗎？ (問於 ilms)

(林柏淵, stalkerking7@gmail.com, 2018-06-10 13:21)

講解有說喔~可以同時讀寫

(吳紹齊, wsc861029@gmail.com, 2018-06-10 13:29)

那理論上可以WAddr跟RAddr為不同值嗎?
因為試了好像不行qq

(林楷宸, 1038790@gmail.com, 2018-06-10 14:33)

同學你好，
可以不同值喔，
我就是不同值的寫法，
你可能在注意一下你是不是有重複給值之類惡問題

By TA.

我這次實作的 RAddr、WAddr 都是設定成一樣，一起變化，經過助教的解釋發現或許不需要這樣，暑假會多嘗試不同方法提升效能。