

Lab5 Bonus Bubble Sort

105031212 吳紹齊

一、目標

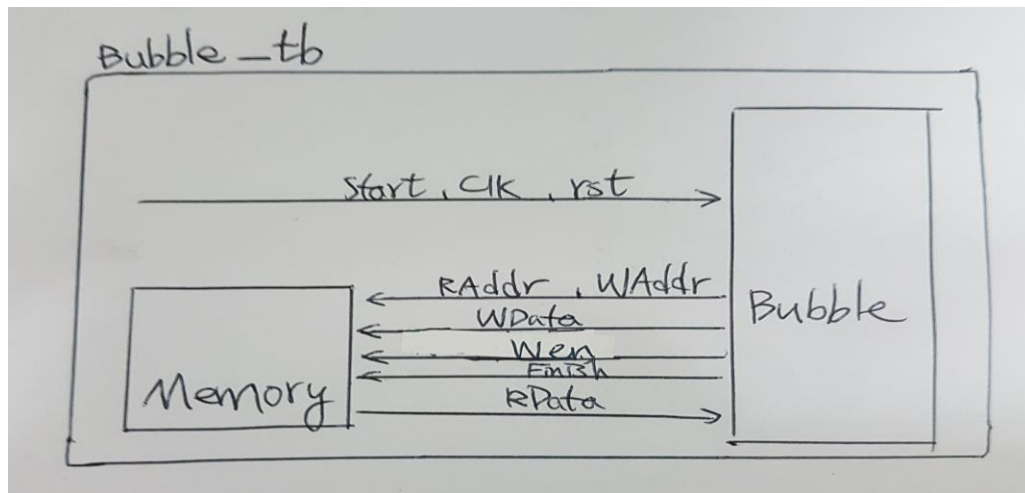
用演算法 bubble sort 的原理對 data 進行排序，須注意的有下列 3 點：

- 由小排到大。
- 每完成一個循環，最後一個 data 都會固定下來，不必再考慮。
- 若已經排好了可以提前結束。

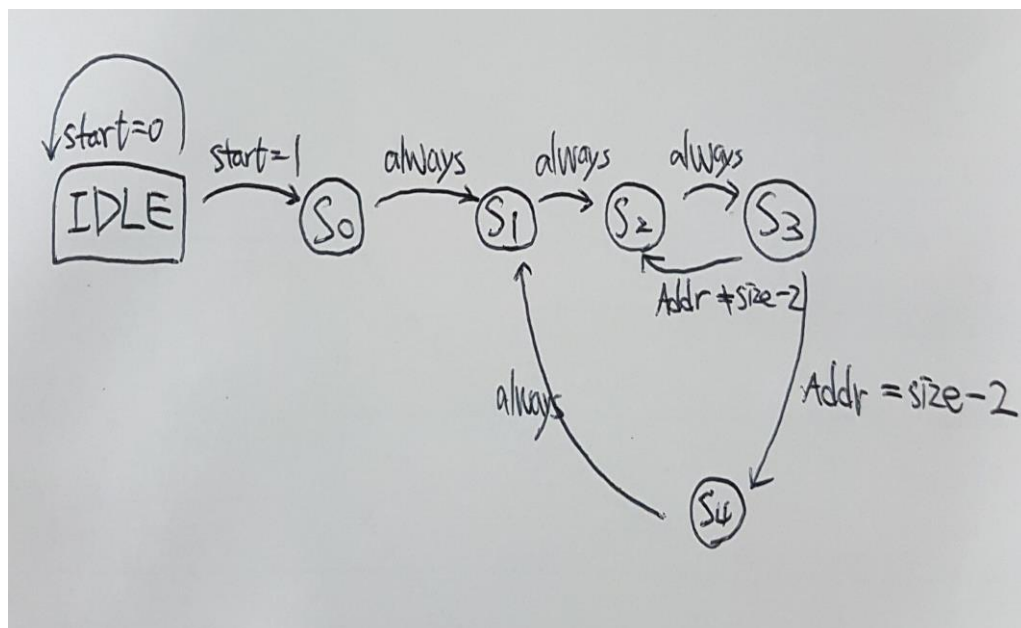
有了以上的觀念，設計出來的 Bubble Sort 我覺得蠻有效率的。

二、設計

Bubble sort 電路、Testbench、Memory(RAM)的關係如下：



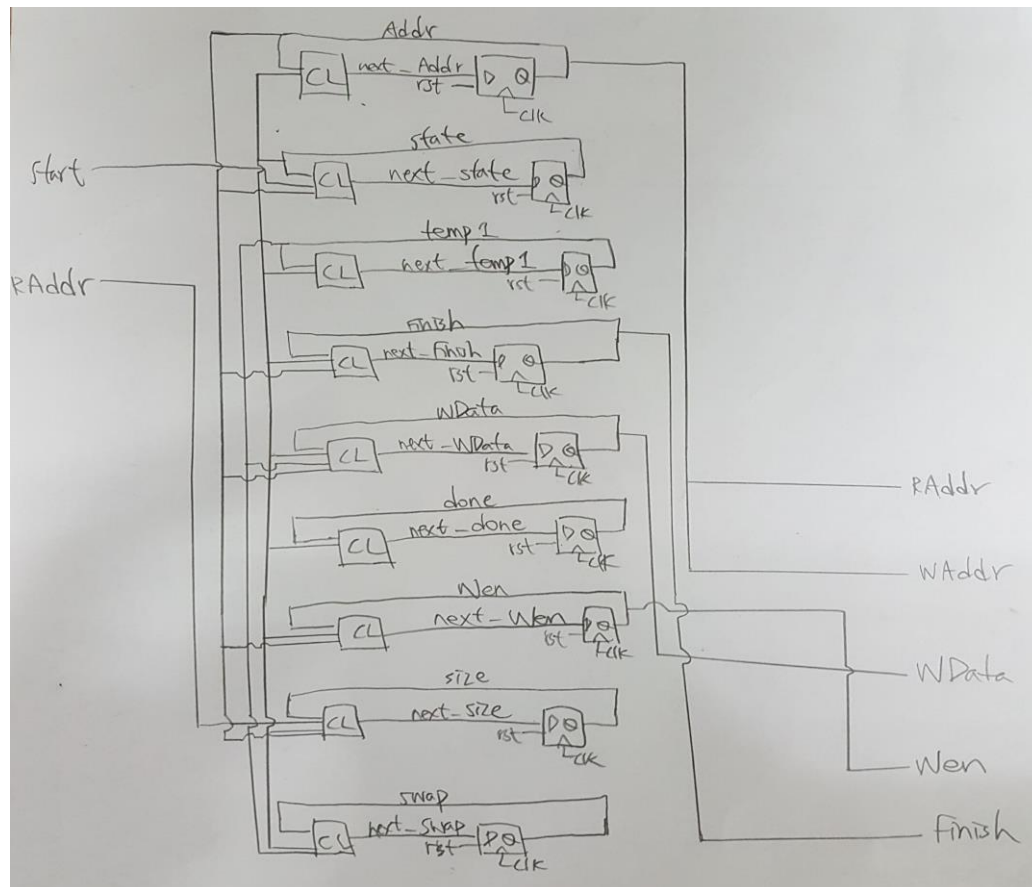
State Transition Graph:



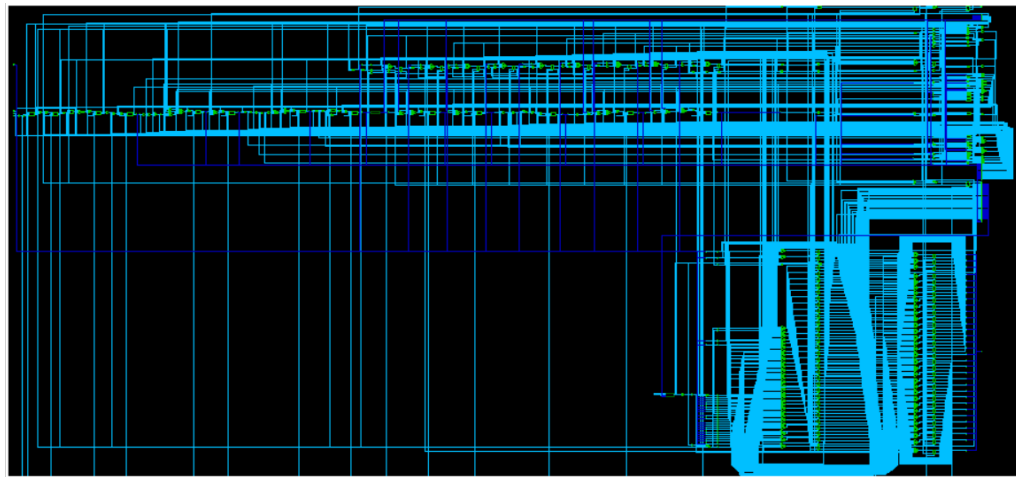
s0、s1 為準備階段，主要處理 s2 時所要用到的其中一個值 temp1，接著在 s2 可以得到兩個值(temp1、temp2)，並比大小。

s3 是寫值的階段，寫完繼續回去 s2 比大小；若是一個循環的最後，則進入 s4 寫入最後一個 data，接著回到 s1 開始新的循環。

Block Diagram:



Dv 模擬電路：



Make sim1: (結果為 Congratulations All PASS !!!)

```
[dld0026@ic26 ~/templ]$ make sim1
rm -rf *.log INCA_libs
ncverilog header.v Bubble.v Bubble_tb.v +define+TEST1 +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
file: header.v
file: Bubble.v
    module worklib.Bubble:v
        errors: 0, warnings: 0
file: Bubble_tb.v
    module worklib.Bubble_tb:v
        errors: 0, warnings: 0
    module worklib.SRAM:v
        errors: 0, warnings: 0
        Caching library 'worklib' ..... Done
    Elaborating the design hierarchy:
    Building instance overlay tables: ..... Done
    Generating native compiled code:
        worklib.Bubble:v <0x2e6db472>
            streams: 5, words: 6230
        worklib.Bubble_tb:v <0x340cd727>
            streams: 6, words: 5779
        worklib.SRAM:v <0x1da8622b>
            streams: 4, words: 1155
    Building instance specific data structures.
    Loading native compiled code: ..... Done
    Design hierarchy summary:
        Instances Unique
        Modules: 3 3
        Registers: 31 31
        Scalar wires: 6 -
        Vectored wires: 4 -
        Always blocks: 6 6
        Initial blocks: 5 5
        Pseudo assignments: 1 1
        Simulation timescale: 100ps
    Writing initial simulation snapshot: worklib.Bubble_tb:v
    Loading snapshot worklib.Bubble_tb:v ..... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may
crash the programs that are using this file.
*Verdi3* : Create FSDB file 'Bubble.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.
congratulations All PASS !!!

Simulation complete via $finish(1) at time 756 NS + 3
./Bubble_tb.v:123 $finish;
ncsim> exit
```

Make sim2: (結果為 Congratulations All PASS !!!)

```
[dld0026@ic26 ~/templ]$ make sim2
rm -rf *.log INCA_libs
ncverilog header.v Bubble_tb.v +define+TEST2 +access+r
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
file: header.v
file: Bubble.v
    module worklib.Bubble:v
        errors: 0, warnings: 0
file: Bubble_tb.v
    module worklib.Bubble_tb:v
        errors: 0, warnings: 0
    module worklib.SRAM:v
        errors: 0, warnings: 0
        Caching library 'worklib' ..... Done
    Elaborating the design hierarchy:
    Building instance overlay tables: ..... Done
    Generating native compiled code:
        worklib.Bubble:v <0x2e6db472>
            streams: 5, words: 6230
        worklib.Bubble_tb:v <0x340cd727>
            streams: 6, words: 5779
        worklib.SRAM:v <0x1da8622b>
            streams: 4, words: 1155
    Building instance specific data structures.
    Loading native compiled code: ..... Done
    Design hierarchy summary:
        Instances Unique
        Modules: 3 3
        Registers: 31 31
        Scalar wires: 6 -
        Vectored wires: 4 -
        Always blocks: 6 6
        Initial blocks: 5 5
        Pseudo assignments: 1 1
        Simulation timescale: 100ps
    Writing initial simulation snapshot: worklib.Bubble_tb:v
    Loading snapshot worklib.Bubble_tb:v ..... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi3* : Create FSDB file 'Bubble.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.
congratulations All PASS !!!

Simulation complete via $finish(1) at time 3348 NS + 3
./Bubble_tb.v:123 $finish;
ncsim> exit
```

Make syn1: (結果為 Congratulations All PASS !!!)

```
Simulation complete via $finish() at time 3348 NS + 3
./Bubble.tb.v:123 $finish:
ncsim> exit
[cd00202@mc26 ~/tmp]$ make synl
m -rf *.log INCA.libs
ncverilog header.V Bubble_syn.v Bubble_tb.v -v /theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v +define+SDF +define+TEST1 +access+fr
ncverilog: 14.10-s005: (c) Copyright 1995-2014 Cadence Design Systems, Inc.
file: header.v
file: Bubble_syn.v
module worklib.Bubble_DW_cmp_0:v
errors: 0, warnings: 0
module worklib.Bubble_DW01_inc_0:v
errors: 0, warnings: 0
module worklib.Bubble:v
errors: 0, warnings: 0
file: Bubble_tb.v
module worklib.Bubble_tb:v
errors: 0, warnings: 0
module worklib.SP4M:v
errors: 0, warnings: 0
file: /theda21_2/CBDK_IC_Contest/cur/Verilog/tsmc13.v
module tsmc13.INVX3:v
errors: 0, warnings: 0
module tsmc13.AND2X1:v
errors: 0, warnings: 0
module tsmc13.AND2X2:v
errors: 0, warnings: 0
module tsmc13.AND3X2:v
errors: 0, warnings: 0
module tsmc13.AOI21X1:v
errors: 0, warnings: 0
module tsmc13.AOI211X1:v
errors: 0, warnings: 0
module tsmc13.AOI22X1:v
errors: 0, warnings: 0
module tsmc13.AOI221X1:v
errors: 0, warnings: 0
module tsmc13.AOI222X1:v
errors: 0, warnings: 0
module tsmc13.AOI222X2:v
errors: 0, warnings: 0
module tsmc13.AOI32X1:v
errors: 0, warnings: 0
module tsmc13.AOI33X1:v
errors: 0, warnings: 0
module tsmc13.AOI28B3X1:v
errors: 0, warnings: 0
module tsmc13.AOI28B2X1:v
errors: 0, warnings: 0
module tsmc13.AOI21X1:v
errors: 0, warnings: 0
module tsmc13.AOI22X1:v
errors: 0, warnings: 0
module tsmc13.NAND2X1:v
errors: 0, warnings: 0
module tsmc13.NAND3X1:v
errors: 0, warnings: 0
module tsmc13.NAND4X1:v
errors: 0, warnings: 0
module tsmc13.NAND2BX1:v
errors: 0, warnings: 0
module tsmc13.NOR2X1:v
errors: 0, warnings: 0
module tsmc13.NOR3X1:v
errors: 0, warnings: 0
```

```

errors: 0, warnings: 0
module tsmc13_XNOR2X1.v
  errors: 0, warnings: 0
module tsmc13_CLKBUF2X3.v
  errors: 0, warnings: 0
module tsmc13_CLKBUF1X1.v
  errors: 0, warnings: 0
module tsmc13_ADD4X4.v
  errors: 0, warnings: 0
module tsmc13_DIFFRX1.v
  errors: 0, warnings: 0
module tsmc13_DIFFNSRX1.v
  errors: 0, warnings: 0
primitive tsmc12_udp_dff.v
  errors: 0, warnings: 0
  Caching library 'tsmc13' ..... Done
  Caching library 'worklib' ..... Done
Elaborating the design hierarchy:
Bubble_OW_cmp_0_2330 (A(temp1), B(Rdata), TC(1'b1), GE_LT(1'b0),
celab: *W,CUVWSP (/Bubble_syn.v,223|21): 1 output port was not connected:
celab: (/Bubble_syn.v:8): EO_NE
  DFFNSRX1 vstate_reg[1] (D(next_state[1]), CKN(clk), SN(1'b1), RN(n397),
celab: *W,CUVWSP (/Bubble_syn.v,391|24): 1 output port was not connected:
celab: (/theda21_2/CBOK_IC_Context/cur/Verilog/tsmc13.v,19089): QN

Reading SDF file from location "/Bubble.sdf"
Annotating SDF timing data:
Compiled SDF file: Bubble.sdf.X
Log file:
Backannotation scope: Bubble_tb.bubble
Configuration file:
MTM control:
Scale factors:
Scale type:
Annotation completed successfully...
SDF statistics: No. of Pathdelays = 1680 Annotated = 100.00% -- No. of Tchecks = 875 Annotated = 94.06%

Path Delays
Total Annotated Percentage
-----
Path Delays 1680 1680 100.00
  $width 283 283 100.00
  $setupthd 566 540 95.41

Building instance overlay tables: ..... Done
Generating native compiled code:
tsmc13_ADD4X4.v <0x60990cd> 284
streams: 4, words: 284
tsmc13_DIFFNSRX1.v <0x3cb6d561> 106
streams: 2, words: 106
tsmc13_DIFFRX1.v <0x5dd5b074> 106
streams: 2, words: 106
tsmc13_XNOR2X1.v <0x2c701b77> 106
streams: 4, words: 284
tsmc13_XNOR2X1.v <0x7c0db14c> 284
streams: 4, words: 284
worklib.Bubble.v <0x490b4ee4> 186
streams: 1, words: 186
worklib.Bubble_tb.v <0x02349b3d> 5853
streams: 6, words: 5853
worklib.SP4M.v <0x5ed76762> 1345
streams: 4, words: 1345

Building instance specific data structures:
Loading native compiled code: ..... Done
Design hierarchy summary:
Instances Unique
-----
Modules: 506 45
UDPs: 30 1
Primitives: 123 8
Timing outputs: 599 19
Registers: 100 13
Scalar wires: 724 1
Expanded wires: 32 1
Always blocks: 3 3
Initial blocks: 5 3
Cont. assignments: 1 11
Pseudo assignments: 1 11
Timing checks: 875 104
Interconnect: 1434 -
Delayed check signals: 283 85
Simulation timescale: 1ps

Writing initial simulation snapshot: worklib.Bubble_tb.v
Loading snapshot: worklib.Bubble_tb.v ..... Done
Verdi3* Loading libscore-usi11.so ..... Done
Verdi3* Enable Parallel Dumping.
Verdi3* Begin traversing the scopes, layer (0).
Verdi3* End of traversing.
Verdi3* run
Verdi3* PSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
Verdi3* PSDB WARNING: The PSDB file already exists. Overwriting the PSDB file may crash the programs that are using this file.
Verdi3* Create PSDB file 'Bubble_syn.fdb'
Verdi3* Begin traversing the scopes, layer (0).
Verdi3* End of traversing.

Congratulations All PASS !!!

Simulation complete via $finish(1) at time 756598 PS + 0
/Bubble_tb.v:123 $finish;

```

```
[d@d0806cpc-2 ~]$ make syn2
rm -rf *.log INC*.v
ncverilog_header.v Bubble_syn.v Bubble_tb.v /thedev2_2/CBOK_IC_Context/cir/Verilog/tsmc13_v +define+SDF +define+TEST2 +accsar+
ncverilog_lib.tlb @RDS9 [C] Copyright 1990-2014 Cadence Design Systems, Inc.
file: header.v
file: Bubble_syn.v
module worklib.Bubble_OW_cmp_0:v
errors: 0 warnings: 0
module worklib.Bubble_OWl_inc_0:v
errors: 0 warnings: 0
module worklib.Bubblelv:
errors: 0 warnings: 0
file: Bubble_tb.v
module worklib.Bubble_tbv:
errors: 0 warnings: 0
module worklib.SPAMV:
errors: 0 warnings: 0
file: /thedev2_2/CBOK_IC_Context/cir/Verilog/tsmc13.v
module tsmc13_INVG2:v
errors: 0 warnings: 0
module tsmc13_ANOX21:v
errors: 0 warnings: 0
module tsmc13_ANOX22:v
errors: 0 warnings: 0
module tsmc13_ANOX23:v
errors: 0 warnings: 0
module tsmc13_AOI31x1:v
errors: 0 warnings: 0
module tsmc13_AOI31x11:v
errors: 0 warnings: 0
module tsmc13_AOI32x1:v
errors: 0 warnings: 0
module tsmc13_AOI32x11:v
errors: 0 warnings: 0
module tsmc13_AOI32x12:v
errors: 0 warnings: 0
module tsmc13_AOI32x13:v
errors: 0 warnings: 0
module tsmc13_NAND2x1:v
errors: 0 warnings: 0
module tsmc13_NAND3x1:v
errors: 0 warnings: 0
module tsmc13_NANO4x1:v
errors: 0 warnings: 0
module tsmc13_NANO2BX1:v
errors: 0 warnings: 0
module tsmc13_NOEX21:v
errors: 0 warnings: 0
module tsmc13_NOR2x1:v
errors: 0 warnings: 0
module tsmc13_NOR3x1:v
errors: 0 warnings: 0
module tsmc13_NOP2x1:v
errors: 0 warnings: 0
module tsmc13_OP2x1:v
errors: 0 warnings: 0
module tsmc13_OAI21x1:v
errors: 0 warnings: 0
module tsmc13_OAI31x1:v
errors: 0 warnings: 0
module tsmc13_OAI32x1:v
errors: 0 warnings: 0
module tsmc13_OAI32x11:v
errors: 0 warnings: 0
module tsmc13_OAI32x12:v
errors: 0 warnings: 0
module tsmc13_OAI32x13:v
errors: 0 warnings: 0
module tsmc13_XNOR2x1:v
errors: 0 warnings: 0
module tsmc13_XNOR2x11:v
errors: 0 warnings: 0
module tsmc13_XNOR2x12:v
errors: 0 warnings: 0
module tsmc13_XNOR2x13:v
errors: 0 warnings: 0
module tsmc13_ADDHX1:v
errors: 0 warnings: 0
module tsmc13_DFFFX1:v
errors: 0 warnings: 0
module tsmc13_DFFNSRX1:v
errors: 0 warnings: 0
primitive tsmc13_wdp_dff:
errors: 0 warnings: 0
Checking library "tsmc13": ..... Done
Checking library "worklib": ..... Done
Elaborating the design hierarchy:
Bubble_OW_cmp_0 r330 (.A(templ), .B(RData), .TC(1'b1), .GE_LT(1'bo))
nclab: *W.CUVWSP (/./Bubble_syn.v.223|21): 1 output port was not connected:
nclab: (/./Bubble_syn.v.8): EO_NE
DFFNSRX1 \state_reg[1] (.D(next_state[1]), .CKN(clk), .SN(1'b1), .RN(n397)).
nclab: *W.CUVWSP (/./Bubble_syn.v.231|24): 1 output port was not connected:
nclab: (/thedev2_2/CBOK_IC_Context/cir/Verilog/tsmc13.v.13085): QN
Reading SDF file from location "/./Bubble.sdf".
Annotating SDES timing dates:
Compiled SDE file: Bubble.sdf.X
Log file:
Backannotation scope: Bubble.tb.bubble
Configuration file:
MTH control:
Scale factors:
Scale type:
Annotation completed successfully...
SDF statistics: No. of PathDelays = 1680 Annotated = 100.00% -- No. of Tchecks = 875 Annotated = 94.06%
Path Delays threshold 26 0 0.00
Switch threshold 322 282 100.00
$setuphold 566 540 95.41
Building instance overlay tables: ..... Done
Generating native compiled code:
tsmc13.ADDHXL:v <0xb9e50ed>
streams: 2 words: 284
tsmc13.DFFNSRX1:v <0xab6264f1>
streams: 2 words: 106
tsmc13.OPFX1:v <0x58de5074>
streams: 2 words: 106
tsmc13.XNOR2X1:v <0xc2761b57>
streams: 4 words: 284
tsmc13.XOR2X1:v <0x7c0bb446>
streams: 4 words: 284
worklib.Bubblelv <0x49bddee>
streams: 1 word: 186
worklib.Bubbletbv <0xd254db3d>
streams: 6 words: 5853
worklib.SPAM:v <0x5ed76762>
streams: 4 words: 1345
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary: Instances Unique
Modules: 506 45
UDPs: 90 1
Primitives: 1226 18
Timing outputs: 539 18
Registers: 100 13
Counters: 724 1
Expanded wires: 32 1
Always blocks: 3 3
Initial blocks: 0 0
Cont. assignments: 1 11
Pseudo assignments: 875 164
Timing checks: 1434 -
Interconnect: 282 85
Simulation timescale: lps
Writing initial simulation snapshot: worklib.Bubble_tb.v
Loading snapshots worklib.Bubble.tb: ..... Done
#Verdi3* Loading libscore_ius1dl.so
#Verdi3*: Enable Parallel Dumping.
ncsim> source $USERCAD/cadence/TMCISIV/cir/tools/ince/files/ncsimrc
ncsim> run
PSDB Dumper for IUS, Release VerId3_J-2014-SF2_S Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
#Verdi3* PSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
#Verdi3*: Create FSDB File: Bubble.spice.fsdb
#Verdi3*: Begin traversing the scopes, layer (0).
#Verdi3*: End of traversing.
Congratulations All PASS !!!
```

三、 問題與討論

1. 終於到最後一個 Lab 了，感謝助教一直以來的 carry，也感謝我的肝不離不棄。
2. Lab5 Bonus 的 RAM 是可以同時讀跟寫的嗎？還有它是給 Address 馬上可以讀寫嗎？（問於 ilms）

(林柏淵, stalkerking7@gmail.com, 2018-06-10 13:21)

講解有說喔~可以同時讀寫

(吳紹齊, wsc861029@gmail.com, 2018-06-10 13:29)

那理論上可以WAddr跟RAddr為不同值嗎？

因為試了好像不行qq

(林楷宸, 1038790@gmail.com, 2018-06-10 14:33)

同學你好，

可以不同值喔，

我就是不同值的寫法，

你可能在注意一下你是不是有重複給值之類惡問題

By TA.

我這次實作的 RAddr、WAddr 都是設定成一樣，一起變化，經過助教的解釋發現或許不需要這樣，暑假會多嘗試不同方法提升效能。