Design Rules Verification Report

Filename : C:\development\shaololllc-usb_breakout\microUSB\shaololllc-usb_breakout_micro

Warnings 0
Rule Violations 13

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=12.7mm) (Preferred=0.203mm) (All)	0
Routing Layers(All)	0
Routing Via (MinHoleWidth=0.25mm) (MaxHoleWidth=0.711mm) (PreferredHoleWidth=0.25mm) (MinWidth=0.25mm)	0
Routing Via (MinHoleWidth=0.254mm) (MaxHoleWidth=6.731mm) (PreferredHoleWidth=0.254mm)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.254mm) (Max=0.254mm) (Prefered=0.254mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.508mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.127mm) (All)	0
Hole Size Constraint (Min=0.254mm) (Max=3.556mm) (All)	2
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.102mm) (All),(All)	2
Silk To Solder Mask (Clearance=0mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.127mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	9
Component Clearance Constraint (Horizontal Gap = 0.254mm, Vertical Gap = 0.254mm) (All),(All)	0
Height Constraint (Min=0mm) (Max=33mm) (Prefered=12.7mm) (All)	0
Total	13

Hole Size Constraint (Min=0.254mm) (Max=3.556mm) (All)
Hole Size Constraint: (4mm > 3.556mm) Pad Free-1(-10.2mm,4.4mm) on Multi-Layer Actual Hole Size = 4mm
Hole Size Constraint: (4mm > 3.556mm) Pad Free-1(-3.7mm,4.4mm) on Multi-Layer Actual Hole Size = 4mm

Minimum Solder Mask Sliver (Gap=0.102mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.102mm) Between Pad uUSB-0(7.26mm,1.95mm) on Top Layer And Pad uUSB-1(6.9mm,3.1mm) on
Minimum Solder Mask Sliver Constraint: (0.1mm < 0.102mm) Between Pad uUSB-0(7.26mm,6.85mm) on Top Layer And Pad uUSB-5(6.9mm,5.7mm) on

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0.3mm < 0.381mm) Between Board Edge And Pad uUSB-0(9.55mm,1.5mm) on Top Layer
Board Outline Clearance(Outline Edge): (0.3mm < 0.381mm) Between Board Edge And Pad uUSB-0(9.55mm,7.3mm) on Top Layer
Board Outline Clearance(Outline Edge): (0.192mm < 0.381mm) Between Board Edge And Text "+5" (3.4mm,0.2mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.2mm < 0.381mm) Between Board Edge And Text "DM" (0.6mm,0.2mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.18mm < 0.381mm) Between Board Edge And Text "GND" (3.3mm,8.1mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.189mm < 0.381mm) Between Board Edge And Text "ID" (1mm,8.1mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.308mm < 0.381mm) Between Board Edge And Track (5.9mm,0.41mm)(5.9mm,8.39mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.308mm < 0.381mm) Between Board Edge And Track (5.9mm,0.41mm)(7.789mm,0.41mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.309mm < 0.381mm) Between Board Edge And Track (5.9mm,8.39mm)(7.789mm,8.39mm) on Top Overlay