Shaoting Zhang

8000 U.S. 290 West Apt. 10407 Austin, TX 78736

Seek Intern/Fulltime Hardware Engineering Position starting at Fall 2017

Education

University of Texas at Dallas

Dallas, TX

sxz152930@utdallas.edu

Mobile: (737)-529-7160

Gender: female

Master Student, Department of ECE

Aug. 2015 - Dec. 2017 (Expected)

- GPA: 11.4/12

 Relevant Courses: VLSI Design, Advanced Digital Logic, Computer Architecture (A), Design and Analysis of Computer Algorithms (A), Dynamics Of Complex Networks and Systems (A), Analog Integrated Circuit Design, Power Management Circuits, Digital Signal Processing, Linear Systems (A), Energy Harvesting, Storage and Powering for Microsystems

Nanjing University of Post and Telecommunications

Nanjing, China

Bachelor of Engineering, Department of Communication Engineering

Sep. 2009 - Jul. 2013

 Relevant Courses: Principles of Communications, Signals and Systems, Principles of Digital & Analog Integrated Circuits, Random Signals and Statistics, Discrete Structures

Work Experience

China Electronics Technology Group Corporation

Nanjing, China Jul. 2013 – Jul. 2014

Silicon Testing Engineer

- Wafer level testing before IC packaging

 Quality testing of power tube inside the gold bonding for silicon BJT (Bipolar Junction Transistor) and LDMOS (Laterally Diffused Metal Oxide Semiconductor). Parameter testing and performance evaluations on output power and power gain fluctuations of BJT and LDMOS

Course Projects

- Advanced Digital Logic:
 - Pump controller design and power, performance, area (PPA) trade-off with Synopsys Design Vision
 - Logic synthesis from VHDL to gate-level netlist using Synopsys Design Vision. Fault detection with automatic test pattern generation and logic simulation
- VLSI Design: The Trivium Stream Cipher
 - Implement the Trivium stream cipher with inverters, NAND gates, NOR gates and Flip-Flops.
 Functional simulation and testing in schematic and layout
- Computer Architecture: Cache Simulation and Optimization
 - Cache performance evaluations varying capacities, associativities and block sizes using SimpleScalar
 - Instruction set optimization with parallelism and pipelining techniques. Adopt a SIMD instruction to unfold the "for" loop. Achieve 26% improvement on the instruction cache miss rate compared with the original C programs with MediaBench test cases
- Algorithms: Design and Analysis: Algorithm Analysis and Implementations
 - Python implementations of sorting and graph algorithms, such as QuickSort, MergeSort, Dijkstra's algorithm, Karger's algorithm and computing strongly connected components
- Dynamics Of Complex Networks and Systems: The Network Modeling for Game Of Thrones
 - Python implementation of the weighted graph for the social network in Game of Thrones
 - Describe and analyze the social network properties like the centrality, diameter and power law

Skills

Languages/Scripting: Python, C language, SPICE/HDL

Applications: Cadence Virtuoso/Schematic, Synopsys Design Vision, Matlab **Miscellaneous:** Self-motivated, good communication and team-work skills.

Immigration Status: F-1 Student Visa (no need for H1B sponsorship)