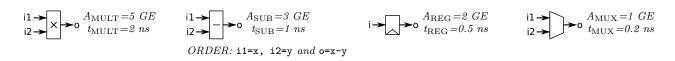
Essentials of Computer Systems - Exercises #2

1 Datapath Design - part 1

Exercise 1.1 Datapath design:

(a) Design a datapath (draw a DFD) with the following functionality: z = 3(b-a) - ac + a. The building blocks available are a multiplier and a subtracter, shown in figure below. You are given an area constraint: you are allowed to use at most 1 multiplier and at most one subtracter.



(b) Fill out the analysis table for the DFD obtained in part (a) ignoring MUXes:

$Analysis\ table$		
latency		
throughput		
critical path delay		
clock period		
# inputs		
# outputs		
# registers		
# subtracters		
# multipliers		
total area in GE		

(c) Fill out the analysis table for the DFD obtained in part (a) including MUXes:

$Analysis\ table$		
latency		
throughput		
critical path delay		
clock period		
# inputs		
# outputs		
# registers		
# multiplexers		
# subtracters		
# multipliers		
total area in GE		

Exercise 1.2 Datapath design:

(a) Design a datapath (draw a DFD) with the following functionality: z = a(a+b) - (bc+a). The building blocks available are a multiplier and an adder, shown in figure below. All inputs are available only in the first clock cycle. The top priority is to minimize the area.

$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	$A_{\text{REG}} = 2 \text{ GE}$ il $A_{\text{REG}} = 0.5 \text{ ns}$ il	$A_{\text{MUX}} = 1 GE$ $t_{\text{MUX}} = 0.2 ns$
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(b) Fill out the analysis table for the DFD obtained in part (a):

$Analysis\ table$		
latency		
throughput		
critical path delay		
clock period		
# inputs		
# outputs		
# registers		
# multiplexers		
# adders		
# multipliers		
total area in GE		

(c) Draw the circuit for the DFD obtained in part (a):