

# CHAPTER 1

# FUNDAMENTAL CONCEPTS

## 1.1 INTRODUCTION

All of us are familiar with the impact of modern digital computers, communication systems, digital display systems, internet, email etc. on society. One of the main causes of this revolution is the advent of *integrated circuits (ICs)*, which became possible because of the tremendous progress in semiconductor technology in recent years. Most of us may not be familiar with the principles of working of computers, communication systems, internet, email, etc. even though these have become an important part of our daily life. The operation of these systems, and many other systems, is based on the principles of digital techniques and these systems are referred to as *digital systems*.

Some of us are familiar with electronic amplifiers. These are used to amplify electrical signals. This type of signals are continuous signals and can have any value in a limited range and are known as *analog signals*. The electronic circuits used to process (amplify) these signals are known as *analog circuits* and the systems built around this kind of operation are known as *analog systems*.

On the other hand, in an electronic calculator, the input is given with the help of switches. This is converted into electrical signals which have two discrete values or levels. One of these may be called as LOW level and the other one as HIGH level. The signal will always be of one of the two levels. Here, the actual value of the signal is immaterial as long as it is within the specified range of LOW or HIGH level. This type of signal is known as a *digital signal* and the circuits inside the calculator used to process these signals are known as *digital circuits*. A calculator is an example of a *digital system*.

There has been an unprecedented growth in digital techniques since Claude Shannon systematised and adapted George Boole's theoretical work in 1938. Developments in semiconductor technology, together with the progress in digital techniques, brought about a revolution in digital electronics when a single chip device known as *microprocessor* was introduced by Intel Corporation of America in 1971.

Since the introduction of microprocessors, the digital systems have gained tremendous power and importance. There is no field of knowledge which has affected our lives as much as the digital theory and applications, in such a short span of time. It has, infact, created a culture which nobody could have imagined till a few years ago. The rate of growth in this field has been unprecedented and the digital technology has become the most powerful technology for all future innovations in every walk of human endeavour whether it is computers, communication systems, information systems, entertainment and consumer products, business,

banking and finance, office machines, homes, cars, education, industrial control systems, scientific and medical instruments, and defence equipment, etc.

Some of the principal reasons for the widespread use of digital techniques and systems are:

- The devices used in digital circuits generally operate in one of the two *states*, known as ON and OFF resulting in a very simple operation.
- There are only a few basic operations in digital circuits which are very easy to understand.
- Digital techniques require Boolean algebra which is very simple and can easily be learnt even in schools.
- Digital circuits require basic concepts of electric network analysis which can easily be learnt at the junior level in colleges. The principal electrical characteristics required are *switching speed* and *loading* considerations. On the other hand, analog circuits and systems involve frequency and time domain concepts, complicated circuit analysis techniques, etc. which make the understanding of these circuits much more difficult than the digital circuits.
- A large number of ICs are available for performing various operations. These are highly reliable, accurate, small in size and the speed of operation is very high. A number of programmable ICs are also available.
- Various ICs are available in a *logic family* with similar electrical characteristics which make the design and development of digital systems very simple and also reduces interfacing problems. Also, a number of logic families based on different technologies are available which help in optimising the system design from the point of view of power requirement and speed of operation.
- The effect of fluctuations in the characteristics of the components, ageing of components, temperature, and noise, etc. is very small in digital circuits.
- Digital circuits have capability of memory which makes these circuits highly suitable for computers, calculators, watches, telephones, etc.
- The display of data and other information is very convenient, accurate and elegant using digital techniques.
- Many students have an opportunity to learn programming of digital computers, hence they have a strong motivation to study the way the digital hardware works.
- It is a very fascinating and challenging field of study because most of the latest electronic systems are digital in nature.

## 1.2 DIGITAL SIGNALS

As mentioned above, a digital signal has two discrete levels or values. Two different representations of digital signals are shown in Fig. 1.1. In each case there are two discrete levels. These levels can be represented using the terms LOW and HIGH. In Fig. 1.1a, lower of the two levels has been designated as LOW level and the higher as HIGH level. In contrast to this, in Fig. 1.1b, higher of the two levels has been designated as LOW level and the lower as HIGH level. Digital systems using the representation of signal shown in Fig. 1.1a are said to employ *positive logic system* and those using the other representation of the signal shown in Fig. 1.1b are said to employ *negative logic system*. The genesis of the term *logic* is given later. In each of the two signals we observe that the voltage corresponding to a given level is not fixed, rather voltages in a limited range are designated as a level. As long as the voltage belongs to a level it will be taken as that level and the exact value of the voltage is immaterial. For example, any voltage in the range of 3.5 to 5 V will be considered as HIGH level in the positive logic system and LOW level in the negative logic system. Similarly, any voltage in the range of 0 to 1 V will be considered as LOW level in the positive logic system and HIGH level in the negative logic system. The actual voltage ranges corresponding to LOW and HIGH level are not

same for all types of circuits and are different for different logic families (see Chapter 4). Unless otherwise specified, we shall be dealing with positive logic system.

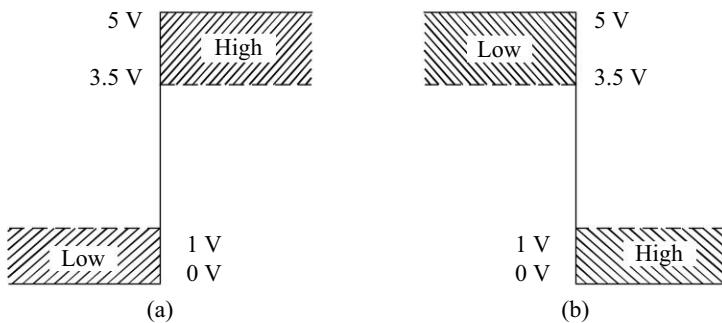


Fig. 1.1 *Digital Signal Representation (a) Positive Logic (b) Negative Logic*

The above discussion brings out one of the main advantages of digital systems, viz. they are less susceptible to noise, fluctuations in the characteristics of components, etc.

The two discrete signal levels HIGH and LOW can also be represented by the *binary digits* 1 and 0 respectively. A *binary digit* (0 or 1) is referred to as a *bit*. Since a digital signal can have only one of the two possible levels 1 or 0, the *binary number system* (see Chapter 2) can be used for the analysis and design of digital systems. The two levels (or states) can also be designated as ON and OFF or TRUE and FALSE. George Boole introduced the concept of binary number system in the studies of the mathematical theory of LOGIC in the work entitled *An Investigation of the Laws of Thought* in 1854 and developed its algebra known as *Boolean algebra*. These logic concepts have been adapted for the design of digital hardware since 1938 when Claude Shannon organised and systematised Boole's work in *Symbolic Analysis of Relay and Switching Circuits*.

### 1.3 BASIC DIGITAL CIRCUITS

In a digital system there are only a few basic operations performed, irrespective of the complexities of the system. These operations may be required to be performed a number of times in a large digital system like digital computer or a digital control system, etc. The basic operations are AND, OR, NOT, and FLIP-FLOP. The AND, OR, and NOT operations are discussed here and the FLIP-FLOP, which is a basic memory element used to store binary information (one bit is stored in one FLIP-FLOP), will be introduced in Chapter 7.

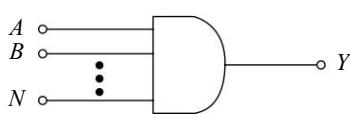


Fig. 1.2 *The Standard Symbol for an AND Gate*

#### 1.3.1 The AND Operation

A circuit which performs an AND operation is shown in Fig. 1.2. It has  $N$  inputs ( $N \geq 2$ ) and one output. Digital signals are applied at the input terminals marked  $A, B, \dots, N$ , the other terminal being ground, which is not shown in the diagram. The output is obtained at the output terminal marked  $Y$  (the other terminal being ground) and it is also a digital signal. The AND operation is defined as: the output of an AND gate is 1 if and only if all the inputs are 1. Mathematically, it is written as

digital signal. The AND operation is defined as: the output of an AND gate is 1 if and only if all the inputs are 1. Mathematically, it is written as

$$\begin{aligned}
 Y &= A \text{ AND } B \text{ AND } C \dots \text{ AND } N \\
 &= A \cdot B \cdot C \cdot \dots \cdot N \\
 &= ABC \dots N
 \end{aligned} \tag{1.1}$$

where  $A, B, C, \dots, N$  are the input variables and  $Y$  is the output variable. The variables are binary, i.e. each variable can assume only one of the two possible values, 0 or 1. The *binary variables* are also referred to as *logical variables*.

Equation (1.1) is known as the *Boolean equation* or the *logical equation* of the AND gate. The term gate is used because of the similarity between the operation of a digital circuit and a gate. For example, for an AND operation the gate opens ( $Y = 1$ ) only when all the inputs are present, i.e. at logic 1 level.

**Truth Table** Since a logical variable can assume only two possible values (0 and 1), therefore, any logical operation can also be defined in the form of a table containing all possible input combinations ( $2^N$  combinations for  $N$  inputs) and their corresponding outputs. This is known as a *truth table* and it contains one row for each one of the input combinations.

For an AND gate with two inputs  $A, B$  and the output  $Y$ , the truth table is given in Table 1.1. Its logical equation is  $Y = AB$  and is read as “ $Y$  equals  $A$  AND  $B$ ”.

Table 1.1 **Truth Table of a 2-Input AND Gate**

Inputs		Output
<b>A</b>	<b>B</b>	<b>Y</b>
0	0	0
0	1	0
1	0	0
1	1	1

Since, there are only two inputs,  $A$  and  $B$ , therefore, the possible number of input combinations is four. It may be observed from the truth table that the input–output relationship for a digital circuit is completely specified by this table in contrast to the input–output relationship for an analog circuit. The pattern in which the inputs are entered in the truth table may also be observed carefully, which is in the ascending order of binary numbers formed by the input variables. (See Chapter 2).

**Logical Multiplication** The AND operation is also referred to as logical multiplication and therefore, it is symbolised algebraically by a multiplication dot (·) as illustrated in Eq. (1.1).

### Example 1.1

You have rented a locker in a bank. Express the process of opening the locker in terms of a digital operation.

#### Solution

The locker door ( $Y$ ) can be opened by using one key ( $A$ ) which is with you and the other key ( $B$ ) which is with the bank executive. When both the keys are used, the locker door opens, i.e., the locker door can be opened ( $Y = 1$ ) only when both the keys are applied ( $A = B = 1$ ). Thus, this process can be expressed as an AND operation

$$Y = A \cdot B$$

### Example 1.2

The voltage waveforms shown in Fig. 1.3 are applied at the inputs of a 2-input AND gate. Determine the output waveform.

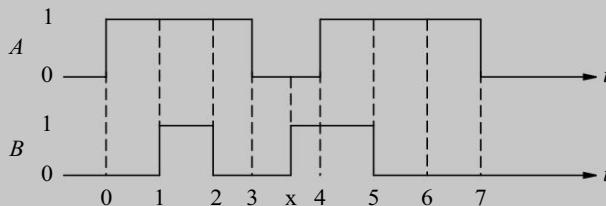


Fig. 1.3

### Solution

Using Table 1.1, we find

From  $t = 0$  to  $t = 1$

$$A = 1, B = 0$$

Therefore,  $Y = 0$

From  $t = 1$  to  $t = 2$

$$A = B = 1$$

Therefore,  $Y = 1$

From  $t = 2$  to  $t = 3$

$$A = 1, B = 0$$

Therefore,  $Y = 0$

From  $t = 3$  to  $t = x$

$$A = 0, B = 0$$

Therefore,  $Y = 0$

From  $t = x$  to  $t = 4$

$$A = 0, B = 1$$

Therefore,  $Y = 0$

From  $t = 4$  to  $t = 5$

$$A = 1, B = 1$$

Therefore,  $Y = 1$

From  $t = 5$  to  $t = 7$

$$A = 1, B = 0$$

Therefore,  $Y = 0$ . It will be 0 for  $t > 7$

The output waveform with reference to the input waveforms are shown in Fig. 1.4.

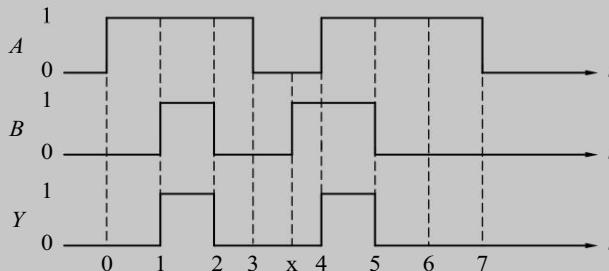


Fig. 1.4

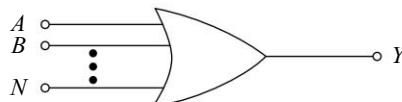


Fig. 1.5 **The Standard Symbol for an OR Gate**

### 1.3.2 The OR Operation

Figure 1.5 shows an OR gate with  $N$  inputs ( $N \geq 2$ ) and one output. The OR operation is defined as: the output of an OR gate is 1 if and only if one or more inputs are 1. Its logical equation is given by

$$Y = A \text{ OR } B \text{ OR } C \dots \text{ OR } N = A + B + C + \dots + N \quad (1.2)$$

The truth table of a 2-input OR gate is given in Table 1.2. Its logic equation is  $Y = A + B$  and is read as “ $Y$  equals  $A$  OR  $B$ ”.

Table 1.2 **Truth Table of a 2-Input OR Gate**

Inputs		Output
<b>A</b>	<b>B</b>	<b>Y</b>
0	0	0
0	1	1
1	0	1
1	1	1

### Example 1.3

In a chemical process an ALARM is required to be activated if either temperature or pressure or both exceed certain limits. Is it possible to express this operation in terms of a digital operation? If yes, find the operation.

#### Solution

Let the temperature and pressure be converted into electrical signals and  $T = 1$  if temperature exceeds the specified limit and  $P = 1$  if pressure exceeds the specified limit. If  $T = 1$  or  $P = 1$  or both  $T$  and  $P$  are 1 then the ALARM is required to be activated, i.e., the signal applied to the ALARM  $Y = 1$ . This operation can be expressed as

$$\begin{aligned} Y &= T \text{ OR } P \\ &= T + P \end{aligned}$$

Which is an OR operation.

### Example 1.4

If the waveforms of Fig. 1.3 are applied at the inputs of a 2-input OR gate, determine the output waveform.

#### Solution

Using Table 1.2, we find

From  $t = 0$  to  $t = 1$

$$A = 1, B = 0$$

Therefore,  $Y = 1$

From  $t = 2$  to  $t = 3$

$$A = 1, B = 0$$

Therefore,  $Y = 1$

From  $t = 1$  to  $t = 2$

$$A = 1, B = 1$$

Therefore,  $Y = 1$

From  $t = 3$  to  $t = x$

$$A = 0, B = 0$$

Therefore,  $Y = 0$

From  $t = x$  to  $t = 7$

$$A = 0, B = 1$$

Therefore,  $Y = 1$

From  $t = 5$  to  $t = 7$

$$A = 1, B = 0$$

Therefore,  $Y = 1$ . It is 0 for  $t > 7$ .

From  $t = 4$  to  $t = 5$

$$A = 1, B = 1$$

Therefore,  $Y = 1$

The output waveform with reference to the input waveforms are shown in Fig. 1.6

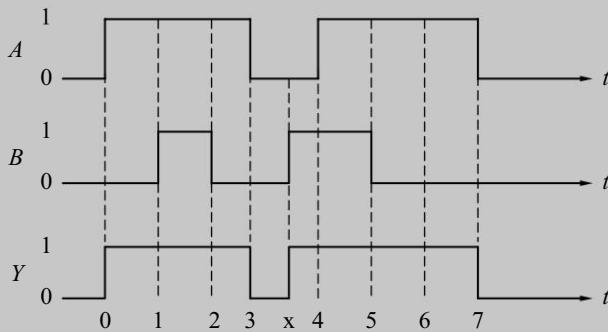


Fig. 1.6

### 1.3.3 The NOT Operation

Figure 1.7 shows a NOT gate, which is also known as an *inverter*. It has one input ( $A$ ) and one output ( $Y$ ). Its logic equation is written as

$$Y = \text{NOT } A \\ = \bar{A} \quad (1.3)$$

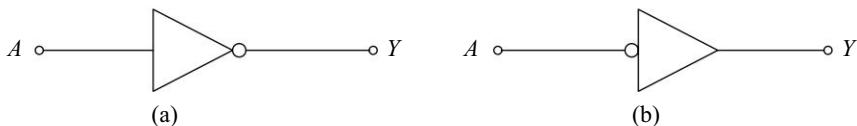


Fig. 1.7 *The Standard Symbols for a NOT Gate*

and is read as “ $Y$  equals NOT  $A$ ” or “ $Y$  equals complement of  $A$ ”. The truth table of a NOT gate is given in Table 1.3.

The NOT operation is also referred to as an *inversion* or *complementation*. The presence of a small circle, known as the *bubble*, always denotes inversion in digital circuits.

Table 1.3 **Truth Table of a NOT Gate**

Input	Output
A	Y
0	1
1	0

**Example 1.5**

If the waveform shown in Fig. 1.8 is applied at the input of an inverter, find its output waveform.

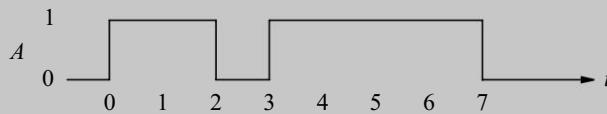


Fig. 1.8

**Solution**

Using Table 1.3, we find

From  $t = 0$  to  $t = 2$

$$A = 1$$

Therefore,  $Y = \text{NOT } A = \text{NOT } 1 = 0$

From  $t = 2$  to  $t = 3$

$$A = 0$$

Therefore,  $Y = \text{NOT } A = \text{NOT } 0 = 1$

From  $t = 3$  to  $t = 7$

$$A = 1$$

Therefore,  $Y = \text{NOT } A = \text{NOT } 1 = 0$

$Y$  will be 1 for  $t > 7$

The output waveform with reference to the input waveform is shown in Fig. 1.9

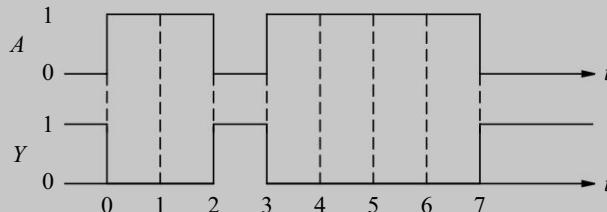


Fig. 1.9

**1.4 NAND AND NOR OPERATIONS**

Any Boolean (or logic) expression can be realised by using the AND, OR and NOT gates discussed above. From these three operations, two more operations have been derived: the NAND operation and NOR operation.

These operations have become very popular and are widely used, the reason being the only one type of gates, either NAND or NOR are sufficient for the realisation of any logical expression. Because of this reason, NAND and NOR gates are known as *universal gates*.

### 1.4.1 The NAND Operation

The NOT-AND operation is known as the NAND operation. Figure 1.10a shows an  $N$  input ( $N \geq 2$ ) AND gate followed by a NOT gate. The operation of this circuit can be described in the following way:

The output of the AND gate ( $Y'$ ) can be written using Eq. (1.1)

$$Y' = AB \dots N \quad (1.4)$$

Now, the output of the NOT gate ( $Y$ ) can be written using Eq. (1.3)

$$Y = \overline{Y'} = \overline{AB \dots N} \quad (1.5)$$

The logical operation represented by Eq. (1.5) is known as the NAND operation. The standard symbol of the NAND gate is shown in Fig. 1.10b. Here, a bubble on the output side of the NAND gate represents NOT operation, inversion or complementation.

The truth table of a 2-input NAND gate is given in Table 1.4. Its logic equation is  $Y = \overline{A \cdot B}$  and, is read as “ $Y$  equals NOT ( $A$  AND  $B$ )”.

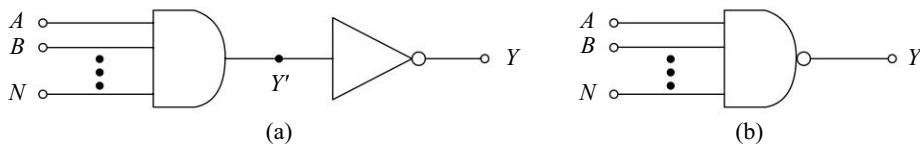


Fig. 1.10 (a) NAND Operation as NOT-AND Operation,  
(b) Standard Symbol for the NAND Gate

Table 1.4 Truth Table of a 2-Input NAND Gate

Inputs		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

The three basic logic operations, AND, OR and NOT can be performed by using only NAND gates. These are given in Fig. 1.11.

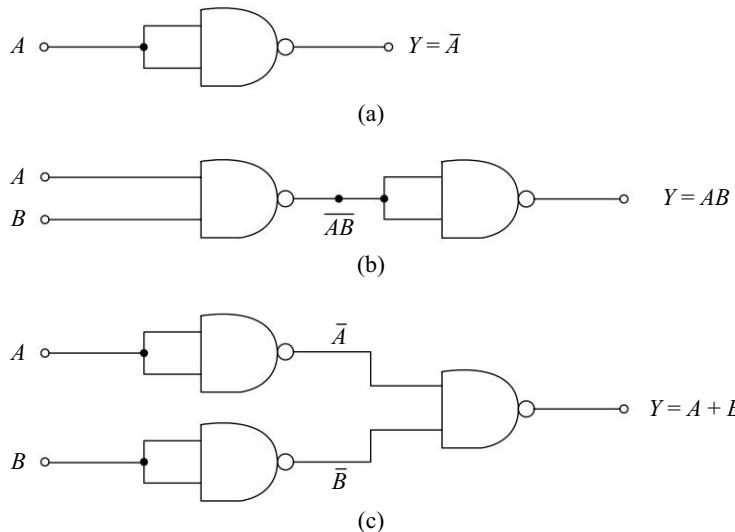


Fig. 1.11 *Realisation of Basic Logic Operations Using NAND Gates*  
 (a) NOT (b) AND (c) OR

### Example 1.6

If the voltage waveforms of Fig. 1.3 are applied at the inputs of a 2-input NAND gate, find the output waveform.

#### Solution

The output waveform will be inverse of the output waveform  $Y$  of Fig. 1.4.

### Example 1.7

What will be the output of a 2-input NAND gate, if one of its inputs is permanently connected to

- (a) logic 0 voltage
- (b) logic 1 voltage

#### Solution

- (a) Figure 1.12a shows a 2-input NAND gate with one of its inputs connected to logic 0 voltage.

In this circuit if  $A = 0$ ,  $Y = 1$ . Similarly, if  $A = 1$ , then also the output  $Y = 1$ .

This shows that the output  $Y$  is 1, irrespective of the other input. In fact, a NAND gate is *disabled* or *inhibited* if one of its inputs is connected to logic 0.

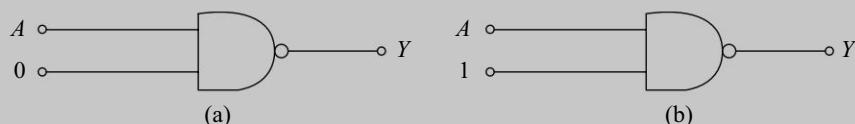


Fig. 1.12 *Circuits for Example 1.7*

(b) Figure 1.12b shows a 2-input NAND gate with one of its inputs connected to logic 1 voltage

Here, if  $A = 1, Y = 0$ ,

and if  $A = 0, Y = 1$

This means  $Y = \overline{A}$

This condition *enables* a NAND gate.

## 1.4.2 The NOR Operation

The NOT-OR operation is known as the NOR operation. Figure 1.13a shows an  $N$  input ( $N \geq 2$ ) OR gate followed by a NOT gate. The operation of this circuit can be described in the following way:

The output of the OR gate  $Y'$  can be written using Eq. (1.2) as

$$Y' = A + B + \dots + N \quad (1.6)$$

and the output of the NOT gate ( $Y$ ) can be written using Eq. (1.3)

$$Y = \overline{Y'} = \overline{A + B + \dots + N} \quad (1.7)$$

The logic operation represented by Eq. (1.7) is known as the NOR operation.

The standard symbol of the NOR gate is shown in Fig. 1.13b. Similar to the NAND gate, a bubble on the output side of the NOR gate represents the NOT operation.

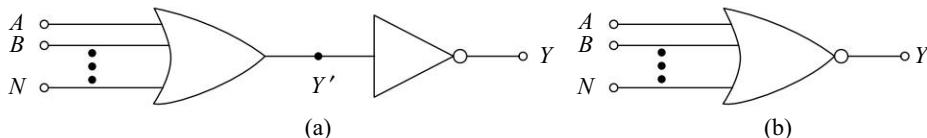


Fig. 1.13 (a) NOR Operation as NOT-OR Operation  
 (b) Standard Symbol for the NOR Gate

Table 1.5 gives the truth table of a 2-input NOR gate. Its logic equation is  $Y = \overline{A + B}$  and is read as “ $Y$  equals NOT ( $A$  OR  $B$ )”.

Table 1.5 Truth Table of a 2-Input NOR Gate

Inputs		Output
$A$	$B$	$Y$
0	0	1
0	1	0
1	0	0
1	1	0

The three basic logic operations, AND, OR, and NOT can be performed by using only the NOR gates. These are given in Fig. 1.14.

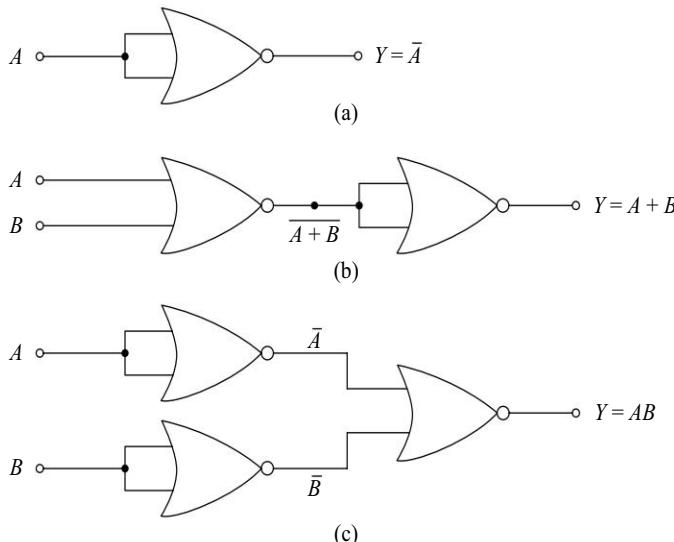


Fig. 1.14 Realisation of Basic Logic Operations Using NOR Gates (a) NOT (b) OR (c) AND

### Example 1.8

If the voltage waveforms of Fig. 1.3 are applied at the inputs of a 2-input NOR gate, determine the output waveform.

#### Solution

The output waveform will be inverse of the output waveform of Fig. 1.6.

### Example 1.9

- If one of the inputs of a NOR gate is connected to logic 0 voltage, find the output voltage in terms of the other input.
- Repeat (a) if one of the inputs is connected to logic 1 voltage.

#### Solution

- From Table 1.5, we observe that if  $A = 0$  then  $Y = \bar{B}$ . This operation is used for enabling a NOR gate.
- Similarly from Table 1.5, we observe that if  $A = 1$ , then  $Y = 0$ . This operation inhibits or disables a NOR gate. Here, the output is 0 irrespective of the  $B$  input.

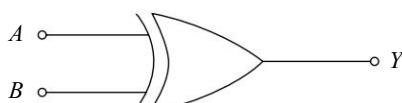


Fig. 1.15 Standard Symbol for EX-OR Gate

## 1.5 EXCLUSIVE-OR AND EXCLUSIVE-NOR OPERATIONS

### 1.5.1 The EXCLUSIVE-OR Operation

The EXCLUSIVE-OR (EX-OR) operation is widely used in digital circuits. It is not a basic operation and can be performed using the basic gates—AND, OR and NOT or universal gates NAND or NOR.

Because of its importance, the standard symbol shown in Fig. 1.15 is used for this operation and it is treated as basic logic element.

The truth table of an EX-OR gate is given in Table 1.6 and its logic equation is written as

$$Y = A \text{ EX-OR } B = A \oplus B \quad (1.8)$$

Table 1.6 **Truth Table of EX-OR Gate**

Inputs		Output
<b>A</b>	<b>B</b>	<b>Y</b>
0	0	0
0	1	1
1	0	1
1	1	0

If we compare the truth table of an EX-OR gate with that of an OR gate given in Table 1.2, we find that the first three rows are same in both. Only the fourth row is different. This circuit finds application where two digital signals are to be compared. From the truth table we observe that when both the inputs are same (0 or 1) the output is 0, whereas when the inputs are not same (one of them is 0 and the other one is 1) the output is 1.

### Example 1.10

The voltage waveforms, shown in Fig.1.3, are applied at the inputs of an EX-OR gate. Determine the output waveform.

#### Solution

Using Table 1.6, we find

From  $t = 0$  to  $t = 1$

$$A = 1, B = 0$$

Therefore,  $Y = 1$

From  $t = x$  to  $t = 4$

$$A = 0, B = 1$$

Therefore,  $Y = 1$

From  $t = 1$  to  $t = 2$

$$A = 1, B = 1$$

Therefore,  $Y = 0$

From  $t = 4$  to  $t = 5$

$$A = 1, B = 1$$

Therefore,  $Y = 0$

From  $t = 2$  to  $t = 3$

$$A = 1, B = 0$$

Therefore,  $Y = 1$

From  $t = 5$  to  $t = 7$

$$A = 1, B = 0$$

Therefore,  $Y = 1$

From  $t = 3$  to  $t = x$

$$A = 0, B = 0$$

Therefore,  $Y = 0$

For  $t > 7$

$$A = 0, B = 0$$

Therefore,  $Y = 0$

The output waveform with reference to the input waveforms are shown in Fig. 1.16.

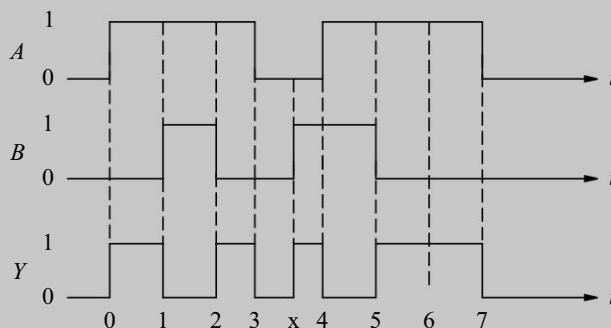


Fig. 1.16

### Example 1.11

Determine the relation between the output  $Y$  and one of its inputs, if its other input is connected to

- (a) logic 0
- (b) logic 1

### Solution

- (a) Let us connect input  $A$  to 0, from the first two rows of the Table 1.6, we observe that  $Y = B$ .
- (b) Similarly if input  $A$  is connected to logic 1 voltage, from the last two rows of the truth table, we observe that

$$Y = \bar{B}$$

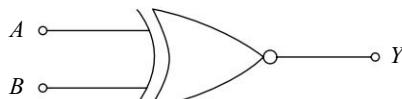


Fig. 1.17 Standard Symbol for EX-NOR Gate

### 1.5.2 The EXCLUSIVE-NOR Operation

Figure 1.17 shows the standard symbol of EXCLUSIVE-NOR (EX-NOR) gate. Its truth table is given in Table 1.7.

Its logic operation is specified as

$$Y = A \text{ EX-NOR } B = \overline{A \text{ EX-OR } B} = \overline{A \oplus B} = A \odot B \quad (1.9)$$

Similar to EX-OR gate, EX-NOR gate is not a basic operation and can be performed using the basic gates or universal gates, but because of its importance, it has been given a standard symbol. The EX-NOR operation is also referred to as the *coincidence* operation because it produces output of 1 when its inputs coincide in value, both 0 or both 1.

Table 1.7 Truth Table of EX-NOR Gate

Inputs		Output
$A$	$B$	$Y$
0	0	1
0	1	0
1	0	0
1	1	1

**Example 1.12**

Repeat Example 1.10 for EX-NOR gate.

***Solution***

The output waveform will be inverse of the output waveform, as shown in Fig. 1.16.

**Example 1.13**

Repeat Example 1.11 for EX-NOR gate

***Solution***

- (a)  $Y = \bar{B}$
- (b)  $Y = B$

**1.6 BOOLEAN ALGEBRA**

As discussed above, the digital signals are discrete in nature and can only assume one of the two values 0 or 1. A number system based on these two digits is known as *binary number system*. In the middle of 19th century, an English mathematician George Boole developed rules for manipulations of binary variables, known as *Boolean algebra*. This is the basis of all digital systems like computers, calculators, etc.

Binary variables can be represented by a letter symbol such as  $A, B, X, Y, \dots$ . The variable can have only one of the two possible values at any time, viz. 0 or 1. The Boolean algebraic theorems are given in Table 1.8.

From these theorems, we observe that the even numbered theorems can be obtained from their preceding odd numbered theorems by (i) interchanging  $+$  and  $\cdot$  signs, and (ii) interchanging 0 and 1.

Theorems which are related in this way are called *duals*.

Table 1.8 **Boolean Algebraic Theorems**

Theorem No.	Theorem
1.1	$A + 0 = A$
1.2	$A \cdot 1 = A$
1.3	$A + 1 = 1$
1.4	$A \cdot 0 = 0$
1.5	$A + A = A$
1.6	$A \cdot A = A$
1.7	$A + \bar{A} = 1$
1.8	$A \cdot \bar{A} = 0$
1.9	$A \cdot (B + C) = AB + AC$
1.10	$A + BC = (A + B)(A + C)$
1.11	$A + AB = A$

(Continued)

Table 1.8 **(Continued)**

Theorem No.	Theorem
1.12	$A(A+B) = A$
1.13	$A + \bar{A}B = (A+B)$
1.14	$A(\bar{A} + B) = AB$
1.15	$AB + A\bar{B} = A$
1.16	$(A+B) \cdot (A+\bar{B}) = A$
1.17	$AB + \bar{A}C = (A+C)(\bar{A}+B)$
1.18	$(A+B)(\bar{A}+C) = AC + \bar{A}B$
1.19	$AB + \bar{A}C + BC = AB + \bar{A}C$
1.20	$(A+B)(\bar{A}+C)(B+C) = (A+B)(\bar{A}+C)$
1.21	$\overline{A \cdot B \cdot C \cdot \dots} = \bar{A} + \bar{B} + \bar{C} + \dots$
1.22	$\overline{A + B + C + \dots} = \bar{A} \cdot \bar{B} \cdot \bar{C} \dots$

Theorems 1.1 to 1.8 involve a single variable only. Each of these theorems can be proved by considering every possible value of the variable. For example, in Theorem 1.1,

if  $A = 0$  then  $0 + 0 = 0 = A$

and if  $A \equiv 1$  then  $1 + 0 \equiv 1 \equiv A$

and hence the theorem is proved.

Theorems 1.9 to 1.20 involve more than one variable and can be proved by making a truth table. For example, Theorem 1.10 can be proved by making the truth table given in Table 1.9.

Table 1.9 *Truth Table to Prove Theorem 1.10*

From the table we observe that there are 8 ( $= 2^3$ ) possible combinations of the three variables  $A$ ,  $B$ , and  $C$ . For each combination, the value of  $A + BC$  is the same as that of  $(A + B)(A + C)$ , which proves the theorem. Theorems 1.21 and 1.22 are known as De Morgan's theorems. These theorems can be proved by first considering the two variable case and then extending this result. From the truth table given in Table 1.10 we get the relations

$$\overline{A \cdot B} = \overline{A} + \overline{B} \quad (1.10)$$

and

$$\overline{A + B} = \overline{A} \cdot \overline{B} \quad (1.11)$$

Table 1.10 **Truth Table to Prove De Morgan's Theorems**

$A$	$B$	$\overline{A}$	$\overline{B}$	$\overline{AB}$	$\overline{A} + \overline{B}$	$\overline{A + B}$	$\overline{A} \cdot \overline{B}$
0	0	1	1	1	1	1	1
0	1	1	0	1	1	0	0
1	0	0	1	1	1	0	0
1	1	0	0	0	0	0	0

Now consider the **NAND** operation of three variables,

$$\begin{aligned} \overline{ABC} &= \overline{(AB) \cdot C} \\ &= \overline{(A \cdot B)} + \overline{C} \\ &= \overline{A} + \overline{B} + \overline{C} \quad \text{using Eq. (1.10)} \end{aligned} \quad (1.12)$$

In a similar way, the **NOR** operation of three variables gives

$$\begin{aligned} \overline{A + B + C} &= \overline{(A + B) + C} \\ &= \overline{(A + B)} \cdot \overline{C} \\ &= \overline{A} \cdot \overline{B} \cdot \overline{C} \quad \text{using Eq. (1.11)} \end{aligned} \quad (1.13)$$

The above results can be easily extended to any number of variables.

A logic problem can be specified in terms of a set of statements. This set of statements can be represented in terms of an equation called the logic equation or in terms of a truth table. A digital circuit using the gates discussed above can be designed to realise a logic equation. In general, it is possible to simplify (minimise) a logic equation. The minimised logic equation will probably need less number of gates and/or less number of inputs for the gates. The techniques used to minimise logic equations will be discussed in Chapter 5. An example of the realisation of a circuit for a given logic equation is given below:

**Example 1.14**

Realise (design) a digital circuit for the logic equation

$$Y = \bar{A} \cdot B + A \cdot \bar{B} \quad (1.14)$$

**Solution**

This equation consists of two input variables  $A$  and  $B$  and one output variable  $Y$ . The variable  $A$  appears as  $\bar{A}$  in the term  $\bar{A} \cdot B$  and as  $A$  in the term  $A \cdot \bar{B}$ . Similarly the variable  $B$  appears as  $B$  in the term  $\bar{A} \cdot B$  and as  $\bar{B}$  in the term  $A \cdot \bar{B}$ . The two terms  $\bar{A} \cdot B$  and  $A \cdot \bar{B}$  are obtained by AND operations and the output  $Y$  is the result of OR operation performed on  $\bar{A} \cdot B$  and  $A \cdot \bar{B}$  terms. The realisation of this equation is obtained using NOT, AND and OR gates as shown in Fig. 1.18.

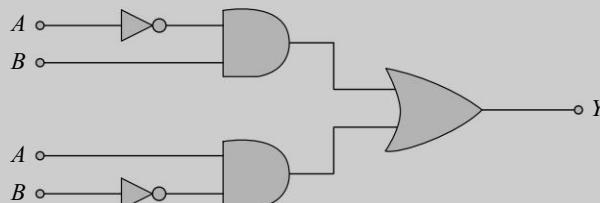


Fig. 1.18 *Realisation of Eq. (1.14)*

## 1.7 EXAMPLES OF IC GATES

All the logic functions introduced in this chapter are commercially available in integrated circuit (IC) form. For example, 7400 IC chip is a quadruple 2-input NAND gate available in 14-pin DIP. It has four identical, independent 2-input NAND gates arranged as shown in Fig. 1.19. It requires a +5 V d.c. supply (to be connected between  $V_{CC}$  and GND pins) for the operation of the gates. Table 1.11 gives some of the available gate ICs. The details of their pin connexions, electrical characteristics, etc. can be obtained from the manufacturers' data catalogues.

Some of the manufacturers are:

- Texas Instruments ([www.ti.com](http://www.ti.com))
- Philips ([www.philips.com](http://www.philips.com))
- Fairchild semiconductor ([www.fairchildsemi.com](http://www.fairchildsemi.com))

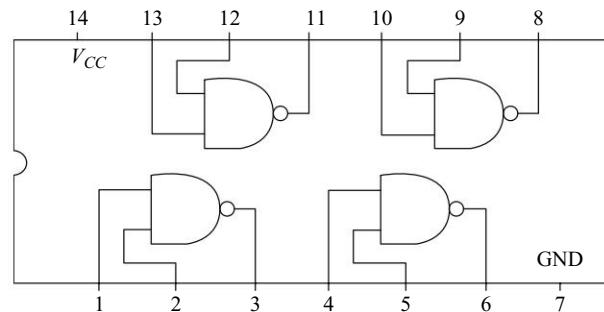


Fig. 1.19 *Block Diagram of 7400 IC*

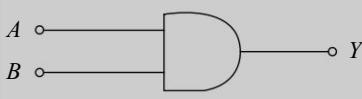
Table 1.11 *Some of the Available IC Gates*

IC No.	Description
7400	Quad 2-input NAND gates
7402	Quad 2-input NOR gates
7404	Hex inverters
7408	Quad 2-input AND gates
7410	Triple 3-input NAND gates
7411	Triple 3-input AND gates
7420	Dual 4-input NAND gates
7421	Dual 4-input AND gates
7427	Triple 3-input NOR gates
7430	8-input NAND gate
7432	Quad 2-input OR gates
7486, 74386	Quad EX-OR gates
74133	13-input NAND gate
74135	Quad EX-OR/NOR gates
74260	Dual 5-input NOR gates

## SUMMARY

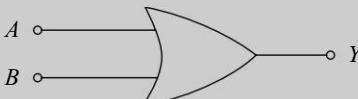
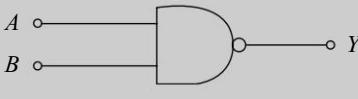
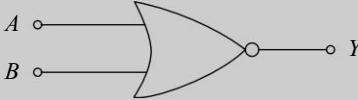
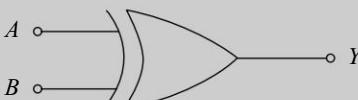
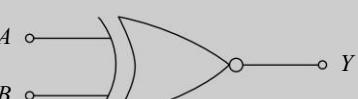
In this chapter, the basic concepts of the digital systems have been discussed. The basic features and advantages of these systems have been given briefly. The level of the treatment has been kept low to avoid any confusion. Table 1.12 summarises the operation of all the gates introduced in this chapter. For convenience, two input gates have been taken and the different symbols used for various operations are also given. A brief exposure to Boolean algebra has also been given. The techniques for the simplification of logic equations will be discussed in Chapter 5.

Table 1.12 *Summary of Logic Gates*

Gate	Logic diagram	Function	Truth table																	
			Inputs		Output															
AND		$Y = A \text{ AND } B$ $= A \cdot B$ $= A \cap B$ $= A \wedge B$ $= AB$	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	A	B	Y	0	0	0	0	1	0	1	0	0	1	1	1		
A	B	Y																		
0	0	0																		
0	1	0																		
1	0	0																		
1	1	1																		

(Continued)

Table 1.12 (Continued)

Gate	Logic diagram	Function	Truth table																		
OR		$Y = A \text{ OR } B$ $= A + B$ $= A \cup B$ $= A \vee B$	<table border="1"> <thead> <tr> <th colspan="2">Inputs</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	Inputs		Output	A	B	Y	0	0	0	0	1	1	1	0	1	1	1	1
Inputs		Output																			
A	B	Y																			
0	0	0																			
0	1	1																			
1	0	1																			
1	1	1																			
NOT (inverter)		$Y = \text{NOT } A$ $= \bar{A}$	<table border="1"> <thead> <tr> <th>Input</th> <th>Output</th> </tr> <tr> <th>A</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> </tbody> </table>	Input	Output	A	Y	0	1	1	0										
Input	Output																				
A	Y																				
0	1																				
1	0																				
NAND		$Y = A \text{ NOT AND } B$ $= A \text{ NAND } B$ $= \bar{A} \cdot \bar{B}$ $= \bar{A} \cap \bar{B}$ $= \bar{A} \wedge \bar{B}$ $= A \uparrow B$ $= \bar{A} \bar{B}$	<table border="1"> <thead> <tr> <th colspan="2">Inputs</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	Inputs		Output	A	B	Y	0	0	1	0	1	1	1	0	1	1	1	0
Inputs		Output																			
A	B	Y																			
0	0	1																			
0	1	1																			
1	0	1																			
1	1	0																			
NOR		$Y = A \text{ NOT OR } B$ $= A \text{ NOR } B$ $= \bar{A} + \bar{B}$ $= \bar{A} \cup \bar{B}$ $= \bar{A} \vee \bar{B}$ $= A \downarrow B$	<table border="1"> <thead> <tr> <th colspan="2">Inputs</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	Inputs		Output	A	B	Y	0	0	1	0	1	0	1	0	0	1	1	0
Inputs		Output																			
A	B	Y																			
0	0	1																			
0	1	0																			
1	0	0																			
1	1	0																			
EX-OR		$Y = A \text{ EX-OR } B$ $= A \oplus B$ $= \bar{A}B + A\bar{B}$	<table border="1"> <thead> <tr> <th colspan="2">Inputs</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	Inputs		Output	A	B	Y	0	0	0	0	1	1	1	0	1	1	1	0
Inputs		Output																			
A	B	Y																			
0	0	0																			
0	1	1																			
1	0	1																			
1	1	0																			
EX-NOR		$Y = \bar{A} \text{ EX-OR } \bar{B}$ $= A \text{ EX-NOR } B$ $= A \odot B$ $= \bar{A}\bar{B} + \bar{A}B$ $= \bar{A}\bar{B} + AB$	<table border="1"> <thead> <tr> <th colspan="2">Inputs</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	Inputs		Output	A	B	Y	0	0	1	0	1	0	1	0	0	1	1	1
Inputs		Output																			
A	B	Y																			
0	0	1																			
0	1	0																			
1	0	0																			
1	1	1																			

## GLOSSARY

**Active-high input** The input terminal is active (or enabled) when held at HIGH logic level.

**Active-high output** The output terminal is at HIGH logic level when active (or enabled).

**Active-low input** The input terminal is active (or enabled) when held at LOW logic level.

**Active-low output** The output terminal is at low logic level when active (or enabled).

**Analog circuit** An electronic circuit that processes analog signals.

**Analog signal** A continuous signal that can have any value in a given range. It is also known as continuous signal.

**Analog system** An electronic system that consists of analog circuits and/or devices.

**AND gate** A logic circuit whose output is 1 if and only if all its inputs are 1.

**Binary** Having two states.

**Binary number system** A number system with base (or radix) 2, i.e. only two symbols 0 and 1 are used to represent any number.

**Binary variable** A variable that can have only two values 0 and 1.

**Bit** A binary digit 0 and 1.

**Boolean algebra** The algebra of binary variables.

**Boolean function** A well defined relationship between binary variables specified by either a Boolean equation or a truth table.

**Boolean variable** Same as the binary variable.

**Bubble** A small circle indicating inversion operation or active-low condition.

**Chip** A piece of silicon (or any semiconductor material) on which an integrated circuit is fabricated.

**Computer** An electronic digital system that processes data. See also digital computer.

**Digital circuit** An electronic circuit that processes digital signals.

**Digital computer** A programmable digital system capable of performing various arithmetic and logical operations.

**Digital electronics** Branch of electronics which deals with the digital devices, circuits and systems.

**Digital signal** A signal with only two discrete values. These are usually represented by LOW and HIGH or 0 and 1.

**Digital system** An electronic system consisting of digital circuits and/or devices.

**DIP (Dual-in-line package)** A semiconductor chip package having two rows of pins perpendicular to the edges of the package.

**Disable** Prohibits an activity from proceeding or output(s) to be produced in a digital circuit. Also known as INHIBIT.

**Dual** Two boolean functions are said to be dual of each other if any one of these is obtained from the other one by (i) interchanging + and · signs, and (ii) interchanging 0 and 1.

**Enable** Allows activity to proceed or output(s) to be produced in a digital circuit.

**EX-NOR (Exclusive-NOR) gate** A two input gate that produces a high output only when both the inputs are same.

**EX-OR (Exclusive-OR) gate** A two input gate whose output is logic 0 when both the inputs are equal and logic 1 when they are unequal.

**False** One of the states of a logic circuit, the other state is true.

**FILP-FLOP** It is a basic memory element in digital systems. It is same as bistable multivibrator.

**Gate** A logic circuit in which the output depends upon the inputs according to some logic rules.

**High-level** The voltage corresponding to logic 1.

**IC package** An integrated circuit chip packaged as a single multilead component. For example DIP.

**Inhibit** Same as disable.

**Integrated circuit (IC)** A small semiconductor chip containing several electronic circuits.

**Inversion** The process of complementing a logic signal.

**Inversion circle** Same as bubble.

**Inverter** A logic gate whose output is the complement of its input.

**Logic circuit** An electronic circuit that operates on digital signals in accordance with a logic function.

**Logic family** A group of logic circuits built around a standardised integrated circuit technology. For example, transistor-transistor logic (TTL), complementary metal-oxide-semiconductor logic (CMOS) etc.

**Logical variable** Same as binary variable.

**Logic gate** Same as gate.

**LOW-level** The voltage corresponding to logic 0.

**Memory** A device that stores binary information.

**Microprocessor** A semiconductor IC chip with the capabilities of CPU of a computer.

**NAND gate** A logic gate whose output is logic 0 if and only if all of its inputs are logic 1.

**Negative logic system** Logic system in which the lower of the two levels is represented by 1 and the higher level is represented by 0.

**Noise** Unwanted electrical signals which are random in nature.

**NOR gate** A logic gate whose output is logic 1 if and only if all of its inputs are logic 0.

**NOT gate** Same as inverter.

**OFF** One of the states of a logic circuit, the other state is ON.

**ON** One of the states of a logic circuit, the other state is OFF.

**OR gate** A logic gate whose output is logic 0 if and only if all its inputs are logic 0.

**Positive logic system** Logic system in which the higher of the two levels is represented by 1 and the lower level is represented by 0.

**Programmable ICs** ICs which can be programmed for desired purpose by a user.

**Switching speed** Speed with which an electronic switch can change from ON to OFF and vice-versa. It is usually expressed in terms of the propagation delay time.

**True** One of the states of a logic circuit, the other state is *False*.

**Truth table** A table that gives outputs for all possible combinations of inputs to a logic circuit.

**Universal gate** A gate that can perform all the basic logical operations, such as NAND, and NOR .

## REVIEW QUESTIONS

- 1.1 Ordinary electrical switch is \_\_\_\_\_ device. (analog/digital)
- 1.2 A train of pulses is \_\_\_\_\_ signal. (analog/digital)
- 1.3 The output of an AND gate is *high* if and only if all its inputs are \_\_\_\_\_. (high/low)
- 1.4 If one of the inputs to an OR gate is *high* its output will be \_\_\_\_\_. (high/low)
- 1.5 An AND gate output will always differ from an OR gate output for the same input conditions. (True/False)
- 1.6 An OR gate is DISABLED by connecting one of its inputs to logic level \_\_\_\_\_. (0/1)
- 1.7 To ENABLE an OR gate, one of its inputs is connected to logic level \_\_\_\_\_. (0/1)
- 1.8 To INHIBIT (or DISABLE) an AND gate one of its inputs is connected to logic level \_\_\_\_\_. (0/1)
- 1.9 To ENABLE an AND gate one of its inputs is connected to logic level \_\_\_\_\_. (0/1)
- 1.10 An AND gate is ENABLED by connecting one of its inputs to logic level \_\_\_\_\_. (0/1)
- 1.11 To DISABLE a NOR gate one of its inputs needs to be connected to logic level \_\_\_\_\_. (0/1)
- 1.12 One of the inputs of an AND gate is labelled as ENABLE. This control input is \_\_\_\_\_. (active-low/active-high)
- 1.13 One of the inputs of a NOR gate is labelled as ENABLE. This control input is \_\_\_\_\_. (active-low/active-high)
- 1.14 The universal gates cannot be used as inverters. (True/False)
- 1.15 EXCLUSIVE-OR and EXCLUSIVE-NOR gates can be used as inverters. (True/False)
- 1.16 An EX-OR gate can be used to compare digital signals. (True/False)
- 1.17 If one of the inputs of an EX-OR gate is *high*, its output will be \_\_\_\_\_. (same as other input/inverse of other input)
- 1.18 The number of rows in a truth table of 4 variables is \_\_\_\_\_. .
- 1.19 A 3-input NOR gate is required to detect the simultaneous occurrence of all the inputs in the LOW state. Its output is \_\_\_\_\_. (active-low/active-high)
- 1.20 The number of 3-input NAND gates in a 14-pin IC is \_\_\_\_\_. .
- 1.21 The minimum member of bits required to distinguish 108 distinct objects is \_\_\_\_\_. .

## PROBLEMS

- 1.1 Which of the following systems are analog and which are digital? Why?
  - (a) Pressure gauge
  - (b) An electronic counter used to count persons entering an exhibition
  - (c) Clinical thermometre
  - (d) Electronic calculator
  - (e) Transistor radio receiver
  - (f) Ordinary electric switch.
  - (g) Electronic Voting Machine (EVM)
- 1.2 In the circuits of Fig. 1.20 the switches may be ON (1) or OFF (0) and will cause the bulb to be ON (1) or OFF (0).
  - (a) Determine all possible conditions of the switches for the bulb to be ON (1)/OFF (0) in each of the circuits.
  - (b) Represent the information obtained in part (a) in the form of truth table.
  - (c) Name the operation performed by each circuit (refer to Table 1.12).

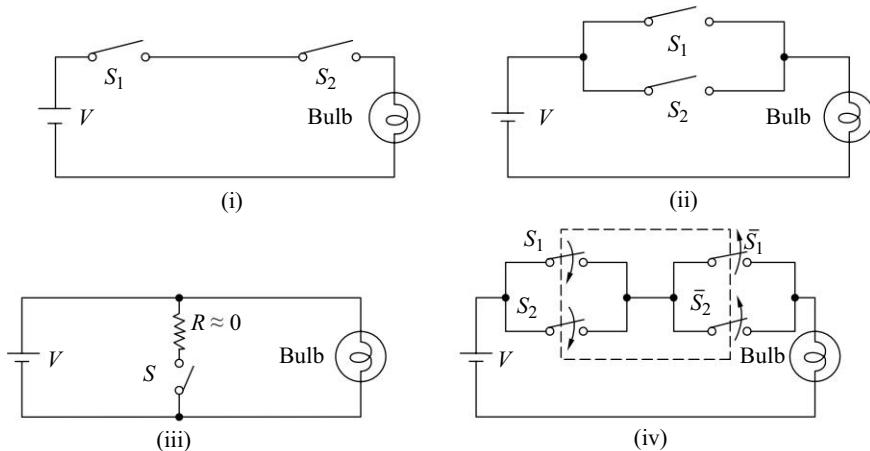


Fig. 1.20 Circuits for Problem 1.2

- 1.3 The voltage waveforms shown in Fig. 1.21 are applied at the inputs of 2-input AND, OR, NAND, NOR, EX-NOR, and EX-OR gates. Determine the output waveform in each case.

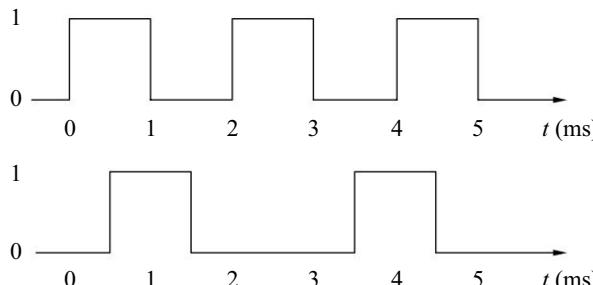


Fig. 1.21 Waveforms for Problem 1.3

- 1.4 Find the relationship between the inputs and output for each of the gates shown in Fig. 1.22. Name the operation performed in each case (refer to Table 1.12).

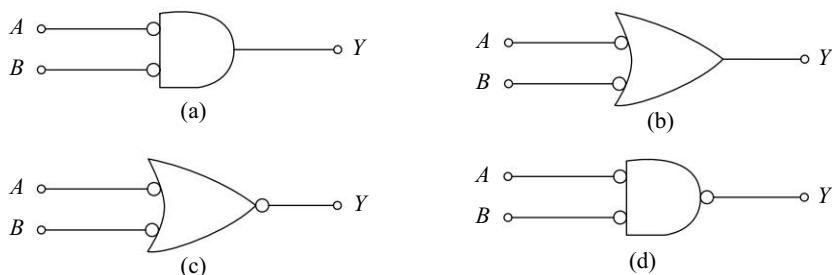


Fig. 1.22 Circuits for Problem 1.4

- 1.5 Make the truth tables for each of the circuits of Figs. 1.11 and 1.14 and verify the operation performed.
- 1.6 For each of the following statements indicate the logic gate(s) AND, OR, NAND, NOR for which it is true.
- All LOW inputs produce a HIGH output.
  - Output is HIGH if and only if all inputs are HIGH.
  - Output is LOW if and only if all inputs are HIGH.
  - Output is LOW if and only if all inputs are LOW.
- 1.7 For the logic expression,

$$Y = A\bar{B} + \bar{A}B$$

- Obtain the truth table.
  - Name the operation performed.
  - Realise this operation using AND, OR, NOT gates.
  - Realise this operation using only NAND gates.
- 1.8 Prove the following:
- A positive logic AND operation is equivalent to a negative logic OR operation and vice-versa.
  - A positive logic NAND operation is equivalent to a negative logic NOR operation and vice-versa.
- 1.9 Prove the following using the Boolean algebraic theorems:
- $A + \bar{A} \cdot B + A \cdot \bar{B} = A + B$
  - $A \cdot B + \bar{A} \cdot B + \bar{A} \cdot \bar{B} = \bar{A} + B$
  - $\bar{A}\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + ABC = AB + BC + CA$
- 1.10 Prove the logic equations of Problem 1.9 using the truth table approach.
- 1.11 Realise the left hand side and the right hand side of the logic equations of problem 1.9 using AND, OR, and NOT gates and find the saving in hardware in each case (number of gates and the number of inputs for the gates).
- 1.12 Prove the following using De Morgan's theorems:
- $AB + CD = \overline{AB} \cdot \overline{CD}$
  - $(A + B) \cdot (C + D) = \overline{(A + B)} + \overline{(C + D)}$
- And hence, prove the following statements:
- An AND-OR configuration is equivalent to a NAND-NAND configuration.
  - An OR-AND configuration is equivalent to a NOR-NOR configuration.
- 1.13 (a) Realise the logic equation (a) of Problem 1.12 using
  - AND and OR gates.
  - only NAND gates.
(b) Realise the logic equation (b) of Problem 1.12 using
  - OR and AND gates.
  - only NOR gates.
- 1.14 Verify that the following operations are commutative and associative
  - AND
  - OR
  - EX-OR
- 1.15 Verify that the following operations are commutative but not associative.
  - NAND
  - NOR

# CHAPTER 4

# DIGITAL LOGIC FAMILIES

## 4.1 INTRODUCTION

The switching characteristics of semiconductor devices have been discussed in Chapter 3. Basically, there are two types of semiconductor devices: bipolar and unipolar. Based on these devices, digital integrated circuits have been made which are commercially available. Various digital functions are being fabricated in a variety of forms using bipolar and unipolar technologies. A group of compatible ICs with the same logic levels and supply voltages for performing various logic functions have been fabricated using a specific circuit configuration which is referred to as a *logic family*.

### 4.1.1 Bipolar Logic Families

The main elements of a bipolar IC are resistors, diodes (which are also capacitors) and transistors. Basically, there are two types of operations in bipolar ICs:

1. Saturated, and
2. Non-saturated.

In saturated logic, the transistors in the IC are driven to saturation, whereas in the case of non-saturated logic, the transistors are not driven into saturation.

The saturated bipolar logic families are:

1. Resistor-transistor logic (RTL),
2. Direct-coupled transistor logic (DCTL),
3. Integrated-injection logic (I<sup>2</sup>L),
4. Diode-transistor logic (DTL),
5. High-threshold logic (HTL), and
6. Transistor-transistor logic (TTL).

The non-saturated bipolar logic families are:

1. Schottky TTL, and
2. Emitter-coupled logic (ECL).

### 4.1.2 Unipolar Logic Families

MOS devices are unipolar devices and only MOSFETs are employed in MOS logic circuits.

The MOS logic families are:

1. PMOS,
2. NMOS, and
3. CMOS (5-V and low-voltage CMOS)

While in PMOS only *p*-channel MOSFETs are used and in NMOS only *n*-channel MOSFETs are used, in complementary MOS (CMOS), both *p*- and *n*-channel MOSFETs are employed and are fabricated on the same silicon chip.

### 4.1.3 BiCMOS Logic Family

BiCMOS logic circuits use CMOS devices for input and logic operations and bipolar devices for output.

## 4.2 CHARACTERISTICS OF DIGITAL ICs

With the widespread use of ICs in digital systems and with the development of various technologies for the fabrication of ICs, it has become necessary to be familiar with the characteristics of IC logic families and their relative advantages and disadvantages. Digital ICs are classified either according to the complexity of the circuit, as the relative number of individual basic gates (2-input NAND gates) it would require to build the circuit to accomplish the same logic function or the number of components fabricated on the chip. The classification of digital ICs is given in Table 4.1.

Table 4.1 *Classification of Digital ICs*

IC Classification	Equivalent individual basic gates	Number of components
Small-scale integration (SSI)	Less than 12	Up to 99
Medium-scale integration (MSI)	12–99	100–999
Large-scale integration (LSI)	100–999	1,000–9,999
Very large-scale integration (VLSI)	Above 1,000	Above 10,000

The various characteristics of digital ICs used to compare their performances are:

1. Speed of operation,
2. Power dissipation,
3. Figure of merit,
4. Fan-out,
5. Current and voltage parameters,
6. Noise immunity,
7. Operating temperature range,
8. Power supply requirements, and
9. Flexibilities available.

## 4.2.1 Speed of Operation

The speed of a digital circuit is specified in terms of the propagation delay time. The input and output waveforms of a logic gate are shown in Fig. 4.1. The delay times are measured between the 50 per cent voltage levels of

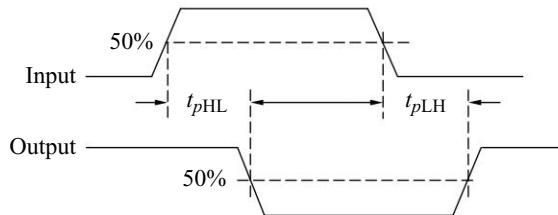


Fig. 4.1 *Input and Output Voltage Waveforms to Define Propagation Delay Times*

input and output waveforms. There are two delay times:  $t_{pHL}$ , when the output goes from the HIGH state to the LOW state and  $t_{pLH}$ , corresponding to the output making a transition from the LOW state to the HIGH state. The propagation delay time of the logic gate is taken as the average of these two delay times.

## 4.2.2 Power Dissipation

This is the amount of power dissipated in an IC. It is

determined by the current,  $I_{cc}$ , that it draws from the  $V_{cc}$  supply, and is given by  $V_{cc} \times I_{cc}$ .  $I_{cc}$  is the average value of  $I_{cc}(0)$  and  $I_{cc}(1)$ . This power is specified in milliwatts. It is known as static power dissipation, i.e., the power consumed by the circuit when input signals are not changing.

## 4.2.3 Figure of Merit

The figure of merit of a digital IC is defined as the product of speed and power. The speed is specified in terms of propagation delay time expressed in nanoseconds.

$$\text{Figure of merit} = \text{propagation delay time (ns)} \times \text{power (mW)}$$

It is specified in pico joules ( $ns \times mW = pJ$ )

A low value of speed-power product is desirable. In a digital circuit, if it is desired to have high speed, i.e. low propagation delay, then there is a corresponding increase in the power dissipation and vice-versa.

## 4.2.4 Fan-Out

This is the number of similar gates which can be driven by a gate. High fan-out is advantageous because it reduces the need for additional drivers to drive more gates.

## 4.2.5 Current and Voltage Parameters

The following currents and voltages are specified which are very useful in the design of digital systems.

*High-level input voltage,  $V_{IH}$ :* This is the minimum input voltage which is recognised by the gate as logic 1.

*Low-level input voltage,  $V_{IL}$ :* This is the maximum input voltage which is recognised by the gate as logic 0.

*High-level output voltage,  $V_{OH}$ :* This is the minimum voltage available at the output corresponding to logic 1.

*Low-level output voltage,  $V_{OL}$ :* This is the maximum voltage available at the output corresponding to logic 0.

*High-level input current,  $I_{IH}$ :* This is the minimum current which must be supplied by a driving source corresponding to 1 level voltage.

*Low-level input current,  $I_{IL}$ :* This is the minimum current which must be supplied by a driving source corresponding to 0 level voltage.

*High-level output current,  $I_{OH}$ :* This is the maximum current which the gate can sink in 1 level.

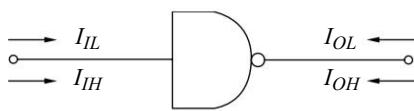


Fig. 4.2 A Gate With Current Directions Marked

*Low-level output current,  $I_{OL}$ :* This is the maximum current which the gate can sink in 0 level.

*High-level supply current,  $I_{CC}$  (1):* This is the supply current when the output of the gate is at logic 1.

*Low-level supply current,  $I_{CC}$  (0):* This is the supply current when the output of the gate is at logic (0).

The current directions are illustrated in Fig. 4.2.

#### 4.2.6 Noise Immunity

The input and output voltage levels defined above are shown in Fig. 4.3. Stray electric and magnetic fields may induce unwanted voltages, known as *noise*, on the connecting wires between logic circuits. This may

cause the voltage at the input to a logic circuit to drop below  $V_{IH}$  or rise above  $V_{IL}$  and may produce undesired operation. The circuit's ability to tolerate noise signals is referred to as the *noise immunity*, a quantitative measure of which is called *noise margin*. Noise margins are illustrated in Fig. 4.3.

The noise margins defined above are referred to as *dc noise margins*. Strictly speaking, the noise is generally thought of as an a.c. signal with amplitude and pulse width. For high speed ICs, a pulse width of a few microseconds is extremely long in comparison to the propagation delay time of the circuit and therefore, may be treated as d.c. as far as the response of the logic circuit is concerned. As the noise pulse width decreases and

approaches the propagation delay time of the circuit, the pulse duration is too short for the circuit to respond. Under this condition, a large pulse amplitude would be required to produce a change in the circuit output. This means that a logic circuit can effectively tolerate a large noise amplitude if the noise is of a very short duration. This is referred to as *ac noise margin* and is substantially greater than the dc noise margin. It is generally supplied by the manufacturers in the form of a curve between noise margin and noise pulse width.

#### 4.2.7 Operating Temperature

The temperature range in which an IC functions properly must be known. The accepted temperature ranges are: 0 to + 70 °C for consumer and industrial applications and -55 °C to +125 °C for military purposes.

#### 4.2.8 Power Supply Requirements

The supply voltage(s) and the amount of power required by an IC are important characteristics required to choose the proper power supply.

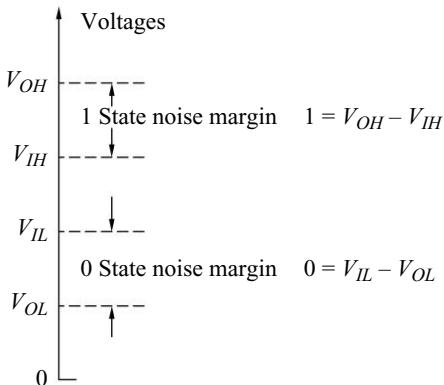


Fig. 4.3 Voltage Levels and Noise Margins of ICs

## 4.2.9 Flexibilities Available

Various flexibilities are available in different IC logic families and these must be considered while selecting a logic family for a particular job. Some of the flexibilities available are:

1. *The breadth of the series:* Type of different logic functions available in the series.
2. *Popularity of the series:* The cost of manufacturing depends upon the number of ICs manufactured. When a large number of ICs of one type are manufactured, the cost per function will be very small and it will be easily available because of multiple sources.
3. *Wired-logic capability:* The outputs can be connected together to perform additional logic without any extra hardware.
4. *Availability of complement outputs:* This eliminates the need for additional inverters.
5. *Type of output:* Passive pull-up, active pull-up, open-collector/drain, and tristate. These will be explained in subsequent sections.

## 4.3 RESISTOR-TRANSISTOR LOGIC (RTL)

The resistor-transistor logic was the most popular form of logic in common use before the development of ICs. RTL circuits consist of resistors and transistors and was the earliest logic family to be integrated. Although RTL has become obsolete now, because of its simplicity and for historical reasons, it is proper to devote some attention to it and introduce some of the important concepts, useful for all types of gates, through this. The basic RTL gate is a NOR gate as shown in Fig. 4.4. For the sake of simplicity, a two-input NOR gate driving  $N$  similar gates is shown in the figure, which can be extended to accommodate a larger number of inputs. The number of input terminals is referred to as the *fan-in*.

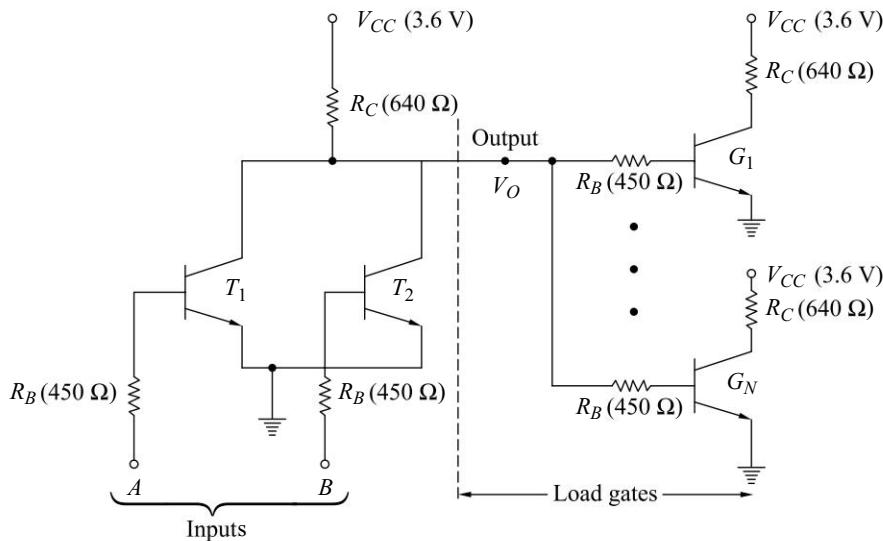


Fig. 4.4 A 2-input RTL NOR Gate Driving  $N$  Similar Gates

### 4.3.1 Logic Operation

Inputs representing the logic levels are applied at  $A$  and  $B$  terminals. The voltage corresponding to LOW level should be low enough to drive the corresponding transistor to cut-off. Similarly, the input voltage corresponding to HIGH level should be high enough to drive the corresponding transistor to saturation.

If both the inputs are LOW, transistors  $T_1$  and  $T_2$  are cut-off and the output is HIGH. A HIGH level on any input will drive the corresponding transistor to saturation causing the output to go LOW. The LOW (0) level output voltage is  $V_{CE,sat}$  of a transistor ( $\sim 0.2$  V) and the HIGH (1) level output voltage depends on the number of gates connected to the output. This causes the output voltage to be variable and is a deciding factor for the fan-out of the gate.

### 4.3.2 Loading Considerations

If all the inputs to the gate are LOW, the output is HIGH and if the gate is not driving any other gate, i.e. no load is connected, the output voltage will be slightly less than  $V_{CC}$  (there is voltage drop across the common collector resistor due to  $I_{CO}$  of  $T_1$  and  $T_2$ ).

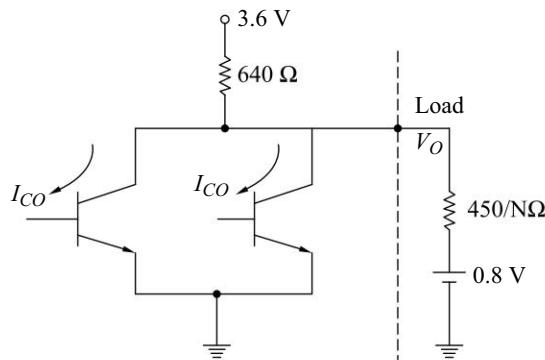


Fig. 4.5 A Circuit Illustrating the Equivalent Circuit at the Input of the Load Gates

When  $N$  similar gates are being driven, the load will be equivalent to a resistor of value  $450/N$  ohms in series with a voltage source of 0.8 V (being the voltage between base and emitter of a transistor in saturation). The relevant portion of the circuit is shown in Fig. 4.5.

The base current for each load transistor is

$$I_B = \left( \frac{3.6 - 0.8}{640 + \frac{450}{N}} \right) \cdot \frac{1}{N} = \frac{2.8}{640N + 450} \quad (4.1)$$

The collector current for the load transistor in saturation is

$$I_{C,sat} = \frac{3.6 - 0.2}{640} = 5.31 \text{ mA} \quad (4.2)$$

The value of  $N$  must satisfy the following relation,

$$h_{FE} \cdot I_B \geq I_{C,sat} \quad (4.3)$$

For  $N = 5$ ,  $I_B = 0.767$  mA. Therefore,  $h_{FE}$  must be greater than 7.

### 4.3.3 Noise Margins

When the output is in 0 state  $V_o = 0.2$  V. If this voltage becomes about 0.5 V (cut-in voltage of transistor), the load transistor comes to conduction which causes malfunction of the circuit. Hence, the logic 0 noise margin  $\Delta 0 \approx 0.3$  V.

The logic 1 noise margin depends upon the number of gates being driven. For  $N = 5$ ,

$$V_o = \frac{90}{90 + 640} \times (3.6) + \frac{640}{90 + 640} \times (0.8) = 1.14 \text{ V} \quad (4.4)$$

For  $h_{FE} = 10$ , the total base current required for load transistors to be driven into saturation will be  $5 \times \left[ \frac{5.31}{10} \right] \text{ mA}$  and the corresponding  $V_o$  must be 1.04 V. Therefore, the noise margin for 1 level is  $\Delta 1 = 1.14 - 1.04 = 0.1 \text{ V}$ .

#### 4.3.4 Propagation Delay Time

The propagation delay time is also affected by the number of gates it drives. When the output of the gate is in LOW state all the load transistors are cut-off and the base-emitter junction of each of these transistors appears to be a capacitor,  $C$ . When the output has to change from LOW to HIGH level due to changes at the input, it will do so with a time constant given by

$$\left( 640 + \frac{450}{N} \right) NC = (640N + 450) C \quad (4.5)$$

The resistance in the collector circuit pulls up the output voltage from LOW to HIGH level and hence is known as the *pull-up resistor*. It is passive pull-up in this case in contrast to an *active pull-up* which can be used to decrease the propagation delay time. Active pull-up will be discussed later.

#### 4.3.5 Current Source Logic

The gate supplies current to the load transistors when in 1 level, whereas the leakage-current (reverse-saturation base current) of load transistors flow through  $T_1$  or  $T_2$  in 0 level. Since the source current is much greater than the sink current, it is known as *current source logic*.

#### 4.3.6 Wired-Logic

If the outputs of the gates are connected together as shown in Fig. 4.6, the output  $Y$  is given by

$$\begin{aligned} Y &= Y_1 \cdot Y_2 \\ &= \overline{A + B} \cdot \overline{C + D} \\ &= \overline{A + B + C + D} \end{aligned}$$

This shows that fan-in can be increased by this connection which is referred to as *wired- AND* or *implied-AND*. The effect of this connection on fan-out, power dissipation and speed of operation can be seen in Prob. 4.3.

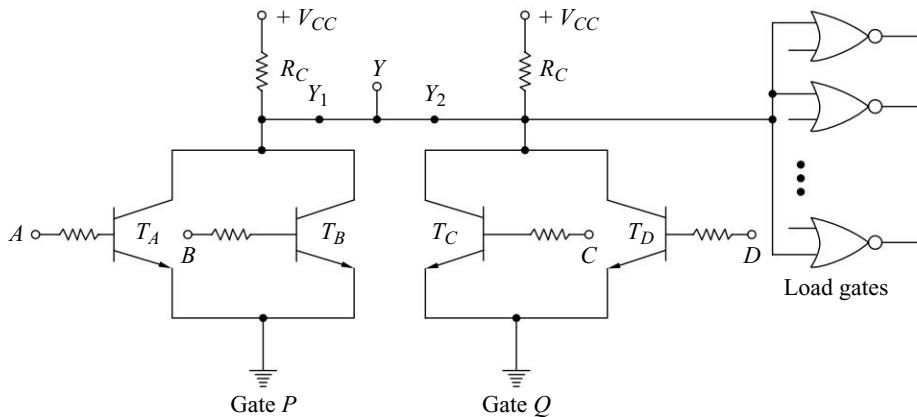


Fig. 4.6 *Wired-AND Connection of RTL Gates Driving Similar Gates*

The characteristics of RTL can be summarised as: Poor noise margin, poor fan-out capabilities, low speed, and high power dissipation.

#### 4.4 DIRECT-COUPLED TRANSISTOR LOGIC (DCTL)

In the RTL gate of Fig. 4.4, if the base resistors  $R_B$  are omitted, we obtain what is known as the direct-coupled transistor logic (DCTL) gate, in which the inputs are directly coupled to the bases. This circuit performs positive NOR logic and the voltages corresponding to logic 1 and 0 levels are  $V_{BE,\text{sat}}$  ( $\sim 0.8$  V) and  $V_{CE,\text{sat}}$  ( $\sim 0.2$  V) respectively. The separation between the logic 1 and 0 level voltages, which is referred to as the *logic swing*, is very small ( $V_{BE,\text{sat}} - V_{CE,\text{sat}} = 0.6$  V). Therefore, the noise margin of this circuit is very poor.

Although the DCTL is simpler than RTL, it never became popular because of the problem of *current hogging*. The gate should be able to drive the transistors of the load gates to saturation corresponding to logic level 1.

This does not pose any problem if all the transistors have same input characteristics but, unfortunately, the input characteristics differ due to the manufacturing tolerances of different IC packages operating at different temperatures. Owing to these differences, the saturation voltages of the load transistors may be different. Let the base-emitter voltages of the transistors corresponding to saturation be 0.78, 0.79, and 0.80 V. The transistor with the base-emitter voltage of 0.78 V, when it enters saturation, will not allow other transistors to enter saturation and will take whole of the current supplied from the driver gate. This is known as *current hogging*.

## 4.5 INTEGRATED-INJECTION LOGIC (I<sup>2</sup>L)

As discussed above, the DCTL suffers from the difficulty of current hogging which makes it unsuitable. However, based on DCTL a new logic referred to as the integrated-injection logic (I<sup>2</sup>L), has been developed. I<sup>2</sup>L has the simplicity of DCTL, uses very small silicon chip area, consumes very little power, and requires only four masks and two diffusions (compared to five masks and three diffusions for BJT) and hence, is easier and cheaper to fabricate. Due to these advantages it is eminently suited for medium- and large-scale integration. It is not used for small-scale integration and is the only saturated bipolar logic employed for large-scale integration. Texas Instruments SBP 9900 is a 16-bit microprocessor using I<sup>2</sup>L technology.

and it is in the range of 0.1 to 0.7 pJ. The silicon area required is very small and packing density in the range 120 to 200 gates per square millimetre have been realised.

## 4.6 DIODE-TRANSISTOR LOGIC (DTL)

The diode-transistor logic is somewhat more complex than RTL but because of its greater fan-out and improved noise margins it has replaced RTL. Its main disadvantage is slower speed and because of this it was modified and emerged as transistor-transistor logic (TTL) which is the most popular logic family today, as far as small- and medium-scale ICs are concerned. Although TTL has completely replaced DTL, for historical reasons as well as for better appreciation of TTL circuit, it is worthwhile discussing the details of DTL.

DTL circuit using discrete components was made using input diodes and a transistor inverter (NOT), which was modified for integrated circuit implementation as shown in Fig. 4.12.

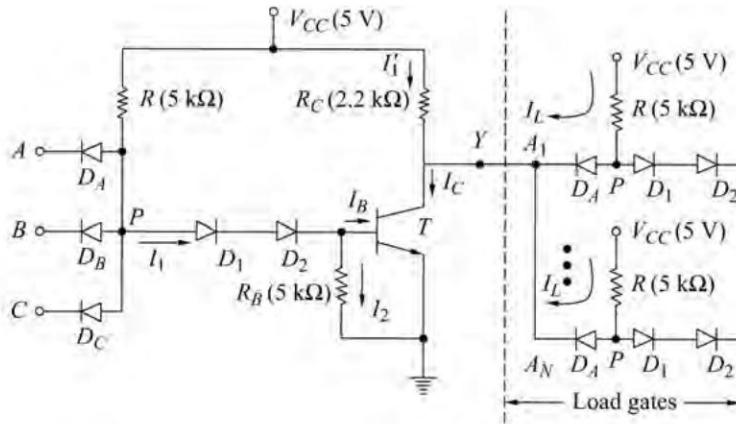


Fig. 4.12 A 3-Input DTL NAND Gate Driving  $N$  Similar Gates

### 4.6.1 Operation of DTL NAND Gate

The basic DTL gate is a NAND gate. A 3-input NAND gate driving  $N$  similar gates is shown in Fig. 4.12. The input diodes  $D_A$ ,  $D_B$ , and  $D_C$  conduct through the resistor  $R$ , if the corresponding input is in the LOW state, while corresponding to HIGH state the diode is nonconducting. Therefore, if at least one of the inputs is LOW, the diode connected to this input conducts and the voltage  $V_p$  at point  $P$  is one diode drop above the low level voltage at the input. The voltage  $V_p$  should be such as to keep  $T$  in cut-off. Therefore, the output of  $T$  is  $V_{CC}$ . On the other hand, if all the three inputs are in HIGH state, the input diodes are cut-off and consequently current flowing from  $V_{CC}$  through  $R$  should be sufficient to drive  $T$  in saturation. Therefore, the output of  $T$  is  $V_{CE,sat}$ .

If we consider the voltages corresponding to logic 1 and 0 as  $V_{CC}$  and  $V_{CE,sat}$  respectively, this circuit performs NAND operation. The following example illustrates the loading (fan-out) considerations and the noise-margins.

## Example 4.1

For the DTL NAND gate of Fig. 4.12 calculate (a) fan-out (b) noise-margins, and (c) average power,  $P$ , dissipated by the gate. The diode and transistor parameters are:

Diode: Voltage across a conducting diode = 0.7 V  
 Cut-in voltage  $V_p = 0.6$  V

Transistor: Cut-in voltage  $V_{\gamma} = 0.5$  V  
 $V_{BE,sat} = 0.8$  V  
 $V_{CE,sat} = 0.2$  V  
 $h_{FE} = 30$

### Solution

(a) As discussed above, the logic levels are:

$$\begin{aligned} \text{LOW level} &= V(0) = V_{CE,sat} = 0.2 \text{ V} \\ \text{HIGH level} &= V(1) = V_{CC} = 5 \text{ V} \end{aligned}$$

(i) If all the inputs are HIGH, the input diodes are reverse-biased. Assuming diodes  $D_1, D_2$  to be conducting and  $T$  to be in saturation, the voltage  $V_p = 0.7 + 0.7 + 0.8 = 2.2$  V.

Writing Kirchhoff's current law (KCL) equation at the base of  $T$ ,

$$I_B = I_1 - I_2$$

where

$$I_1 = \frac{V_{CC} - V_p}{R} = \frac{5 - 2.2}{5} = 0.56 \text{ mA}$$

and

$$I_2 = \frac{V_{BE,sat}}{R_B} = \frac{0.8}{5} = 0.16 \text{ mA}$$

which gives a base current  $I_B = 0.4$  mA. The collector current (without load gates connected) is

$$I_C = \frac{V_{CC} - V_{CE,sat}}{R_C} = \frac{5 - 0.2}{2.2} = 2.182 \text{ mA}$$

Since  $h_{FE} \times I_B = 30 \times 0.4 = 12$  mA is greater than  $I_C$  (2.182 mA), it is confirmed that the transistor is in saturation and the output is in LOW state. Now, if  $N$  load gates are fed from this gate, the input diodes of the driven gates will conduct through the output transistor  $T$ , i.e.  $T$  acts as a sink for the current in the input to the gates it drives. Assuming that all the other inputs to each of the load gates are HIGH except the one driven by

$T$ , the current  $I_L = \frac{V_{CC} - V_p}{R} = \frac{5 - 0.9}{5} = 0.82$  mA. This current is referred to as *standard load*. The fan-out is given by  $I_C \leq h_{FE} I_L$ , or  $0.82 N + 2.182 \leq 12$  mA or  $N < 12$  since  $N$  must be an integer. A conservative choice is  $N = 10$ . The Maximum collector current rating of  $T$  must be about 12 mA.

(ii) If at least one of the inputs is LOW, the corresponding input diode conducts and  $V_p = 0.2 + 0.7 = 0.9$  V. The minimum voltage required for  $D_1, D_2$ , and  $T$  to be conducting is  $0.6 + 0.6 + 0.5 = 1.7$  V, which confirms that  $D_1, D_2$  are nonconducting and hence  $T$  is cut-off. Consequently, the output voltage is  $V_{CC}$  (5 V) if the load gates are not connected.

If the load gates are connected, the input diodes of the load gates are nonconducting, which means the reverse-saturation current of these diodes must be supplied through the collector resistor  $R_C$ , which will

produce a voltage drop across  $R_c$  and consequently the output voltage corresponding to HIGH state will be a little less than  $V_{CC}$ . The maximum current which can be supplied by the gate will depend upon  $V_{OH}$ . The fan-out is determined on the basis of maximum current.

- (b) (i) If all the inputs are HIGH, the output is LOW. Since  $V_p = 2.2$  V, the input diodes are reverse-biased by  $5 - 2.2 = 2.8$  V. Since the cut-in voltage of the diode is 0.6 V, a negative noise spike of at least 3.4 V present at the input will cause malfunction of the circuit, i.e. the 0 level noise margin  $\Delta 0 = 3.4$  V.
- (ii) If at least one input is LOW, the output is HIGH. Since  $V_p = 0.9$  V and a voltage of at least 1.7 V [part a (ii)] is required for  $D_1$ ,  $D_2$ , and  $T$  to conduct, therefore a positive noise spike of at least 0.8 V will cause malfunction of the circuit, i.e. the 1 level noise margin  $\Delta 1 = 0.8$  V.
- (c) The power  $P(0)$  when the output is LOW is given by  $P(0) = V_{CC}(I_1 + I'_1) = 5(0.56 + 2.182) = 13.71$  mW. When the output is in the HIGH state at least one of the input diodes conduct. Therefore,  $I_1 = 0.82$  mA and  $I'_1 = 0$  Hence  $P(1) = (0.82)(5) = 4.1$  mW.

If we assume that the occurrence of LOW and HIGH is equally likely then the average power is

$$P_{av} = \frac{P(0) + P(1)}{2} = \frac{13.71 + 4.1}{2} = 8.905 \text{ mW}$$

## 4.6.2 Propagation Delays

Delays are associated with the turning-on (*turn-on delay*) and the turning-off (*turn-off delay*) of the output transistor. While turning on, any capacitance shunting the output of the gate discharges rapidly through the low impedance of the output transistor in saturation. On the other hand, at turn-off the shunt capacitor must charge through the pull-up resistor  $R_c$  in addition to the storage time delay. The turn-off delay is considerably larger than the turn-on delay, often by a factor of 2 or 3. The propagation delay time of commercially available DTL gates are of the order of 30 to 80 ns.

## 4.6.3 Current Sink Logic

This gate supplies the reverse-saturation current of input diodes of the load gates in 1 state and sinks the current flowing through the forward-biased input diodes of the load gates in the output transistor of the gate in 0 state. Since the sink current is much greater than the source current, this is known as *current sink logic*.

## 4.6.4 Wired-Logic

If the outputs of gates are connected together as shown in Fig. 4.13, additional logic is performed without additional hardware. This type of connection is referred to as *wired-logic*, *wired- AND*, or *implied-AND*.

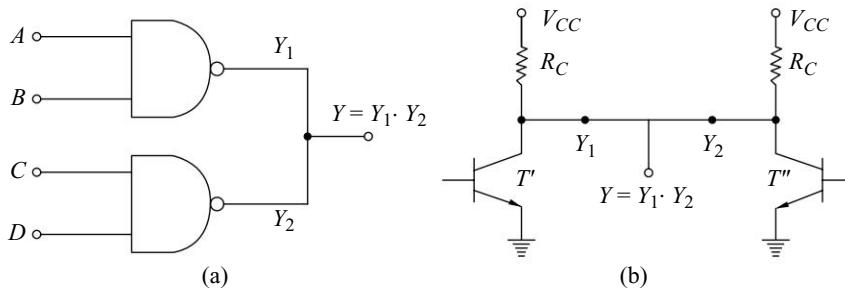


Fig. 4.13 The Wired-AND Connection of DTL Gates

If  $Y_1 = Y_2 = 1$ , then  $Y = 1$ , whereas if any one ( $Y_1$  or  $Y_2$ ) or both are 0, then  $Y = 0$ . The output is

$$Y = Y_1 Y_2 = (\overline{AB}) \cdot (\overline{CD}) = \overline{AB + CD} \quad (4.7)$$

Let us consider the effect of wired-AND connection on power dissipation, speed, and fan-out. The power dissipation in LOW output state  $P(0)$  increases because of reduction in effective collector resistor ( $R_C \parallel R_C = R_C/2$ ). Consequently, the speed of operation increases due to reduction in charging resistor ( $R_C/2$ ).

There is an effective reduction in the fan-out of the gate in the wired-AND connection. If only one output transistor (say  $T'$ ) is conducting, then this transistor must not only sink the current of the load gates and the current due to its own pull-up resistor but must also sink the current in the pull-up resistor of the other output transistor  $T''$ . This situation makes it necessary to reduce the allowable fan-out of each gate in the wired-AND connection.

#### 4.6.5 Modified Integrated DTL NAND Gate

From Ex. 4.1 we note that the fan-out may be increased by increasing the base current of the output transistor. This can be done by replacing  $D_1$  by a transistor  $T_1$ , as illustrated in Fig. 4.14.

The circuit can be analysed in a similar way as in Ex. 4.1 (Prob. 4.9). Its fan-out is considerably higher than that of the circuit of Fig. 4.12.

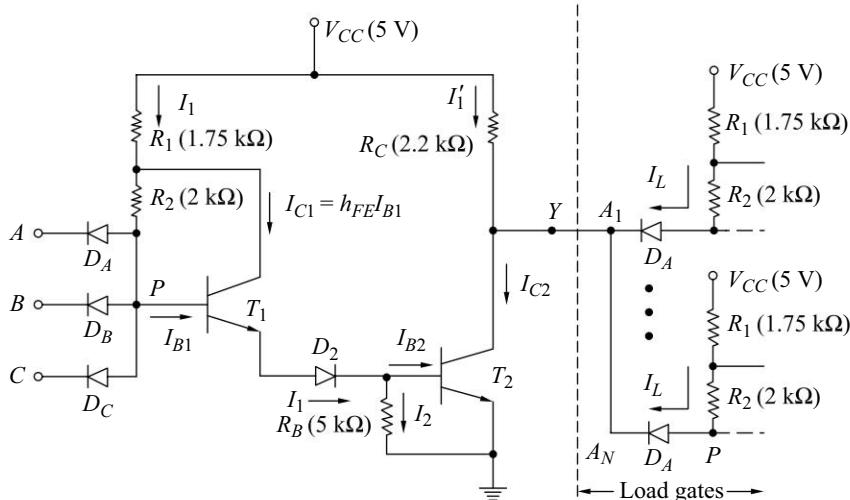
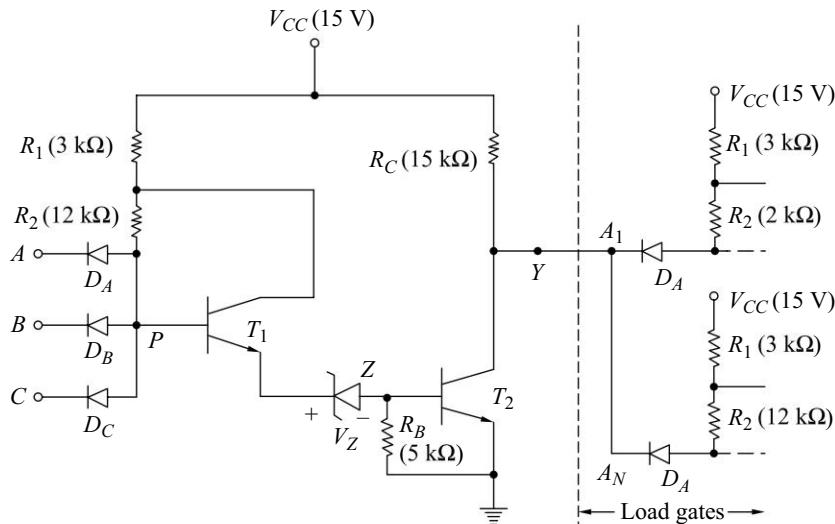


Fig. 4.14 A Modified Integrated 3-Input DTL NAND Gate Driving  $N$  Similar Gates

#### 4.7 HIGH-THRESHOLD LOGIC (HTL)

Due to the presence of electric motors, on-off control circuits, high voltage switches, etc. in an industrial environment, the noise level is quite high and the logic families discussed so far do not perform the intended functions. For this purpose, the DTL gate of Fig. 4.14 has been redesigned with a higher supply voltage (15 V instead of 5 V). The diode  $D_2$  has been replaced by a Zener diode with a Zener breakdown voltage of 6.9 V and the resistances have been modified so that approximately the same currents are obtained as in DTL. A 3-input HTL NAND gate with a fan-out of  $N$  is shown in Fig. 4.15. The circuit can be analysed to determine the noise-margins, fan-out and power dissipation (Prob. 4.10).

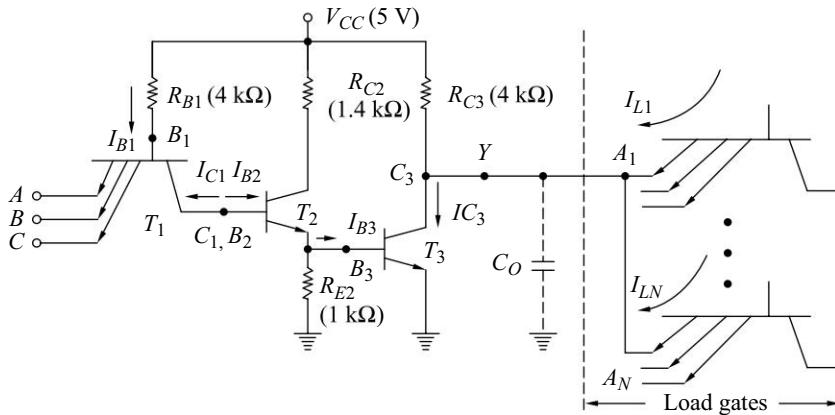
Fig. 4.15 A 3-Input HTL NAND Gate Driving  $N$  Similar Gates

The propagation delay time is adversely affected due to large resistance values. It is as high as hundreds of nano-seconds. The temperature sensitivity of the HTL gate is considerably less than that of DTL (Prob. 4.12).

## 4.8 TRANSISTOR-TRANSISTOR LOGIC (TTL)

The transistor-transistor logic (TTL) is the most successful bipolar logic which was evolved in the 1960s and has survived for more than four decades. TTL families use transistors, both to perform logic functions and to provide high output drive capability.

The NAND gate is the basic TTL logic circuit. Figure 4.16 shows a 3-input TTL NAND gate driving  $N$  similar gates. It uses a multiple-emitter transistor  $T_1$ . The number of inputs (fan-in) to the gate is same as the number of emitters fabricated during its manufacturing.

Fig. 4.16 A 3-Input TTL NAND Gate Driving  $N$  Similar Gates

### 4.8.1 Operation of TTL NAND GATE

Let us assume that the load gates are not present and the voltages for logic 0 and 1 are  $V_{CE,sat} \approx 0.2$  V and  $V_{CC} = 5$  V respectively.

The following voltages are assumed for  $p-n$  junction (diode operation) and transistors.

$p-n$  junction: Voltage across a conducting diode = 0.7 V

Cut-in voltage  $V_r = 0.6$  V

Transistor: Cut-in voltage  $V_r = 0.5$  V

$V_{BE,sat} = 0.8$  V

$V_{CE,sat} = 0.2$  V

**Condition I** At least one input is LOW. The emitter-base junction of  $T_1$  corresponding to the input in the LOW state is forward-biased making voltage at  $B_1$ ,  $V_{B1} = 0.2 + 0.7 = 0.9$  V. For base-collector junction of  $T_1$  to be forward-biased, and for  $T_2$  and  $T_3$  to be conducting,  $V_{B1}$  is required to be at least  $0.6 + 0.5 + 0.5 = 1.6$  V. Hence,  $T_2$  and  $T_3$  are OFF.

Since  $T_3$  is OFF, therefore  $Y = V(1) = V_{CC}$ .

Figure 4.17(a) illustrates the circuit corresponding to this condition.

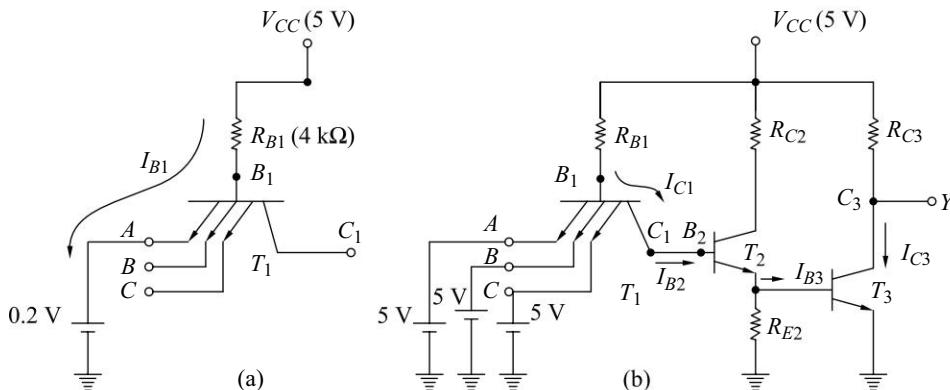


Fig. 4.17 Circuits Illustrating the Operation of TTL NAND Gate. (a) At least One of the Inputs is LOW  
(b) All the Inputs are HIGH

**Condition II** All inputs are HIGH. The emitter-base junctions of  $T_1$  are reverse-biased. If we assume that  $T_2$  and  $T_3$  are ON, then  $V_{B2} = V_{C1} = 0.8 + 0.8 = 1.6$  V. Since  $B_1$  is connected to  $V_{CC}$  (5 V) through  $R_{B1}$ , the collector-base junction of  $T_1$  is forward-biased. The transistor  $T_1$  is operating in the active inverse mode, making  $I_{C1}$  flow in the reverse direction. This current flows into the base of  $T_2$  driving  $T_2$  and  $T_3$  into saturation. Therefore,  $Y = V(0) \approx 0.2$  V.

Figure 4.17(b) illustrates the circuit corresponding to this condition.

The above operation shows that the gate of Fig. 4.16 operates as a NAND gate. From conditions I and II, it appears that  $T_1$  is acting as back-to-back diodes. The importance of  $T_1$  will become clear from condition III.

**Condition III** Let the circuit be operating under condition II when one of the inputs suddenly goes to  $V(0)$ . The corresponding emitter-base junction of  $T_1$  starts conducting and  $V_{B1}$  drops to 0.9 V.  $T_2$  and  $T_3$  will be turned off when the stored base charge is removed. Since  $V_{C1} = V_{B2} = 1.6$  V, therefore the collector-base

junction of  $T_1$  is back-biased, making  $T_1$  operate in the normal active region. This large collector current of  $T_1$  is in a direction which helps in the removal of stored base charge in  $T_2$  and  $T_3$  and improves the speed of circuit. The direction of the collector current is same as the current  $I_{C1}$  shown in Fig.4.16. The output voltage is pulled-up by the time constant  $T = R_{C3} \cdot C_o$ . Resistance  $R_{C3}$  is known as *pull-up resistor*.

## 4.8.2 Current Sink Logic

When at least one of the inputs is LOW, current  $I_{B1}$  from  $V_{CC}$  source flows through the input signal.

$$I_{B1} = \frac{V_{CC} - V_{B1}}{R_{B1}} = \frac{5 - 0.9}{4} \text{ mA} = 1.025 \text{ mA}$$

When all the inputs are HIGH, the emitter-base junctions of  $T_1$  are reverse-biased. Therefore, current drawn from the input source is the reverse saturation current of a *p-n* junction which is very small (a few  $\mu\text{A}$ ).

When the gate is driving other gates, similar conditions as discussed above will exist at the output of the driving gate. This shows that the load current  $I_L$  due to each load gate will flow through the collector of the transistor  $T_3$ , this means the output of the driving gate has to sink its  $I_{C3,\text{sat}}$  as well as the load currents corresponding to the output in the LOW state. When the output is in the HIGH state, the driving gate sources the leakage currents of load devices which is very small in comparison to the sinking current. Therefore, the TTL is known as *Current sink Logic*.

## 4.8.3 Fan-Out

The fan-out( $N$ ) of a gate depends upon the maximum collector current rating of the transistor  $T_3$ . The total collector current  $I_{C3} = I_{C3,\text{sat}} + N \cdot I_L$ , when the output is in the LOW state.

## 4.8.4 Power Dissipation

The currents drawn from the  $V_{CC}$  supply will be different for the two conditions, i.e., when the output is in the LOW state and when the output is in the HIGH state. The power consumption in the LOW output state  $P(0)$  will be due to  $I_{B1}$ , whereas the power consumption when the output is in the HIGH state  $P(1)$  will be due to the currents flowing through  $R_{C2}$ ,  $R_{C3}$ , and the leakage currents of load devices. Therefore the average power consumption is  $\frac{p(0) + p(1)}{2}$

## 4.8.5 Wired-Logic

If the output of gates are connected together as shown in Fig. 4.13, additional logic is performed. Its detailed operation is given in section 4.6.4.

## 4.8.6 Propagation Delays

The propagation delays have been discussed in section 4.6.2. The speed of the circuit can be improved by decreasing  $R_{C3}$  which decreases the time constant  $(R_{C3} \cdot C_o)$  with which the output capacitance charges from 0 to 1 logic level. Such a reduction, however, would increase dissipation and would make it more difficult for  $T_3$  to saturate.

## 4.8.7 Active Pull-up

It is possible in TTL gates to hasten the charging of output capacitance without corresponding increase in power dissipation with the help of an output circuit arrangement (Fig. 4.18) referred to as an *active pull-up* or *totem-pole* output.

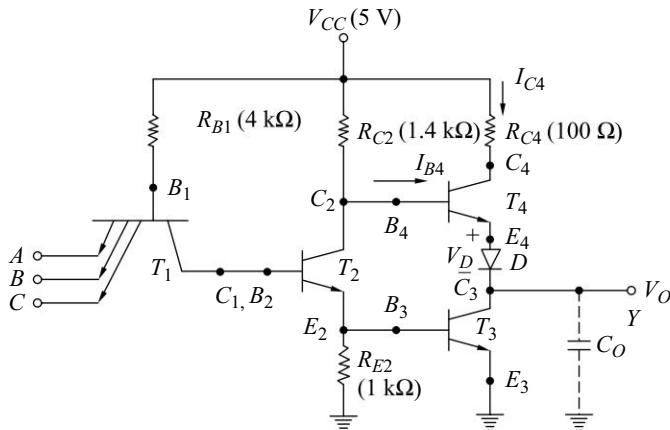


Fig. 4.18 A TTL Gate with Totem-Pole Output Driver

The operation of the circuit can qualitatively be described as: For output  $Y$  to be in LOW state, transistor  $T_4$  and diode  $D$  are cut-off. When the output makes a transition from LOW to HIGH corresponding to any input going to LOW, transistor  $T_4$  enters saturation and supplies current for the charging of the output capacitor with a small time constant. This current decreases and eventually becomes zero under steady-state condition when  $Y = V(1)$ .

Diode  $D$  is used in the circuit to keep  $T_4$  in cut-off when the output is at logic 0. Corresponding to this,  $T_2$  and  $T_3$  are in saturation, therefore,

$$V_{C2} = V_{B4} = V_{BE3, \text{sat}} + V_{CE2, \text{sat}} = 0.8 + 0.2 = 1.0 \text{ V} \quad (4.8)$$

Since  $V_O = V_{CE3, \text{sat}} \approx 0.2 \text{ V}$ , the voltage across the base-emitter junction of  $T_4$  and diode  $D$  equals  $1.0 - 0.2 = 0.8 \text{ V}$ , which means  $T_4$  and  $D$  are cut-off.

If one of the inputs drops to LOW logic level,  $T_2$  and  $T_3$  go to cut-off. The output voltage cannot change instantaneously (being the voltage across  $C_O$ ) and because of  $T_2$  going to cut-off, the voltage at the base of  $T_4$  rises driving it to saturation.

As soon as  $T_2$  is cut-off,

$$\begin{aligned} V_{B4} &= V_{BE4, \text{sat}} + V_D + V_O \\ &= 0.8 + 0.7 + 0.2 = 1.7 \text{ V} \end{aligned} \quad (4.9)$$

Therefore,

$$I_{B4} = \frac{V_{CC} - V_{B4}}{R_{C2}} = \frac{5 - 1.7}{1.4} = 2.36 \text{ mA} \quad (4.10)$$

and

$$\begin{aligned} I_{C4} &= \frac{V_{CC} - V_{CE4, \text{sat}} - V_D - V_O}{R_{C4}} \\ &= \frac{5 - 0.2 - 0.7 - 0.2}{0.1} = 39 \text{ mA} \end{aligned} \quad (4.11)$$

Hence,  $T_4$  is in saturation if  $h_{FE}$  exceeds  $\frac{39}{2.36} = 16.5$ .

The output voltage  $V_o$  rises exponentially towards  $V_{cc}$  with the time constant  $= (R_{c4} + R_{CS4} + R_f) C_o$ , where  $R_{CS4}$  is the saturation resistance of  $T_4$  and  $R_f$  is the forward resistance of the diode.

As  $V_O$  increases, the base and collector currents of  $T_4$  are decreased and eventually  $T_4$  just comes out of conduction at steady-state. Therefore,

$$V(1) = V_{CC} - V_{\gamma}(T_4) - V_{\gamma}(\text{diode}) = 5 - 0.5 - 0.6 = 3.9 \text{ V}$$

Now, if the output is at  $V(1)$  and all the inputs go to HIGH,  $T_2$  goes ON. Consequently  $T_4$  and  $D$  go OFF and  $T_3$  conducts. The capacitor  $C_O$  discharges through  $T_3$  and as  $V_O$  approaches  $V(0)$ ,  $T_3$  enters into saturation.

From the above discussion it is clear that the maximum current is drawn from the supply when the output makes a transition from  $V(0)$  to  $V(1)$  and equals  $I_{C4} + I_{R4} = 39 + 2.4 = 41.4$  mA.

This current spike generates noise in the power supply distribution system and increases power dissipation in the gate, more so when it is operated at high frequencies.

#### 4.8.8 Wired-AND for Totem Pole Output TTL

Wired-AND connection must not be used for totem-pole output circuits because of the current spike problem discussed above (Prob. 4.16). TTL circuits with open-collector outputs are available which can be used for wired-AND connections.

#### 4.8.9 Open-Collector Output

A circuit with open-collector output is same as the circuit of Fig. 4.16 except for the collector-resistor  $R_{C3}$  of  $T_3$  which is missing. The collector terminal  $C_3$  is available outside the IC and the passive pull-up is to be connected externally. Naturally, the advantages of active pull-up are not available in this. Gates with open-collector output can be used for wired-AND operation (Prob.4.18).

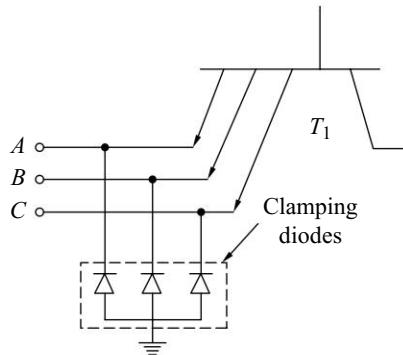


Fig. 4.19 *A Portion of a TTL Gate Showing the Clamping Diodes*

#### 4.8.10 Unconnected Inputs

If any input of a TTL gate is left disconnected (open or floating) the corresponding E-B junction of  $T_1$  will not be forward-biased. Hence, it acts exactly in the same way as if a logic 1 is applied to that input. Therefore, in TTL ICs, all unconnected inputs are treated as logical 1s. However, the unused inputs should either be connected to some used input(s) or returned to  $V_{CC}$  through a resistor.

#### 4.8.11 Clamping Diodes

Clamping diodes are commonly used in all TTL gates to suppress the ringing caused from the fast voltage

transitions found in TTL. These diodes shown in Fig. 4.19 clamp the negative undershoot at approximately  $-0.7\text{ V}$ .

- (iii) The low power dissipation series LS, and ALS have minimum power requirement and are suitable for battery operated circuits. Out of these series ALS series has the minimum propagation delay and therefore it is fast replacing other series.
- (iv) S and AS series have very low propagation delay. The AS series is fast replacing S series because of its lower dissipation and propagation delay.
- (v) 74F (FastTTL) family is the most popular choice for new TTL design. It is between 74AS and 74ALS in the speed power trade off.

## 4.11 Emitter-Coupled Logic (ECL)

Emitter-coupled logic (ECL) is the fastest of all logic families and therefore is used in applications where very high speed is essential. High speeds have become possible in ECL because the transistors are used in difference amplifier configuration, in which they are never driven into saturation and thereby the storage time is eliminated. Here, rather than switching the transistors from ON to OFF and vice-versa, they are switched between cut-off and active regions. Propagation delays of less than 1 ns per gate have become possible in ECL.

Basically, ECL is realised using difference amplifier in which the emitters of the two transistors are connected and hence it is referred to as emitter-coupled logic. A 3-input ECL gate is shown in Fig. 4.21, which has three parts: The middle part is the difference amplifier which performs the logic operation.

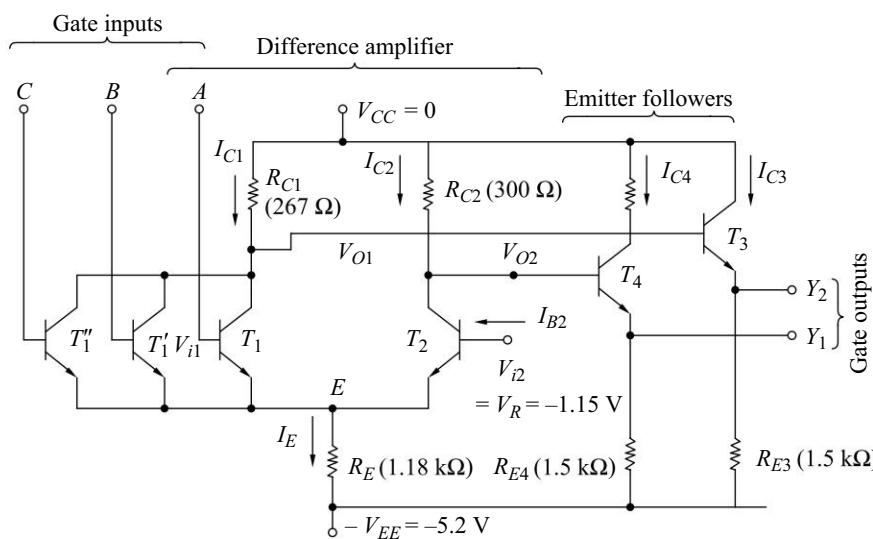


Fig. 4.21 A 3-Input ECL OR/NOR Gate

Emitter followers are used for d.c. level shifting of the outputs, so that  $V(0)$  and  $V(1)$  are same for the inputs and the outputs. Note that two output  $Y_1$  and  $Y_2$  are available in this circuit which are complementary.  $Y_1$  corresponds to OR logic and  $Y_2$  to NOR logic and hence it is named as an OR/NOR gate.

Additional transistors are used in parallel to  $T_1$  to get the required fan-in. There is a fundamental difference between all other logic families (including MOS logic) and ECL as far as the supply voltage is concerned. In ECL, the positive end of the supply is connected to ground in contrast to other logic families in which negative end of the supply is grounded. This is done to minimise the effect of noise induced in the power supply (Prob. 4.22), and protection of the gate from an accidental short circuit developing between the output of a gate and ground (Prob. 4.23). The voltage corresponding to  $V(0)$  and  $V(1)$  are both negative due to positive end of the supply being connected to ground. The symbol of an ECL OR/NOR gate is shown in Fig. 4.22.

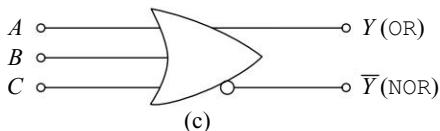


Fig. 4.22 The Symbol for a 3-Input OR/NOR Gate

the positive end of the supply is connected to ground in contrast to other logic families in which negative end of the supply is grounded. This is done to minimise the effect of noise induced in the power supply (Prob. 4.22), and protection of the gate from an accidental short circuit developing between the output of a gate and ground (Prob. 4.23). The voltage corresponding to  $V(0)$  and  $V(1)$  are both negative due to positive end of

the supply being connected to ground. The symbol of an ECL OR/NOR gate is shown in Fig. 4.22.

### Example 4.2

- (a) Verify that the circuit of Fig. 4.21 performs OR/NOR operations. (b) Show that the transistors in this circuit operate in the active region and not in saturation. (c) Calculate the noise margins. (d) Find the average power dissipated by the gate.

Assume a base-emitter voltage of 0.7 V for a transistor conducting in active region.

#### Solution

- (a) (i) Assume all inputs to be LOW.

Let us assume that the input transistors  $T_1$ ,  $T'_1$ ,  $T''_1$  are cut-off and  $T_2$  is conducting in the active region. The voltage at the common emitter is  $V_E = V_{i2} - V_{BE2} = -1.15 - 0.7 = -1.85$  V. The current

$$I_E = \frac{V_E - (-V_{EE})}{R_E} = \frac{-1.85 + 5.2}{1.18} = 2.84 \text{ mA}$$

Since  $I_{B2} \ll I_{C2}$ , therefore  $I_{C2} \approx I_E$

$$V_{O2} = -0.3 I_{C2} = -0.3 (2.84) = -0.852 \text{ V}$$

Transistor  $T_4$  will be conducting and the output at  $Y_1 = V_{O2} - V_{BE4} = -0.852 - 0.7 = -1.55$  V which is assumed to be  $V(0)$ .

Therefore, if all the inputs are at  $V(0) = -1.55$  V, then the base-to-emitter voltage of the input transistor is

$$V_{BE} = V_{i1} - V_E = -1.55 + 1.85 = 0.3 \text{ V}$$

which is less than the cut-in voltage (0.5 V) of the transistor and hence the input transistors are non-conducting, as was assumed above.

The base and collector of  $T_3$  are effectively at the same potential, hence  $T_3$  behaves as a diode. The current flowing through this diode is approximately 3 mA which corresponds to a voltage of about 0.75 V across the diode. Therefore, the voltage at  $Y_2 = -0.75$  V which is assumed to be  $V(1)$ . This shows that  $Y_1$  and  $Y_2$  are complementary, i.e.  $Y_2 = \bar{Y}_1$ .

- (ii) Assume at least one input to be HIGH. Corresponding to this the input transistor  $T_1$  is assumed to be conducting and  $T_2$  to be cut-off.

$$\text{Then } V_E = V_{i1} - V_{BE1} = -0.75 - 0.7 = -1.45 \text{ V}$$

Hence,  $V_{BE2} = V_{i2} - V_E = -1.15 + 1.45 = 0.3$  V which verifies the assumption that  $T_2$  is cut-off.

The voltage

$$V_{o1} = -R_{C1} \times I_{C1}$$

where

$$\begin{aligned} I_{C1} &= \frac{V_E - (-V_{EE})}{R_E} \\ &= \frac{(-1.45 + 5.2)}{1.18} = 3.18 \text{ mA} \end{aligned}$$

Since the collector current of  $T_1$  is higher than the collector current of  $T_2$  when it is conducting, hence  $R_{C1} < R_{C2}$  to get the same voltage levels.

This gives voltage at  $Y_2 = -1.55 = V(0)$ . The voltage at  $Y_1 = -0.75 = V(1)$ . From (i) and (ii) above, we see that OR function is performed at  $Y_1$  and NOR at  $Y_2$ . Hence it is an OR/NOR gate. Its voltages corresponding to logic 0 and 1 are  $-1.55$  V and  $-0.75$  V, respectively. The logic swing is  $0.8$  V.

- (b) From part (a) (i), the voltage between collector and base of  $T_2$  is  $V_{CB2} = V_{o2} - V_{i2} = -0.85 + 1.15 = 0.30$  V which shows that the C-B junction is reverse-biased and hence  $T_2$  is operating in its active region.

From part (a) (ii), the voltage between the collector and base of  $T_1$  is

$$V_{CB1} = V_{o1} - V_{i1} = -0.85 + 0.75 = -0.1 \text{ V}$$

This shows that the C-B junction of  $T_1$  is forward-biased but its magnitude is much less than the cut-in voltage and hence  $T_1$  is operating in its active region.

- (c) From part (a)(i), the base-emitter voltage of the input transistors is  $0.3$  V which is  $0.2$  V less than the cut-in voltage. Hence the noise margin  $\Delta 0 = 0.2$  V.

From part (a) (ii) the base-emitter voltage of  $T_2$  is  $0.3$  V which again gives a noise margin  $\Delta 1 = 0.2$  V. The noise margins are equal and are quite small.

- (d) From part (a) (i),

$$I_{C2} = 2.84 \text{ mA}$$

and

$$I_{C3} = \frac{5.2 - 0.75}{1.5} = 2.97 \text{ mA}$$

$$I_{C4} = \frac{5.2 - 1.55}{1.5} = 2.43 \text{ mA}$$

From part (a) (ii),

$$I_{C1} = 3.18 \text{ mA}$$

$$I_{C3} = 2.43 \text{ mA}$$

$$I_{C4} = 3.97 \text{ mA}$$

Therefore, average  $I_E = \frac{2.84 + 3.18}{2} = 3.01$  mA. The total power supply current drain

$$I_{EE} = 3.01 + 2.97 + 2.42 = 8.41 \text{ mA}$$

Therefore, the power dissipation =  $V_{EE} \cdot I_{EE} = (5.2) (8.41) = 43.7$  mW

#### 4.11.1 Fan-Out

If all the inputs are LOW, the input transistors are cut-off. Therefore the input resistance is very high. On the other hand, if an input is HIGH, the input resistance is that of an emitter follower which is also high. Therefore, the input impedance is always high.

The output resistance is either that of an emitter follower or the forward resistance of a diode ( $T_3$  or  $T_4$  acts as a diode) which is always low. Because of the low output impedance and high input impedance, the fan-out is large.

### 4.11.2 Wired-OR Logic

The outputs of two or more ECL gates can be connected to obtain additional logic without using additional hardware. The wired-OR configurations are shown in Fig. 4.23.

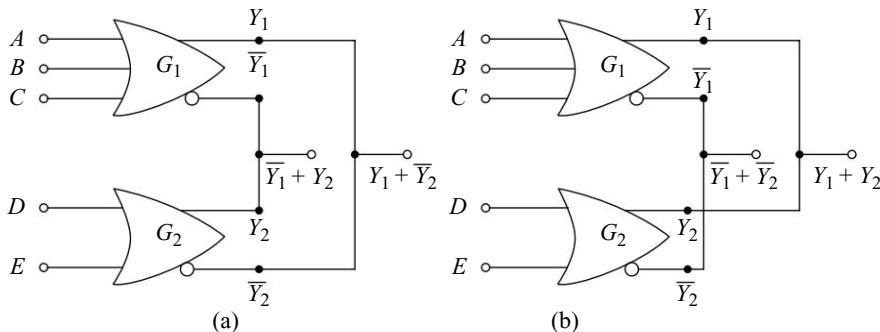


Fig. 4.23 **Wired-OR Connection of ECL Gates**

### 4.11.3 Open-Emitter Outputs

Similar to open-collector output in TTL, open-emitter outputs are available in ECL which is useful for wired-OR applications.

### 4.11.4 Unconnected Inputs

If any input of an ECL gate is left unconnected, the corresponding E-B junction of the input transistor will not be conducting. Hence it acts as if a logic 0 level voltage is applied to that input. Therefore, in ECL ICs, all unconnected inputs are treated as logic 0s.

### 4.11.5 ECL Families

There are two popular ECL families: 10xxx (or 10K) series and 100xxx (or 100K) series. The 100K series is the fastest of all logic families and has a propagation delay time less than 1 ns. Their voltage specifications are given in Table 4.5.

Table 4.5 **Voltage Specifications of ECL Series**

Series	Supply voltage $V_{EE}$ , V	$V_{OL}$ V	$V_{OH}$ V	$V_{IL}$ V	$V_{IH}$ V
10K	5.2	-1.7	-0.9	-1.4	-1.2
100k	4.5	-17	-0.9	-1.4	-1.2

## 4.12 INTERFACING ECL AND TTL

It is often necessary to mix logic circuits of different families in the design of a digital system to realise the speed and power requirements by choosing the appropriate logic families for different parts of the system. Consider the

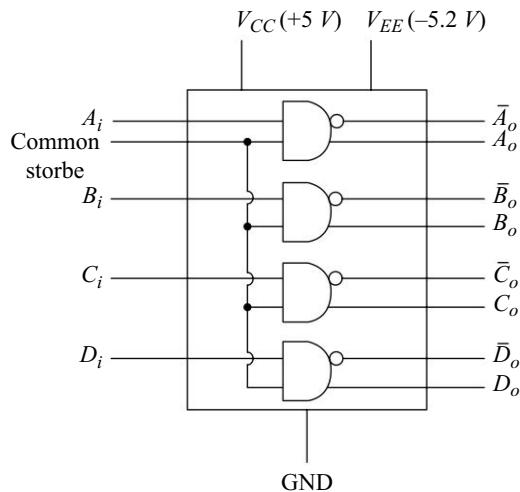


Fig. 4.24 **Logic Diagram of MC10H124 TTL-to-ECL Translator**

interfacing between TTL and ECL gates. The logic levels in the two systems are entirely different and therefore level shifting circuits are required to be interposed between TTL and ECL gates. For TTL-to-ECL and ECL-to-TTL interfacing two level translator ICs are available. Interfacing using these ICs are described below.

### 4.12.1 TTL-to-ECL Translator

The MC10H124 is a quad TTL-to-ECL translator IC. It is a 16-pin IC and its logic diagram is shown in Fig. 4.24. It uses two power supplies; one positive and another negative for the generation of proper logic levels for ECL and TTL.

The logic levels of the translator circuit are:

$$\begin{aligned} V_{IH} &= 2 \text{ V}, V_{IL} = 0.8 \text{ V} \\ V_{OH} &= -0.98 \text{ V}, V_{OL} = -1.63 \text{ V} \end{aligned}$$

From Table 4.3, we have  $V_{OH} = 2.4 \text{ V}$  and  $V_{OL} = 0.4 \text{ V}$  for TTL ICs. Comparing the output logic levels of TTL

and the input logic levels of the translator IC, we observe,

$$\begin{aligned} V_{IH} \text{ (Translator)} &< V_{OH} \text{ (TTL)} \\ V_{IL} \text{ (Translator)} &> V_{OL} \text{ (TTL)} \end{aligned}$$

which shows that the input logic levels of the translator are compatible with the output logic levels of TTL.

Similarly, comparing the output logic levels of the translator with the input logic levels of ECL (Table 4.5), we obtain

$$\begin{aligned} V_{IH} \text{ (ECL)} &< V_{OH} \text{ (Translator)} \\ V_{IL} \text{ (ECL)} &> V_{OL} \text{ (Translator)} \end{aligned}$$

which demonstrates that the output logic levels of the translator are compatible with the input logic levels of ECL.

Figure 4.25 shows a TTL NAND gate driving an ECL NOR gate through a TTL-to-ECL translator gate.

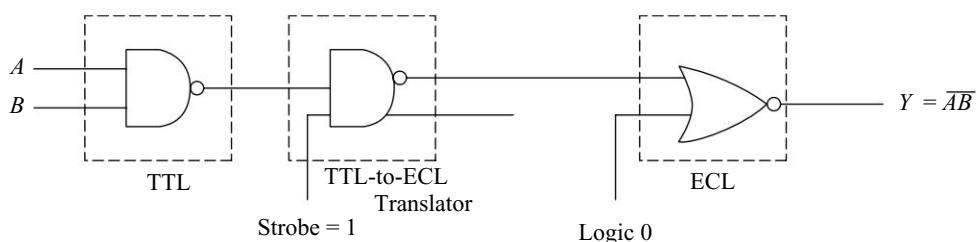


Fig. 4.25 **A TTL NAND Gate Driving an ECL NOR Gate Through a TTL-to-ECL Translator**

### 4.12.2 ECL-to-TTL Translator

The MC10H125 is a quad ECL-to-TTL translator IC. It is a 16-pin IC and its logic diagram is shown in Fig. 4.26. It also uses two power supplies for the generation of proper logic levels for ECL and TTL. Its logic levels are:

$$V_{IH} = -1.13 \text{ V}, \quad V_{IL} = -1.48 \text{ V}$$

$$V_{OH} = 2.5 \text{ V}, \quad V_{OL} = 0.5 \text{ V}$$

Its input logic levels are compatible with ECL and the output logic levels are compatible with TTL (Prob. 4.26).

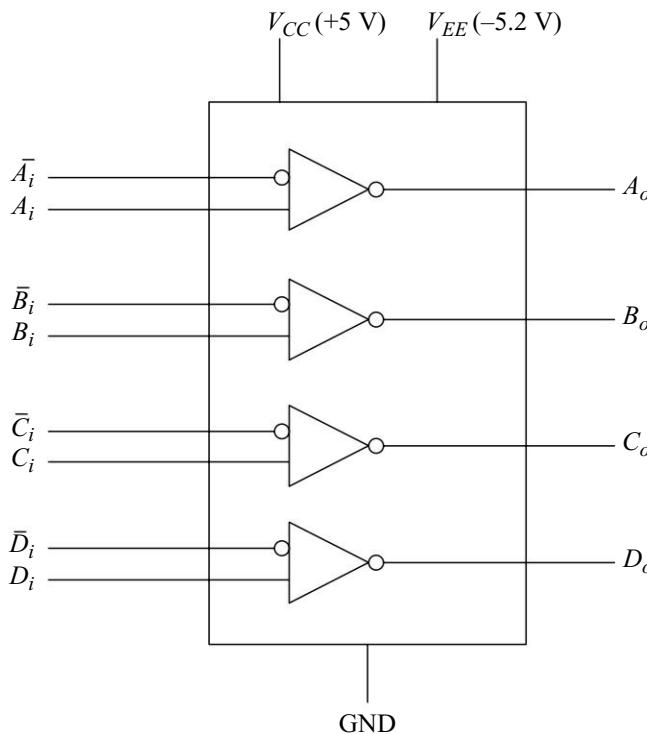


Fig. 4.26 Logic Diagram of MC10H125 ECL-to-TTL Translator

### 4.13 MOS LOGIC

MOSFETs have become very popular for logic circuits due to high density of fabrication and low power dissipation. When MOS devices are used in logic circuits, there can be circuits in which either only  $p$ - or only  $n$ -channel devices are used. Such circuits are referred to as PMOS and NMOS logic respectively. It is also possible to fabricate enhancement mode  $p$ -channel and  $n$ -channel MOS devices on the same chip. Such devices are referred to as complementary MOSFETs and logic based on these devices is known as CMOS logic. The power dissipation is extremely small for CMOS and hence CMOS logic has become very popular.

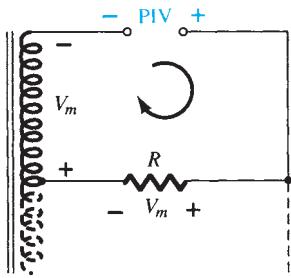


FIG. 2.63

Determining the PIV level for the diodes of the CT transformer full-wave rectifier.

**PIV** The network of Fig. 2.63 will help us determine the net PIV for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and  $V_m$  as established by the adjoining loop results in

$$\begin{aligned} \text{PIV} &= V_{\text{secondary}} + V_R \\ &= V_m + V_m \end{aligned}$$

and

$$\text{PIV} \geq 2V_m \quad \text{CT transformer, full-wave rectifier} \quad (2.13)$$

**EXAMPLE 2.17** Determine the output waveform for the network of Fig. 2.64 and calculate the output dc level and the required PIV of each diode.

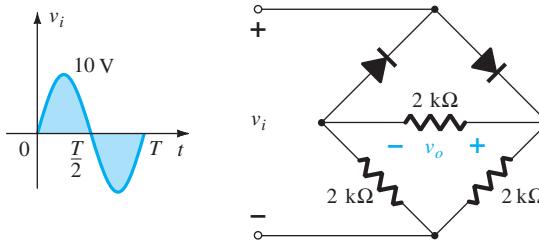


FIG. 2.64  
Bridge network for Example 2.17.

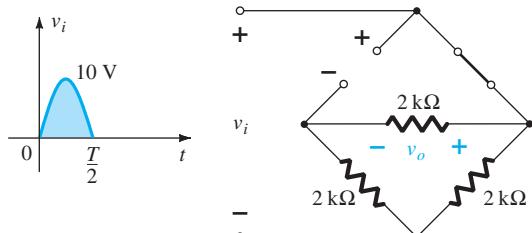


FIG. 2.65

Network of Fig. 2.64 for the positive region of  $v_i$ .

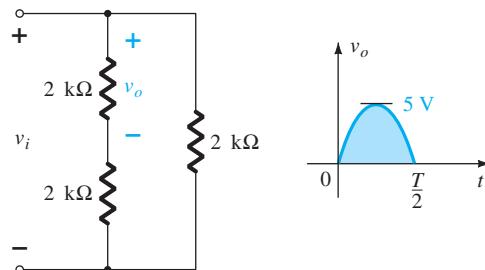


FIG. 2.66

Redrawn network of Fig. 2.65.

**Solution:** The network appears as shown in Fig. 2.65 for the positive region of the input voltage. Redrawing the network results in the configuration of Fig. 2.66, where  $v_o = \frac{1}{2}v_i$  or  $V_{o_{\max}} = \frac{1}{2}V_{i_{\max}} = \frac{1}{2}(10 \text{ V}) = 5 \text{ V}$ , as shown in Fig. 2.66. For the negative part of the input, the roles of the diodes are interchanged and  $v_o$  appears as shown in Fig. 2.67.

The effect of removing two diodes from the bridge configuration is therefore to reduce the available dc level to the following:

$$V_{dc} = 0.636(5 \text{ V}) = 3.18 \text{ V}$$

or that available from a half-wave rectifier with the same input. However, the PIV as determined from Fig. 2.59 is equal to the maximum voltage across  $R$ , which is 5 V, or half of that required for a half-wave rectifier with the same input.

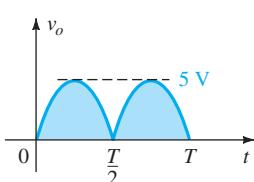


FIG. 2.67

Resulting output for Example 2.17.

## 2.8 CLIPPERS

The previous section on rectification gives clear evidence that diodes can be used to change the appearance of an applied waveform. This section on clippers and the next on clamps will expand on the wave-shaping abilities of diodes.

**Clippers** are networks that employ diodes to “clip” away a portion of an input signal without distorting the remaining part of the applied waveform.

The half-wave rectifier of Section 2.6 is an example of the simplest form of diode clipper—one resistor and a diode. Depending on the orientation of the diode, the positive or negative region of the applied signal is “clipped” off.

There are two general categories of clippers: *series* and *parallel*. The series configuration is defined as one where the diode is in series with the load, whereas the parallel variety has the diode in a branch parallel to the load.

## Series

The response of the series configuration of Fig. 2.68a to a variety of alternating waveforms is provided in Fig. 2.68b. Although first introduced as a half-wave rectifier (for sinusoidal waveforms), there are no boundaries on the type of signals that can be applied to a clipper.

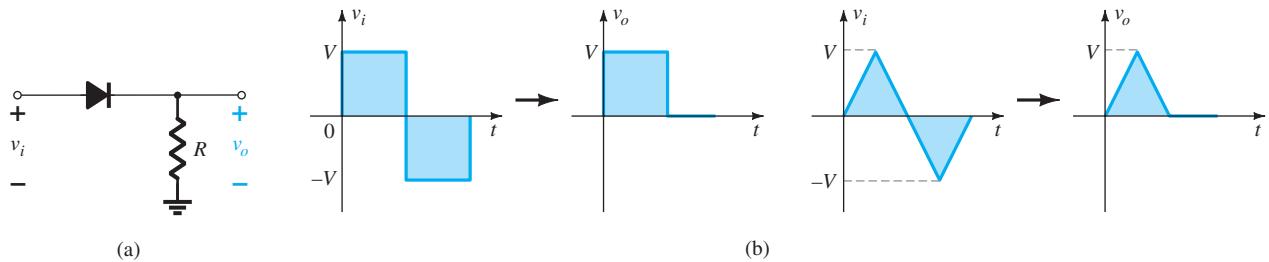


FIG. 2.68  
Series clipper.

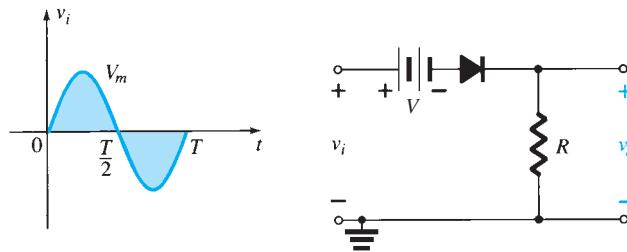


FIG. 2.69  
Series clipper with a dc supply.

The addition of a dc supply to the network as shown in Fig. 2.69 can have a pronounced effect on the analysis of the series clipper configuration. The response is not as obvious because the dc supply can aid or work against the source voltage, and the dc supply can be in the leg between the supply and output or in the branch parallel to the output.

There is no general procedure for analyzing networks such as the type in Fig. 2.69, but there are some things one can do to give the analysis some direction.

First and most important:

**1. Take careful note of where the output voltage is defined.**

In Fig. 2.69 it is directly across the resistor  $R$ . In some cases it may be across a combination of series elements.

Next:

**2. Try to develop an overall sense of the response by simply noting the “pressure” established by each supply and the effect it will have on the conventional current direction through the diode.**

In Fig. 2.69, for instance, any positive voltage of the supply will try to turn the diode on by establishing a conventional current through the diode that matches the arrow in the diode symbol. However, the added dc supply  $V$  will oppose that applied voltage and try to keep the diode in the “off” state. The result is that any supply voltage greater than  $V$  volts will turn the diode on and conduction can be established through the load resistor. Keep in mind that we are dealing with an ideal diode for the moment, so the turn-on voltage is simply 0 V. In general, therefore, for the network of Fig. 2.69 we can conclude that the

diode will be on for any voltage  $v_i$  that is greater than  $V$  volts and off for any lesser voltage. For the “off” condition, the output would be 0 V due to the lack of current, and for the “on” condition it would simply be  $v_o = v_i - V$  as determined by Kirchhoff’s voltage law.

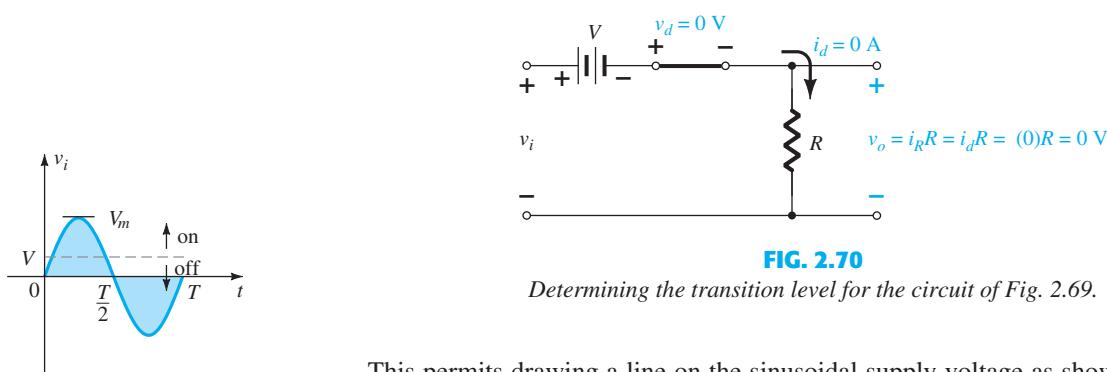
### 3. Determine the applied voltage (transition voltage) that will result in a change of state for the diode from the “off” to the “on” state.

This step will help to define a region of the applied voltage when the diode is on and when it is off. On the characteristics of an ideal diode this will occur when  $V_D = 0$  V and  $I_D = 0$  mA. For the approximate equivalent this is determined by finding the applied voltage when the diode has a drop of 0.7 V across it (for silicon) and  $I_D = 0$  mA.

This exercise was applied to the network of Fig. 2.69 as shown in Fig. 2.70. Note the substitution of the short-circuit equivalent for the diode and the fact that the voltage across the resistor is 0 V because the diode current is 0 mA. The result is  $v_i - V = 0$ , and so

$$v_i = V \quad (2.14)$$

is the transition voltage.



**FIG. 2.70**  
Determining the transition level for the circuit of Fig. 2.69.

This permits drawing a line on the sinusoidal supply voltage as shown in Fig. 2.71 to define the regions where the diode is on and off.

For the “on” region, as shown in Fig. 2.72, the diode is replaced by a short-circuit equivalent, and the output voltage is defined by

$$v_o = v_i - V \quad (2.15)$$

For the “off” region, the diode is an open circuit,  $I_D = 0$  mA, and the output voltage is

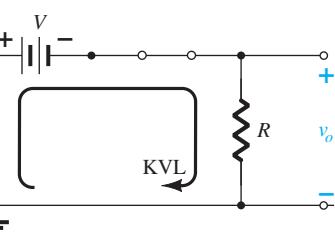
$$v_o = 0$$

### 4. It is often helpful to draw the output waveform directly below the applied voltage using the same scales for the horizontal axis and the vertical axis.

Using this last piece of information, we can establish the 0-V level on the plot of Fig. 2.73 for the region indicated. For the “on” condition, Eq. (2.15) can be used to find the output voltage when the applied voltage has its peak value:

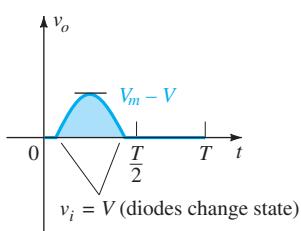
$$v_{o_{\text{peak}}} = V_m - V$$

and this can be added to the plot of Fig. 2.73. It is then simple to fill in the missing section of the output curve.



**FIG. 2.72**

Determining  $v_o$  for the diode in the “on” state.



**FIG. 2.73**

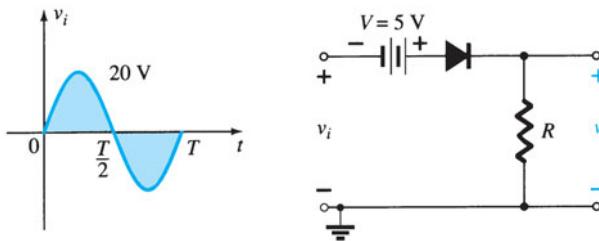
Sketching the waveform of  $v_o$  using the results obtained for  $v_o$  above and below the transition level.

**EXAMPLE 2.18** Determine the output waveform for the sinusoidal input of Fig. 2.74.

**Solution:**

**Step 1:** The output is again directly across the resistor  $R$ .

**Step 2:** The positive region of  $v_i$  and the dc supply are both applying “pressure” to turn the diode on. The result is that we can safely assume the diode is in the “on” state for the entire range of positive voltages for  $v_i$ . Once the supply goes negative, it would have to exceed the dc supply voltage of 5 V before it could turn the diode off.



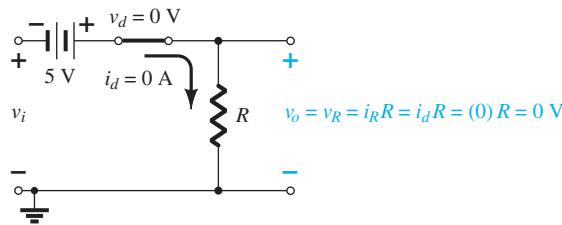
**FIG. 2.74**  
Series clipper for Example 2.18.

**Step 3:** The transition model is substituted in Fig. 2.75, and we find that the transition from one state to the other will occur when

$$v_i + 5 \text{ V} = 0 \text{ V}$$

or

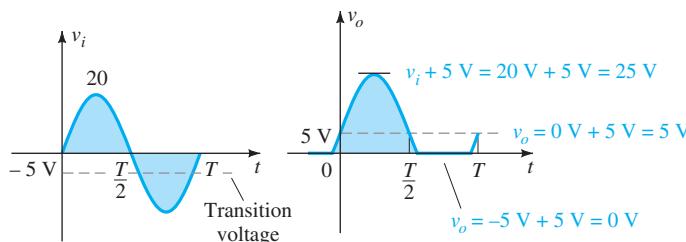
$$v_i = -5 \text{ V}$$



**FIG. 2.75**  
Determining the transition level for the clipper of Fig. 2.74.

**Step 4:** In Fig. 2.76 a horizontal line is drawn through the applied voltage at the transition level. For voltages less than  $-5 \text{ V}$  the diode is in the open-circuit state and the output is  $0 \text{ V}$ , as shown in the sketch of  $v_o$ . Using Fig. 2.76, we find that for conditions when the diode is on and the diode current is established the output voltage will be the following, as determined using Kirchhoff's voltage law:

$$v_o = v_i + 5 \text{ V}$$

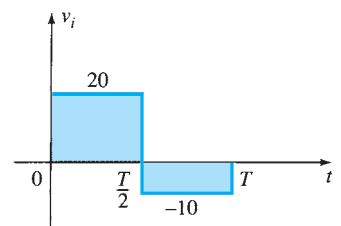


**FIG. 2.76**  
Sketching  $v_o$  for Example 2.18.

The analysis of clipper networks with square-wave inputs is actually easier than with sinusoidal inputs because only two levels have to be considered. In other words, the network can be analyzed as if it had two dc level inputs with the resulting  $v_o$  plotted in the proper time frame. The next example demonstrates the procedure.

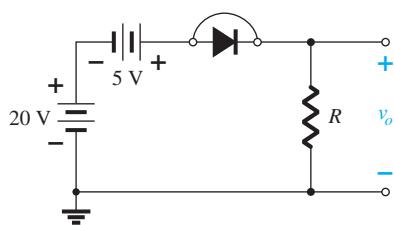
**EXAMPLE 2.19** Find the output voltage for the network examined in Example 2.18 if the applied signal is the square wave of Fig. 2.77.

**Solution:** For  $v_i = 20 \text{ V}$  ( $0 \rightarrow T/2$ ) the network of Fig. 2.78 results. The diode is in the short-circuit state, and  $v_o = 20 \text{ V} + 5 \text{ V} = 25 \text{ V}$ . For  $v_i = -10 \text{ V}$  the network of Fig. 2.79

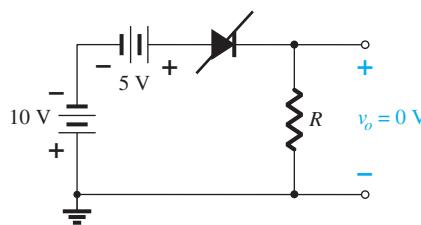


**FIG. 2.77**  
Applied signal for Example 2.19.

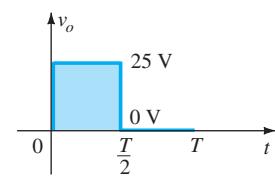
results, placing the diode in the “off” state, and  $v_o = i_R R = (0)R = 0$  V. The resulting output voltage appears in Fig. 2.80.



**FIG. 2.78**  
 $v_o$  at  $v_i = +20$  V.



**FIG. 2.79**  
 $v_o$  at  $v_i = -10$  V.

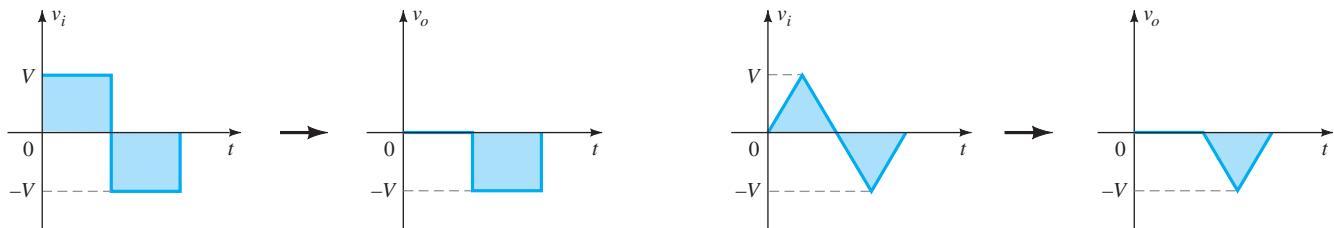
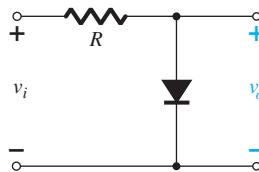


**FIG. 2.80**  
Sketching  $v_o$  for Example 2.19.

Note in Example 2.19 that the clipper not only clipped off 5 V from the total swing, but also raised the dc level of the signal by 5 V.

### Parallel

The network of Fig. 2.81 is the simplest of parallel diode configurations with the output for the same inputs of Fig. 2.68. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.

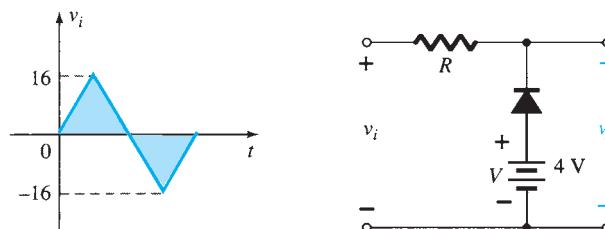


**FIG. 2.81**  
Response to a parallel clipper.

**EXAMPLE 2.20** Determine  $v_o$  for the network of Fig. 2.82.

**Solution:**

**Step 1:** In this example the output is defined across the series combination of the 4-V supply and the diode, not across the resistor  $R$ .



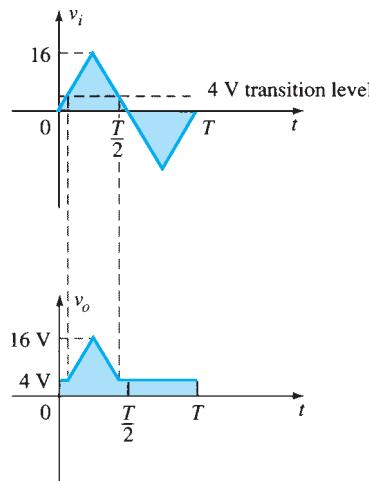
**FIG. 2.82**  
Example 2.20.

**Step 2:** The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the “on” state for a good portion of the negative region of the input signal. In fact, it is interesting to note that since the output is directly across the series combination, when the diode is in its short-circuit state the output voltage will be directly across the 4-V dc supply, requiring that the output be fixed at 4 V. In other words, when the diode is on the output will be 4 V. Other than that, when the diode is an open circuit, the current through the series network will be 0 mA and the voltage drop across the resistor will be 0 V. That will result in  $v_o = v_i$  whenever the diode is off.

**Step 3:** The transition level of the input voltage can be found from Fig. 2.83 by substituting the short-circuit equivalent and remembering the diode current is 0 mA at the instant of transition. The result is a change in state when

$$v_i = 4 \text{ V}$$

**Step 4:** In Fig. 2.84 the transition level is drawn along with  $v_o = 4 \text{ V}$  when the diode is on. For  $v_i \geq 4 \text{ V}$ ,  $v_o = 4 \text{ V}$ , and the waveform is simply repeated on the output plot.



**FIG. 2.84**  
Sketching  $v_o$  for Example 2.20.

To examine the effects of the knee voltage  $V_K$  of a silicon diode on the output response, the next example will specify a silicon diode rather than the ideal diode equivalent.

**EXAMPLE 2.21** Repeat Example 2.20 using a silicon diode with  $V_K = 0.7 \text{ V}$ .

**Solution:** The transition voltage can first be determined by applying the condition  $i_d = 0 \text{ A}$  at  $v_d = V_D = 0.7 \text{ V}$  and obtaining the network of Fig. 2.85. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$v_i + V_K - V = 0$$

and

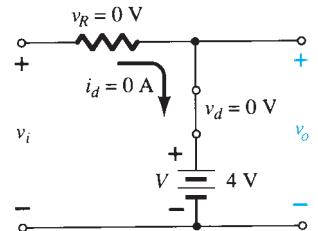
$$v_i = V - V_K = 4 \text{ V} - 0.7 \text{ V} = 3.3 \text{ V}$$

For input voltages greater than 3.3 V, the diode will be an open circuit and  $v_o = v_i$ . For input voltages less than 3.3 V, the diode will be in the “on” state and the network of Fig. 2.86 results, where

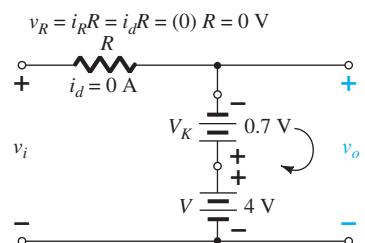
$$v_o = 4 \text{ V} - 0.7 \text{ V} = 3.3 \text{ V}$$

The resulting output waveform appears in Fig. 2.87. Note that the only effect of  $V_K$  was to drop the transition level to 3.3 from 4 V.

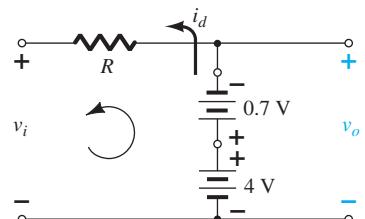
There is no question that including the effects of  $V_K$  will complicate the analysis somewhat, but once the analysis is understood with the ideal diode, the procedure, including the effects of  $V_K$ , will not be that difficult.



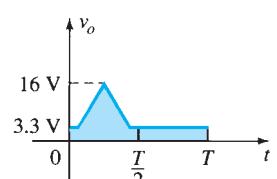
**FIG. 2.83**  
Determining the transition level for Example 2.20.



**FIG. 2.85**  
Determining the transition level for the network of Fig. 2.82.



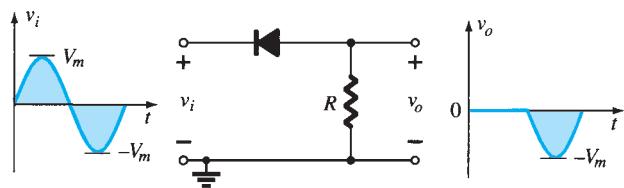
**FIG. 2.86**  
Determining  $v_o$  for the diode of Fig. 2.82 in the “on” state.



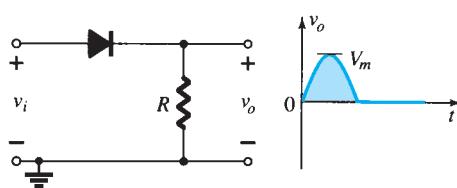
**FIG. 2.87**  
Sketching  $v_o$  for Example 2.21.

### Simple Series Clippers (Ideal Diodes)

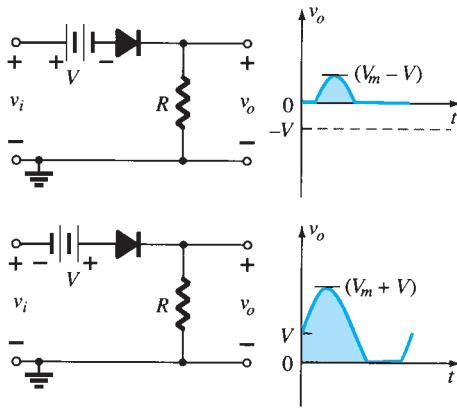
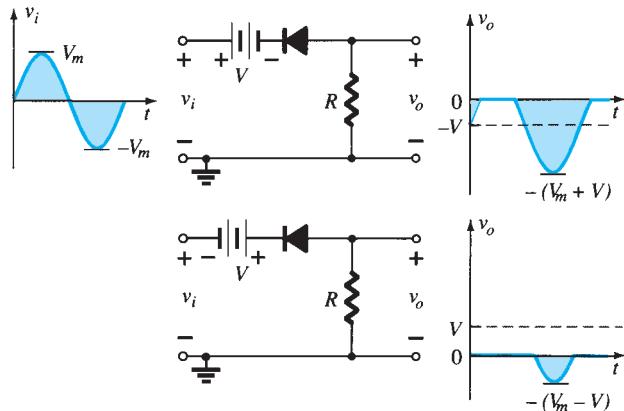
#### POSITIVE



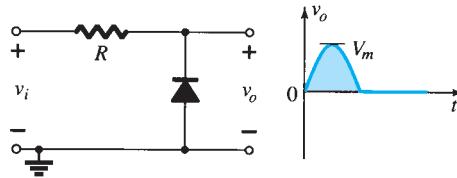
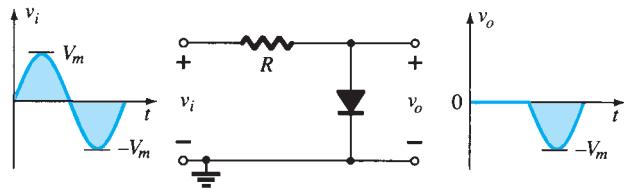
#### NEGATIVE



### Biased Series Clippers (Ideal Diodes)



### Simple Parallel Clippers (Ideal Diodes)



### Biased Parallel Clippers (Ideal Diodes)

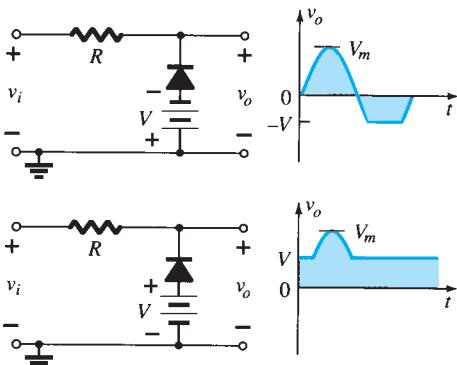
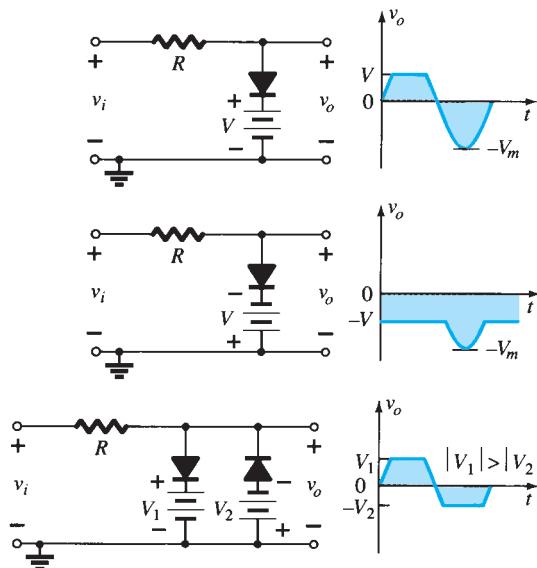


FIG. 2.88

Clipping circuits.

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in Fig. 2.88. In particular, note the response of the last configuration, with its ability to clip off a positive and a negative section as determined by the magnitude of the dc supplies.

## 2.9 CLAMPERS

The previous section investigated a number of diode configurations that clipped off a portion of the applied signal without changing the remaining part of the waveform. This section will examine a variety of diode configurations that shift the applied signal to a different level.

*A clamer is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.*

Additional shifts can also be obtained by introducing a dc supply to the basic structure. The chosen resistor and capacitor of the network must be chosen such that the time constant determined by  $\tau = RC$  is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we assume that for all practical purposes the capacitor fully charges or discharges in five time constants.

The simplest of clamer networks is provided in Fig. 2.89. It is important to note that the capacitor is connected directly between input and output signals and the resistor and the diode are connected in parallel with the output signal.

*Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.*

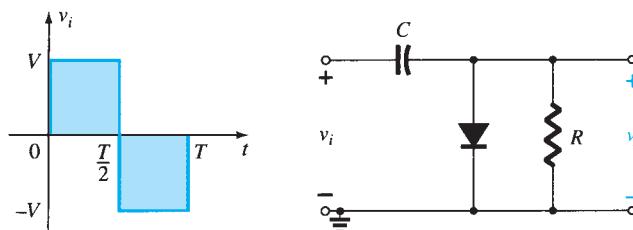


FIG. 2.89  
Clamer.

There is a sequence of steps that can be applied to help make the analysis straightforward. It is not the only approach to examining clammers, but it does offer an option if difficulties surface.

**Step 1: Start the analysis by examining the response of the portion of the input signal that will forward bias the diode.**

**Step 2: During the period that the diode is in the “on” state, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.**

For the network of Fig. 2.89 the diode will be forward biased for the positive portion of the applied signal. For the interval 0 to  $T/2$  the network will appear as shown in Fig. 2.90. The short-circuit equivalent for the diode will result in  $v_o = 0$  V for this time interval, as shown in the sketch of  $v_o$  in Fig. 2.92. During this same interval of time, the time constant determined by  $\tau = RC$  is very small because the resistor  $R$  has been effectively “shorted out” by the conducting diode and the only resistance present is the inherent (contact, wire) resistance of the network. The result is that the capacitor will quickly charge to the peak value of  $V$  volts as shown in Fig. 2.90 with the polarity indicated.

**Step 3: Assume that during the period when the diode is in the “off” state the capacitor holds on to its established voltage level.**

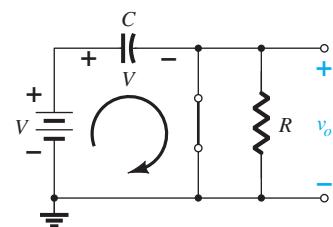


FIG. 2.90  
Diode “on” and the capacitor charging to  $V$  volts.

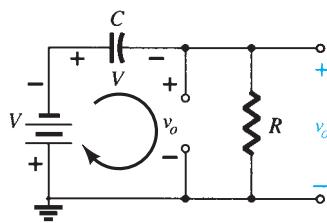


FIG. 2.91

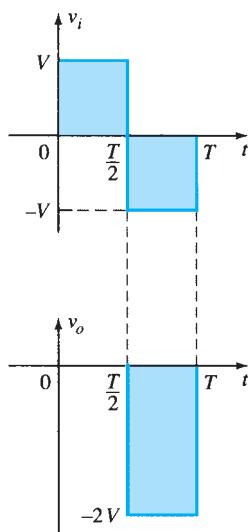
Determining  $v_o$  with the diode “off.”

FIG. 2.92

Sketching  $v_o$  for the network of Fig. 2.91.

**Step 4: Throughout the analysis, maintain a continual awareness of the location and defined polarity for  $v_o$  to ensure that the proper levels are obtained.**

When the input switches to the  $-V$  state, the network will appear as shown in Fig. 2.91, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both “pressuring” current through the diode from cathode to anode. Now that  $R$  is back in the network the time constant determined by the  $RC$  product is sufficiently large to establish a discharge period  $5\tau$ , much greater than the period  $T/2 \rightarrow T$ , and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since  $V = Q/C$ ) during this period.

Since  $v_o$  is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig. 2.91. Applying Kirchhoff's voltage law around the input loop results in

$$-V - V - v_o = 0$$

and

$$v_o = -2V$$

The negative sign results from the fact that the polarity of  $2V$  is opposite to the polarity defined for  $v_o$ . The resulting output waveform appears in Fig. 2.92 with the input signal. The output signal is clamped to 0 V for the interval 0 to  $T/2$  but maintains the same total swing (2V) as the input.

**Step 5: Check that the total swing of the output matches that of the input.**

This is a property that applies for all clamping networks, giving an excellent check on the results obtained.

**EXAMPLE 2.22** Determine  $v_o$  for the network of Fig. 2.93 for the input indicated.

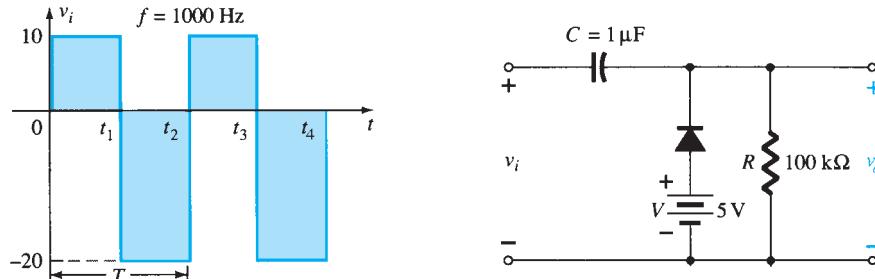


FIG. 2.93

Applied signal and network for Example 2.22.

**Solution:** Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period  $t_1 \rightarrow t_2$  of the input signal since the diode is in its short-circuit state. For this interval the network will appear as shown in Fig. 2.94. The output is across  $R$ , but it is also directly across the 5-V battery if one follows the direct connection between the defined terminals for  $v_o$  and the battery terminals. The result is  $v_o = 5$  V for this interval. Applying Kirchhoff's voltage law around the input loop results in

$$-20V + V_C - 5V = 0$$

and

$$V_C = 25V$$

The capacitor will therefore charge up to 25 V. In this case the resistor  $R$  is not shorted out by the diode, but a Thévenin equivalent circuit of that portion of the network that includes the battery and the resistor will result in  $R_{Th} = 0 \Omega$  with  $E_{Th} = V = 5$  V. For the period  $t_2 \rightarrow t_3$  the network will appear as shown in Fig. 2.95.

The open-circuit equivalent for the diode removes the 5-V battery from having any effect on  $v_o$ , and applying Kirchhoff's voltage law around the outside loop of the network results in

$$+10V + 25V - v_o = 0$$

and

$$v_o = 35V$$

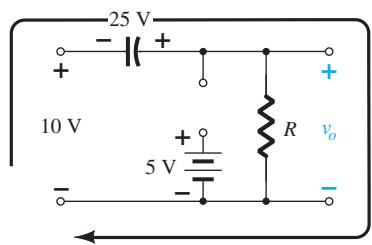


FIG. 2.95

Determining  $v_o$  with the diode in the “off” state.

The time constant of the discharging network of Fig. 2.95 is determined by the product  $RC$  and has the magnitude

$$\tau = RC = (100 \text{ k}\Omega)(0.1 \mu\text{F}) = 0.01 \text{ s} = 10 \text{ ms}$$

The total discharge time is therefore  $5\tau = 5(10 \text{ ms}) = 50 \text{ ms}$ .

Since the interval  $t_2 \rightarrow t_3$  will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.96 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

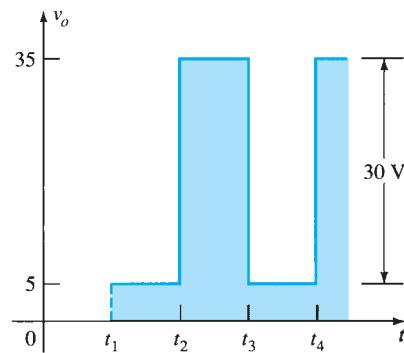
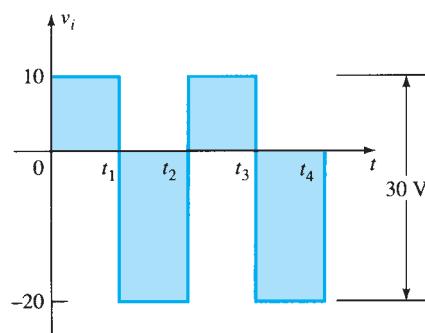


FIG. 2.96

$v_i$  and  $v_o$  for the clamp of Fig. 2.93.

**EXAMPLE 2.23** Repeat Example 2.22 using a silicon diode with  $V_K = 0.7 \text{ V}$ .

**Solution:** For the short-circuit state the network now takes on the appearance of Fig. 2.97, and  $v_o$  can be determined by Kirchhoff's voltage law in the output section:

$$+5 \text{ V} - 0.7 \text{ V} - v_o = 0$$

and

$$v_o = 5 \text{ V} - 0.7 \text{ V} = 4.3 \text{ V}$$

For the input section Kirchhoff's voltage law results in

$$-20 \text{ V} + V_C + 0.7 \text{ V} - 5 \text{ V} = 0$$

and

$$V_C = 25 \text{ V} - 0.7 \text{ V} = 24.3 \text{ V}$$

For the period  $t_2 \rightarrow t_3$  the network will now appear as in Fig. 2.98, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10 \text{ V} + 24.3 \text{ V} - v_o = 0$$

and

$$v_o = 34.3 \text{ V}$$

The resulting output appears in Fig. 2.99, verifying the statement that the input and output swings are the same.

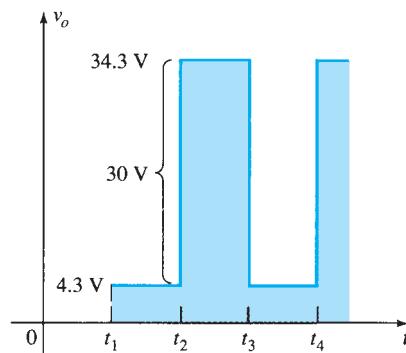


FIG. 2.99

Sketching  $v_o$  for the clamp of Fig. 2.93 with a silicon diode.

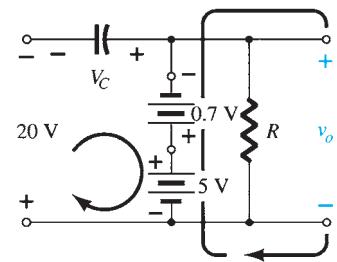


FIG. 2.97

Determining  $v_o$  and  $V_C$  with the diode in the "on" state.

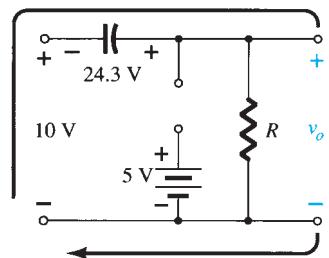


FIG. 2.98

Determining  $v_o$  with the diode in the open state.

## Clamping Networks

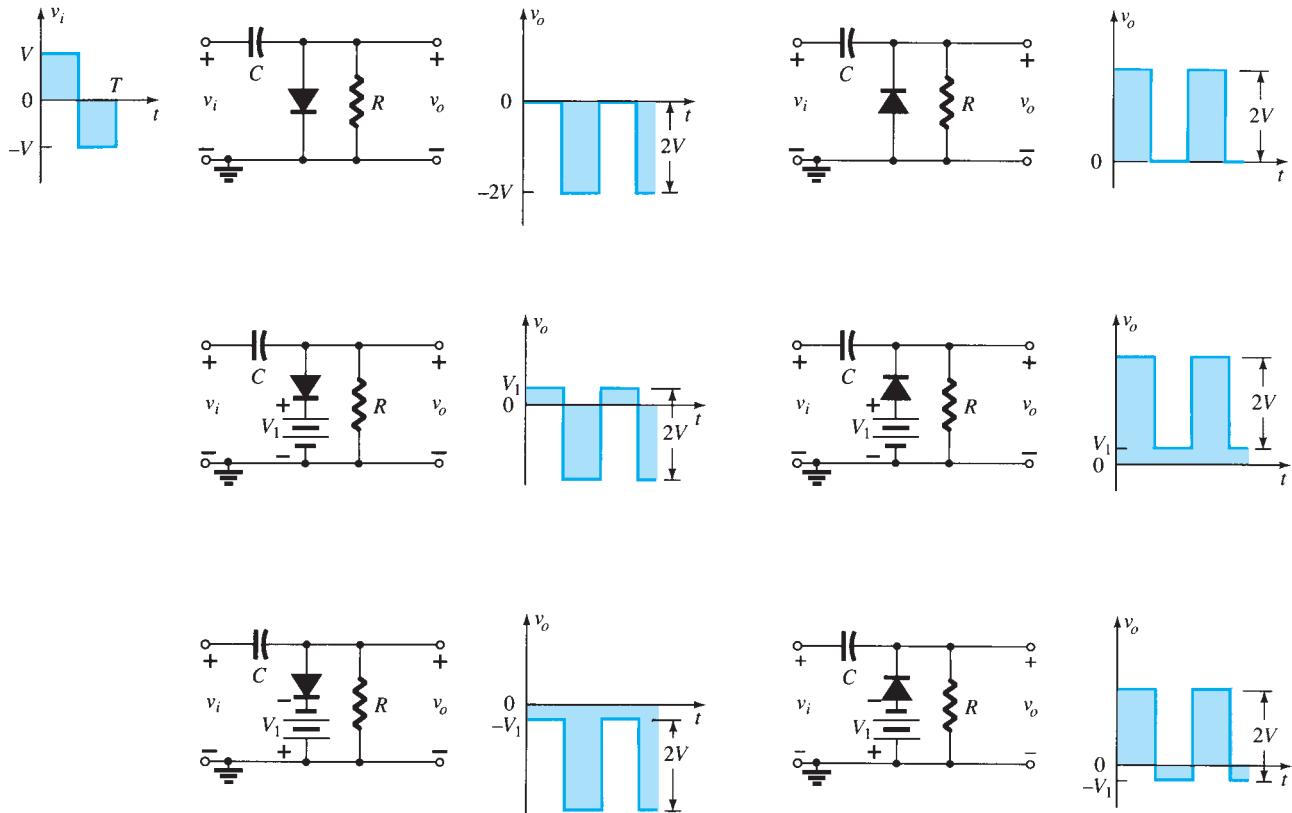


FIG. 2.100

Clamping circuits with ideal diodes ( $5\tau = 5RC \gg T/2$ ).

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.100. Although all the waveforms appearing in Fig. 2.100 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.101 for a network appearing in the bottom right of Fig. 2.100.

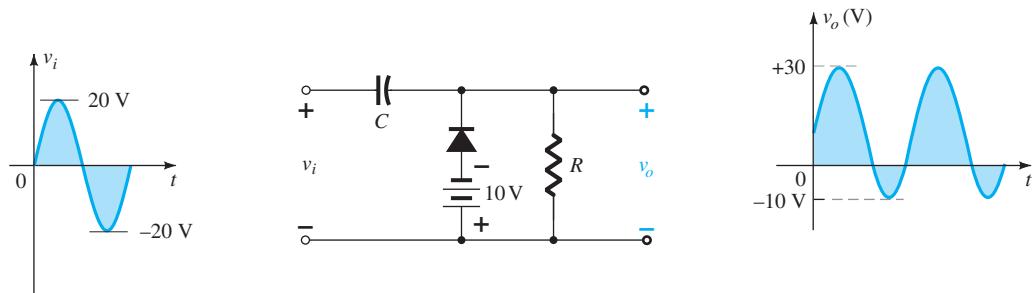


FIG. 2.101

Clamping network with a sinusoidal input.

## 2.10 NETWORKS WITH A DC AND AC SOURCE

The analysis thus far has been limited to circuits with a single dc, ac, or square wave input. This section will expand that analysis to include both an ac and a dc source in the same configuration. In Fig. 2.102 the simplest of two-source networks has been constructed.

\*30. Sketch  $v_o$  for the network of Fig. 2.174 and determine the dc voltage available.

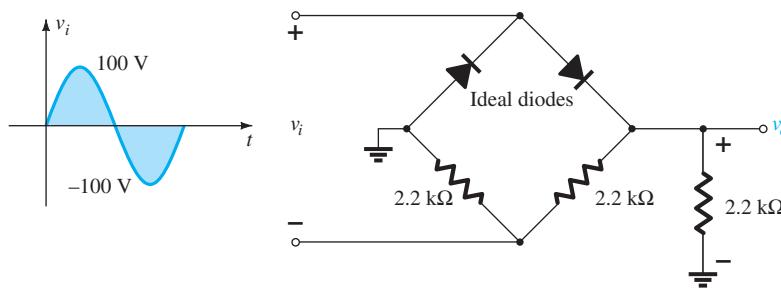


FIG. 2.174  
Problem 30.

\*31. Sketch  $v_o$  for the network of Fig. 2.175 and determine the dc voltage available.

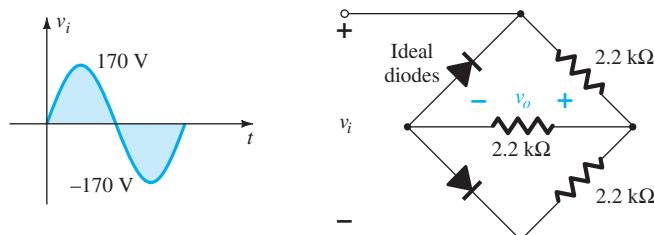


FIG. 2.175  
Problem 31.

## 2.8 Clippers

32. Determine  $v_o$  for each network of Fig. 2.176 for the input shown.

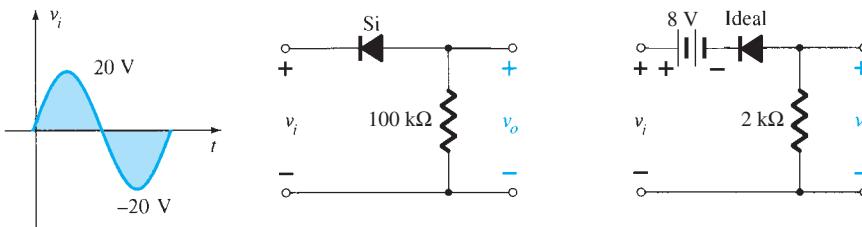


FIG. 2.176  
Problem 32.

33. Determine  $v_o$  for each network of Fig. 2.177 for the input shown.

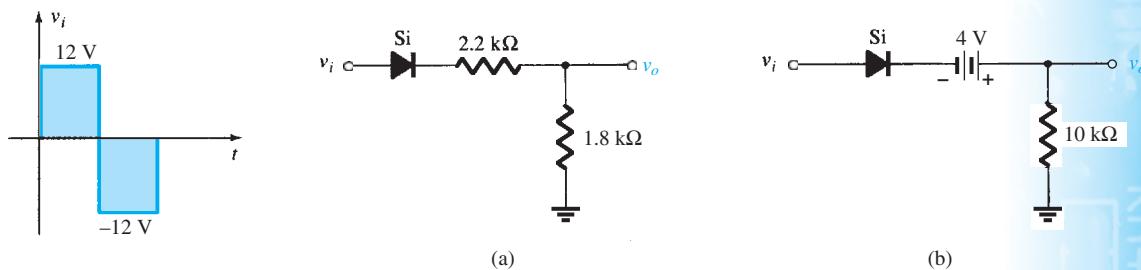


FIG. 2.177  
Problem 33.

\*34. Determine  $v_o$  for each network of Fig. 2.178 for the input shown.

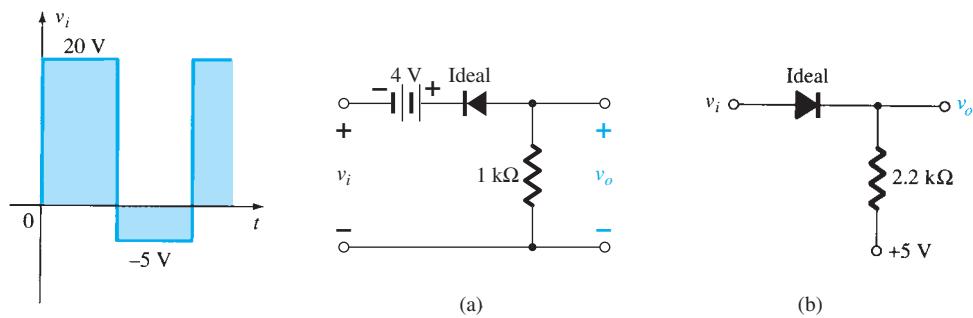


FIG. 2.178

Problem 34.

\*35. Determine  $v_o$  for each network of Fig. 2.179 for the input shown.

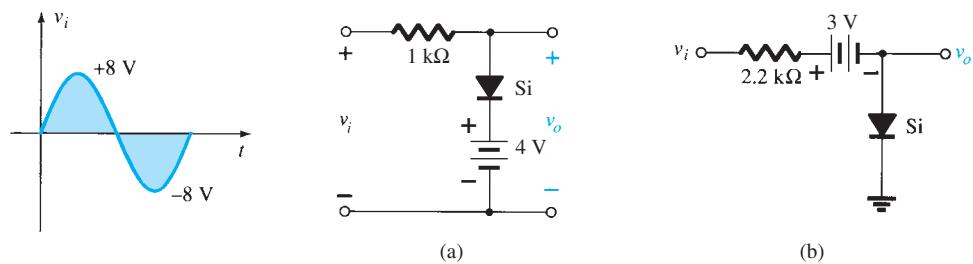


FIG. 2.179

Problem 35.

36. Sketch  $i_R$  and  $v_o$  for the network of Fig. 2.180 for the input shown.

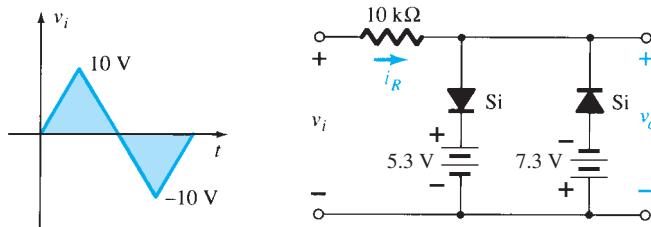


FIG. 2.180

Problem 36.

## 2.9 Clampers

37. Sketch  $v_o$  for each network of Fig. 2.181 for the input shown.

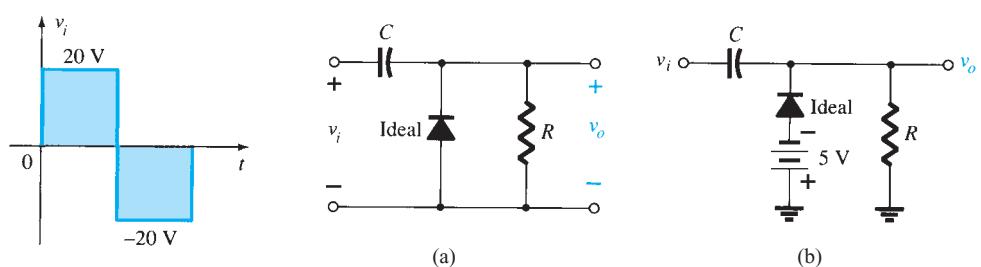


FIG. 2.181

Problem 37.

38. Sketch  $v_o$  for each network of Fig. 2.182 for the input shown.

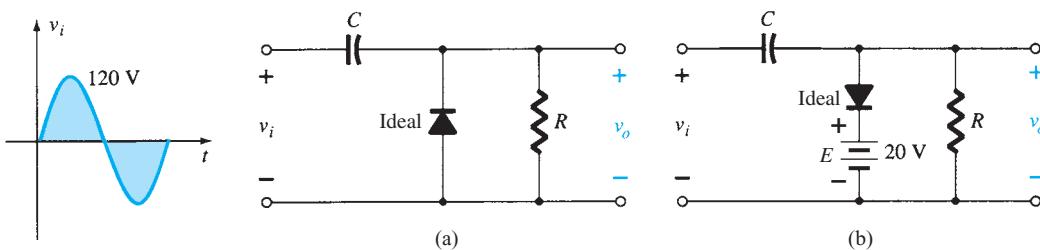


FIG. 2.182

Problem 38.

\*39. For the network of Fig. 2.183:

- Calculate  $5\tau$ .
- Compare  $5\tau$  to half the period of the applied signal.
- Sketch  $v_o$ .

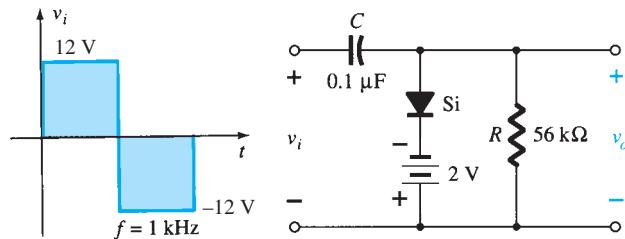


FIG. 2.183

Problem 39.

\*40. Design a clamper to perform the function indicated in Fig. 2.184.

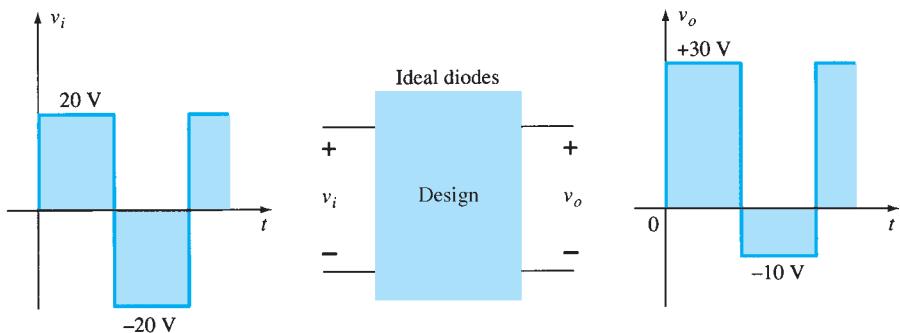


FIG. 2.184

Problem 40.

\*41. Design a clamper to perform the function indicated in Fig. 2.185.

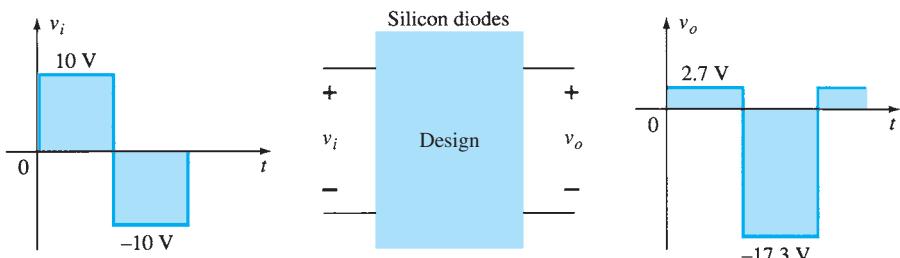


FIG. 2.185

Problem 41.