

FIG. 2.63

Determining the PIV level for the diodes of the CT transformer full-wave rectifier.

PIV The network of Fig. 2.63 will help us determine the net PIV for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and V_m as established by the adjoining loop results in

$$\begin{aligned} \text{PIV} &= V_{\text{secondary}} + V_R \\ &= V_m + V_m \end{aligned}$$

and

$$\text{PIV} \geq 2V_m \quad \text{CT transformer, full-wave rectifier} \quad (2.13)$$

EXAMPLE 2.17 Determine the output waveform for the network of Fig. 2.64 and calculate the output dc level and the required PIV of each diode.

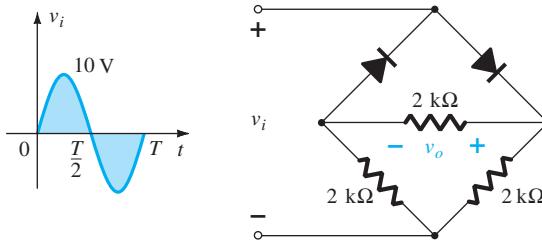


FIG. 2.64
Bridge network for Example 2.17.

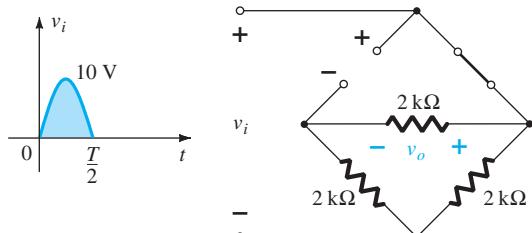


FIG. 2.65

Network of Fig. 2.64 for the positive region of v_i .

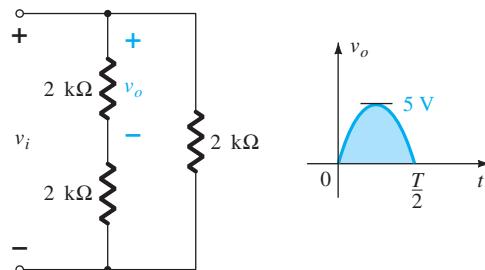


FIG. 2.66

Redrawn network of Fig. 2.65.

Solution: The network appears as shown in Fig. 2.65 for the positive region of the input voltage. Redrawing the network results in the configuration of Fig. 2.66, where $v_o = \frac{1}{2}v_i$ or $V_{o_{\text{max}}} = \frac{1}{2}V_{i_{\text{max}}} = \frac{1}{2}(10 \text{ V}) = 5 \text{ V}$, as shown in Fig. 2.66. For the negative part of the input, the roles of the diodes are interchanged and v_o appears as shown in Fig. 2.67.

The effect of removing two diodes from the bridge configuration is therefore to reduce the available dc level to the following:

$$V_{\text{dc}} = 0.636(5 \text{ V}) = 3.18 \text{ V}$$

or that available from a half-wave rectifier with the same input. However, the PIV as determined from Fig. 2.59 is equal to the maximum voltage across R , which is 5 V, or half of that required for a half-wave rectifier with the same input.

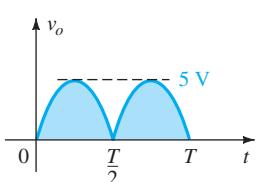


FIG. 2.67

Resulting output for Example 2.17.

2.8 CLIPPERS

The previous section on rectification gives clear evidence that diodes can be used to change the appearance of an applied waveform. This section on clippers and the next on clamps will expand on the wave-shaping abilities of diodes.

Clippers are networks that employ diodes to “clip” away a portion of an input signal without distorting the remaining part of the applied waveform.

The half-wave rectifier of Section 2.6 is an example of the simplest form of diode clipper—one resistor and a diode. Depending on the orientation of the diode, the positive or negative region of the applied signal is “clipped” off.

There are two general categories of clippers: *series* and *parallel*. The series configuration is defined as one where the diode is in series with the load, whereas the parallel variety has the diode in a branch parallel to the load.

Series

The response of the series configuration of Fig. 2.68a to a variety of alternating waveforms is provided in Fig. 2.68b. Although first introduced as a half-wave rectifier (for sinusoidal waveforms), there are no boundaries on the type of signals that can be applied to a clipper.

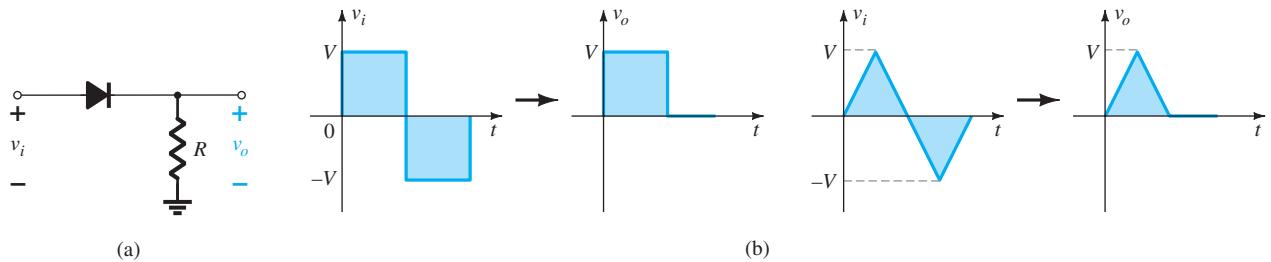


FIG. 2.68
Series clipper.

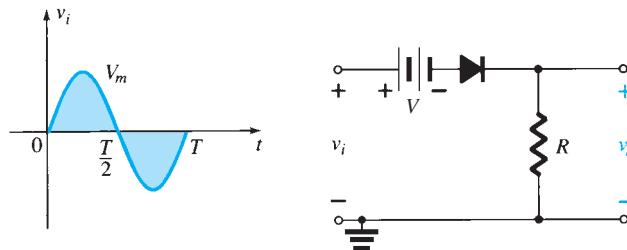


FIG. 2.69
Series clipper with a dc supply.

The addition of a dc supply to the network as shown in Fig. 2.69 can have a pronounced effect on the analysis of the series clipper configuration. The response is not as obvious because the dc supply can aid or work against the source voltage, and the dc supply can be in the leg between the supply and output or in the branch parallel to the output.

There is no general procedure for analyzing networks such as the type in Fig. 2.69, but there are some things one can do to give the analysis some direction.

First and most important:

1. Take careful note of where the output voltage is defined.

In Fig. 2.69 it is directly across the resistor R . In some cases it may be across a combination of series elements.

Next:

2. Try to develop an overall sense of the response by simply noting the “pressure” established by each supply and the effect it will have on the conventional current direction through the diode.

In Fig. 2.69, for instance, any positive voltage of the supply will try to turn the diode on by establishing a conventional current through the diode that matches the arrow in the diode symbol. However, the added dc supply V will oppose that applied voltage and try to keep the diode in the “off” state. The result is that any supply voltage greater than V volts will turn the diode on and conduction can be established through the load resistor. Keep in mind that we are dealing with an ideal diode for the moment, so the turn-on voltage is simply 0 V. In general, therefore, for the network of Fig. 2.69 we can conclude that the

diode will be on for any voltage v_i that is greater than V volts and off for any lesser voltage. For the “off” condition, the output would be 0 V due to the lack of current, and for the “on” condition it would simply be $v_o = v_i - V$ as determined by Kirchhoff’s voltage law.

3. Determine the applied voltage (transition voltage) that will result in a change of state for the diode from the “off” to the “on” state.

This step will help to define a region of the applied voltage when the diode is on and when it is off. On the characteristics of an ideal diode this will occur when $V_D = 0$ V and $I_D = 0$ mA. For the approximate equivalent this is determined by finding the applied voltage when the diode has a drop of 0.7 V across it (for silicon) and $I_D = 0$ mA.

This exercise was applied to the network of Fig. 2.69 as shown in Fig. 2.70. Note the substitution of the short-circuit equivalent for the diode and the fact that the voltage across the resistor is 0 V because the diode current is 0 mA. The result is $v_i - V = 0$, and so

$$v_i = V \quad (2.14)$$

is the transition voltage.

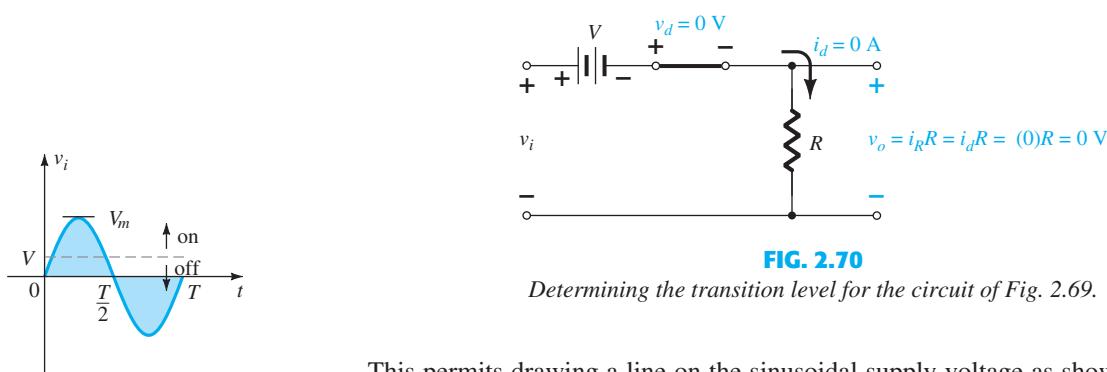


FIG. 2.70
Determining the transition level for the circuit of Fig. 2.69.

This permits drawing a line on the sinusoidal supply voltage as shown in Fig. 2.71 to define the regions where the diode is on and off.

For the “on” region, as shown in Fig. 2.72, the diode is replaced by a short-circuit equivalent, and the output voltage is defined by

$$v_o = v_i - V \quad (2.15)$$

For the “off” region, the diode is an open circuit, $I_D = 0$ mA, and the output voltage is

$$v_o = 0$$

4. It is often helpful to draw the output waveform directly below the applied voltage using the same scales for the horizontal axis and the vertical axis.

Using this last piece of information, we can establish the 0-V level on the plot of Fig. 2.73 for the region indicated. For the “on” condition, Eq. (2.15) can be used to find the output voltage when the applied voltage has its peak value:

$$v_{o_{\text{peak}}} = V_m - V$$

and this can be added to the plot of Fig. 2.73. It is then simple to fill in the missing section of the output curve.

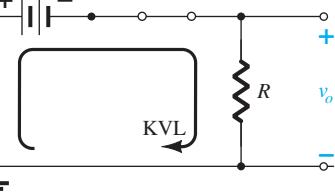


FIG. 2.72

Determining v_o for the diode in the “on” state.

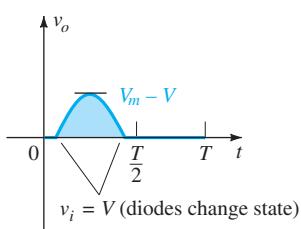


FIG. 2.73

Sketching the waveform of v_o using the results obtained for v_o above and below the transition level.

EXAMPLE 2.18 Determine the output waveform for the sinusoidal input of Fig. 2.74.

Solution:

Step 1: The output is again directly across the resistor R .

Step 2: The positive region of v_i and the dc supply are both applying “pressure” to turn the diode on. The result is that we can safely assume the diode is in the “on” state for the entire range of positive voltages for v_i . Once the supply goes negative, it would have to exceed the dc supply voltage of 5 V before it could turn the diode off.

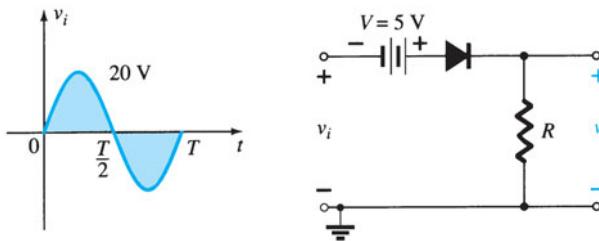


FIG. 2.74
Series clipper for Example 2.18.

Step 3: The transition model is substituted in Fig. 2.75, and we find that the transition from one state to the other will occur when

$$v_i + 5 \text{ V} = 0 \text{ V}$$

or

$$v_i = -5 \text{ V}$$

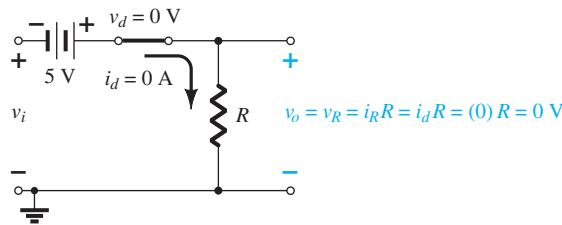


FIG. 2.75
Determining the transition level for the clipper of Fig. 2.74.

Step 4: In Fig. 2.76 a horizontal line is drawn through the applied voltage at the transition level. For voltages less than -5 V the diode is in the open-circuit state and the output is 0 V , as shown in the sketch of v_o . Using Fig. 2.76, we find that for conditions when the diode is on and the diode current is established the output voltage will be the following, as determined using Kirchhoff's voltage law:

$$v_o = v_i + 5 \text{ V}$$

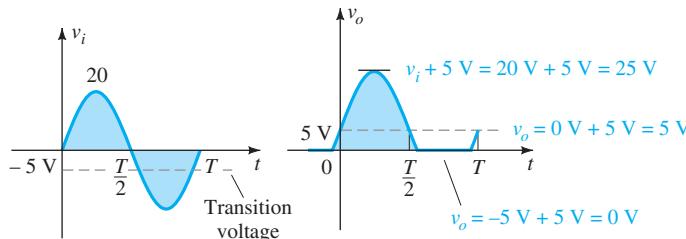


FIG. 2.76
Sketching v_o for Example 2.18.

The analysis of clipper networks with square-wave inputs is actually easier than with sinusoidal inputs because only two levels have to be considered. In other words, the network can be analyzed as if it had two dc level inputs with the resulting v_o plotted in the proper time frame. The next example demonstrates the procedure.

EXAMPLE 2.19 Find the output voltage for the network examined in Example 2.18 if the applied signal is the square wave of Fig. 2.77.

Solution: For $v_i = 20 \text{ V}$ ($0 \rightarrow T/2$) the network of Fig. 2.78 results. The diode is in the short-circuit state, and $v_o = 20 \text{ V} + 5 \text{ V} = 25 \text{ V}$. For $v_i = -10 \text{ V}$ the network of Fig. 2.79

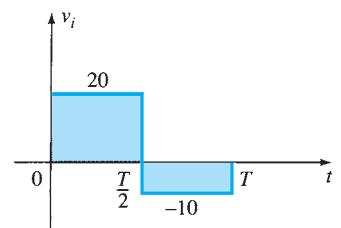


FIG. 2.77
Applied signal for Example 2.19.

results, placing the diode in the “off” state, and $v_o = i_R R = (0)R = 0$ V. The resulting output voltage appears in Fig. 2.80.

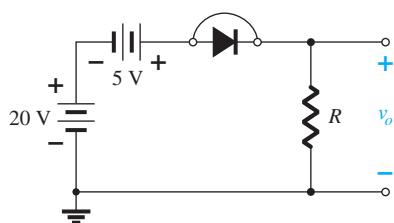


FIG. 2.78
 v_o at $v_i = +20$ V.

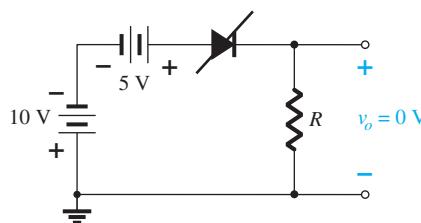


FIG. 2.79
 v_o at $v_i = -10$ V.

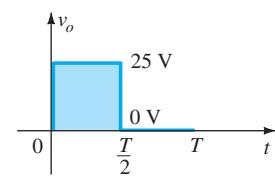


FIG. 2.80
Sketching v_o for Example 2.19.

Note in Example 2.19 that the clipper not only clipped off 5 V from the total swing, but also raised the dc level of the signal by 5 V.

Parallel

The network of Fig. 2.81 is the simplest of parallel diode configurations with the output for the same inputs of Fig. 2.68. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.

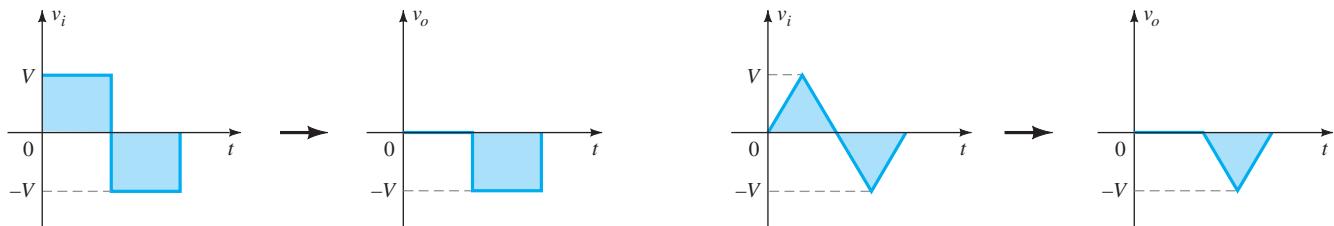
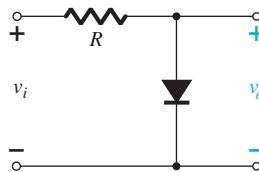


FIG. 2.81
Response to a parallel clipper.

EXAMPLE 2.20 Determine v_o for the network of Fig. 2.82.

Solution:

Step 1: In this example the output is defined across the series combination of the 4-V supply and the diode, not across the resistor R .

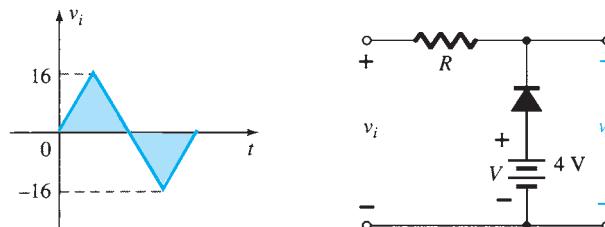


FIG. 2.82
Example 2.20.

Step 2: The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the “on” state for a good portion of the negative region of the input signal. In fact, it is interesting to note that since the output is directly across the series combination, when the diode is in its short-circuit state the output voltage will be directly across the 4-V dc supply, requiring that the output be fixed at 4 V. In other words, when the diode is on the output will be 4 V. Other than that, when the diode is an open circuit, the current through the series network will be 0 mA and the voltage drop across the resistor will be 0 V. That will result in $v_o = v_i$ whenever the diode is off.

Step 3: The transition level of the input voltage can be found from Fig. 2.83 by substituting the short-circuit equivalent and remembering the diode current is 0 mA at the instant of transition. The result is a change in state when

$$v_i = 4 \text{ V}$$

Step 4: In Fig. 2.84 the transition level is drawn along with $v_o = 4 \text{ V}$ when the diode is on. For $v_i \geq 4 \text{ V}$, $v_o = 4 \text{ V}$, and the waveform is simply repeated on the output plot.

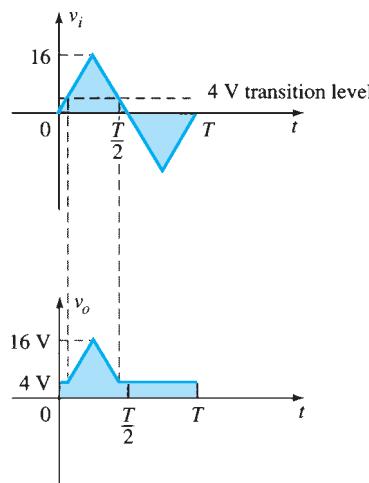


FIG. 2.84
Sketching v_o for Example 2.20.

To examine the effects of the knee voltage V_K of a silicon diode on the output response, the next example will specify a silicon diode rather than the ideal diode equivalent.

EXAMPLE 2.21 Repeat Example 2.20 using a silicon diode with $V_K = 0.7 \text{ V}$.

Solution: The transition voltage can first be determined by applying the condition $i_d = 0 \text{ A}$ at $v_d = V_D = 0.7 \text{ V}$ and obtaining the network of Fig. 2.85. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$v_i + V_K - V = 0$$

and

$$v_i = V - V_K = 4 \text{ V} - 0.7 \text{ V} = 3.3 \text{ V}$$

For input voltages greater than 3.3 V, the diode will be an open circuit and $v_o = v_i$. For input voltages less than 3.3 V, the diode will be in the “on” state and the network of Fig. 2.86 results, where

$$v_o = 4 \text{ V} - 0.7 \text{ V} = 3.3 \text{ V}$$

The resulting output waveform appears in Fig. 2.87. Note that the only effect of V_K was to drop the transition level to 3.3 from 4 V.

There is no question that including the effects of V_K will complicate the analysis somewhat, but once the analysis is understood with the ideal diode, the procedure, including the effects of V_K , will not be that difficult.

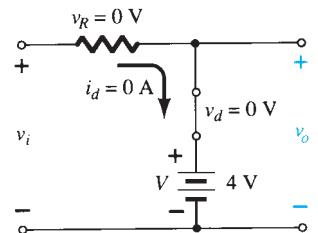


FIG. 2.83
Determining the transition level for Example 2.20.

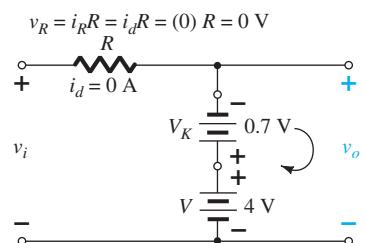


FIG. 2.85
Determining the transition level for the network of Fig. 2.82.

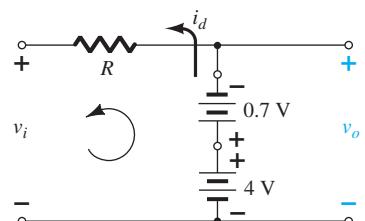


FIG. 2.86
Determining v_o for the diode of Fig. 2.82 in the “on” state.

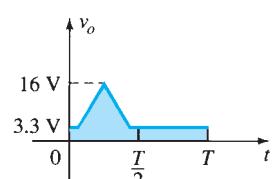
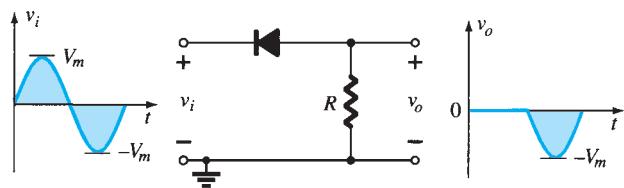


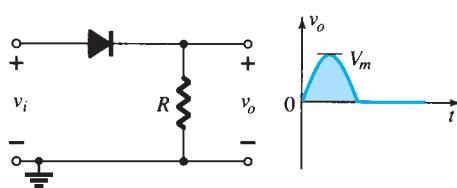
FIG. 2.87
Sketching v_o for Example 2.21.

Simple Series Clippers (Ideal Diodes)

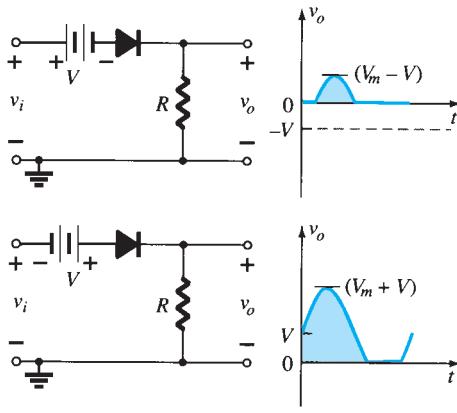
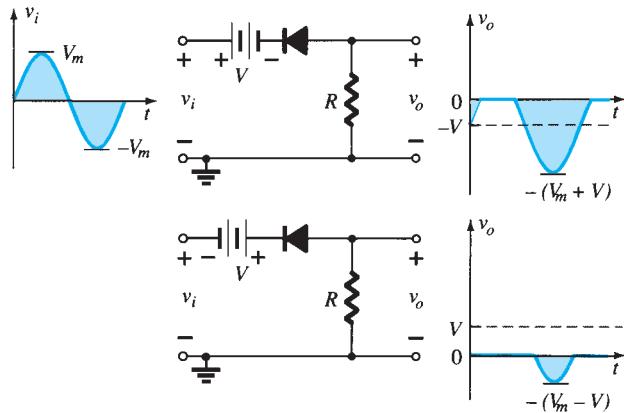
POSITIVE



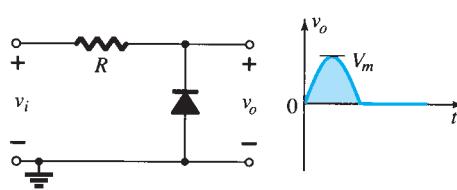
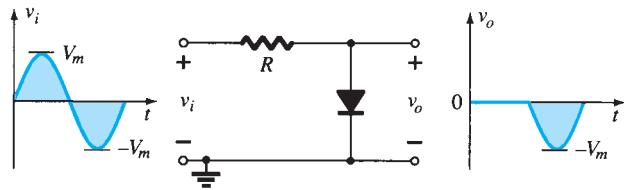
NEGATIVE



Biased Series Clippers (Ideal Diodes)



Simple Parallel Clippers (Ideal Diodes)



Biased Parallel Clippers (Ideal Diodes)

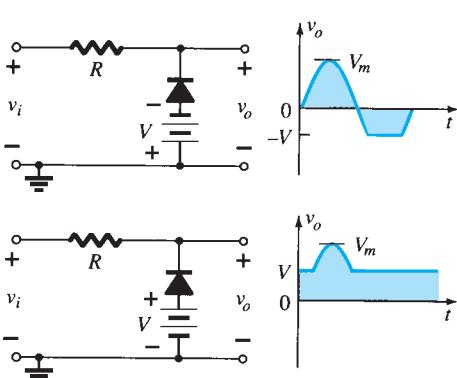
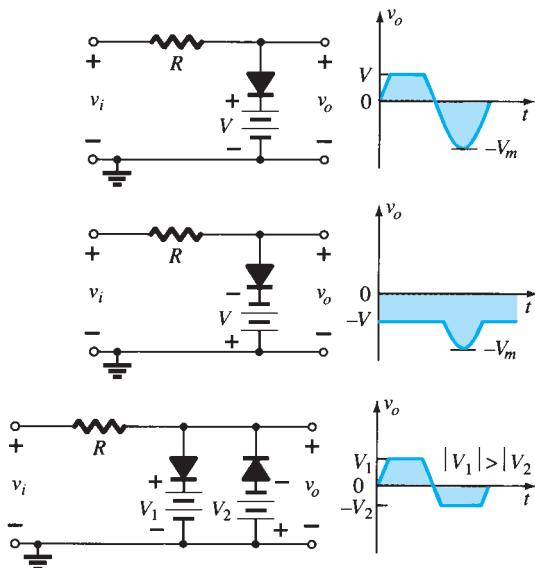


FIG. 2.88

Clipping circuits.

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in Fig. 2.88. In particular, note the response of the last configuration, with its ability to clip off a positive and a negative section as determined by the magnitude of the dc supplies.

2.9 CLAMPERS

The previous section investigated a number of diode configurations that clipped off a portion of the applied signal without changing the remaining part of the waveform. This section will examine a variety of diode configurations that shift the applied signal to a different level.

A clamer is a network constructed of a diode, a resistor, and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal.

Additional shifts can also be obtained by introducing a dc supply to the basic structure. The chosen resistor and capacitor of the network must be chosen such that the time constant determined by $\tau = RC$ is sufficiently large to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we assume that for all practical purposes the capacitor fully charges or discharges in five time constants.

The simplest of clamer networks is provided in Fig. 2.89. It is important to note that the capacitor is connected directly between input and output signals and the resistor and the diode are connected in parallel with the output signal.

Clamping networks have a capacitor connected directly from input to output with a resistive element in parallel with the output signal. The diode is also in parallel with the output signal but may or may not have a series dc supply as an added element.

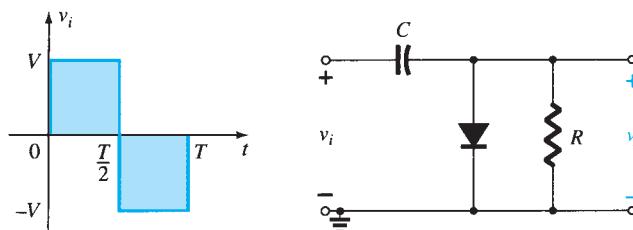


FIG. 2.89
Clamer.

There is a sequence of steps that can be applied to help make the analysis straightforward. It is not the only approach to examining clammers, but it does offer an option if difficulties surface.

Step 1: Start the analysis by examining the response of the portion of the input signal that will forward bias the diode.

Step 2: During the period that the diode is in the “on” state, assume that the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.

For the network of Fig. 2.89 the diode will be forward biased for the positive portion of the applied signal. For the interval 0 to $T/2$ the network will appear as shown in Fig. 2.90. The short-circuit equivalent for the diode will result in $v_o = 0$ V for this time interval, as shown in the sketch of v_o in Fig. 2.92. During this same interval of time, the time constant determined by $\tau = RC$ is very small because the resistor R has been effectively “shorted out” by the conducting diode and the only resistance present is the inherent (contact, wire) resistance of the network. The result is that the capacitor will quickly charge to the peak value of V volts as shown in Fig. 2.90 with the polarity indicated.

Step 3: Assume that during the period when the diode is in the “off” state the capacitor holds on to its established voltage level.

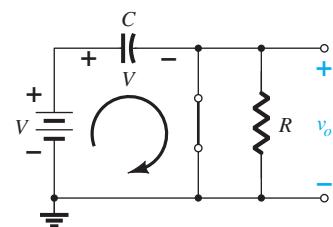


FIG. 2.90
Diode “on” and the capacitor charging to V volts.

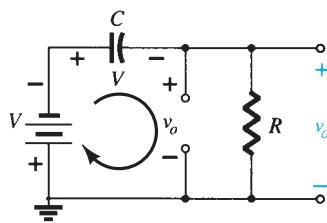


FIG. 2.91

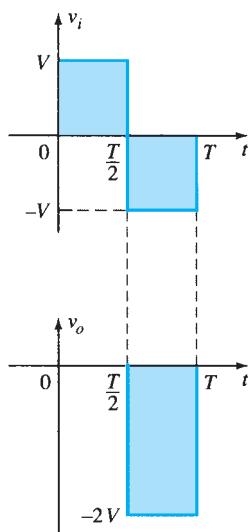
Determining v_o with the diode “off.”

FIG. 2.92

Sketching v_o for the network of Fig. 2.91.

Step 4: Throughout the analysis, maintain a continual awareness of the location and defined polarity for v_o to ensure that the proper levels are obtained.

When the input switches to the $-V$ state, the network will appear as shown in Fig. 2.91, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both “pressuring” current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period 5τ , much greater than the period $T/2 \rightarrow T$, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since $V = Q/C$) during this period.

Since v_o is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig. 2.91. Applying Kirchhoff's voltage law around the input loop results in

$$-V - V - v_o = 0$$

and

$$v_o = -2V$$

The negative sign results from the fact that the polarity of $2V$ is opposite to the polarity defined for v_o . The resulting output waveform appears in Fig. 2.92 with the input signal. The output signal is clamped to 0 V for the interval 0 to $T/2$ but maintains the same total swing (2V) as the input.

Step 5: Check that the total swing of the output matches that of the input.

This is a property that applies for all clamping networks, giving an excellent check on the results obtained.

EXAMPLE 2.22 Determine v_o for the network of Fig. 2.93 for the input indicated.

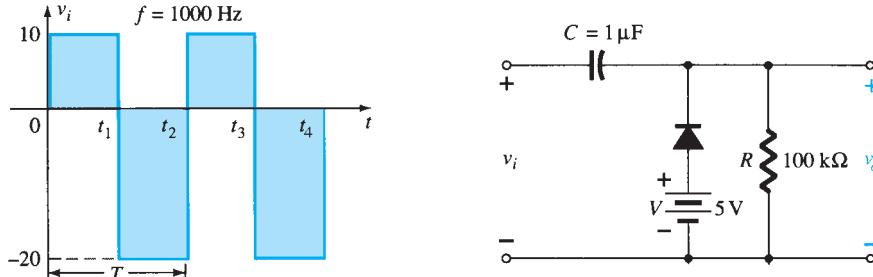


FIG. 2.93

Applied signal and network for Example 2.22.

Solution: Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in its short-circuit state. For this interval the network will appear as shown in Fig. 2.94. The output is across R , but it is also directly across the 5-V battery if one follows the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5V$ for this interval. Applying Kirchhoff's voltage law around the input loop results in

$$-20V + V_C - 5V = 0$$

and

$$V_C = 25V$$

The capacitor will therefore charge up to 25 V. In this case the resistor R is not shorted out by the diode, but a Thévenin equivalent circuit of that portion of the network that includes the battery and the resistor will result in $R_{Th} = 0 \Omega$ with $E_{Th} = V = 5V$. For the period $t_2 \rightarrow t_3$ the network will appear as shown in Fig. 2.95.

The open-circuit equivalent for the diode removes the 5-V battery from having any effect on v_o , and applying Kirchhoff's voltage law around the outside loop of the network results in

$$+10V + 25V - v_o = 0$$

and

$$v_o = 35V$$

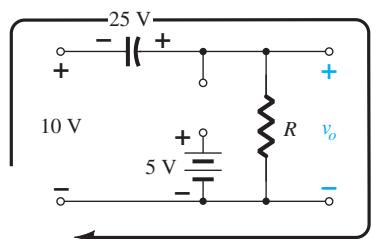


FIG. 2.95

Determining v_o with the diode in the “off” state.

The time constant of the discharging network of Fig. 2.95 is determined by the product RC and has the magnitude

$$\tau = RC = (100 \text{ k}\Omega)(0.1 \mu\text{F}) = 0.01 \text{ s} = 10 \text{ ms}$$

The total discharge time is therefore $5\tau = 5(10 \text{ ms}) = 50 \text{ ms}$.

Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.96 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

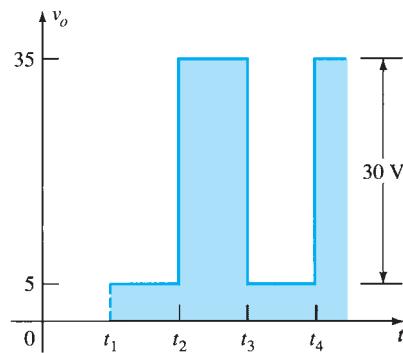
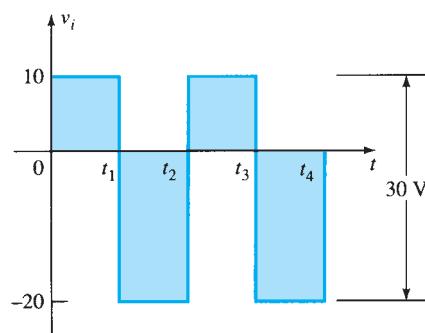


FIG. 2.96

v_i and v_o for the clamp of Fig. 2.93.

EXAMPLE 2.23 Repeat Example 2.22 using a silicon diode with $V_K = 0.7 \text{ V}$.

Solution: For the short-circuit state the network now takes on the appearance of Fig. 2.97, and v_o can be determined by Kirchhoff's voltage law in the output section:

$$+5 \text{ V} - 0.7 \text{ V} - v_o = 0$$

and

$$v_o = 5 \text{ V} - 0.7 \text{ V} = 4.3 \text{ V}$$

For the input section Kirchhoff's voltage law results in

$$-20 \text{ V} + V_C + 0.7 \text{ V} - 5 \text{ V} = 0$$

and

$$V_C = 25 \text{ V} - 0.7 \text{ V} = 24.3 \text{ V}$$

For the period $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.98, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10 \text{ V} + 24.3 \text{ V} - v_o = 0$$

and

$$v_o = 34.3 \text{ V}$$

The resulting output appears in Fig. 2.99, verifying the statement that the input and output swings are the same.

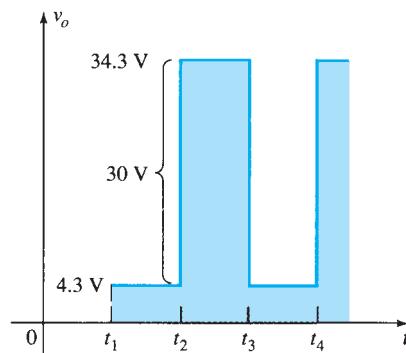


FIG. 2.99

Sketching v_o for the clamp of Fig. 2.93 with a silicon diode.

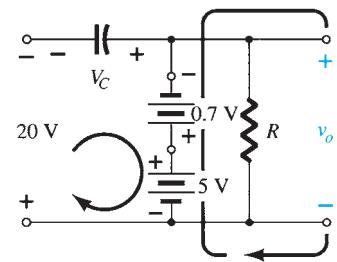


FIG. 2.97

Determining v_o and V_C with the diode in the "on" state.

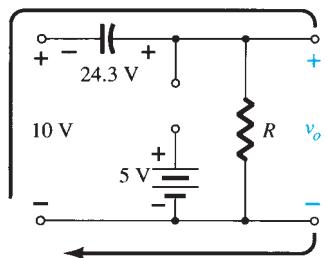


FIG. 2.98

Determining v_o with the diode in the open state.

Clamping Networks

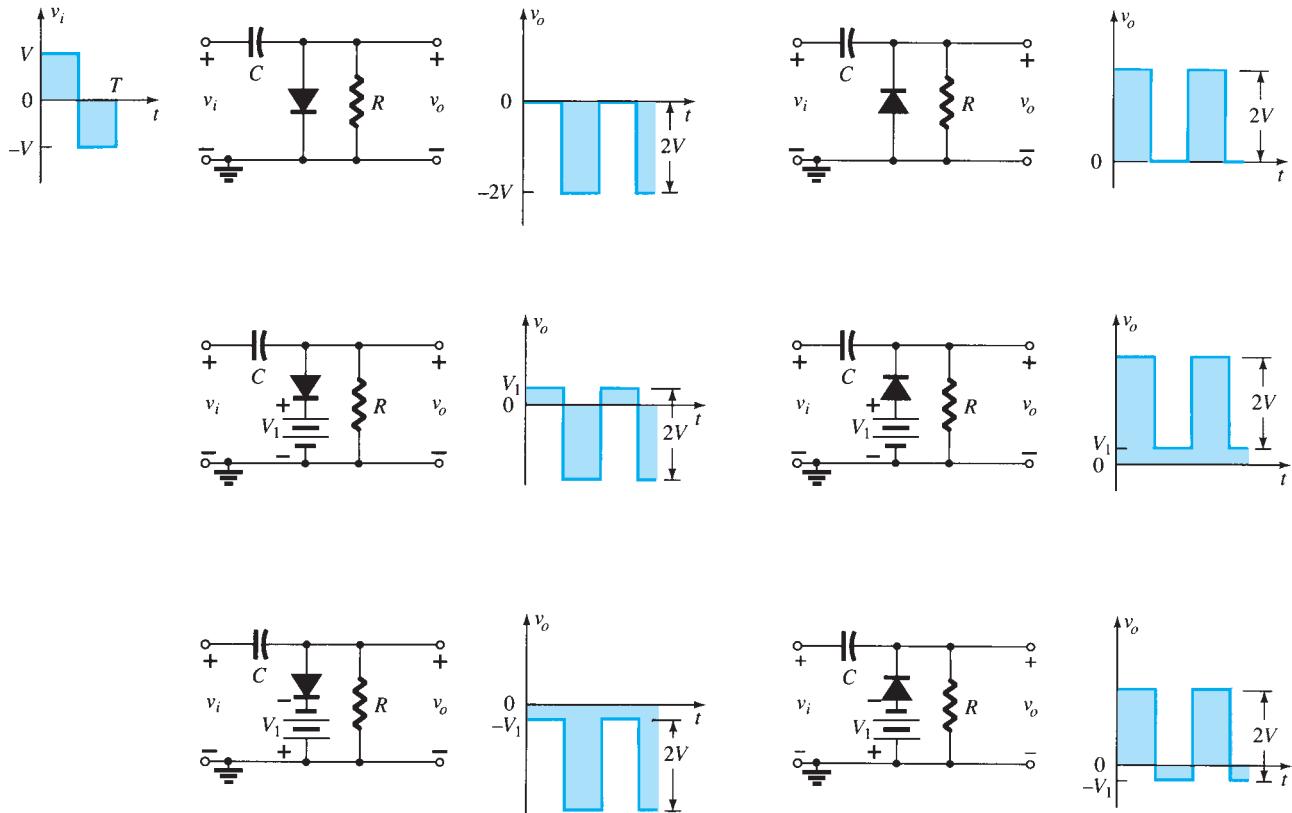


FIG. 2.100
Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.100. Although all the waveforms appearing in Fig. 2.100 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.101 for a network appearing in the bottom right of Fig. 2.100.

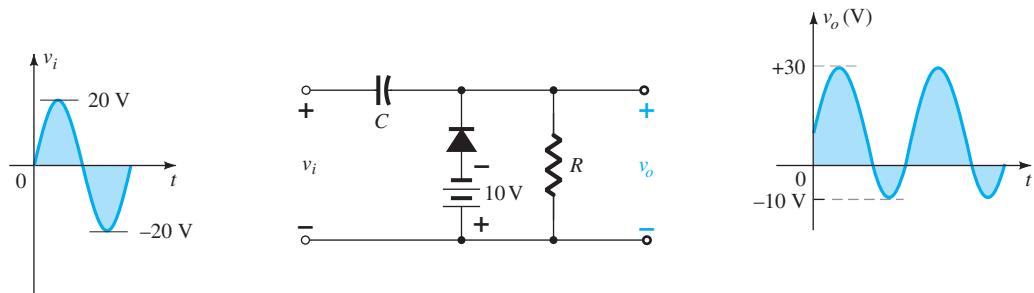


FIG. 2.101
Clamping network with a sinusoidal input.

2.10 NETWORKS WITH A DC AND AC SOURCE

The analysis thus far has been limited to circuits with a single dc, ac, or square wave input. This section will expand that analysis to include both an ac and a dc source in the same configuration. In Fig. 2.102 the simplest of two-source networks has been constructed.

*30. Sketch v_o for the network of Fig. 2.174 and determine the dc voltage available.

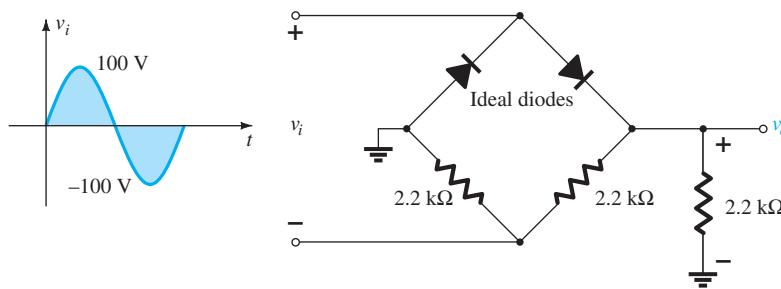


FIG. 2.174
Problem 30.

*31. Sketch v_o for the network of Fig. 2.175 and determine the dc voltage available.

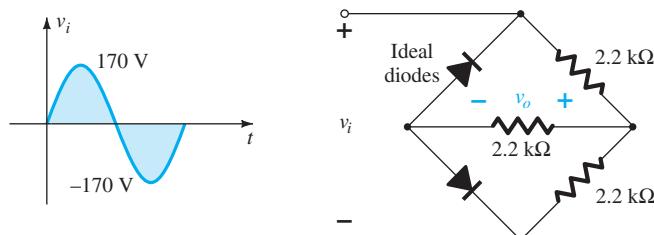


FIG. 2.175
Problem 31.

2.8 Clippers

32. Determine v_o for each network of Fig. 2.176 for the input shown.

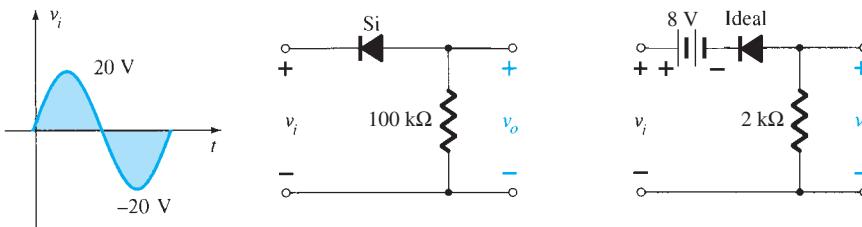


FIG. 2.176
Problem 32.

33. Determine v_o for each network of Fig. 2.177 for the input shown.

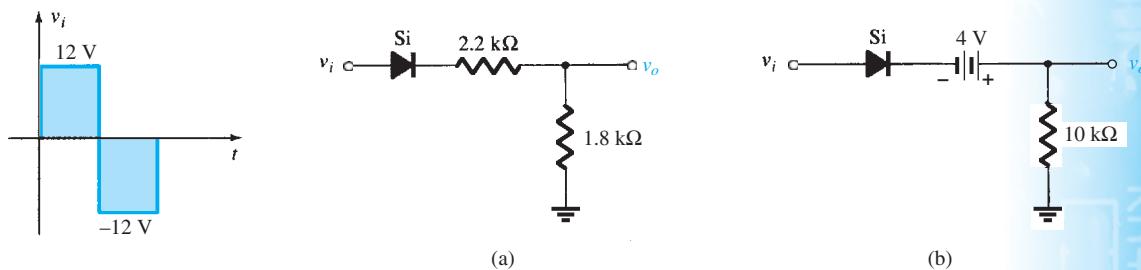


FIG. 2.177
Problem 33.

*34. Determine v_o for each network of Fig. 2.178 for the input shown.

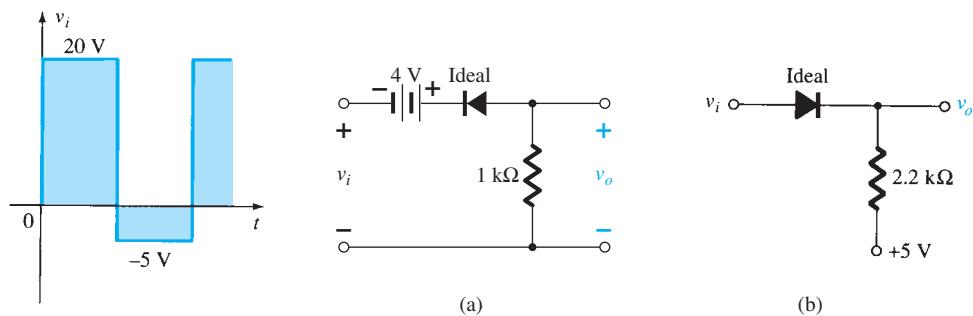


FIG. 2.178

Problem 34.

*35. Determine v_o for each network of Fig. 2.179 for the input shown.

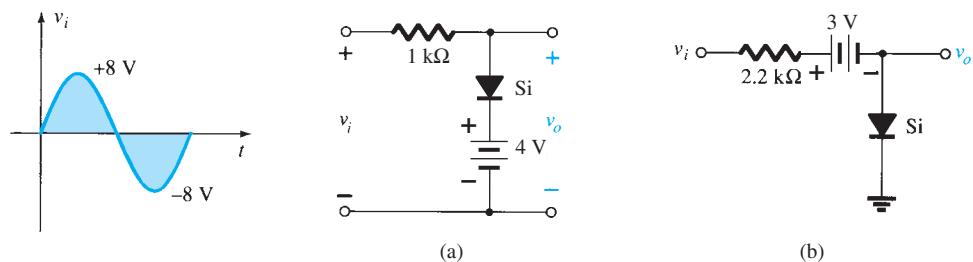


FIG. 2.179

Problem 35.

36. Sketch i_R and v_o for the network of Fig. 2.180 for the input shown.

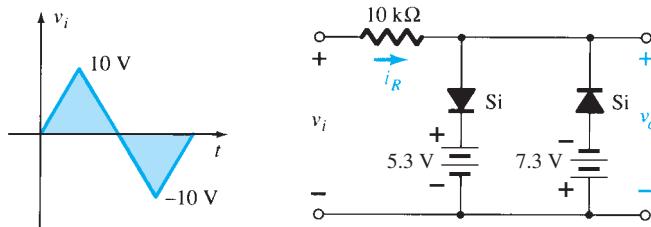


FIG. 2.180

Problem 36.

2.9 Clampers

37. Sketch v_o for each network of Fig. 2.181 for the input shown.

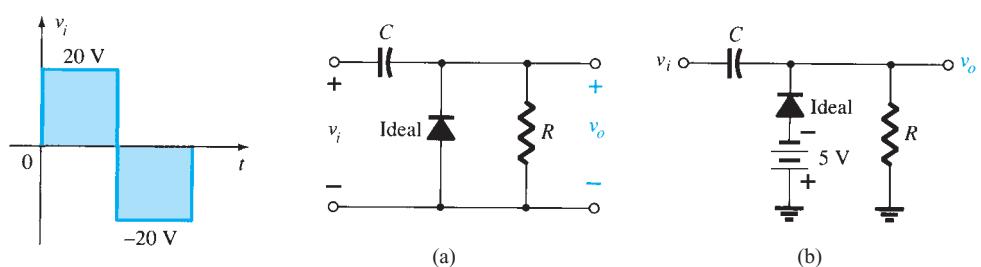


FIG. 2.181

Problem 37.

38. Sketch v_o for each network of Fig. 2.182 for the input shown.

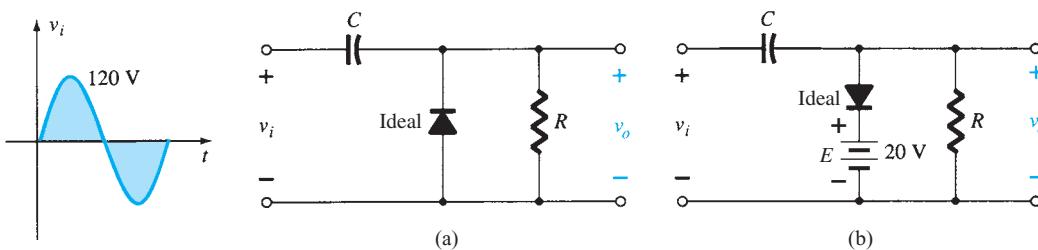


FIG. 2.182

Problem 38.

*39. For the network of Fig. 2.183:

- Calculate 5τ .
- Compare 5τ to half the period of the applied signal.
- Sketch v_o .

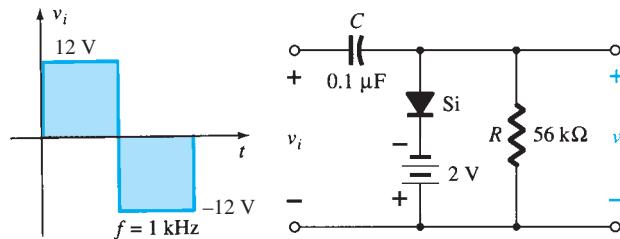


FIG. 2.183

Problem 39.

*40. Design a clamper to perform the function indicated in Fig. 2.184.

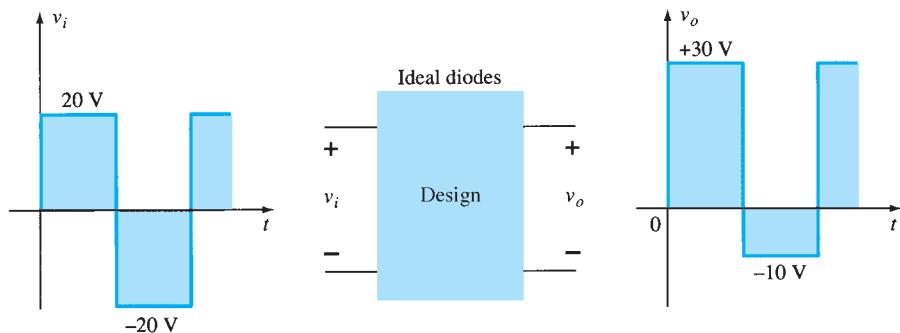


FIG. 2.184

Problem 40.

*41. Design a clamper to perform the function indicated in Fig. 2.185.

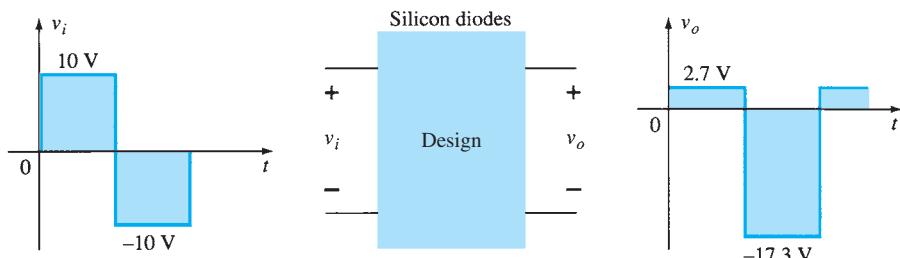


FIG. 2.185

Problem 41.

CHAPTER 1

Introduction to Op Amps

LEARNING OBJECTIVES

Upon completing this introductory chapter on op amps, you will be able to:

- Understand why analog circuitry using op amps is still required in computer-based systems.
- Draw the circuit symbol for a general-purpose op amp such as the 741 and show the pin numbers for each terminal.
- Name and identify at least three types of package styles that house a general-purpose op amp.
- Identify the manufacturer, op amp, and package style from the PIN.
- Correctly place an order for an op amp.
- Identify the pins of an op amp from the top or bottom view.
- Identify the power supply common on a circuit schematic, and state why you must do so.
- Breadboard an op amp circuit.

1-0 INTRODUCTION

One of the most versatile and widely used electronic devices in linear applications is the operational amplifier, most often referred to as the op amp. Op amps are popular because they are low in cost, easy to use, and fun to work with. They allow you to build useful circuits without needing to know about their complex internal circuitry. Op amps are usually very forgiving of wiring errors because of their self-protecting internal circuitry.

The word *operational* in operational amplifiers originally stood for mathematical operations. Early op amps were used in circuits that could add, subtract, multiply, and even solve differential equations. These operations have given way to digital computers because of their speed, accuracy, and versatility. However, digital computers were not the demise of the op amp.

1-1 IS THERE STILL A NEED FOR ANALOG CIRCUITRY?

1-1.1 Analog and Digital Systems

You often hear an expression similar to “It is a digital world.” This usually is followed by a statement such as “Is there a reason for studying analog circuitry, including op amps and other linear integrated circuits, when so many applications use a computer?” It is true that more and more functions are being done and problems are being solved by microcomputers, microcontrollers, or digital signal processing chips and systems today than ever before. This trend of going digital will continue at an even faster pace because software packages are better and easier to use, computers are faster and more accurate, and data can be stored and transferred over networks. However, as more digital systems are created for data acquisition and process control, more interface circuits using op amps and other linear integrated circuits are also required. These integrated systems now require designers to understand the principles of both the analog and the digital world in order to obtain the best performance of a system at a reasonable cost.

In the past, op amps were studied as separate entities and entire analog systems were developed using only analog circuitry. In some specialized real-time applications, this is still true but most systems that find their way to the marketplace are a combination of analog and digital. A typical data acquisition system block diagram is shown in

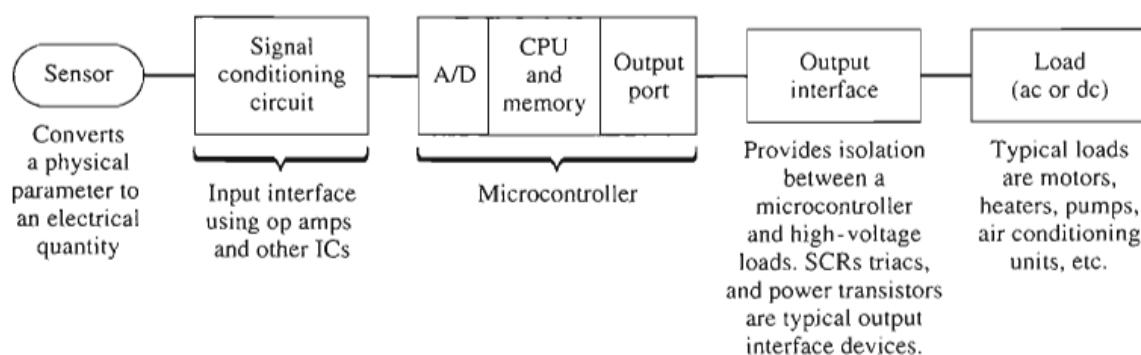


FIGURE 1-1 Typical data acquisition block diagram.

Fig. 1-1. It uses a sensor to convert a physical parameter (such as temperature, pressure, or flow) into an electrical parameter (such as voltage, current, or resistance). Unfortunately, sensors rarely produce an output whose electrical parameter or value is suitable for direct input into the computer through an analog-to-digital (A/D) converter. Thus an input interface circuit using op amps or other linear ICs is needed to condition the signal for the computer's A/D. Similarly, at the computer's output another analog circuit is needed to interface and isolate the computer's low voltage from a high-voltage ac or dc load. This text is designed to show applications of op amps and other linear integrated circuits in these combined analog and digital systems.

1-1.2 Op Amp Development

Op amps are designed using a wide variety of fabrication techniques. Originally they contained only bipolar transistors, but now there are a host of devices that use field-effect transistors within the op amp. Junction field-effect transistors at the input draw very small currents and allow the input voltages to be varied between the power supply limits. MOS transistors in the output circuitry allow the output terminal to go within millivolts of the power supply limits.

Op amps designed with bipolar inputs and complementary MOS outputs, appropriately named BiMOS, are faster and have a higher frequency response than the general-purpose op amps. Manufacturers have also designed dual (2) and quad (4) op amp packages. Hence, the package that once housed a single op amp can now contain two or four op amps. In the quad package, all four op amps share the same power supply and ground pins.

1-1.3 Op Amps Become Specialized

Inevitably, general-purpose op amps were redesigned to optimize or add certain features. Special function ICs that contain more than a single op amp were then developed to perform complex functions.

You need only to look at linear data books to appreciate their variety. Only a few examples are

1. High current and/or high voltage capability
2. Sonar send/receive modules
3. Multiplexed amplifiers
4. Programmable gain amplifiers
5. Automotive instrumentation and control
6. Communication ICs
7. Radio/audio/video ICs
8. Electrometer ICs for very high input impedance circuits
9. ICs that operate from a single supply
10. ICs that operate from rail to rail

General-purpose op amps will be around for a long time. However, more complex integrated circuits on a single chip are being developed. These devices combine analog with digital circuitry. In fact, with improved very large scale integrated (VLSI) technology, entire systems are being fabricated on a single large chip.

A single-chip computer is today's reality. A single-chip TV set will happen eventually. Before learning how to use op amps, it is wise to learn what they look like and how to buy them. As previously stated, the op amp's greatest use will be as a part in a system that interfaces the real world of analog voltage with the digital world of the computer, as will be shown throughout this text. If you want to understand the system, you must understand the workings of one of its most important components.

1-2 741 GENERAL-PURPOSE OP AMP

1-2.1 Circuit Symbol and Terminals

The 741 op amp has been "around" for a number of years. However, it still is a great device to begin with because it is inexpensive, rugged, and easy to obtain. The op-amp symbol in Fig. 1-2 is a triangle that points in the direction of signal flow. This component has

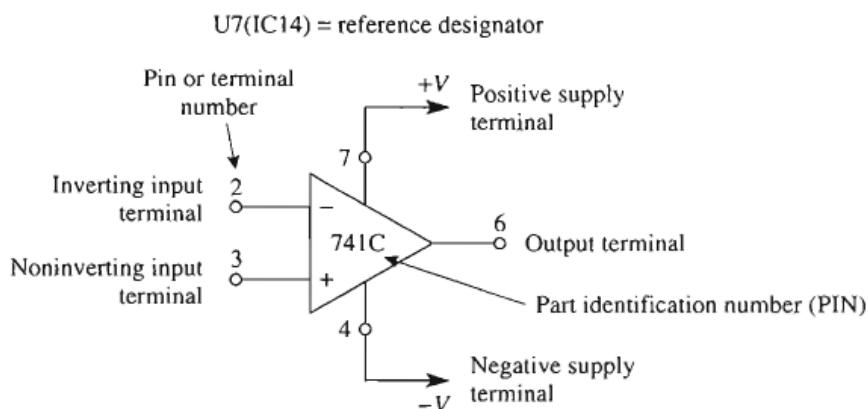


FIGURE 1-2 Circuit symbol for the general-purpose op amp. Pin numbering is for an 8-pin mini-DIP package.

a *part identification number* (PIN) placed within the triangular symbol. The PIN refers to a particular op amp with specific characteristics. The 741C op amp illustrated here is a general-purpose op amp that is used throughout the book for illustrative purposes.

The op amp may also be coded on a circuit schematic with a *reference designator* such as U7, IC14, and so on. Its PIN is then placed beside the reference designator in the parts list of the circuit schematic. All op amps have at least five terminals: (1) The positive power supply terminal V_{CC} or $+V$ at pin 7, (2) the negative power supply terminal V_{EE} or $-V$ at pin 4, (3) output pin 6, (4) the inverting (−) input terminal at pin 2, and (5) the noninverting (+) input terminal at pin 3. Some general-purpose op amps have additional specialized terminals. (The pins above refer to the 8-pin mini-DIP case discussed in the following section.)

1-2.2 Simplified Internal Circuitry of a General-Purpose Op Amp

General-purpose op amps are multistage systems. As shown in Fig. 1-3(a), the basic op amp consists of an input stage with two input terminals, an output stage with one output terminal, and an intermediate stage that connects the output signal of the input stage to the input terminal of the output stage.

Dc power is applied from a bipolar supply to the op amp's external power supply terminals and thus to each internal stage of the op amp. Depending on the application, input signals, $V_{(+)}$ and $V_{(-)}$, can be positive, negative, or zero. The resulting output voltage is measured across the load resistor R_L , which is connected between the op amp's output terminal and common. The output voltage, V_o , depends on the input signals and characteristics of the op amp.

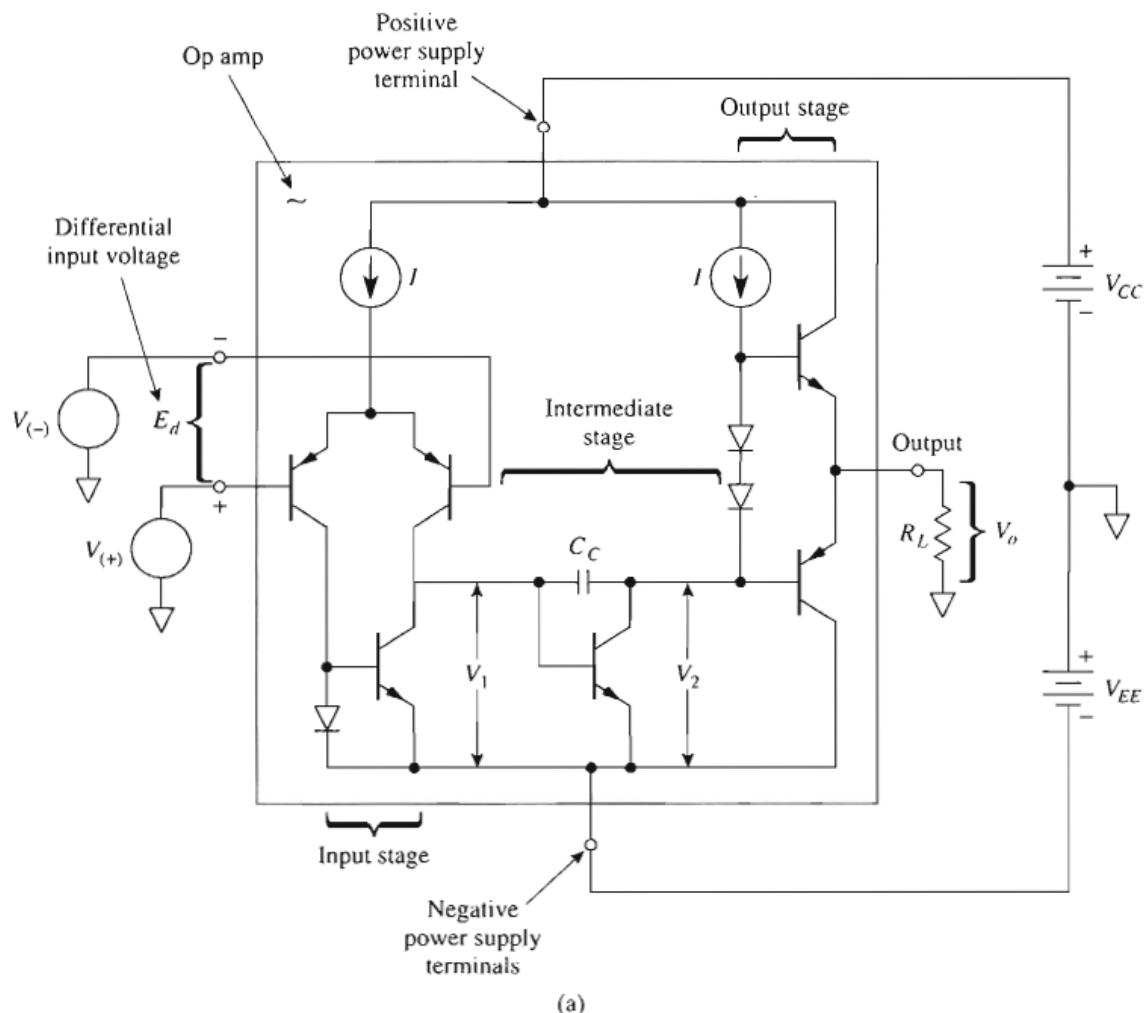


FIGURE 1-3 (a) Simplified block diagram of a general-purpose operational amplifier with external connections; (b) external connections using the op amps circuit symbol.

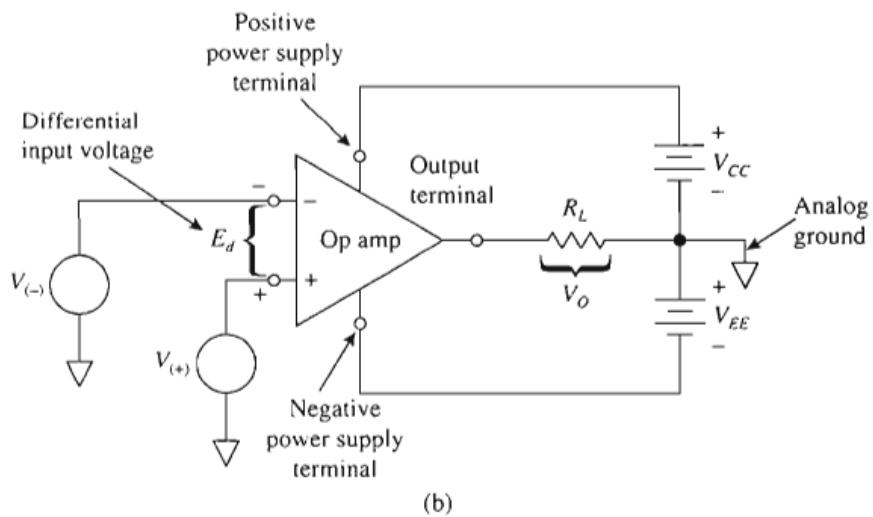


FIGURE 1-3(b)

1-2.3 Input Stage—Differential Amplifier

The input stage of the op amp in Fig. 1-3(a) is called a differential amplifier. It has very high input impedance as well as a large voltage gain. When input signals $V_{(+)}$ and $V_{(-)}$ are applied, the difference voltage, E_d , is amplified by this stage and appears as the output voltage V_1 . (Examples of how E_d is calculated are given in Chapter 2.)

1-2.4 Intermediate Stage—Level Shifter

Signal voltage V_1 at the output of the differential amplifier is directly coupled to the input of the intermediate level shifter stage. This stage performs two functions. First, it shifts the dc voltage level at the output of the differential amplifier to a value required to bias the output stage. Second, this stage allows input signal V_1 to pass nearly unaltered and become the input signal V_2 for the output stage.

1-2.5 Output Stage—Push-Pull

The signal voltage V_2 at the output of the intermediate stage is coupled directly into the output stage. The most common output stage is a *pnp-npn* push-pull transistor configuration. Using a push-pull circuit as the final stage allows the op amp to have a very low output resistance. As shown in Figs. 1-3(a) and (b), load resistor R_L is connected between the output terminal and common to develop output voltage V_o .

This simplified model of the op amp in Fig. 1-3(a) presents the basic information on its internal architecture. The actual circuitry is more complicated, but the functions are similar.

1-3 PACKAGING AND PINOUTS

1-3.1 Packaging

The op amp is fabricated on a tiny silicon chip and packaged in a suitable case. Fine-gage wires connect the chip to external leads extending from a metal, plastic, or ceramic package. Common op amp packages are shown in Figs. 1-4(a) to (d).

The metal can package shown in Fig. 1-4(a) is available with 3, 5, 8, 10, and 12 leads. The silicon chip is bonded to the bottom metal sealing plane to expedite the dissipation of heat. In Fig. 1-4(a) the tab identifies pin 8, and the pins are numbered counterclockwise when you view the metal can from the top.

The popular 14-pin and 8-pin dual-in-line packages (DIPs) are shown in Figs. 1-4(b) and (c). Either plastic or ceramic cases are available. As viewed from the top, a notch or dot identifies pin 1 and terminals are numbered counterclockwise.

Complex integrated circuits involving many op amps and other ICs can now be fabricated on a single large chip or by interconnecting many chips and placing them in a single package. For ease of manufacture and assembly, pads replace the leads. The resulting

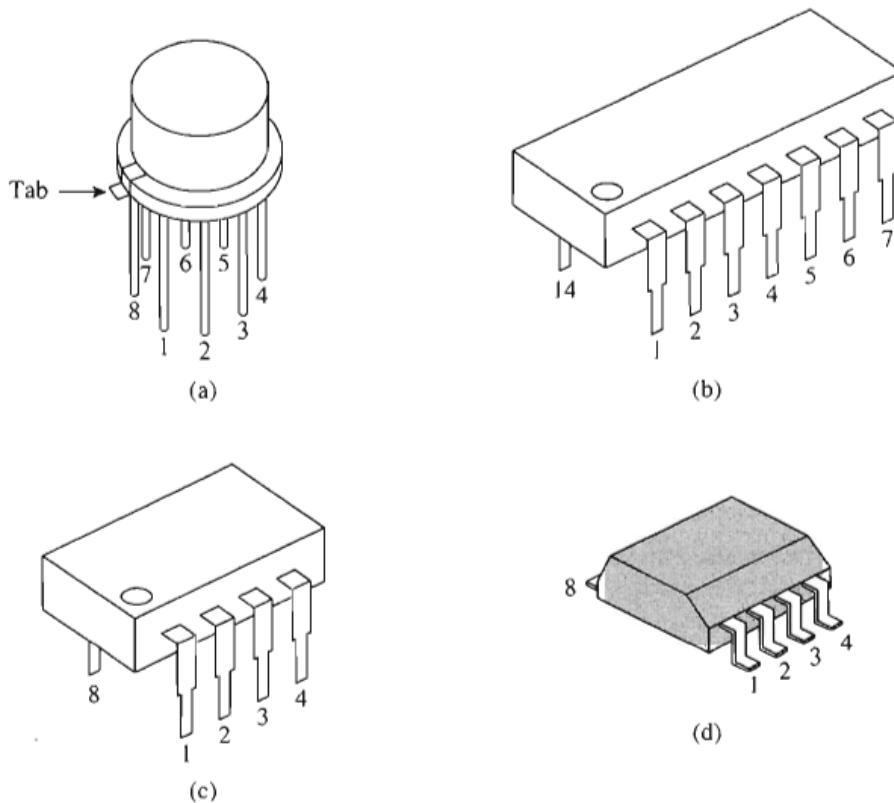


FIGURE 1-4 The three most popular op amp packages are the metal can in (a) and the 14- and 8-pin dual-in-line packages in (b) and (c), respectively. For systems requiring high density, surface-mounted technology (SMT) packages are used as shown in (d).

structure is called surface-mounted technology (SMT), shown in Fig. 1-4(d). These packages provide a higher circuit density for a package of a given size. Additionally, SMTs have lower noise and improved frequency-response characteristics. SMT components are available in (1) *plastic lead chip carriers* (PLCCs), (2) *small outline integrated circuits* (SOICs), and (3) *leadless ceramic chip carriers* (LCCCs).

1-3.2 Combining Symbol and Pinout

Manufacturers are now combining the circuit symbol for an op amp together with the package view into a single drawing. For example, the four most common types of packages that house a 741 chip are shown in Fig. 1-4. Compare Figs. 1-5(a) and (d) to see that

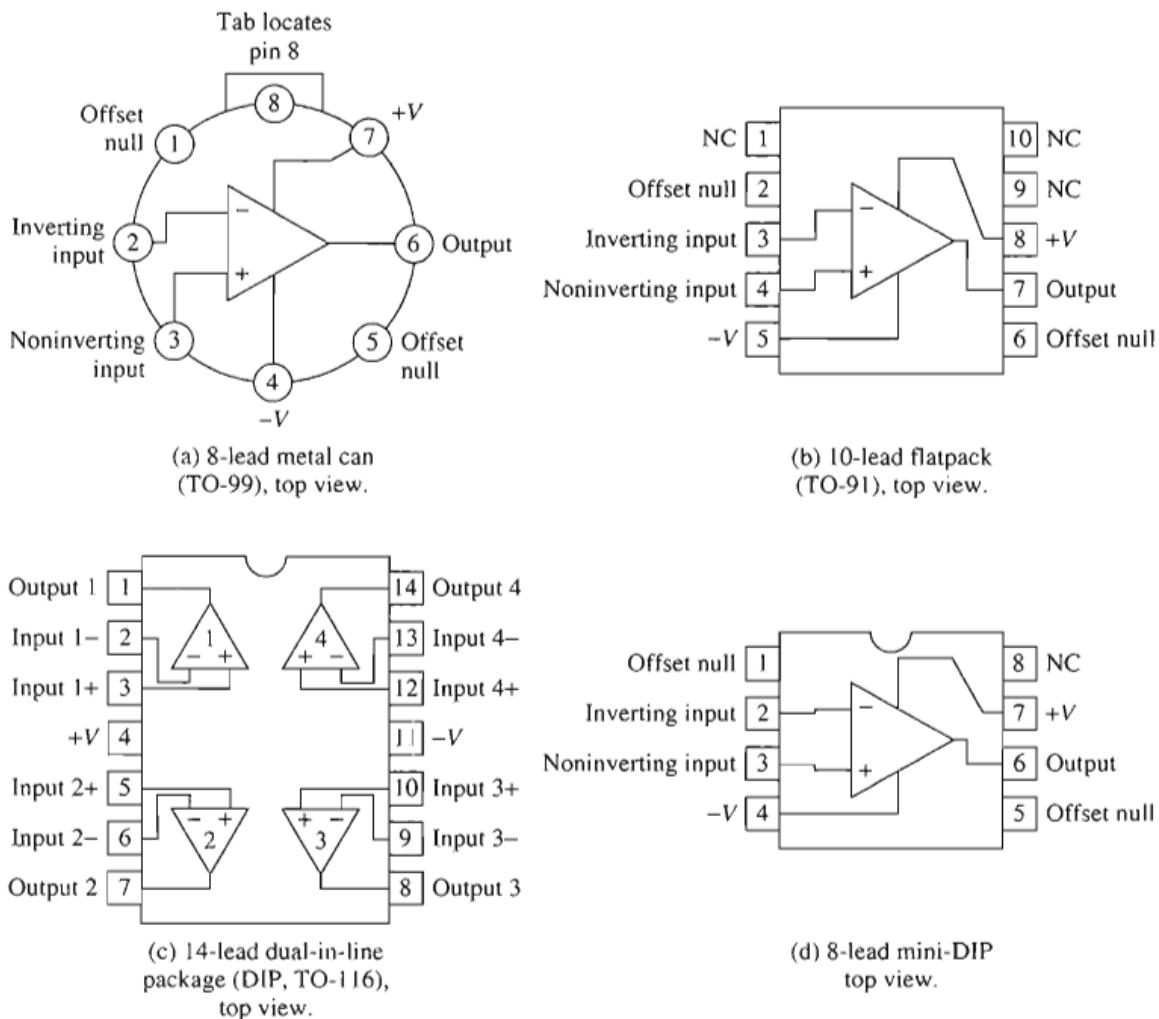


FIGURE 1-5 Connection diagrams for typical op amp packages. The abbreviation NC stands for “no connection.” That is, these pins have no internal connection, and the op amp’s terminals can be used for spare junction terminals. Diagram (c) shows how four op amps can be configured in a single package. Not shown in (c) are the internal connections for $+V$ and $-V$.

the numbering schemes are identical for an 8-pin can and an 8-pin DIP. A notch or dot identifies pin 1 on the DIPs, and a tab identifies pin 8 on the TO-5 (or the similar TO-99) package. From a top view, the pin count proceeds counterclockwise.

The final tasks in this chapter are to learn how to buy a specific type of op amp and to present advice on basic breadboarding techniques.

1-4 HOW TO IDENTIFY OR ORDER AN OP AMP

1-4.1 The Identification Code

Each type of op amp has a letter–number identification code. This code answers four questions:

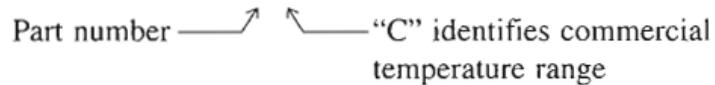
1. What type of op amp is it? (Example: 741.)
2. Who made it? (Example: Analog Devices.)
3. How good is it? (Example: the guaranteed temperature range for operation.)
4. What kind of package houses the op amp chip? (Example: plastic DIP.)

Not all manufacturers use precisely the same code, but most use an identification code that consists of four parts written in the following order: (1) letter prefix, (2) circuit designator, (3) letter suffix, and (4) military specification code.

Letter prefix. The letter prefix code usually consists of two or three letters that identify the manufacturer. The following examples list some of the codes used by a manufacturer. You may wish to visit their Web site to obtain data sheets and application notes about a particular product. Their main Web site address is given.

Letter prefix	Manufacturer	Manufacturer's Web Site
AD/OP	Analog Devices	www.analog.com
INA/OPA	Burr-Brown	www.burr-brown.com
CD	Cirrus Logic	www.cirrus.com
LF/LT/LTC	Linear Technology	www.linear-tech.com
MAX	Maxim	www.maxim-ic.com
MC	Motorola	www.motorola.com
LF/LM/LMC/LMV	National Semiconductor	www.national.com
TL/TLC/TH/TM	Texas Instruments	www.ti.com

Circuit designation. The circuit designator consists of three to seven numbers and letters. They identify the type of op amp and its temperature range. For example:

324C
 Part number  "C" identifies commercial temperature range

The three *temperature-range codes* are as follows:

1. C: commercial, 0 to 70°C
2. I: industrial, -25 to 85°C
3. M: military, -55 to 125°C

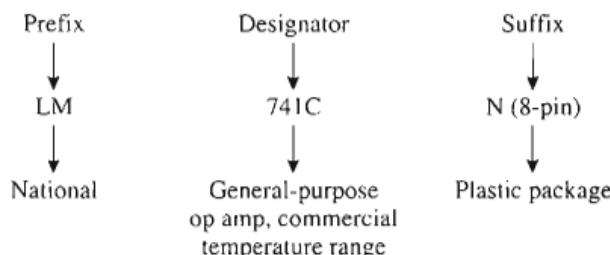
Letter suffix. A one- or two-letter suffix identifies the package style that houses the op amp chip. You need the package style to get the correct pin connections from the data sheet (see Appendix 1). Three of the most common package suffix codes are

Package code	Description
D	Plastic dual-in-line for surface mounting on a pc board
J	Ceramic dual-in-line
N, P	Plastic dual-in-line for insertion into sockets. (Leads extend through the top surface of a pc board and are soldered to the bottom surface.)

Military specification code. The military specification code is used only when the part is for high-reliability applications.

1-4.2 Order Number Example

A 741 general-purpose op amp would be completely identified in the following way:



1-5 SECOND SOURCES

Some op amps are so widely used that they are made by more than one manufacturer. This is called *second sourcing*. The company (Fairchild) who designed and made the original 741 contracted for licenses with other manufacturers to make 741s in exchange for a license to make op amps or other devices.

As time went on, the original 741 design was modified and improved by all manufacturers. The present 741 has evolved over several generations. Thus, if you order a 741 8-pin DIP from a supplier, it may have been built by Texas Instruments (TL741), Analog Devices (AD741), National Semiconductor (LM741), or others. Therefore, always check the manufacturer's data sheets that correspond to the device you have. You will then have information on its exact performance and a key to the identification codes on the device.

1-6 BREADBOARDING OP AMP CIRCUITS

1-6.1 The Power Supply

Power supplies for general-purpose op amps are bipolar. As shown in Fig. 1-6(a), the typical commercially available power supply outputs ± 15 V. The common point between the $+15$ V supply and -15 V is called the *power supply common*. It is shown with a common symbol for two reasons. First, *all* voltage measurements are made with respect to this point. Second, the power supply common is usually wired to the third wire of the line cord that extends ground (usually from a water pipe in the basement) to the chassis containing the supply.

The schematic drawing of a portable supply is shown in Fig. 1-6(b). This is offered to reinforce the idea that a bipolar supply contains two separate power supplies connected in series aiding.

1-6.2 Breadboarding Suggestions

It should be possible to breadboard and test the performance of all circuits presented in this text. A few circuits require printed circuit board construction. Before we proceed to learn how to use an op amp, it is prudent to give some time-tested advice on breadboarding a circuit:

1. Do all wiring with power off.
2. Keep wiring and component leads as short as possible.
3. Wire the $+V$ and $-V$ supply leads *first* to the op amp. It is surprising how often this vital step is omitted.
4. Try to wire all ground leads to one tie point, the power supply common. This type of connection is called *star grounding*. Do not use a ground bus, because you may create a ground loop, thereby generating unwanted noise voltages.
5. Recheck the wiring before applying power to the op amp.

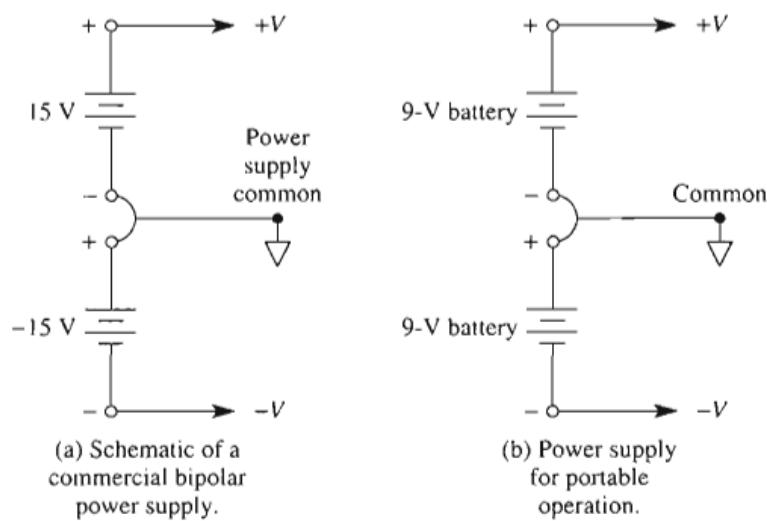


FIGURE 1-6 Power supplies for general-purpose op amps must be bipolar.

6. Connect signal voltages to the circuit only after the op amp is powered.
7. Take all measurements with respect to common. For example, if a resistor is connected between two terminals of an IC, do not connect either a meter or an oscilloscope across the resistor; instead, measure the voltage on one side of the resistor with respect to common, then the voltage on the other side, and calculate the voltage across the resistor.
8. Avoid using ammeters, if possible. Measure the voltage as in step 7 and calculate current.
9. Disconnect the input signal before the dc power is removed. Otherwise, the IC may be destroyed.
10. These ICs will stand much abuse. But *never*:
 - a. Reverse the polarity of the power supplies,
 - b. Drive the op amp's input pins above or below the potentials at the $+V$ and $-V$ terminal, or
 - c. Leave an input signal connected with no power on the IC.
11. If unwanted oscillations appear at the output and the circuit connections seem correct:
 - a. Connect a $0.1\text{-}\mu\text{F}$ capacitor between the op amp's $+V$ pin and ground and another $0.1\text{-}\mu\text{F}$ capacitor between the op amp's $-V$ pin and ground.
 - b. Shorten your leads, and
 - c. Check the test instrument, signal generator, load, and power supply ground leads. They should come together at one point.
12. The same principles apply to all other linear ICs.

We now proceed to our first experience with an op amp.

PROBLEMS

- 1-1. In the term *operational amplifier*, what does the word *operational* stand for?
- 1-2. Is the LM324 op amp a single op amp housed in one package, a dual op amp in one package, or a quad op amp in one package?
- 1-3. With respect to an op amp, what does the abbreviation PIN stand for?
- 1-4. Does the letter prefix of a PIN identify the manufacturer or the package style?
- 1-5. Does the letter suffix of a PIN identify the manufacturer or the package style?
- 1-6. Which manufacturer makes the AD741CN?
- 1-7. Does the tab on a metal can package identify pin 1 or pin 8?
- 1-8. Which pin is identified by the dot on an 8-pin mini-DIP?
- 1-9. (a) How do you identify power supply common on a circuit schematic?
(b) Why do you need to do so?
- 1-10. When breadboarding an op amp circuit, should you use a ground bus or star grounding?
- 1-11. Search a manufacturer's Web site and download a 741 data sheet.
 - (a) What is the manufacturer's identification code?
 - (b) What package styles are available?
 - (c) List three applications that the 741 op amp can be used in.

CHAPTER 2

First Experiences with an Op Amp

LEARNING OBJECTIVES

Upon completing this chapter on first experiences with an op amp, you will be able to:

- Briefly describe the task performed by the power supply and input and output terminals of an op amp.
- Show how the single-ended output voltage of an op amp depends on its open-loop gain and differential input voltage.
- Calculate the differential input voltage E_d , and the resulting output voltage V_o .
- Draw the circuit schematic for an inverting or noninverting zero-crossing detector.
- Draw the output voltage waveshape of a zero-crossing detector if you are given the input voltage waveshape.
- Draw the output–input voltage characteristics of a zero-crossing detector.
- Sketch the schematic of a noninverting or inverting voltage-level detector.

- Describe at least two practical applications of voltage-level detectors.
- Analyze the action of a pulse-width modulator and tell how it can interface an analog signal with a microcomputer.
- Use voltage reference ICs to design precise voltage-level detectors.
- Use SPICE to analyze a basic comparator circuit.

2-0 INTRODUCTION

The name *operational amplifier* was originally given to early high-gain vacuum-tube amplifiers designed to perform mathematical operations of addition, subtraction, multiplication, division, differentiation, and integration. They could also be interconnected to solve differential equations.

The modern successor of those amplifiers is the *linear integrated-circuit op amp*. It inherits the name, works at lower voltages, and is available in a variety of specialized forms. Today's op amp is so low in cost that millions are now used annually. Their low cost, versatility, and dependability have expanded their use far beyond applications envisioned by early designers. Some present-day uses for op amps are in the fields of signal conditioning, process control, communications, computers, power and signal sources, displays, and testing or measuring systems. The op amp is still basically a very good high-gain dc amplifier.

One's first experience with a linear IC op amp should concentrate on its most important and fundamental properties. Accordingly, our objectives in this chapter will be to identify each terminal of the op amp and to learn its purpose, some of its electrical limitations, and how to apply it usefully.

2-1 OP AMP TERMINALS

Remember from Fig. 1-2 that the circuit symbol for an op amp is an arrowhead that symbolizes high gain and points from input to output in the direction of signal flow. Op amps have five basic terminals: two for supply power, two for input signals, and one for output. Internally they are complex, as was shown by the schematic diagram in Fig. 1-3(a). It is not necessary to know much about the internal operation of the op amp in order to use it. We will refer to certain internal circuitry, when appropriate. The people who

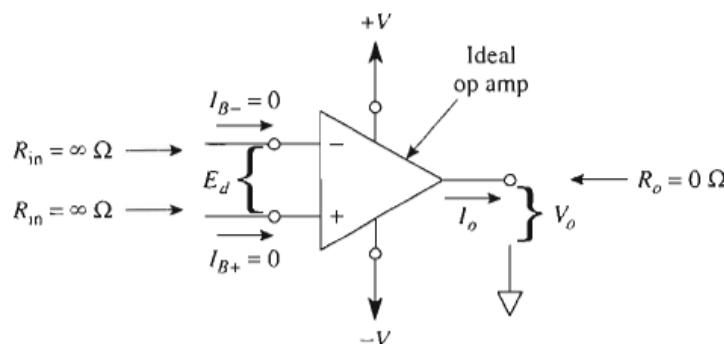


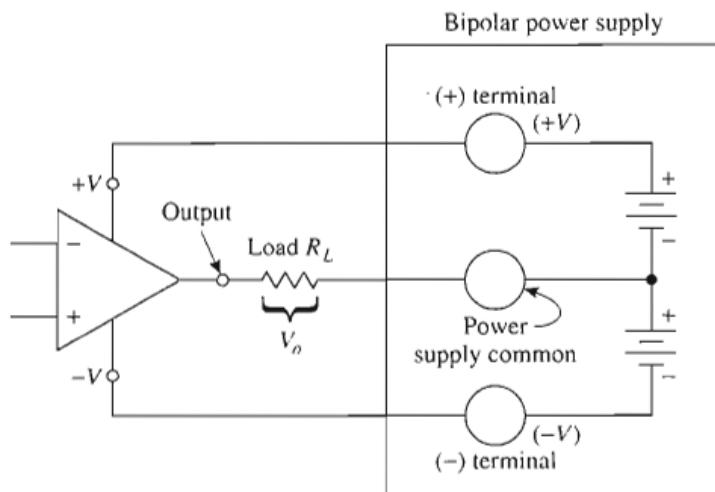
FIGURE 2-1 The ideal op amp has infinite gain and input resistances plus zero output resistance.

design and build op amps have done such an outstanding job that external components connected to the op amp determine what the overall system will do.

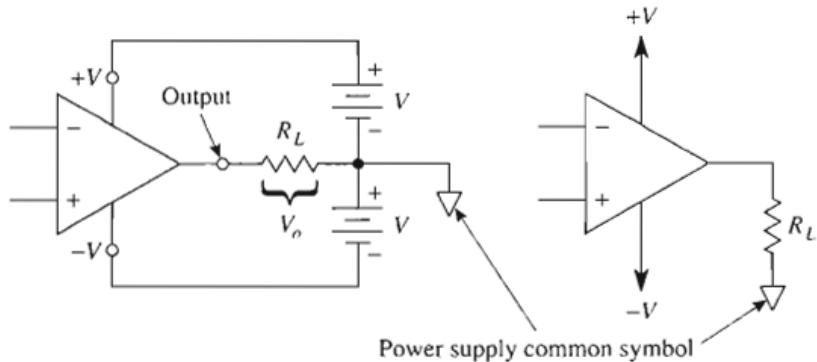
The ideal op amp of Fig. 2-1 has infinite gain and infinite frequency response. The input terminals draw no signal or bias currents and exhibit infinite input resistance. Output impedance is zero ohms, and the power supply voltages are without limit. We now examine the function of each op amp terminal to learn something about the limitations of a real op amp.

2-1.1 Power Supply Terminals

Op amp terminals labeled $+V$ and $-V$ identify those op amp terminals that must be connected to the power supply (see Fig. 2-2 and Appendices 1 and 2). Note that the power supply has *three* terminals: positive, negative, and power supply common. The power supply common terminal may or may not be wired to earth ground via the third wire of line cord. *All voltage measurements are made with respect to power supply common.*



(a) Actual wiring from power supply to op amp.



(b) Typical schematic representations of supplying power to an op amp.

FIGURE 2-2 Wiring power and load to an op amp.

The power supply in Fig. 2-2 is called a bipolar or split supply and has typical values of ± 15 V. Some op amps are now designed to operate from a single-polarity supply such as +5 or +15 V and ground. Note that the common is *not* wired to the op amp in Fig. 2-2. Currents returning to the supply from the op amp must return through external circuit elements such as the load resistor R_L . The maximum supply voltage that can be applied between +V and -V is typically 36 V or ± 18 V.

2-1.2 Output Terminal

In Fig. 2-2 the op amp's output terminal is connected to one side of the load resistor R_L . The other side of R_L is wired to ground. Output voltage V_o is measured with respect to ground. Since there is only one output terminal in an op amp, it is called a *single-ended output*. There is a limit to the current that can be drawn from the output terminal of an op amp, usually on the order of 5 to 10 mA. There are also limits on the output terminal's voltage levels; these limits are set by the supply voltages and by the op amp's output transistors (see also Appendix 1, "Output Voltage Swing as a Function of Supply Voltage"). These output transistors need about 1 to 2 V from collector to emitter to ensure that they are acting as amplifiers and not as switches. Thus the output terminal can rise approximately to within 1 V of +V and drop to within 2 V of -V. The upper limit of V_o is called the *positive saturation voltage*, $+V_{sat}$, and the lower limit is called the *negative saturation voltage*, $-V_{sat}$. For example, with a supply voltage of ± 15 V, $+V_{sat} = +14$ V and $-V_{sat} = -13$ V. Therefore, V_o is restricted to a symmetrical peak-to-peak swing of ± 13 V. Both current and voltage limits place a *minimum* value on the load resistance R_L of 2 k Ω . However, op amps are now available especially for applications that operate from low supply voltages (+3.3 V) and have MOS rather than bipolar output transistors. The output of these op amps can be brought to within millivolts of either +V or -V.

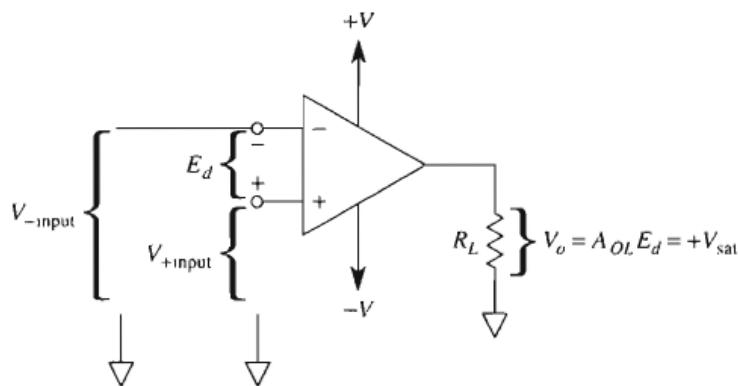
Most op amps, like the 741, have internal circuitry that automatically limits current drawn from the output terminal. Even with a short circuit for R_L , output current is limited to about 25 mA, as noted in Appendix 1. This feature prevents destruction of the op amp in the event of a short circuit.

2-1.3 Input Terminals

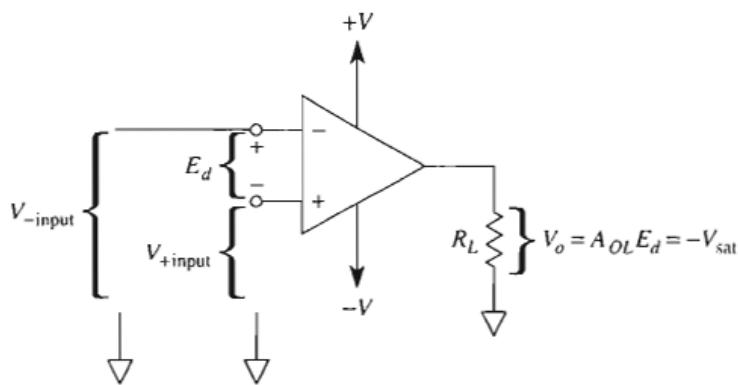
In Fig. 2-3 there are two input terminals, labeled - and +. They are called *differential input terminals* because output voltage V_o depends on the *difference* in voltage between them, E_d , and the gain of the amplifier, A_{OL} . As shown in Fig. 2-3(a), the output terminal is positive with respect to ground when the (+) input is positive with respect to, or above, the (-) input. When E_d is reversed in Fig. 2-3(b) to make the (+) input negative with respect to, or below, the (-) input, V_o becomes negative with respect to ground.

We conclude from Fig. 2-3 that the polarity of the output terminal is the same as the polarity of (+) input terminal with respect to the (-) input terminal. Moreover, the polarity of the output terminal is opposite or inverted from the polarity of the (-) input terminal. For these reasons, the (-) input is designated the *inverting input* and the (+) input the *noninverting input* (see Appendix 1).

It is important to emphasize that the polarity of V_o depends only on the *difference* in voltage between inverting and noninverting inputs. This difference voltage can be found by



(a) V_o goes positive when the (+) input is more positive than (above) the (−) input, $E_d = (+)$.



(b) V_o goes negative when the (+) input is less positive than (below) the (−) input, $E_d = (-)$.

FIGURE 2-3 Polarity of *single-ended* output voltage V_o depends on the polarity of *differential* input voltage E_d . If the (+) input is *above* the (−) input, E_d is positive and V_o is *above* ground at $+V_{sat}$. If the (+) input is *below* the (−) input, E_d is negative and V_o is *below* ground at $-V_{sat}$.

$$E_d = \text{voltage at the (+) input} - \text{voltage at the (−) input} \quad (2-1)$$

Both input voltages are *measured with respect to ground*. The sign of E_d tells us (1) the polarity of the (+) input with respect to the (−) input and (2) the polarity of the output terminal with respect to ground. This equation holds if the inverting input is grounded, if the noninverting input is grounded, and even if both inputs are above or below ground potential. Thus, if the polarity of E_d matches the op amp's symbol, the output voltage goes to $+V_{sat}$. When the polarity of E_d is opposite the op amp's symbol, the output voltage goes to $-V_{sat}$.

Review. We have chosen the words in Fig. 2-3 very carefully. They simplify analysis of open-loop operation (no connection from output to either input). Another memory aid is this: If the (+) input is *above* the (−) input, the output is *above* ground and at $+V_{sat}$. If the (+) input is *below* the (−) input, the output is *below* ground at $-V_{sat}$.

2-1.4 Input Bias Currents and Offset Voltage

The input terminals of real op amps draw tiny bias currents and signal currents to activate the internal transistors. The input terminals also have a small imbalance called *input*

offset voltage, V_{io} . It is modeled as a voltage source V_{io} in series with the (+) input. In Chapter 9, the effects of V_{io} are explained in detail.

We must learn much more about op amp circuit operation, particularly involving negative feedback, before we can measure bias currents and offset voltage. For this reason, in these introductory chapters we will assume that both are negligible.

2-2 OPEN-LOOP VOLTAGE GAIN

2-2.1 Definition

Refer to Fig. 2-3. Output voltage V_o is determined by E_d and the *open-loop voltage gain*, A_{OL} . A_{OL} is called open-loop voltage gain because possible feedback connections from output terminal to input terminals are left open. Accordingly, V_o is expressed by the relationship

$$\begin{aligned} \text{output voltage} &= \text{differential input voltage} \times \text{open-loop gain} \\ V_o &= E_d \times A_{OL} \end{aligned} \quad (2-2)$$

2-2.2 Differential Input Voltage, E_d

The value of A_{OL} is extremely large, often 200,000 or more. Recall from Section 2-1.2 that V_o can never exceed the positive or negative saturation voltages $+V_{sat}$ and $-V_{sat}$. For a ± 15 -V supply, the saturation voltages are approximately ± 13 V. Thus, for the op amp to act as an amplifier, E_d must be limited to a maximum voltage of ± 65 μ V. This conclusion is reached by rearranging Eq. (2-2).

$$\begin{aligned} E_{d\ max} &= \frac{+V_{sat}}{A_{OL}} = \frac{13\text{ V}}{200,000} = 65\text{ }\mu\text{V} \\ -E_{d\ max} &= \frac{-V_{sat}}{A_{OL}} = \frac{-13\text{ V}}{200,000} = -65\text{ }\mu\text{V} \end{aligned}$$

In the laboratory or shop it is difficult to measure 65 μ V, because induced noise, 60-Hz hum, and leakage currents on the typical test setup can easily generate a millivolt (1000 μ V). Furthermore, it is difficult and inconvenient to measure very high gains. The op amp also has tiny internal unbalances that act as a small voltage that may exceed E_d . As mentioned in Section 2-1.4, this small voltage is called an *offset voltage* and is discussed in Chapter 9.

2-2.3 Conclusions

There are three conclusions to be drawn from these brief comments. First, V_o in the circuit of Fig. 2-3 either will be at one of the limits $+V_{sat}$ or $-V_{sat}$ or will be oscillating between these limits. Don't be disturbed, because this behavior is what a high-gain amplifier usually does. Second, to maintain V_o between these limits we must go to a feedback

type of circuit that forces V_o to depend on stable, precision elements such as resistors and capacitors. Feedback circuits are introduced in Chapter 3.

Without learning any more about the op amp, it is possible to understand basic comparator applications. In a comparator application, the op amp performs not as an amplifier but as a device that tells when an unknown voltage is below, above, or just equal to a known reference voltage. Before introducing the op amp as a comparator in the next section, Example 2-1 is given to illustrate ideas presented thus far.

Example 2-1

In Fig. 2-3, $+V = 15$ V, $-V = -15$ V, $+V_{sat} = +13$ V, $-V_{sat} = -13$ V, and gain $A_{OL} = 200,000$. Assuming ideal conditions, find the magnitude and polarity of V_o for each of the following input voltages. These input voltages are given with respect to ground.

	Voltage at (-) input	Voltage at (+) input
(a)	$-10 \mu\text{V}$	$-15 \mu\text{V}$
(b)	$-10 \mu\text{V}$	$+15 \mu\text{V}$
(c)	$-10 \mu\text{V}$	$-5 \mu\text{V}$
(d)	$+1.000001$ V	$+1.000000$ V
(e)	$+5 \text{ mV}$	0 V
(f)	0 V	$+5 \text{ mV}$

Solution The polarity of V_o is the same as the polarity of the (+) input with respect to the (-) input. The (+) input is more negative than the (-) input in (a), (d), and (e). This is shown by Eq. (2-1), and therefore V_o will go negative. From Eq. (2-2), the magnitude of V_o is A_{OL} times the difference, E_d , between voltages at the (+) and (-) inputs, but if $A_{OL} \times E_d$ exceeds $+V$ or $-V$, then V_o must stop at $+V_{sat}$ or $-V_{sat}$. Calculations are summarized as follows:

E_d [using Eq. (2-1)]	Polarity of (+) input with respect to (-) input	Theoretical V_o [from Eq. (2-2)]	Actual V_o
(a) $-5 \mu\text{V}$	-	$-5 \mu\text{V} \times 200,000 = -1.0$ V	-13 V
(b) $25 \mu\text{V}$	+	$25 \mu\text{V} \times 200,000 = 5.0$ V	$+13$ V
(c) $5 \mu\text{V}$	+	$5 \mu\text{V} \times 200,000 = 1.0$ V	$+13$ V
(d) $-1 \mu\text{V}$	-	$-1 \mu\text{V} \times 200,000 = -0.2$ V	-13 V
(e) -5 mV	-	$-5 \text{ mV} \times 200,000 = -1000$ V	-13 V
(f) 5 mV	+	$5 \text{ mV} \times 200,000 = 1000$ V	$+13$ V

2-3 ZERO-CROSSING DETECTORS

2-3.1 Noninverting Zero-Crossing Detector

The op amp in Fig. 2-4(a) operates as a comparator. Its (+) input compares voltage E_i with a reference voltage of 0 V ($V_{ref} = 0$ V). When E_i is above V_{ref} , V_o equals $+V_{sat}$. This is because the voltage at the (+) input is more positive than the voltage at the (−) input. Therefore, the sign of E_d in Eq. (2-1) is positive. Consequently, V_o is positive, from Eq. (2-2).

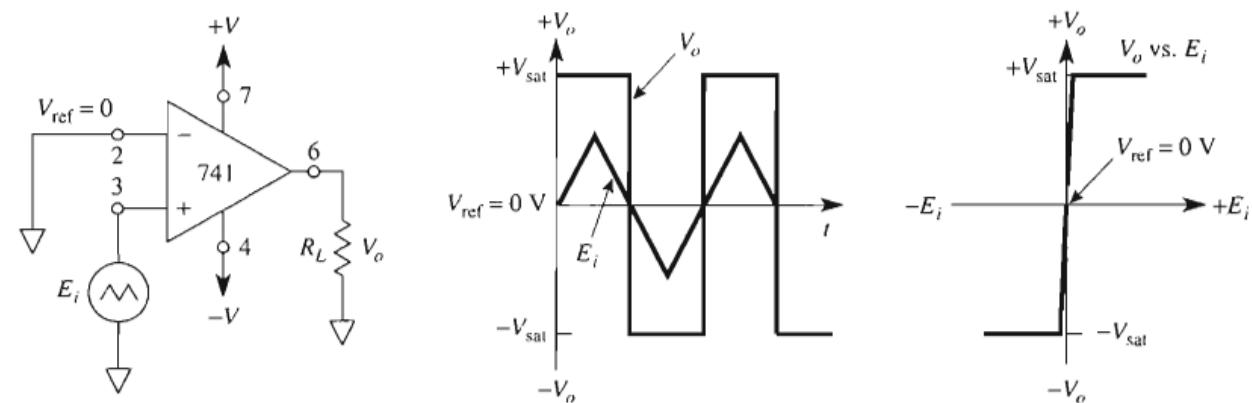
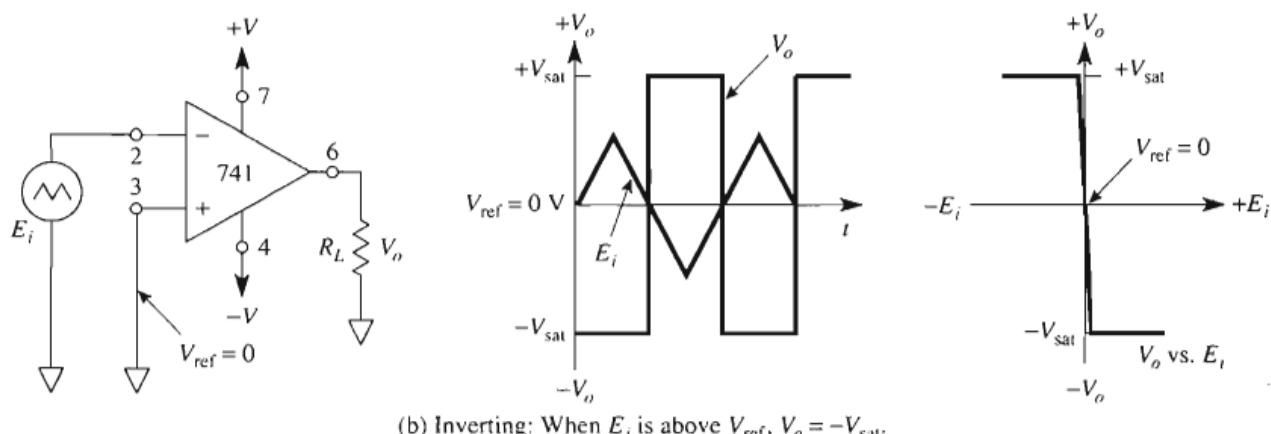
(a) Noninverting: When E_i is above V_{ref} , $V_o = +V_{sat}$.(b) Inverting: When E_i is above V_{ref} , $V_o = -V_{sat}$.

FIGURE 2-4 Zero-crossing detectors, noninverting in (a) and inverting in (b). If the signal E_i is applied to the (+) input, the circuit action is noninverting. If the signal E_i is applied to the (−) input, the circuit action is inverting.

The polarity of V_o “tells” if E_i is above or below V_{ref} . The *transition* of V_o tells *when* E_i crossed the reference and in what direction. For example, when V_o makes a positive-going transition from $-V_{sat}$ to $+V_{sat}$, it indicates that E_i just crossed 0 in the positive direction. The circuit of Fig. 2-4(a) is a noninverting zero-crossing detector.

2-3.2 Inverting Zero-Crossing Detector

The op amp's (–) input in Fig. 2-4(b) compares E_i with a reference voltage of 0 V ($V_{ref} = 0$ V). This circuit is an *inverting zero-crossing detector*. The waveshapes of V_o versus time and V_o versus E_i in Fig. 2-4(b) can be explained by the following summary:

1. If E_i is more positive than V_{ref} , then V_o equals $-V_{sat}$.
2. Where E_i crosses the reference going positive, V_o makes a negative-going transition from $+V_{sat}$ to $-V_{sat}$.

Summary. If the signal or voltage to be monitored is connected to the (+) input, a noninverting comparator results. If the signal or voltage to be monitored is connected to the (–) input, an inverting comparator results.

When $V_o = +V_{sat}$, the signal is *above* (more positive than) V_{ref} in a noninverting comparator and *below* (more negative than) V_{ref} in an inverting comparator.

2-4 POSITIVE- AND NEGATIVE-VOLTAGE-LEVEL DETECTORS

2-4.1 Positive-Level Detectors

In Fig. 2-5 a positive reference voltage V_{ref} is applied to one of the op amp's inputs. This means that the op amp is set up as a comparator to detect a positive voltage. If the voltage to be sensed, E_i , is applied to the op amp's (+) input, the result is a *noninverting positive-level detector*. Its operation is shown by the waveshapes in Fig. 2-5(a). When E_i is above V_{ref} , V_o equals $+V_{sat}$. When E_i is below V_{ref} , V_o equals $-V_{sat}$.

If E_i is applied to the inverting input as in Fig. 2-5(b), the circuit is an inverting positive-level detector. Its operation can be summarized by the statement: When E_i is above V_{ref} , V_o equals $-V_{sat}$. This circuit action can be seen more clearly by observing the plot of E_i and V_{ref} versus time in Fig. 2-5(b).

2-4.2 Negative-Level Detectors

Figure 2-6(a) is a *noninverting negative-level detector*. This circuit detects when input signal E_i crosses the negative voltage $-V_{ref}$. When E_i is above $-V_{ref}$, V_o equals $+V_{sat}$. When E_i is below $-V_{ref}$, $V_o = -V_{sat}$. The circuit of Fig. 2-6(b) is an *inverting negative-level detector*. When E_i is above $-V_{ref}$, V_o equals $-V_{sat}$, and when E_i is below $-V_{ref}$, V_o equals $+V_{sat}$.

2-5 TYPICAL APPLICATIONS OF VOLTAGE-LEVEL DETECTORS

2-5.1 Adjustable Reference Voltage

ICs are available to set precise voltage references. These reference chips will be introduced in the next section. In this section a resistive divider network is used to set V_{ref} . Figure 2-7 shows how to make an adjustable reference voltage. Two 10-k Ω resistors and

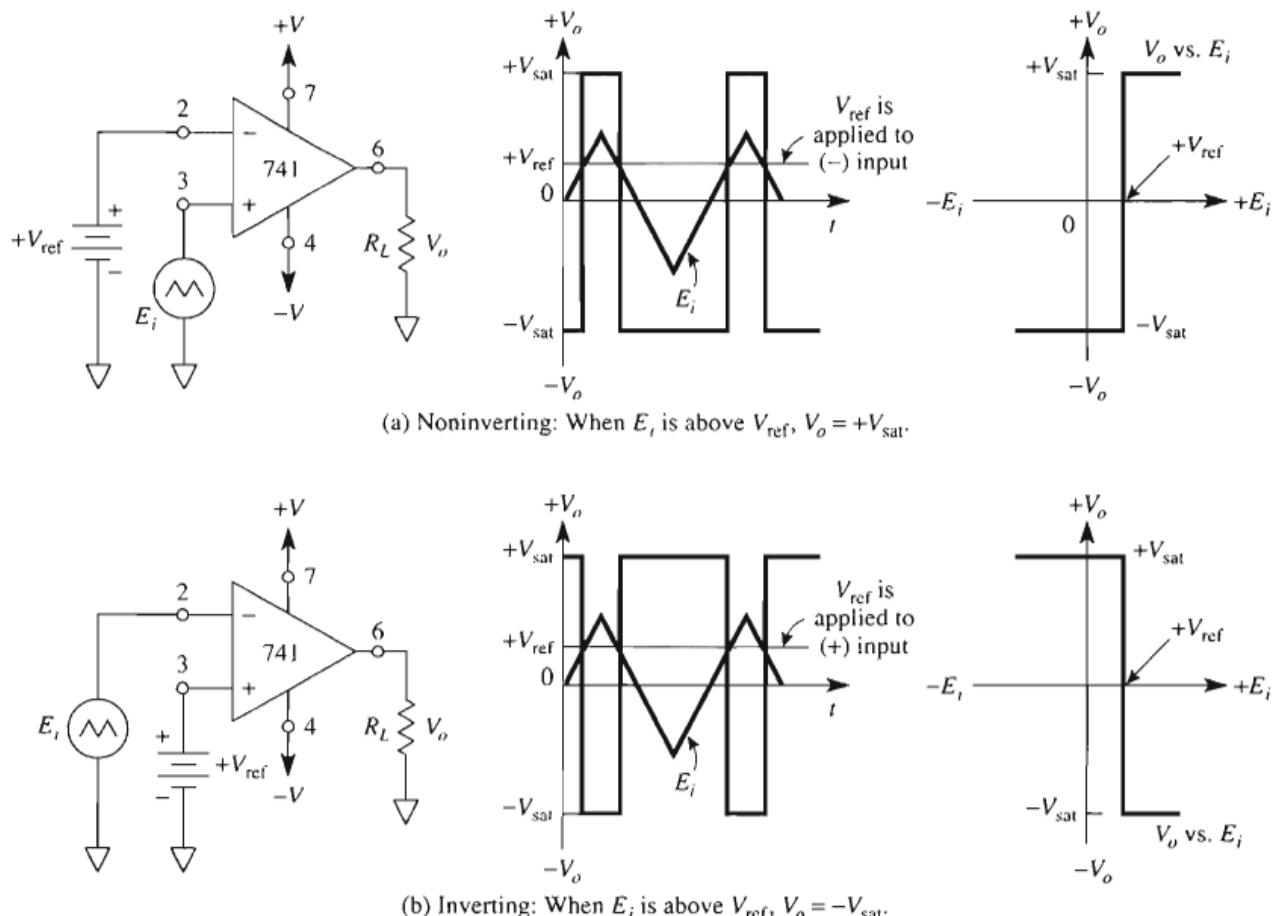


FIGURE 2-5 Positive-voltage-level detector, noninverting in (a) and inverting in (b). If the signal E_i is applied to the (+) input, the circuit action is noninverting. If the signal E_i is applied to the (-) input, the circuit action is inverting.

a $10\text{-k}\Omega$ potentiometer are connected in series to make a 1-mA voltage divider. Each kilohm of resistance corresponds to a voltage drop of 1 V. V_{ref} can be set to any value between -5 and $+5$ V. Remove the $-V$ connection to the bottom $10\text{-k}\Omega$ resistor and substitute a ground. You now have a 0.5-mA divider, and V_{ref} can be adjusted from 5 to 10 V.

2-5.2 Sound-Activated Switch

Figure 2-8 first shows how to make an adjustable reference voltage of 0 to 100 mV. Pick a $10\text{-k}\Omega$ pot, $5\text{-k}\Omega$ resistor, and $+15\text{-V}$ supply to generate a convenient large adjustable voltage of 0 to 10 V. Next connect a 100:1 (approximately) voltage divider that divides the 0-to-10-V adjustment down to the desired 0-to-100-mV adjustable reference voltage. (Note: Pick the large $100\text{-k}\Omega$ divider resistor to be 10 times the potentiometer resistance; this avoids loading down the 0-to-10-V adjustment.)

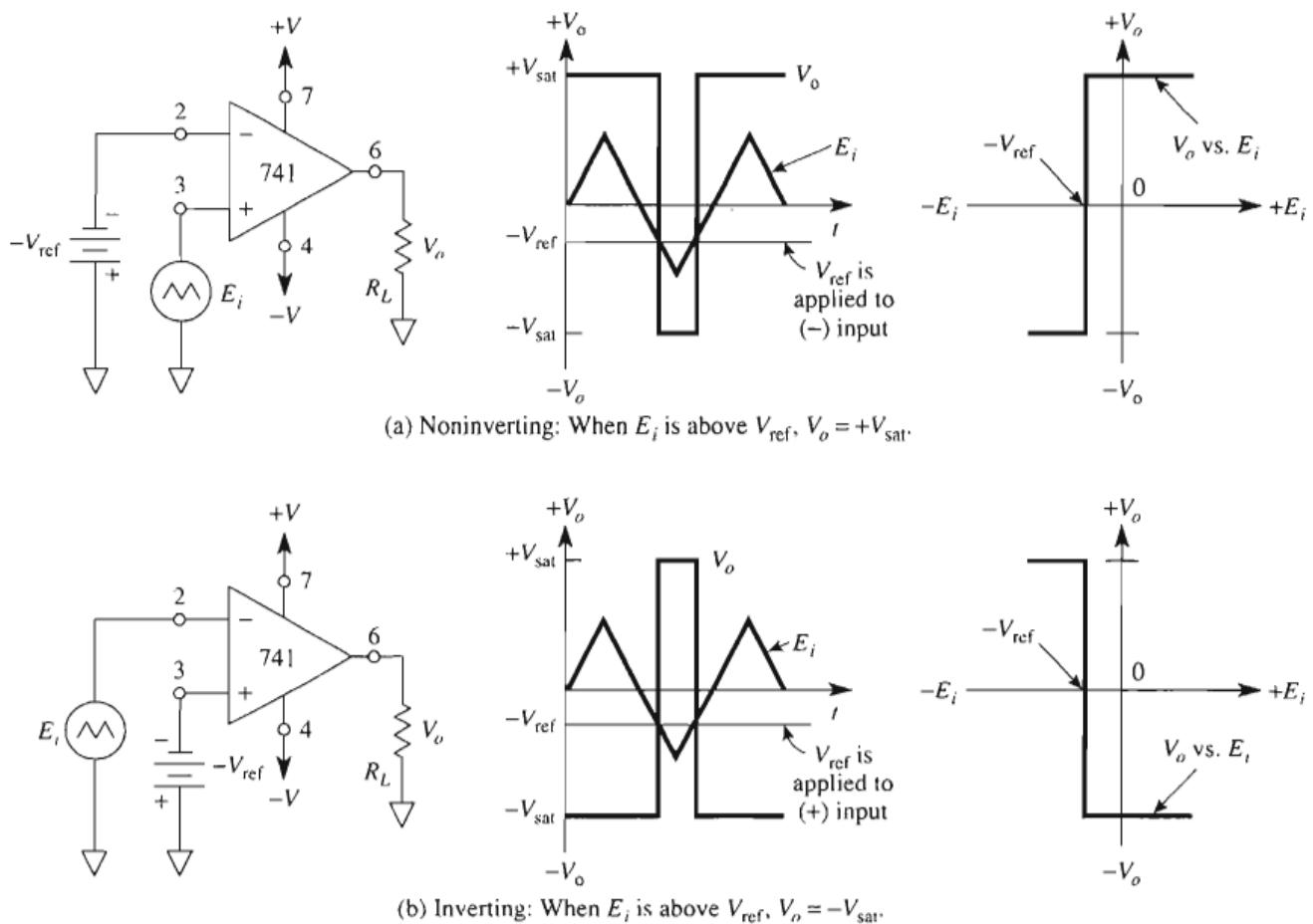


FIGURE 2-6 Negative-voltage-level detector, noninverting in (a) and inverting in (b).

A practical application that uses a positive level detector is the sound-activated switch shown in Fig. 2-8. Signal source E_i is a microphone, and an alarm circuit is connected to the output. The procedure to arm the sound switch is as follows:

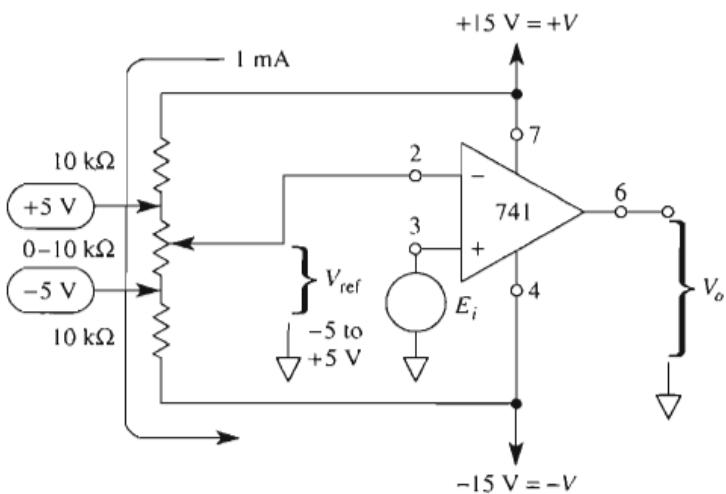


FIGURE 2-7 A variable reference voltage can be obtained by using the op amp's bipolar supply along with a voltage-divider network. (Note: Any fluctuations in the power supply result in a change in V_{ref} ; hence, the need to use a stable or precise voltage may be a requirement in your system.)

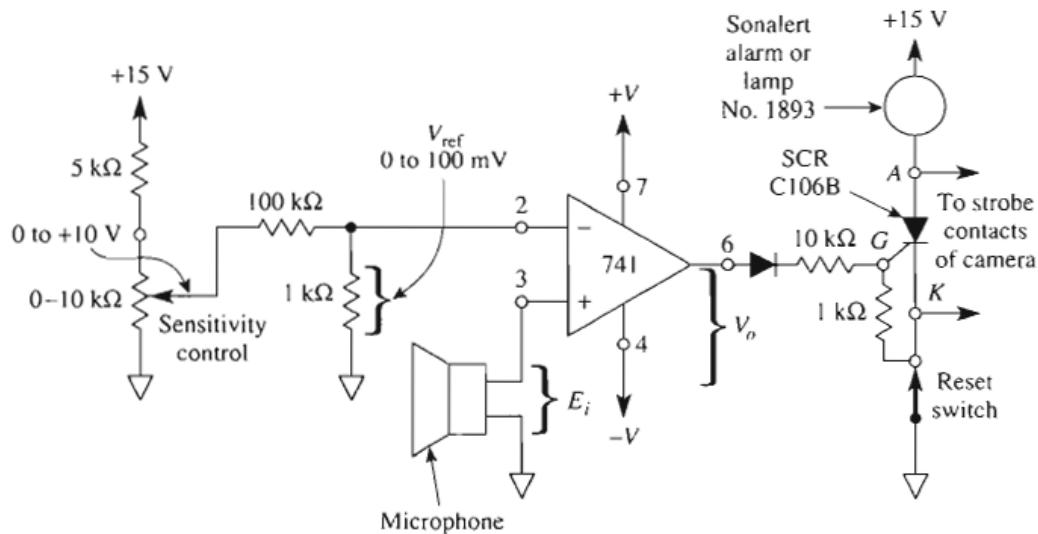


FIGURE 2-8 A sound-activated switch is made by connecting the output of a noninverting voltage-level detector to an alarm circuit.

1. Open the reset switch to turn off both SCR and alarm.
2. In a quiet environment, adjust the sensitivity control until V_o just swings to $-V_{sat}$.
3. Close the reset switch. The alarm should remain off.

Any noise signal will now generate an ac voltage and be picked up by the microphone as an input. The first positive swing of E_i above V_{ref} drives V_o to $+V_{sat}$. The diode now conducts a current pulse of about 1 mA into the gate, G , of the silicon-controlled rectifier (SCR). Normally, the SCR's anode, A , and cathode, K , terminals act like an open switch. However, the gate current pulse makes the SCR turn on, and now the anode and cathode terminals act like a closed switch. The audible or visual alarm is now activated. Furthermore, the alarm stays on because once an SCR has been turned on, it stays on until its anode-cathode circuit is opened.

The circuit of Fig. 2-8 can be modified to photograph high-speed events such as a bullet penetrating a glass bulb. Some cameras have mechanical switch contacts that close to activate a stroboscopic flash. To build this sound-activated flash circuit, remove the alarm and connect anode and cathode terminals to the strobe input in place of the camera switch. Turn off the room lights. Open the camera shutter and fire the rifle at the glass bulb. The rifle's sound activates the switch. The strobe does the work of apparently stopping the bullet in midair. Close the shutter. The position of the bullet in relation to the bulb in the picture can be adjusted experimentally by moving the microphone closer to or farther away from the rifle.

2-5.3 Light-Column Voltmeter

A light-column voltmeter displays a column of light whose height is proportional to voltage. Manufacturers of audio and medical equipment may replace analog meter panels with light-column voltmeters because they are easier to read at a distance.

A light-column voltmeter is constructed in the circuit of Fig. 2-9. R_{cal} is adjusted so that 1 mA flows through the equal resistor divider network R_1 to R_{10} . Ten separate reference voltages are established in 1-V steps from 1 V to 10 V.

When $E_i = 0$ V or is less than 1 V, the outputs of all op amps are at $-V_{sat}$. The silicon diodes protect the light-emitting diodes against excessive reverse bias voltage. When

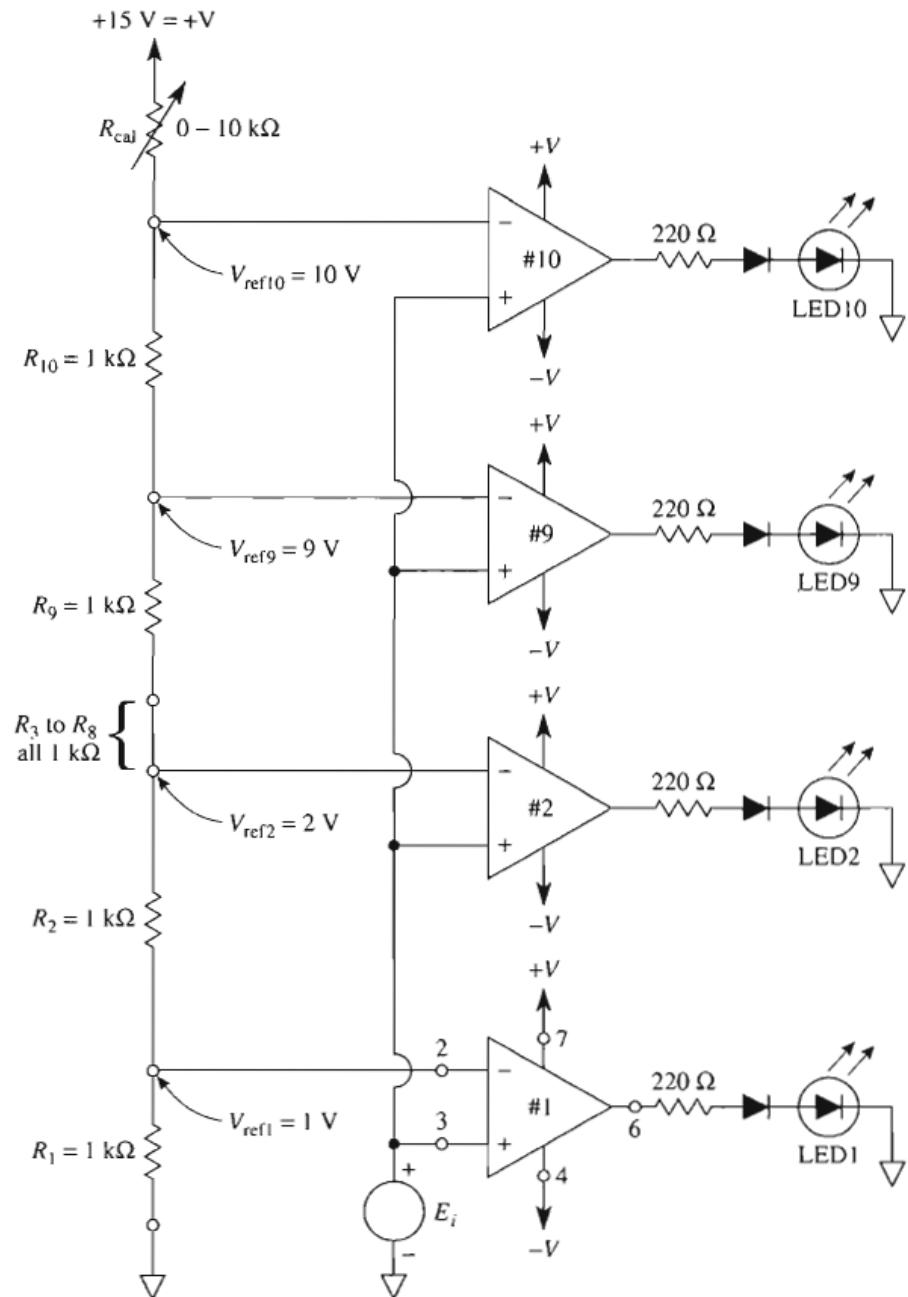


FIGURE 2-9 Light-column voltmeter. Reference voltages to each op amp are in steps of 1 V. As E_i is increased from 1 V to 10 V, LED1 through LED10 light in sequence. R_1 to R_{10} are 1% resistors. The op amps are 741 8-pin mini-DIPS.

E_i is increased to a value between 1 and 2 V, only the output of op amp 1 goes positive to light LED1. Note that the op amp's output current is automatically limited by the op amp to its short-circuit value approximately 20 to 25 mA. The $220\text{-}\Omega$ output resistors divert heat away from the op amp.

As E_i is increased, the LEDs light in numerical order. This circuit can also be built using two-and-one-half LM324 quad op amps; some manufacturers have designed IC packages for this particular application, such as National Semiconductor's LM3914.

2-5.4 Smoke Detector

Another practical application of a voltage-level detector is a smoke or dust particle detector, as shown in Fig. 2-10. The lamp and photoconductive cell are mounted in an enclosed chamber that admits smoke or dust but not external light. The photoconductor is a light-sensitive resistor. In the absence of smoke or dust, very little light strikes the photoconductor and its resistance stays at some high value, typically several hundred kilohms. The $10\text{-k}\Omega$ sensitivity control is adjusted until the alarm turns off.

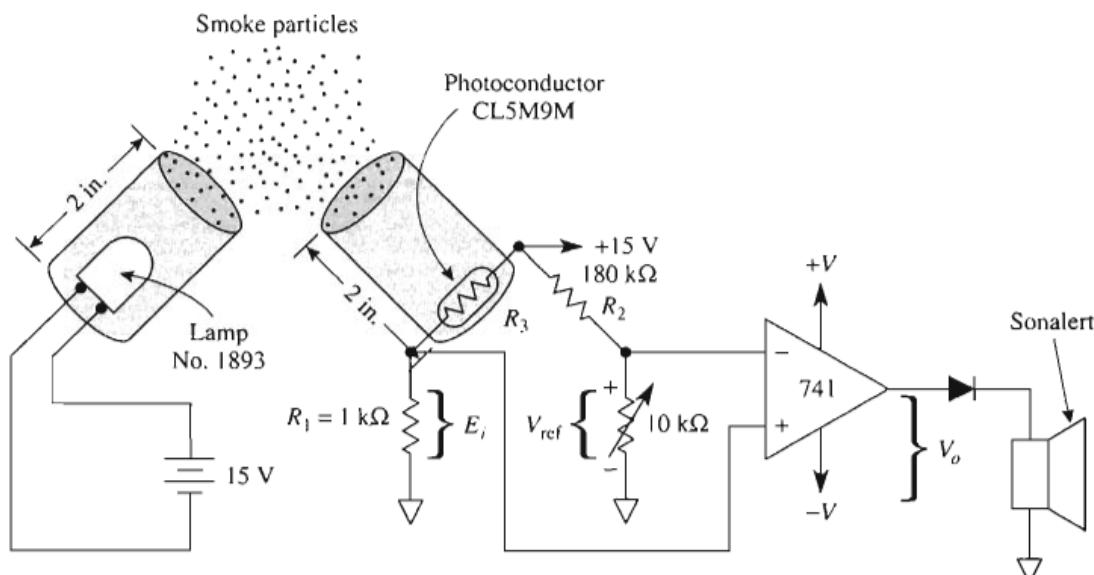


FIGURE 2-10 With no smoke or dust present the $10\text{-k}\Omega$ sensitivity control is adjusted until the alarm stops. Light reflected off any smoke or dust particles causes the alarm to sound.

Any particles entering the chamber cause light to reflect off the particles and strike the photoconductor. This, in turn, causes the photoconductor's resistance to decrease and the voltage across R_1 to increase. As E_i increases above V_{ref} , V_o switches from $-V_{\text{sat}}$ to $+V_{\text{sat}}$, causing the alarm to sound. The alarm circuit of Fig. 2-10 does not include an SCR. Therefore, when the particles leave the chamber, the photoconductor's resistance increases and the alarm turns off. If you want the alarm to stay on, use the SCR alarm circuit shown in Fig. 2-8. The lamp and photoresistor must be mounted in a flat black, lightproof box that admits smoke. Ambient (room) light prevents proper operation. The resistive network

at the input of the op amp forms a Wheatstone bridge. This circuit can be used to monitor the level of dust particles in a clean room environment.

2-6 VOLTAGE REFERENCE ICs

2-6.1 Introduction

Voltage reference ICs are used to provide a precise voltage for circuit and system designers, especially when setting the reference voltage for comparator circuits as well as A/D or D/A converters. Any fluctuation on the reference pin(s) of converter devices produces an inaccuracy in the conversion. Fluctuations on the reference input to a comparator can result in data being lost or erroneous data being sent to a computer system. In Figs. 2-7 and 2-8, we needed a reference voltage, V_{ref} , and used a resistor divider network connected between the supply voltages or the positive supply and ground. Although this circuit may be adequate for some quick-testing or low-cost designs, a better solution is to use a precision voltage reference chip. Many of these chips are inexpensive (less than a dollar), set a constant output voltage independent of temperature, and can be operated from a wide range of input power supply voltages. Variations in power supply voltages do not affect their output reference voltage. Some of these chips use the bandgap diode principle to produce a constant voltage of 1.2 V. This temperature-independent voltage is followed by an amplifier and buffer (amplifiers and buffers are topics covered in Chapter 3) to provide standard output voltages such as 2.5 V, 5 V, or 10 V. Other reference chips use a Zener diode as the reference followed by a buffer and amplifier to provide output voltages such as +5 V and -10 V, as well as ± 5 V and ± 10 V tracking outputs. Some of the most commonly used IC voltage reference chips are the REF-01 (+10 V), REF-02 (5 V), and REF-03 (2.5 V). We'll use the REF-02 IC as an introduction to precision voltage reference devices.

2-6.2 REF-02

The REF-02 IC outputs a stable +5.0 V, which can be adjusted by $\pm 6\%$ (± 300 mV) using one external potentiometer as shown in Fig. 2-11(a). The 10-k Ω potentiometer allows the actual output voltage to be adjusted from 4.7 to 5.3 V. Thus for an 8-bit A/D converter the reference voltage can be set to 5.12 V, creating a resolution of 20 mV/bit. (Resolution of A/D converters is discussed in detail in Chapter 14.) The REF-02 can operate from an input supply voltage of from 7 to 40 V, making it an ideal voltage reference device for a wide range of applications. Two common package styles are shown in Figs. 2-11(b) and (c).

2-6.3 REF-02/Voltage Level Detector Applications

Figure 2-11(d) shows how the REF-02 can be connected to an op amp comparator to set the reference voltage at 5.0 V. In this circuit, the adjustment potentiometer is not used and the REF-02 is used in its basic configuration. In this application, V_{ref} for the comparator

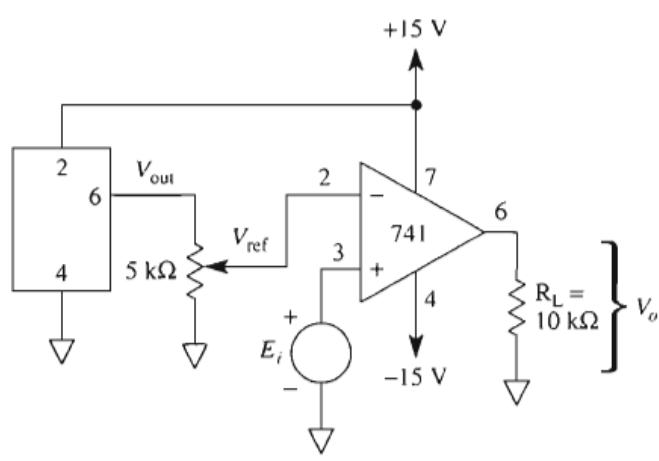
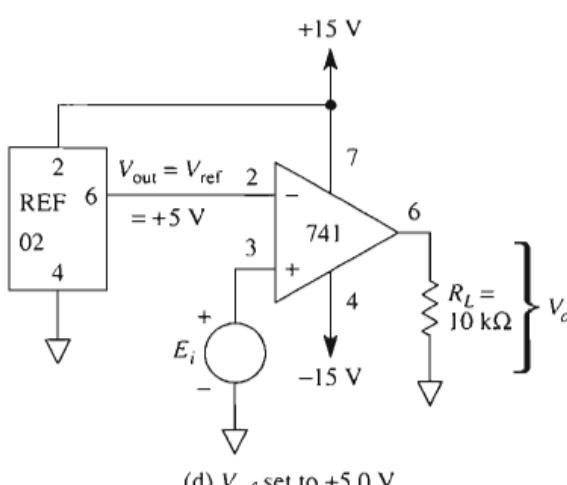
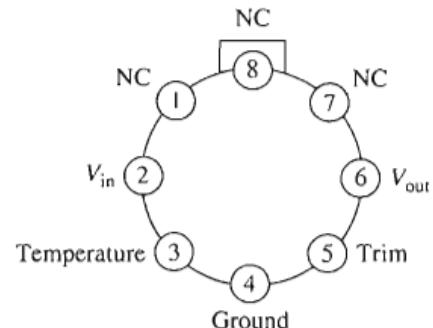
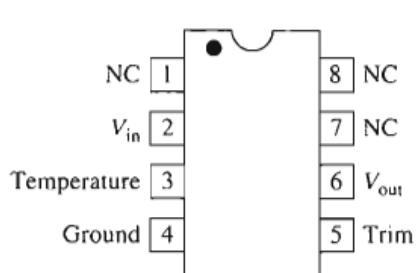
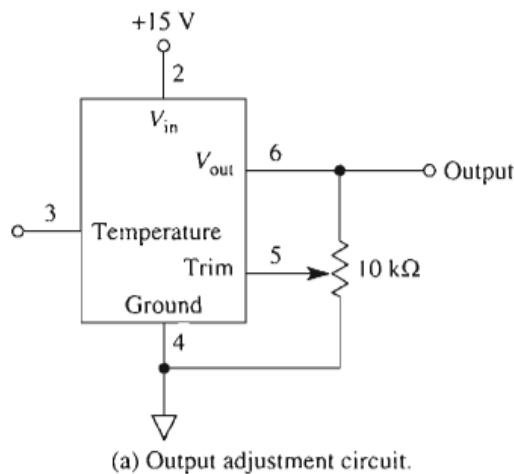


FIGURE 2-11 REF-02 pin assignments, package styles, and use with an op amp comparator.

should be within ± 15 mV because the manufacturer's specification for output voltage of the REF-02 is 0.3% of 5.0 V. If your design requires closer tolerance of V_{ref} , use the output adjustment circuit shown in Fig. 2-11(a).

If your application requires a stable but variable reference voltage of 0 to 5.0 V you still may use the REF-02 with a potentiometer connected between the REF-02's output terminal and common, as shown in Fig. 2-11(e). (Note: The 5-k Ω potentiometer in this figure allows us to vary V_{ref} for the comparator.) This potentiometer is not being used to adjust the output voltage of the REF-02 but rather the input reference to the comparator so that V_{ref} can be varied from 0 to 5.0 V. You still may use the circuit of Fig. 2-11(a) if you need to set the REF-02's maximum output voltage to 5.0 V \pm 300 mV. The temperature pin (pin 3) is used if the REF-02 is being used as a temperature sensor. For an example, refer to Analog Devices' Web Site, specifically the REF-02's data sheet, to see this device as a sensor in a temperature controller application.

2-7 SIGNAL PROCESSING WITH VOLTAGE-LEVEL DETECTORS

2-7.1 Introduction

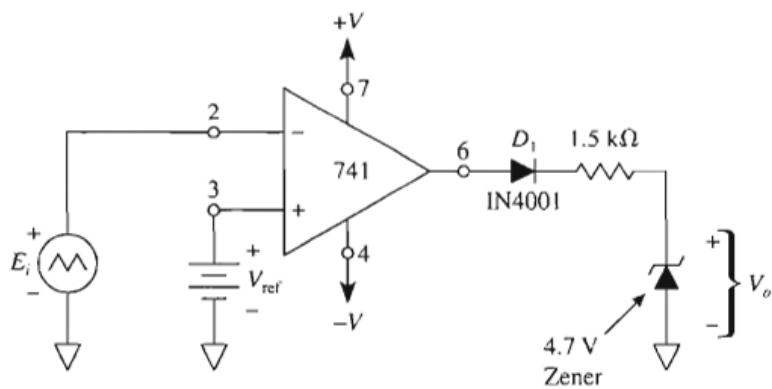
Armed with only the knowledge gained thus far, we will make a sine-to-square wave converter, an analog-to-digital converter, and a pulse-width modulator out of the versatile op amp. These open-loop comparator (or voltage-level detector) applications are offered to show how easy it is to use op amps.

2-7.2 Sine-to-Square Wave Converter

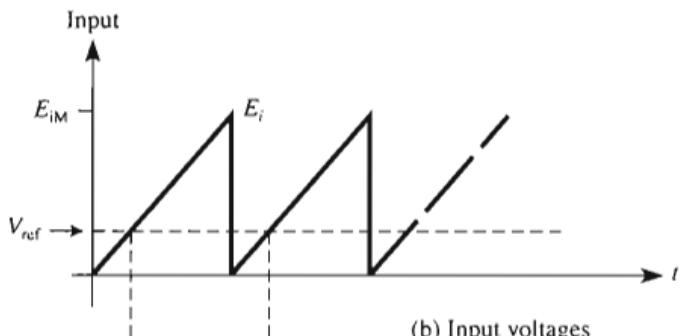
The zero-crossing detector of Fig. 2-4 will convert the output of a sine-wave from a function generator into a variable-frequency square wave. If E_i is a sine wave, triangular wave, or a wave of any other shape that is symmetrical around zero, the zero-crossing detector's output will be square. The frequency of E_i should be below 100 Hz, for reasons that are explained in Chapter 10.

2-7.3 Sawtooth-to-Pulse Wave Converter

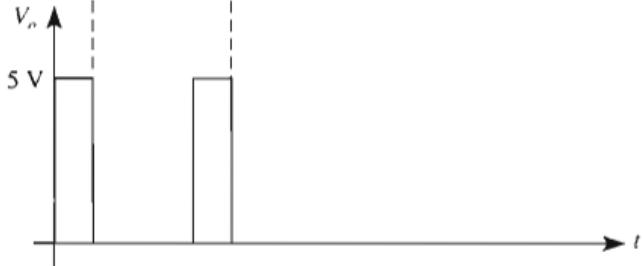
Zener Diode Method: The voltage level detector circuits of Section 2-4 can be used to convert a sawtooth wave to a pulse wave provided that the output of the op amp is modified to create only a positive pulse. This modification is shown in Fig. 2.12(a) and consists of a silicon diode, a resistor, and a zener diode in series. When the output voltage of the op amp is at $+V_{sat}$, the resistor limits the current to approximately 5 mA, enough current to cause zener breakdown. For this condition the output voltage of the circuit, V_o , equals the zener voltage, V_z 5.4.7 V in Fig. 2.12(a). When the op amp's output voltage is at $-V_{sat}$, diode D1 is reversed biased and the op amp's output current is zero, hence $V_o = 0$ V. This circuit is a quick way of converting a sawtooth-to-pulse wave that is TTL compatible. The input and output waveforms are shown in Figs. 2.12(b) and (c), respectively. For this application, however, a better method is to use an integrated circuit called a comparator because we can get V_o to swing between 0 and 5 V without the external diodes.



(a) Sawtooth-to-pulse wave converter circuit



(b) Input voltages



(c) Pulse output wave

FIGURE 2-12 A modification to a basic voltage-level detector converts a sawtooth wave to a pulse wave.

Comparator Method: Although comparator circuits are covered in detail in Chapter 4, comparator integrated circuit LM339 is introduced here so that a computer interfacing application using voltage-level detectors may be studied in the next section.

2-7.4 Quad Voltage Comparator, LM339

The pinouts and operation of a specialized op amp, the LM339, are shown in Figs. 2-13 and 2-14. The LM339 houses four independent op amps that have been specially designed to be flexible voltage comparators. We examine its operation by analyzing the role played by each terminal.

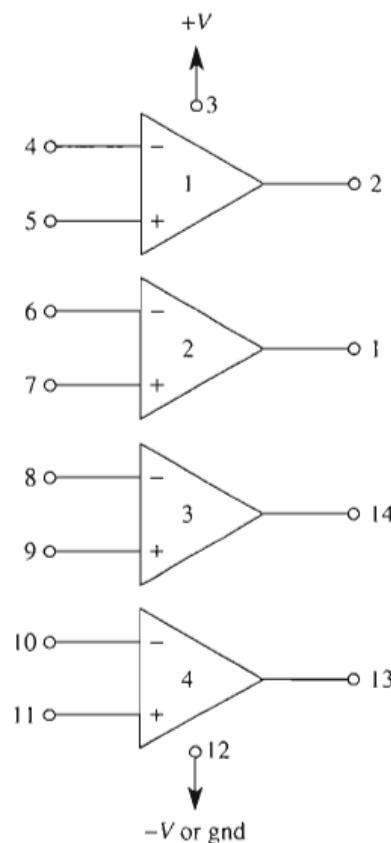


FIGURE 2-13 Connection diagram for the LM339 quad comparator. Four voltage comparators are contained in one 14-pin dual-in-line package.

Power supply terminals. Pins 3 and 12 are positive and negative supply voltage terminals, respectively, for all four comparators. Maximum supply voltage between pins 3 and 12 is ± 18 V. In most applications, the negative supply terminal, pin 12, is grounded. Then pin 3 can be any voltage from 2 to 36 V dc. The LM339 is used primarily for single-supply operation.

Output terminals. The output terminal of each op amp is an open-collector *npn* transistor. Each transistor collector is connected to the respective output terminals 2, 1, 14, and 13. All emitters are connected together and then to pin 12. If pin 12 is grounded, the output terminal acts like a switch. A closed switch extends the ground from pin 12 to the output terminal [see Fig. 2-14(b)].

If you want the output to go high when the switch is open, you must install a pull-up resistor and an external voltage source. As shown in Fig. 2-14(a), this feature allows easy interfacing between a ± 15 -V analog system and a 5-V digital system. The output terminal should not sink more than 16 mA.

Input terminals. The input terminals are differential. Use Eq. (2-1) to determine the sign for E_d . If E_d is positive, the output switch is *open*, as in Fig. 2-14(a). If E_d is negative, the output switch is *closed*, as in Fig. 2-14(b). Unlike many other op amps, the input terminals can be brought down to ground potential when pin 12 is grounded.

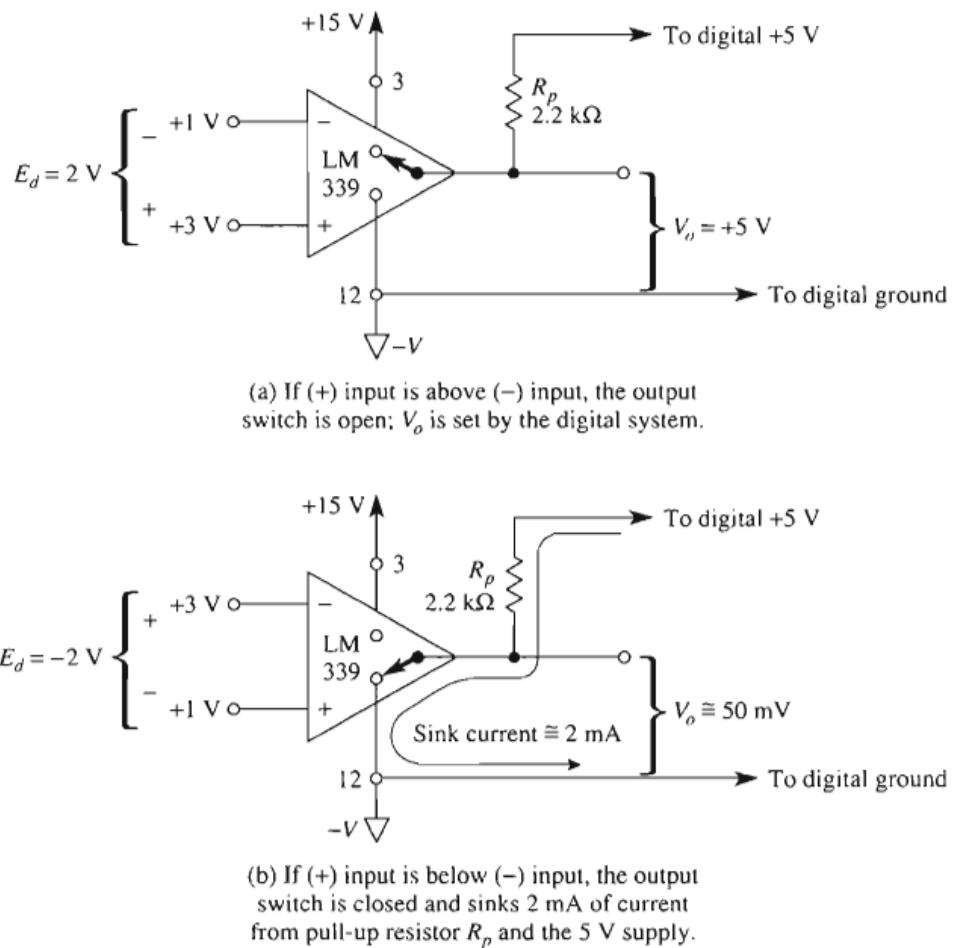


FIGURE 2-14 Operation of an LM339 (open collector output) comparator. When E_d is positive in (a), V_o goes high. V_o is determined by an external positive supply, pull-up resistor R_p and any external load resistor. If E_d is negative as in (b), the output goes low to essentially ground potential.

Summary. If the (+) input of an LM339 is *above* its (-) input, the output is pulled *high* by the pull-up resistor. If the (+) input is *below* the (-) input, the output is pulled *down* to the ground potential at pin 12. We now have information to analyze a pulse-width modulator application.

2-8 COMPUTER INTERFACING WITH VOLTAGE-LEVEL DETECTORS

2-8.1 Introduction

There are many characteristics of our environment or manufacturing processes that change very slowly. Examples are room temperature or the temperature of a large acid bath. A transducer can convert temperature changes to resistance or current changes. In Chapters 5 and 8 we show how you can convert these resistance or current changes into voltage changes quite easily with an op amp and a few parts.

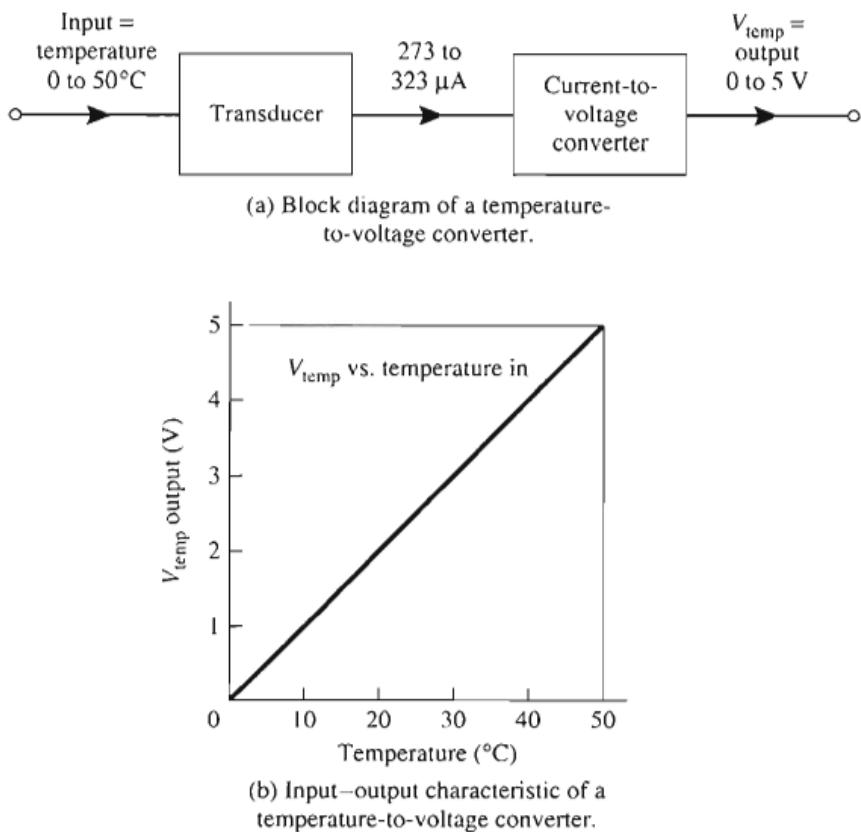


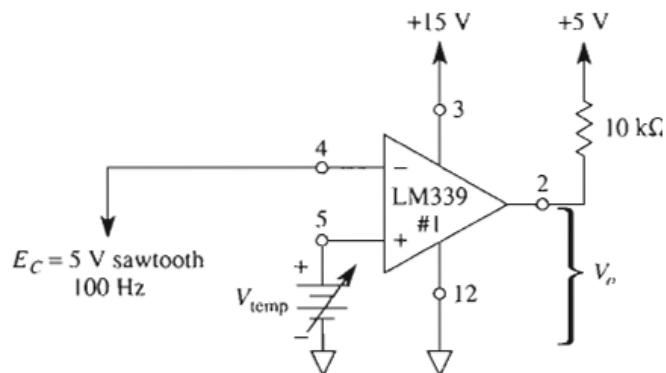
FIGURE 2-15 An example of how room or a process temperature is measured electronically.

Assume that you have available a circuit that gives 0 to 5 V out for a room-temperature change of 0° to 50°C (see Fig. 2-15). The output, V_{temp} , can now be used as a measurement of temperature, or it can be used to control temperature. Suppose that you want to send this temperature information to a computer so that the computer could monitor, control, or change room temperature. A voltage-level detector can accomplish this task. To understand how this can be done, we present a *pulse-width modulator* using the LM339 comparator.

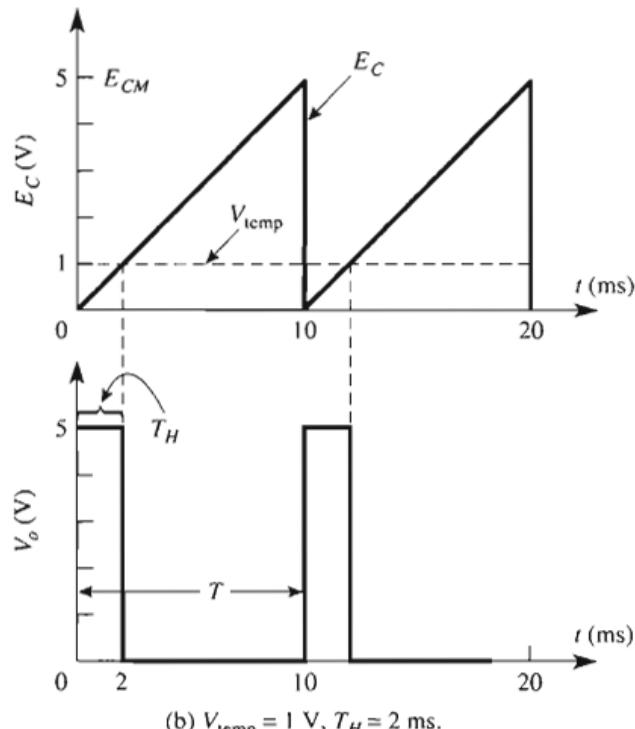
2-8.2 Pulse-Width Modulator, Noninverting

The LM339 comparator in Fig. 2-16(a) compares two input voltages, E_c and V_{temp} . [Figure 2-16(b) is similar to Fig. 2-12(a).] A sawtooth wave, E_c , with constant frequency is connected to the (−) input. It is called a *carrier wave*. V_{temp} is a temperature-controlled voltage. Its rate of change must be much less than that of E_c . In this design, V_{temp} is the signal from the temperature transducer. It can be treated as a variable reference voltage when Fig. 2-16(a) is compared to Fig. 2-12(a) or Fig. 2-5(b).

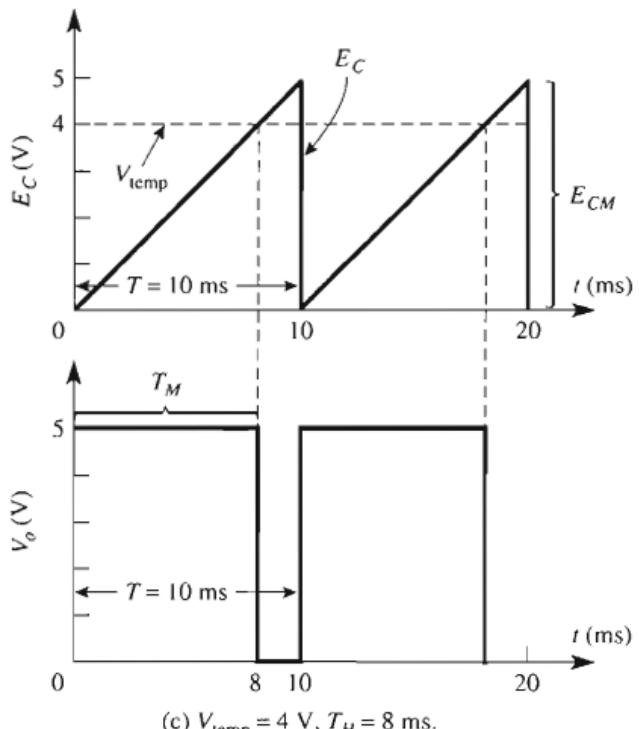
In this circuit the *input signal is defined as V_{temp} . The output is defined as the high time, T_H of V_o* . In Fig. 2-16(b), the output stays high for 2 ms when $V_{\text{temp}} = 1$ V. If V_{temp} increases to 4 V, high time T_H increases to 8 ms as in Fig. 2-16(c).



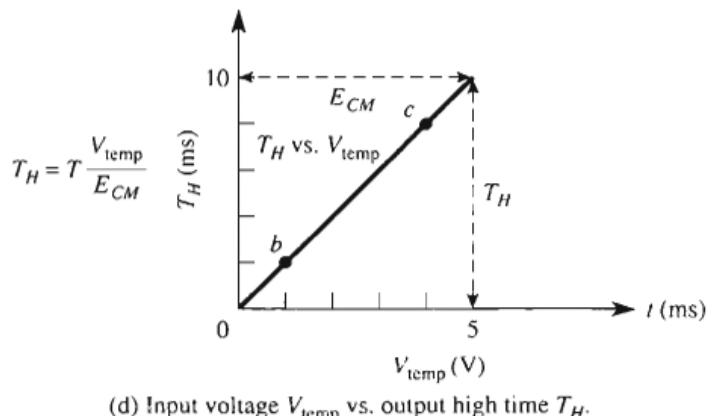
(a) Noninverting pulse-width-modulator circuit.



(b) $V_{\text{temp}} = 1 \text{ V}$, $T_H = 2 \text{ ms}$.



(c) $V_{\text{temp}} = 4 \text{ V}$, $T_H = 8 \text{ ms}$.



(d) Input voltage V_{temp} vs. output high time T_H .

FIGURE 2-16 V_{temp} is defined as the input signal in (a). As V_{temp} increases from 0 to 5 V, the high time of output voltage V_o increases from 0 to 10 ms. The circuit is called a *noninverting pulse-width modulator*.

Operation of the circuit is summarized by the input-output characteristics in Fig. 2-16(d). The width of output pulse T_H is changed (modulated) by V_{temp} . The constant period of the output wave is set by E_c . Thus E_c carries the information contained in V_{temp} . V_o is then said to be a pulse-width-modulated wave. The input-output equation is

$$\text{output } T_H = (V_{\text{temp}}) \frac{T}{E_{CM}} \quad (2-3)$$

where T = period of sawtooth carrier wave

E_{CM} = maximum peak voltage of a sawtooth carrier

Example 2-2 shows that the pulse-width modulator can also be called a *duty-cycle controller*.

Example 2-2

A 10-V, 50-Hz sawtooth wave is pulse-width modulated by a 4-V signal. Find the output's (a) high time; (b) duty cycle.

Solution Period T is found from the reciprocal of the frequency:

$$T = \frac{1}{f} = \frac{1}{50 \text{ Hz}} = 20 \text{ ms}$$

(a) From Eq. (2-3),

$$T_H = (4 \text{ V}) \frac{20 \text{ ms}}{10 \text{ V}} = 8 \text{ ms}$$

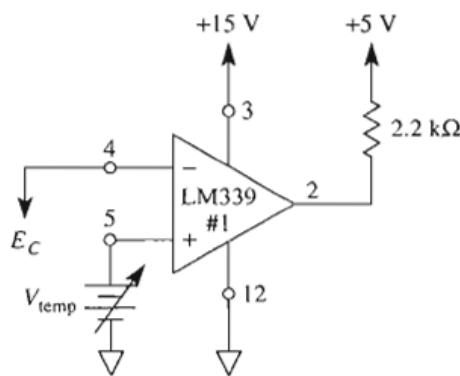
(b) Duty cycle is defined as the ratio of high time to the period and is expressed in percent:

$$\begin{aligned} \text{duty cycle} &= \frac{T_H}{T} \times 100 \\ &= \frac{8 \text{ ms}}{20 \text{ ms}} \times 100 \end{aligned} \quad (2-4)$$

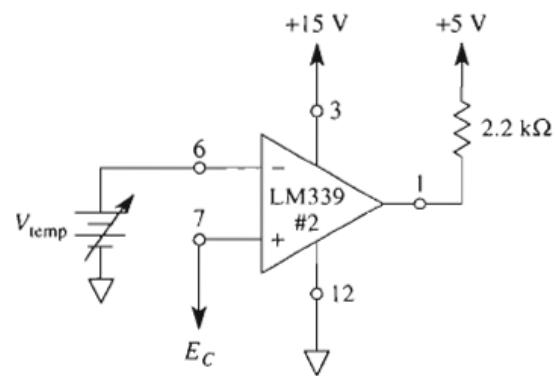
Thus the output stays high for 40% of each signal.

2-8.3 Inverting and Noninverting Pulse-Width Modulators

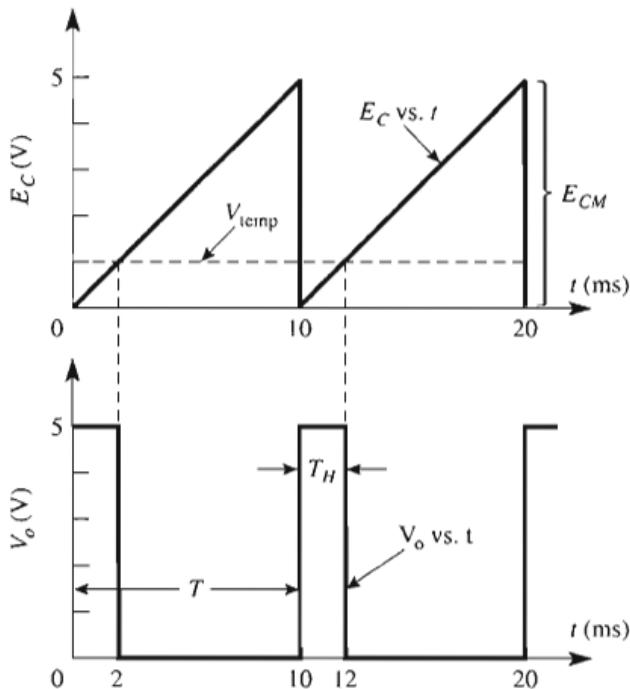
Figure 2-17 shows the difference between noninverting and inverting pulse-width modulators. If signal V_{temp} is applied to the (+) input, the circuit is defined as noninverting [see Figs. 2-17(a), (b), and (c)]. The *slope* of T_H versus V_{temp} rises to the right and is *positive* or *noninverting*.



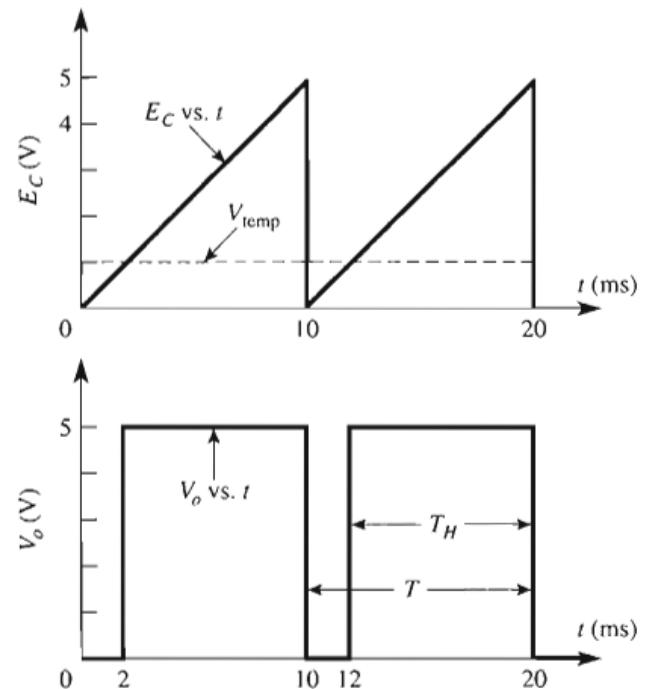
(a) Noninverting PWM.



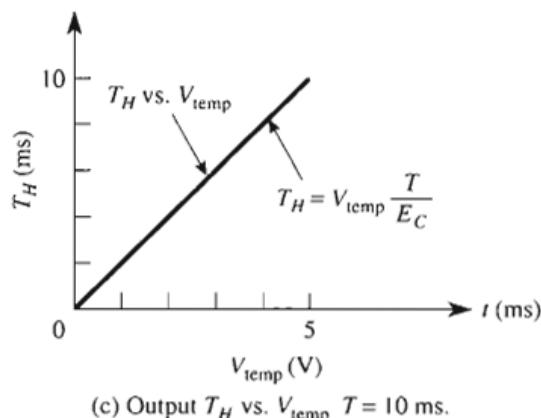
(d) Inverting PWM.



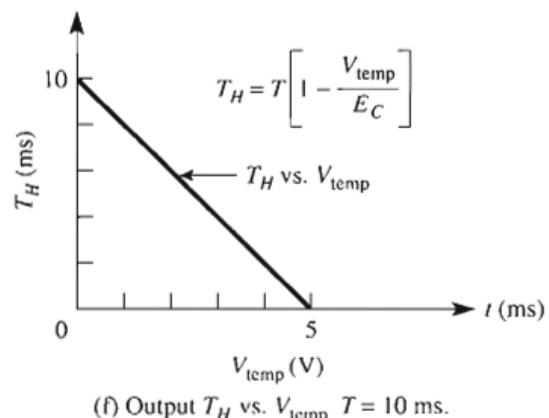
(b) Input and output wave forms for $V_{\text{ref}} = 1 \text{ V}$.



(e) Input and output wave forms for $V_{\text{ref}} = 1 \text{ V}$.



(c) Output T_H vs. V_{temp} $T = 10 \text{ ms}$.



(f) Output T_H vs. V_{temp} $T = 10 \text{ ms}$.

FIGURE 2-17 Output high time *increases* as input V_{temp} *increases* in a noninverting pulse-width modulator [see (a), (b), and (c)]. Output high time *decreases* as V_{temp} *increases* in an inverting pulse-width modulator.

V_{temp} is applied to the $(-)$ input in Fig. 2-17(d). As V_{temp} increases, T_H decreases. The slope of T_H versus V_{temp} is shown in Fig. 2-17(f) and is *negative*. The inverting performance equation is

$$T_H = T \left(1 - \frac{V_{\text{temp}}}{E_{CM}} \right) \quad (2-5)$$

Example 2-3

Calculate the output high time if $V_{\text{temp}} = 4$ V in Fig. 2-17(d).

Solution From Eq. (2-5),

$$T_H = 10 \text{ ms} \left(1 - \frac{4 \text{ V}}{5 \text{ V}} \right) = 2 \text{ ms}$$

2-9 A PULSE-WIDTH MODULATOR INTERFACE TO A MICROCONTROLLER

Either circuit of Fig. 2-17 can be used to transmit temperature information as a pulse-width modulated signal to a computer. The advantage of such an analog interface circuit is to eliminate a voltage drop over distances of several hundred feet. Thus the pulse-width modulator can interface an analog signal with an input port of a microcontroller (see Fig. 2-18). The temperature is first converted to a voltage by the sensor. A noninverting pulse-width modulator then converts this analog voltage to an output that is digital in nature; that is, its output is either high or low and the high time is directly proportional to temperature.

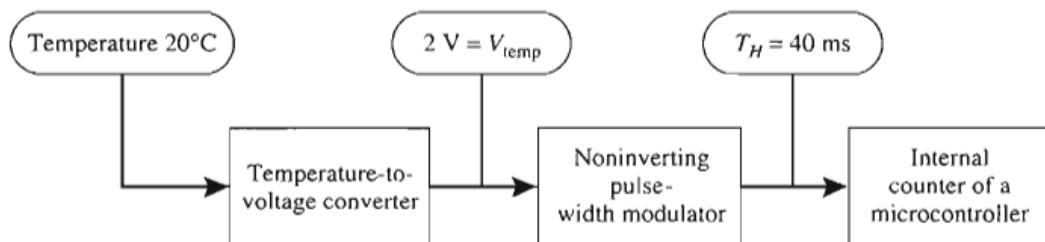


FIGURE 2-18 Block diagram of a computerized temperature measurement.

The computer programmer can perform the analog-to-digital conversion of the high time to a digital code. This may be done by using a 1-ms timing loop and counting the number of times that the loop is executed. Another and more efficient method is to use the internal counter designed into most microcontrollers. The 0-to-5-V transition of V_o is

used to start the microcontroller's counter and the 5-to-0-V transition stops the counter. The count, which is automatically stored in one of the microcontroller's internal registers, is directly proportional to the temperature.

2-10 OP AMP COMPARATOR CIRCUIT SIMULATION

2-10.1 Introduction

PSpice is a software package for analog and digital design analysis. Students who are studying op amps usually have already used PSpice in previous courses, so all the PSpice fundamentals are not introduced; however, enough introduction steps are included throughout this text to allow first-time users to create and analyze their circuits.

2-10.2 Creating, Initializing, and Simulating a Circuit

Let us create and analyze the noninverting positive-level detector circuit shown in Fig. 2-5(a). We will use a sine wave for the input signal because it is easy to obtain from the basic parts list. (Note: The parts list does not contain a triangular waveform although one can be created, which we will do in a later chapter.) To create and simulate Fig. 2-5(a), open a new worksheet either by clicking on **File => New**, or if the PSpice window is not open, double-click on the Schematics icon in the window. If necessary, enlarge the work area to fill the entire screen.

The basic parts list browser may be obtained by clicking **Draw** from the Menu bar and then clicking **Get New Part** from the drop-down menu. These steps will be represented by

Draw => Get New Part

A shortcut for obtaining the parts list is to click the icon on the toolbar. (Note: The icon symbol is different for different versions of PSpice.) Either method produces a pop-up menu that contains the **Parts Browser's** basic list. Click **Advanced >>** and the basic menu expands to include a window to show you the part before you place it in the work area. Other libraries of parts can be obtained by clicking on the **Libraries** button.

The general guidelines for creating and simulating a circuit in PSpice are:

1. Open a new work area.
2. Obtain each part from the parts list and place it in the work area. Then close the parts list.
3. Arrange the parts the way they appear in the circuit schematic.
4. Interconnect the parts.
5. Change any attribute value(s) for a part if necessary.
6. Initialize setup parameters—**Analysis => Setup**.
7. Initialize probe setup if you want a plot—**Analysis => Probe Setup**
8. Save the schematic as a file with the .SCH extension.
9. Ensure there are no wiring errors—**Analysis => Create Netlist**.
10. Execute the program to observe the results—**Analysis => Simulate**.

Let us create the noninverting positive-level detector circuit of Fig. 2-5(a) by calling up the following parts and placing them in the work area. It is easier if you get all the parts at once and place them in the right section of the work area, close the parts list, and then arrange the parts as they appear in the circuit schematic. For this application, we will use three dc supplies for $+V$, $-V$, and V_{ref} .

Draw => Get New Part

Part	Number	Version 6.2 Library
=> UA741	pins 1 and 5 are shown but not used	eval.slb
=> VDC	place three for $+V$, $-V$, and V_{ref}	source.slb
=> VSIN	sine wave	source.slb
=> GLOBAL	place six	port.slb
=> AGND	analog ground, place five	port.slb
=> R	resistor for RL	analog.slb

Close the parts list and arrange the parts as in Fig. 2-5(a). (Note: The op amp PSpice model comes from the parts list with the inverting terminal at the bottom and the noninverting terminal at the top of the diagram. For now we will leave it with this orientation. The terminals can be switched if the op amp is rotated twice and then flipped. In this new orientation, however, $+V$ is at the bottom and $-V$ is at the top.) To interconnect the parts, click **Draw => Wire** or click the thin Pencil icon in the toolbar. Figure 2-19 shows how the parts can be interconnected.

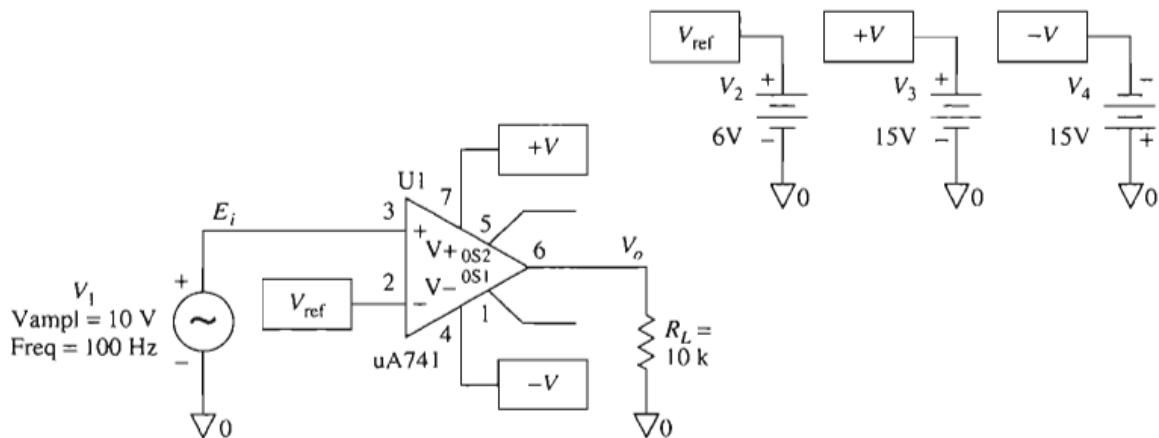


FIGURE 2-19 PSpice model of a noninverting comparator circuit.

The parts in this circuit that require setting new values (attributes) are the three dc supply voltages; the six globals; the sine wave's amplitude, frequency, and offset; and the value of R_L . Changing a part's attributes is done by first double-clicking on the part or value to be changed and then entering the new value. Double-clicking highlights the part or value in red and then opens an attribute box that allows you to enter the new value.

One at a time, double-click on 0 V and set the voltages at the supplies as:

+V = 15 V

-V = 15 V (Note the orientation of this supply.)

Vref = 6 V

One at a time, set the six GLOBAL labels as:

+V—at pin 7 of the op amp and that connected to +15 V

-V—at pin 4 of the op amp and that connected to -15 V

Vref—at pin 2 of the op amp and the source used for **Vref**.

Similarly the label of the resistor and its value can be changed to R_L and 10 k Ω , respectively. To change the attributes of the input sine-wave signal, double-click the symbol and a VSIN attribute box appears. One at a time, change each attribute by double-clicking the attribute and setting the new value in the window. For this circuit, amplitude, frequency, and offset values have to be changed as shown:

AMPL = to 10 V => **Save Attr** => **Change Display** => **Both name and value**

FREQ = to 100 Hz => **Save Attr** => **Change Display** => **Both name and value**

VOFF = to 0 V => **Save Attr** (not necessary to change display for this application)

In this application, we want a plot of E_i , V_{ref} , and V_o versus time similar to what is shown in Fig. 2-5(a). In order to do this, we first must add the location of E_i and V_o to the op amp's inverting and output terminals, respectively. The location of V_{ref} is already shown on the circuit diagram. This step is done by double-clicking the "wire" connection at the point of interest and entering the label in the window of the pop-up box. Figure 2-19 shows the completed schematic ready for analysis. To obtain these plots, open **Analysis** => **Probe Setup** and click Automatically Run Probe After Simulation. Now open **Analysis** => **Setup** and click the box next to **Transient**. An x appears indicating it has been selected. Now click on **Transient** and set Print Step to 0.05 ms and Final Time to 20 ms. This will allow Probe to display two complete cycles of a 100-Hz sine wave.

Save the file by **File** => **Save** or by clicking the Disk icon in the toolbar. You may use any file name but be sure to use extension .SCH. A check of the wiring corrections is done by creating a netlist—**Analysis** => **Create Netlist**. A warning appears if there are any wiring errors. Click OK and a list of the error location(s) is obtained. If there are no errors, then the circuit is ready to run the simulation program. This step is done by **Analysis** => **Simulate** or using the hot key F11. The Probe window (a black screen) appears. To plot the graphs, use **Trace** => **Add** and click **V[Ei]**, **V[Vref]**, and **V[Vo]** and then OK. The three waveforms should now be plotted as shown in Fig. 2-20. To add labels to the graphs, use **Tools** => **Label** => **Text** and a text box appears. Type in the label you wish to place on the graph and then click OK. Use the mouse to place the label where you want it and repeat the procedure for any new labels. To add arrows, use **Tools** => **Label** => **Arrow**. Use the mouse to place the tail of the arrow at the starting point and draw out the arrow. Click the left mouse button to stop and the completed arrow is drawn.

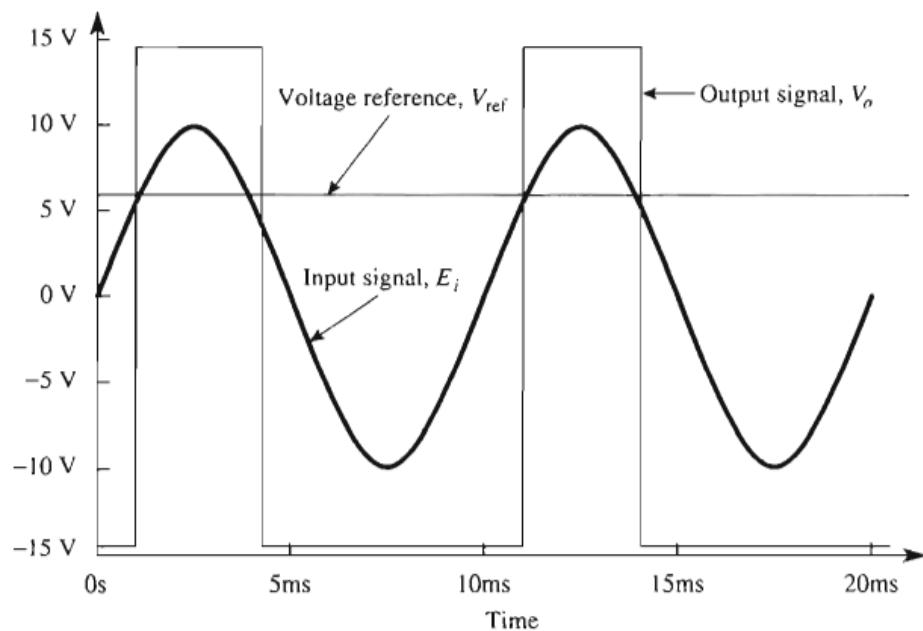


FIGURE 2-20 PSpice output display for a 10-V sine wave input and a reference level of 6 V.

PROBLEMS

- 2-1. Name the five basic terminals of an op amp.
- 2-2. Name the manufacturer of an AD741 op amp.
- 2-3. A 741 op amp is manufactured in an 8-pin dual-in-line package. What are the terminal numbers for the (a) inverting input; (b) noninverting input; (c) output?
- 2-4. A 741 op amp is connected to a ± 15 -V supply. What are the output terminal's operating limits under normal conditions with respect to (a) output voltage; (b) output current?
- 2-5. When the load resistor of an op amp is short-circuited, what is the op amp's (a) output voltage; (b) approximate output current?
- 2-6. Both op amps of Fig. P2-6 are in 14-pin dual-in-line packages. (a) Number the terminals. (b) Calculate E_d . (c) Find V_o .

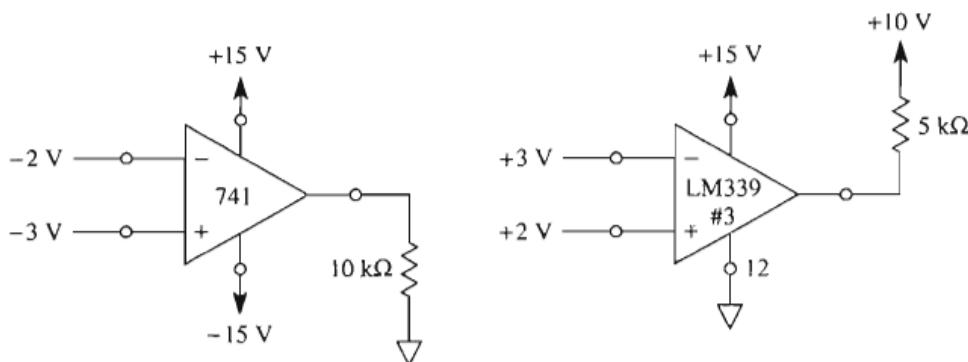


FIGURE P2-6

- 2-7. E_i is applied to the (−) input and ground to the (+) input of a 741 in Fig. P2-7. Sketch accurately (a) V_o vs. t and (b) V_o vs. E_i .

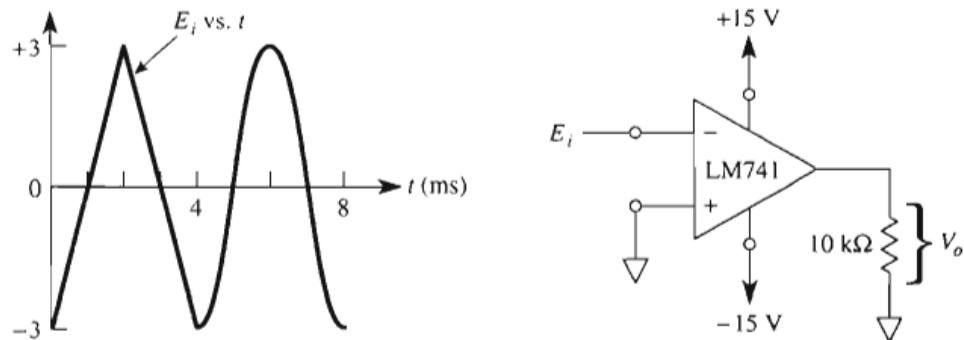


FIGURE P2-7

- 2-8. Swap the input connections to E_i and ground in Fig. P2-7. Sketch (a) V_o vs. t and (b) V_o vs. E_i .
- 2-9. Refer to Problems 2-7 and 2-8. Which circuit is the noninverting zero-crossing detector, and which is the inverting zero-crossing detector?
- 2-10. To which input would you connect a reference voltage to make an inverting level detector?
- 2-11. You need a 741 noninverting voltage-level detector. (a) Will the output be at $+V_{sat}$ or $-V_{sat}$ when the signal voltage is above the reference voltage? (b) To which input do you connect the signal?
- 2-12. Design a reference voltage that can be varied from 0 to -5 V. Assume that the negative supply voltage is -15 V.
- 2-13. Design a 0 to $+50$ mV adjustable reference voltage. Derive it from the $+15$ -V supply.
- 2-14. The frequency of carrier wave E_c is constant at 50 Hz in Fig. P2-14. If $V_{temp} = 5$ V, (a) calculate high time T_H ; (b) plot V_o vs. time.

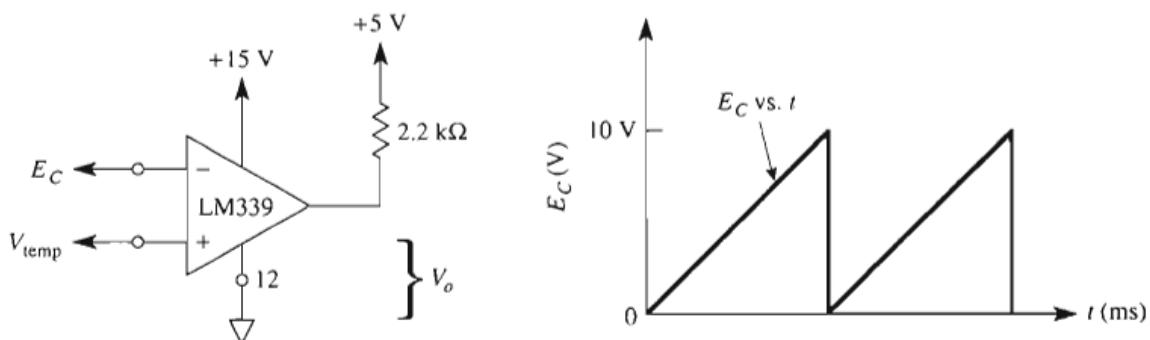


FIGURE P2-14

- 2-15. Assume that V_{temp} is varied from 0 V to $+10$ V in Problem 2-14. Plot T_H vs. V_{temp} .

- 2-16. In Fig. P2-16, E_{in} is a triangle wave. The amplitude is -5 V to $+5 \text{ V}$ and the frequency is 100 Hz. Sketch accurately the graphs of (a) V_o vs. E_{in} ; (b) V_o vs. t .

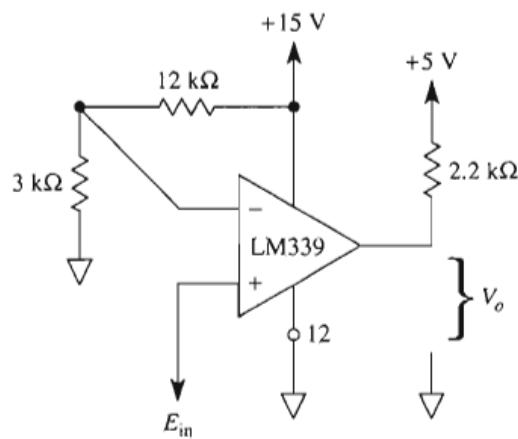


FIGURE P2-16

- 2-17. Draw the schematic of a circuit whose output voltage will go positive to $+V_{sat}$, when the input signal crosses $+5 \text{ V}$ in the positive direction.
- 2-18. Is the solution of Problem 2-17 classified as an inverting or noninverting comparator?
- 2-19. Draw a circuit whose output goes to $+V_{sat}$ when the input signal is below -4 V . The output should be at $-V_{sat}$ when the input is above -4 V .
- 2-20. Does the solution circuit for Problem 2-19 represent an (a) inverting or noninverting, (b) positive- or negative-voltage-level detector?

CHAPTER 3

Inverting and Noninverting Amplifiers

LEARNING OBJECTIVES

Upon completing this chapter on inverting and noninverting amplifiers, you will be able to:

- Draw the circuit for an inverting amplifier and calculate all voltages and currents for a given input signal.
- Draw the circuit for a noninverting amplifier and calculate all voltages and currents.
- Plot the output voltage waveshape and output–input characteristics of either an inverting or a noninverting amplifier for any input voltage waveshape.
- Design an amplifier to meet a gain and input resistance specification.
- Build an inverting or noninverting adder and audio mixer.
- Use a voltage follower to make an ideal voltage source.
- Create a negative output voltage from a positive reference voltage.
- Add a dc offset voltage to an ac signal voltage.

- Measure the average value of several signals.
- Design with single-supply op amps.
- Build a subtractor.
- Design a signal conditioning circuit for a temperature sensor.
- Analyze inverting and noninverting amplifier circuits using PSpice.

3-0 INTRODUCTION

This chapter uses the op amp in one of its most important applications—making an amplifier. An *amplifier* is a circuit that receives a signal at its input and delivers an undistorted larger version of the signal at its output. All circuits in this chapter have one feature in common: An external feedback resistor is connected between the output terminal and (−) input terminal. This type of circuit is called a *negative feedback circuit*.

There are many advantages obtained with negative feedback, all based on the fact that circuit performance no longer depends on the open-loop gain of the op amp, A_{OL} . By adding the feedback resistor, we form a loop from output to (−) input. The resulting circuit now has a *closed-loop gain* or *amplifier gain*, A_{CL} , which is independent of A_{OL} (provided that A_{OL} is much larger than A_{CL}).

As will be shown, the closed-loop gain, A_{CL} , depends only on external resistors. For best results 1% resistors should be used, and A_{CL} will be known within 1%. Note that adding external resistors does not change the open-loop gain A_{OL} . A_{OL} still varies from op amp to op amp, so adding negative feedback will allow us to ignore changes in A_{OL} as long as A_{OL} is large. We begin with the inverting amplifier to show that A_{CL} depends simply on the ratio of two resistors.

3-1 THE INVERTING AMPLIFIER

3-1.1 Introduction

The circuit of Fig. 3-1 is one of the most widely used op amp circuits. It is an amplifier whose closed-loop gain from E_i to V_o is set by R_f and R_i . It can amplify ac or dc signals. To understand how this circuit operates, we make two realistic simplifying assumptions that were introduced in Chapter 2.

1. The voltage E_d between the (+) and (−) inputs is essentially 0 if V_o is not in saturation.
2. The current drawn by either the (+) or the (−) input terminal is negligible.

3-1.2 Positive Voltage Applied to the Inverting Input

In Fig. 3-1, positive voltage E_i is applied through input resistor R_i to the op amp's (−) input. Negative feedback is provided by feedback resistor R_f . The voltage between the (+) and (−) inputs is essentially equal to 0 V. Therefore, the (−) input terminal is also at

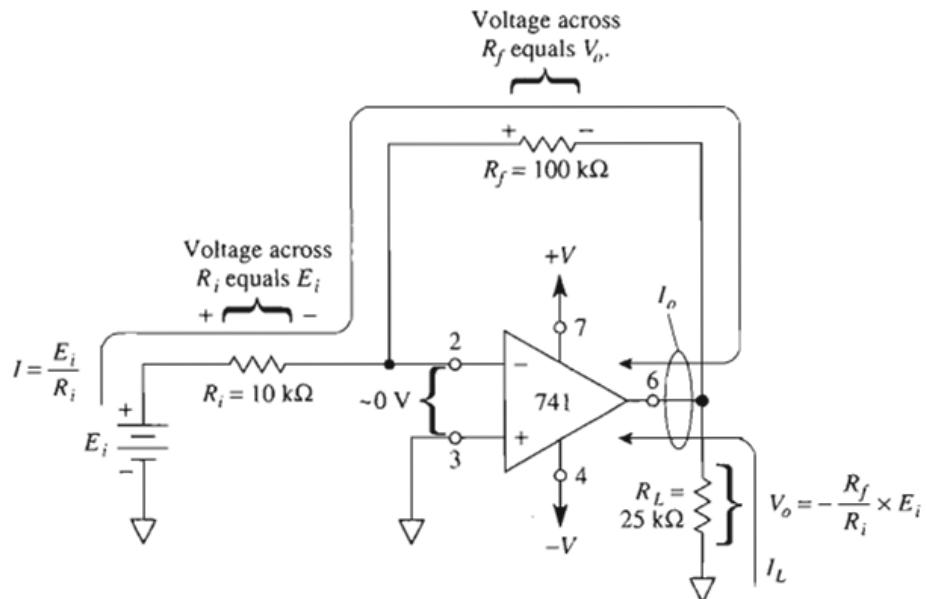


FIGURE 3-1 A positive input voltage is applied to the (−) input of an inverting amplifier. R_i converts this voltage to a current, I ; R_f converts I back into an amplified version of E_i .

0 V, so ground potential is at the (−) input. For this reason, the (−) input is said to be at *virtual ground*.

Since one side of R_i is at E_i and the other is at 0 V, the voltage drop across R_i is E_i . The current I through R_i is found from Ohm's law:

$$I = \frac{E_i}{R_i} \quad (3-1a)$$

R_i includes the resistance of the signal generator. This point is discussed further in Section 3-5.2.

All of the input current I flows through R_f , since a negligible amount is drawn by the (−) input terminal. Note that the current through R_f is set by R_i and E_i ; not by R_f , V_o , or the op amp.

The voltage drop across R_f is simply $I (R_f)$, or

$$V_{R_f} = I \times R_f = \frac{E_i}{R_i} R_f \quad (3-1b)$$

As shown in Fig. 3-1, one side of R_f and one side of load R_L are connected. The voltage from this connection to ground is V_o . The other sides of R_f and of R_L are at ground potential. Therefore, V_o equals V_{R_f} (the voltage across R_f). To obtain the polarity of V_o , note that the left side of R_f is at ground potential. The current direction established by E_i forces the right side of R_f to go negative. Therefore, V_o is negative when E_i is positive. Equating V_o with V_{R_f} and adding a minus sign to signify that V_o goes negative when E_i goes positive, we have

$$V_o = -E_i \frac{R_f}{R_i} \quad (3-2a)$$

Now, introducing the definition that the closed-loop gain of the amplifier is A_{CL} , we rewrite Eq. (3-2a) as

$$A_{CL} = \frac{V_o}{E_i} = -\frac{R_f}{R_i} \quad (3-2b)$$

The minus sign in Eq. (3-2b) shows that the polarity of the output V_o is inverted with respect to E_i . For this reason, the circuit of Fig. 3-1 is called an *inverting amplifier*.

3-1.3 Load and Output Currents

The load current I_L that flows through R_L is determined only by R_L and V_o and is furnished from the op amp's output terminal. Thus $I_L = V_o/R_L$. The current I through R_f must also be furnished by the output terminal. Therefore, the op amp output current I_o is

$$I_o = I + I_L \quad (3-3)$$

Example 3-1

For Fig. 3-1, let $R_f = 100 \text{ k}\Omega$, $R_i = 10 \text{ k}\Omega$, and $E_i = 1 \text{ V}$. Calculate (a) I ; (b) V_o ; (c) A_{CL} .

Solution (a) From Eq. (3-1a),

$$I = \frac{E_i}{R_i} = \frac{1 \text{ V}}{10 \text{ k}\Omega} = 0.1 \text{ mA}$$

(b) From Eq. (3-2a),

$$V_o = -\frac{R_f}{R_i} \times E_i = -\frac{100 \text{ k}\Omega}{10 \text{ k}\Omega} (1 \text{ V}) = -10 \text{ V}$$

(c) Using Eq. (3-2b), we obtain

$$A_{CL} = -\frac{R_f}{R_i} = -\frac{100 \text{ k}\Omega}{10 \text{ k}\Omega} = -10$$

This answer may be checked by taking the ratio of V_o to E_i :

$$A_{CL} = \frac{V_o}{E_i} = \frac{-10 \text{ V}}{1 \text{ V}} = -10$$

Example 3-2

Using the values given in Example 3-1 and $R_L = 25 \text{ k}\Omega$, determine (a) I_L ; (b) the total current into the output pin of the op amp.

Solution (a) Using the value of V_o calculated in Example 3-1, we obtain

$$I_L = \frac{V_o}{R_L} = \frac{10 \text{ V}}{25 \text{ k}\Omega} = 0.4 \text{ mA}$$

The direction of current is shown in Fig. 3-1.

(b) Using Eq. (3-3) and the value of I from Example 3-1, we obtain

$$I_o = I + I_L = 0.1 \text{ mA} + 0.4 \text{ mA} = 0.5 \text{ mA}$$

The input resistance seen by E_i is R_i . In order to keep input resistance of the circuit high, R_i should be equal to or greater than $10 \text{ k}\Omega$.

Note: The maximum value of I_o is usually between 5 and 10 mA.

3-1.4 Negative Voltage Applied to the Inverting Input

Figure 3-2 shows a negative voltage, E_i , applied via R_i to the inverting input. All the principles and equations of Sections 3-1.1 to 3-1.3 still apply. The only difference between Figs. 3-1 and 3-2 is the direction of the currents. Reversing the polarity of the input voltage, E_i , reverses the direction of all currents and the voltage polarities. Now the output of the amplifier will go positive when E_i goes negative.

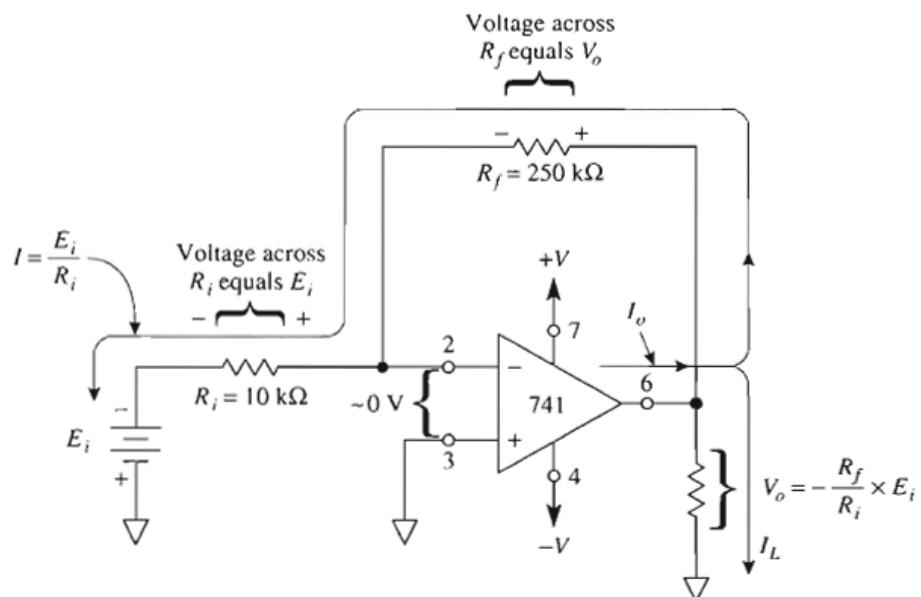


FIGURE 3-2 Negative voltage applied to the (−) input of an inverting amplifier.

Example 3-3

For Fig. 3-2, let $R_f = 250 \text{ k}\Omega$, $R_i = 10 \text{ k}\Omega$, and $E_i = -0.5 \text{ V}$. Calculate (a) I ; (b) the voltage across R_f ; (c) V_o .

Solution (a) From Eq. (3-1a),

$$I = \frac{E_i}{R_i} = \frac{0.5 \text{ V}}{10 \text{ k}\Omega} = 50 \mu\text{A} = 0.05 \text{ mA}$$

(b) From Eq. (3-1b),

$$\begin{aligned} V_{R_f} &= I \times R_f \\ &= (50 \mu\text{A})(250 \text{ k}\Omega) \\ &= 12.5 \text{ V} \end{aligned}$$

(c) From Eq. (3-2a),

$$V_o = -\frac{R_f}{R_i} \times E_i = -\frac{250 \text{ k}\Omega}{10 \text{ k}\Omega} (-0.5 \text{ V}) = +12.5 \text{ V}$$

Thus the magnitude of the output voltage does equal the voltage across R_f , and $A_{CL} = -25$.

Example 3-4

Using the values in Example 3-3, determine (a) R_L for a load current of 2 mA; (b) I_o ; (c) the circuit's input resistance.

Solution (a) Using Ohm's law and V_o from Example 3-3,

$$R_L = \frac{V_o}{I_L} = \frac{12.5 \text{ V}}{2 \text{ mA}} = 6.25 \text{ k}\Omega$$

(b) From Eq. (3-3) and Example 3-3,

$$I_o = I + I_L = 0.05 \text{ mA} + 2 \text{ mA} = 2.05 \text{ mA}$$

(c) The circuit's input resistance, or the resistance seen by E_i , is $R_i = 10 \text{ k}\Omega$.

A PSpice model and simulation results are given in Section 3-13.

3-1.5 Voltage Applied to the Inverting Input

Figure 3-3(a) shows an ac signal voltage E_i applied via R_i to the inverting input. For the positive half-cycle, the voltage polarities and the direction of currents are the same as in Fig. 3-1. For the negative half-cycle voltage, the polarities and direction of currents are the same as in Fig. 3-2. The output waveform is the negative (or 180° out of phase) of the

input wave as shown in Fig. 3-3(b). That is, when E_i is positive, V_o is negative; and vice versa. The equations developed in Section 3-1.2 are applicable to Fig. 3-3 for ac voltages.

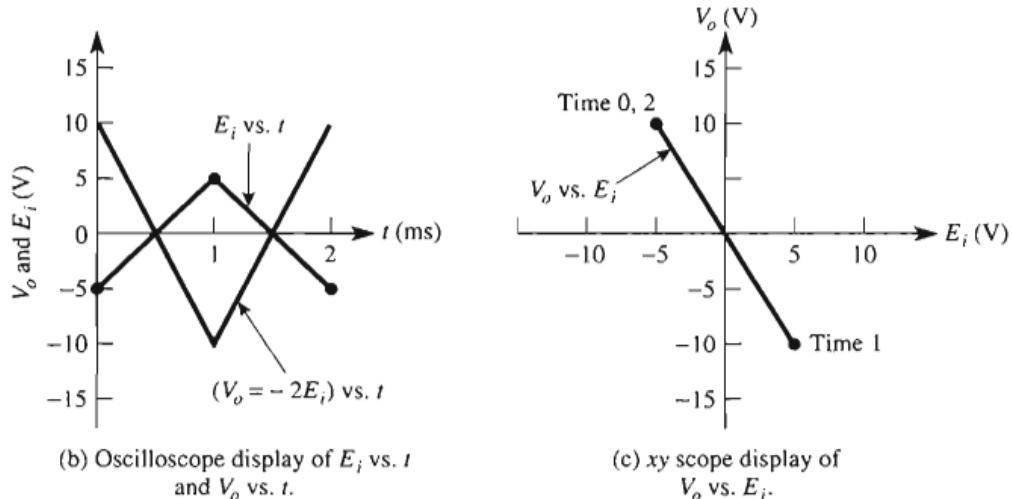
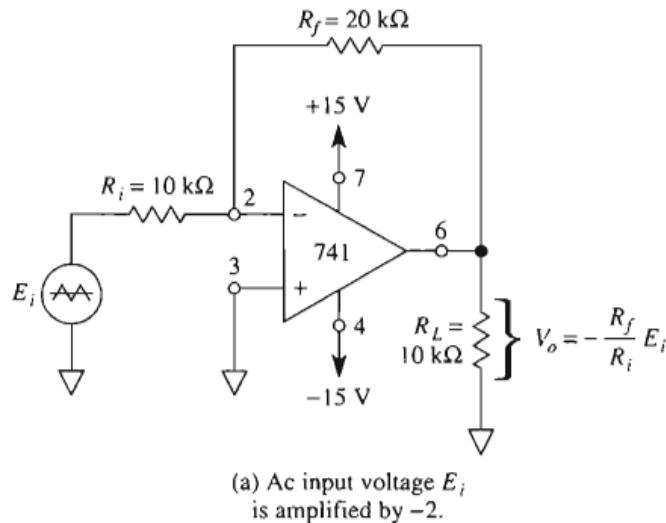


FIGURE 3-3 The inverting amplifier circuit in (a) has an ac input signal and a gain of -2 . Time plots are shown in (b) and the output–input characteristic in (c). Note that the slope of V_o versus E_i in (c) is the closed loop gain A_{CL} (rise/run = V_o/E_i).

Example 3-5

For the circuit of Fig. 3-3, $R_f = 20 \text{ k}\Omega$ and $R_i = 10 \text{ k}\Omega$, calculate the voltage gain A_{CL} .

Solution From Eq. (3-2b),

$$A_{CL} = -\frac{R_f}{R_i} = -\frac{20 \text{ k}\Omega}{10 \text{ k}\Omega} = -2$$

Example 3-6

If the input voltage in Example 3-5 is -5 V, determine the output voltage.

Solution Using Eq. (3-2a) or rearranging Eq. (3-2b), we obtain

$$V_o = -\frac{R_f}{R_i} \times E_i = A_{CL} E_i = (-2)(-5 \text{ V}) = 10 \text{ V}$$

See time 0 in Figs. 3-3(b) and (c). The frequency of the output and input signals is the same.

A PSpice model and simulation are given in Section 3-13. The simulation uses a 5-V-peak sine wave with a frequency set at 500 Hz as the input signal.

3-1.6 Design Procedure

Following is an example of the design procedure for an inverting amplifier.

Design Example 3-7

Design an amplifier with a gain of -25 . The input resistance R_{in} should equal or exceed $10 \text{ k}\Omega$.

Design Procedure

1. Choose the circuit type illustrated in Figs. 3-1 to 3-3.
2. Pick $R_i = 10 \text{ k}\Omega$ (safe, prudent choice).
3. Calculate R_f from $R_f = (\text{gain})(R_i)$. (For this calculation, use the magnitude of gain.)

3-1.7 Analysis Procedure

You are interviewing for a job in the electronics field. The technical interviewer asks you to analyze the circuit. Assume that you recognize the circuit as that of an inverting amplifier. Then,

1. Look at R_i . State that the input resistance of the circuit equals the resistance of R_i .
2. Divide the value of R_f by the value of R_i . State that the magnitude of gain equals R_f/R_i . Also, the output voltage will be negative when the input voltage is positive.

3-2 INVERTING ADDER AND AUDIO MIXER

3-2.1 Inverting Adder

In the circuit of Fig. 3-4, V_o equals the sum of the input voltages with polarity reversed. Expressed mathematically,

$$V_o = -(E_1 + E_2 + E_3) \quad (3-4)$$

Circuit operation is explained by noting that the summing point S and the $(-)$ input are at ground potential. Current I_1 is set by E_1 and R , I_2 by E_2 and R , and I_3 by E_3 and R . Expressed mathematically,

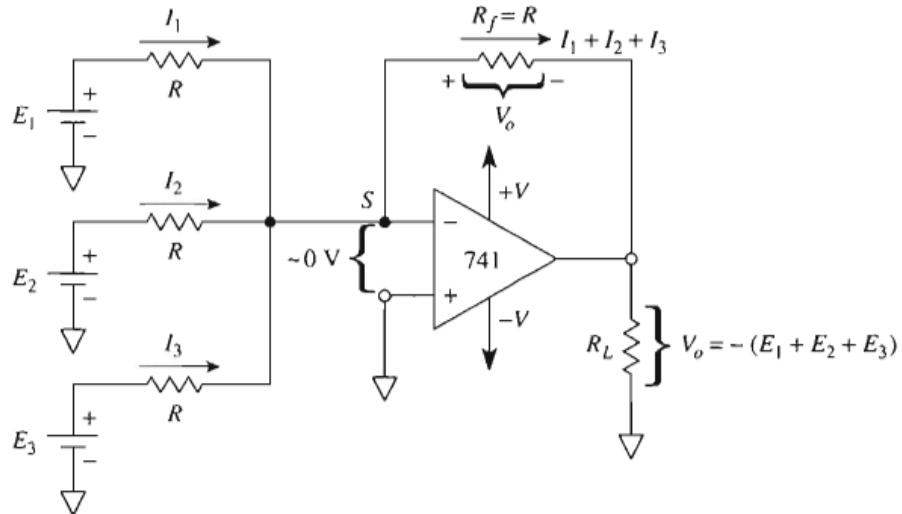


FIGURE 3-4 Inverting adder, $R = 10 \text{ k}\Omega$.

$$I_1 = \frac{E_1}{R}, \quad I_2 = \frac{E_2}{R}, \quad I_3 = \frac{E_3}{R} \quad (3-5)$$

Since the $(-)$ input draws negligible current, I_1 , I_2 , and I_3 all flow through R_f . That is, the sum of the input currents flows through R_f and sets up a voltage drop across R_f equal to V_o , or

$$V_o = -(I_1 + I_2 + I_3)R_f$$

Substituting for the currents from Eq. (3-5) and substituting R for R_f , we obtain Eq. (3-4):

$$V_o = -\left(\frac{E_1}{R} + \frac{E_2}{R} + \frac{E_3}{R}\right)R = -(E_1 + E_2 + E_3)$$

Example 3-8

In Fig. 3-4, $E_1 = 2 \text{ V}$, $E_2 = 3 \text{ V}$, $E_3 = 1 \text{ V}$, and all resistors are $10 \text{ k}\Omega$. Evaluate V_o .

Solution From Eq. (3-4), $V_o = -(2 \text{ V} + 3 \text{ V} + 1 \text{ V}) = -6 \text{ V}$. The PSpice model for this circuit is shown in Fig. 3-24.

Example 3-9

If the polarity of E_3 is reversed in Fig. 3-4 but the values are the same as in Example 3-8, find V_o .

Solution From Eq. (3-4), $V_o = -(2 \text{ V} + 3 \text{ V} - 1 \text{ V}) = -4 \text{ V}$.

If only two input signals, E_1 and E_2 , are needed, simply replace E_3 with a short circuit to ground. If four signals must be added, simply add another equal resistor R between the fourth signal and the summing point S . Equation (3-4) can be changed to include any number of input voltages.

3-2.2 Audio Mixer

In the adder of Fig. 3-4, all the input currents flow through feedback resistor R_f . This means that I_1 does not affect I_2 or I_3 . More generally, the input currents do *not* affect one another because each “sees” ground potential at the summing node. Therefore, the input currents—and consequently the input voltages E_1 , E_2 , and E_3 —do *not* interact.

This feature is especially desirable in an audio mixer. For example, let E_1 , E_2 , and E_3 be replaced by microphones. The ac voltages from each microphone will be added or mixed at every instant. Then if one microphone is carrying guitar music, it will not come out of a second microphone facing the singer. If a 100-k Ω volume control is installed between each microphone and associated input resistor, their relative volumes can be adjusted and added. A weak singer can then be heard above a very loud guitar.

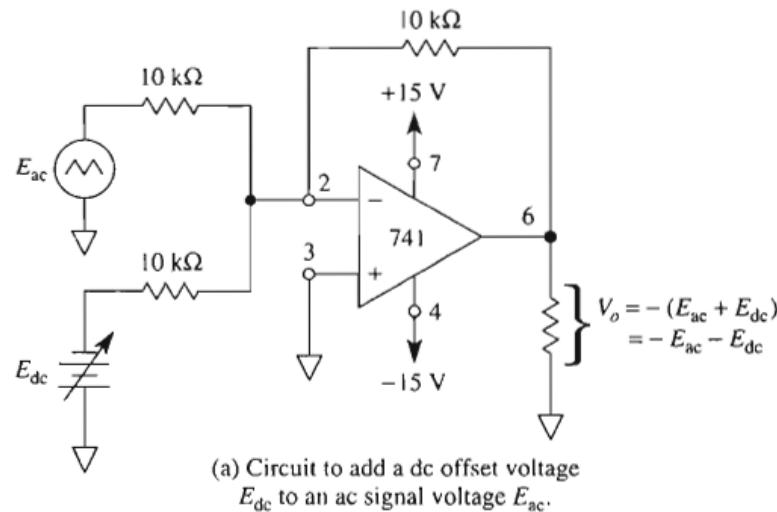
3-2.3 DC Offsetting an AC Signal

Some applications require that you add a dc offset voltage or current to an ac signal. Suppose that you must transmit an audio signal via an infrared emitting diode (IRED) or light-emitting diode. It is first necessary to bias the IRED on with a dc current. Then the audio signal can be superimposed as an ac current that rides on or modulates the dc current. The result is a light or infrared beam whose intensity changes directly with the audio signal. We illustrate this principle by an example.

Example 3-10

Design a circuit that allows you to add a dc voltage to a triangle wave.

Solution Select a two-channel adder circuit as in Fig. 3-5(a). A variable dc offset voltage E_{dc} , is connected to one channel. The ac signal, E_{ac} , is connected to the other.



(a) Circuit to add a dc offset voltage E_{dc} to an ac signal voltage E_{ac} .

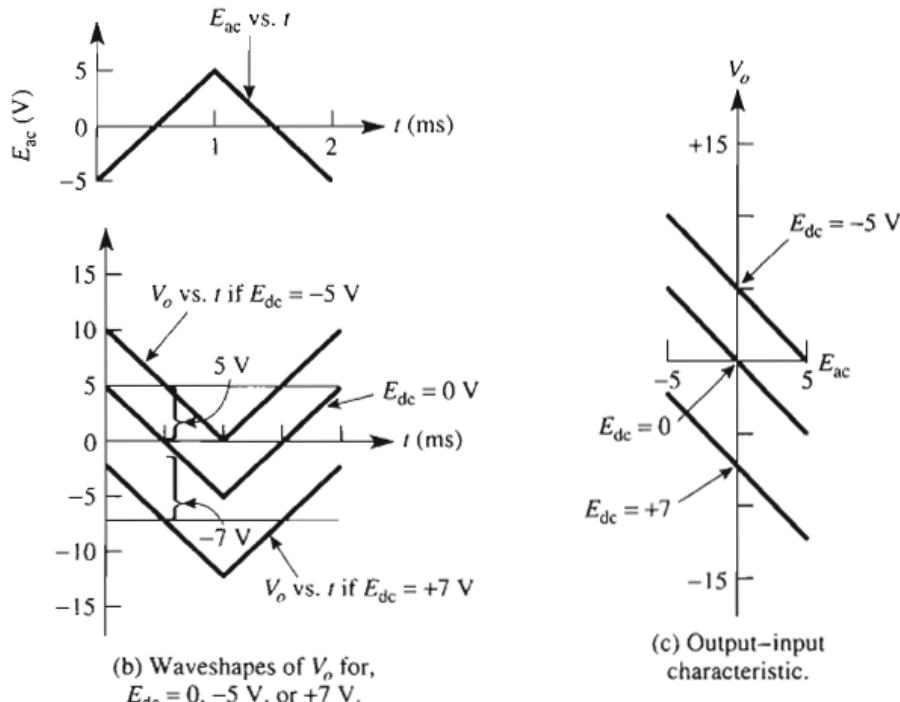


FIGURE 3-5 E_{ac} is transmitted with a gain of -1 . If E_{dc} is *positive*, the average (dc) value of V_o is shifted *negative* by the same value.

Circuit analysis. If E_{dc} is 0 V , E_{ac} appears inverted at V_o (gain is -1) [see Figs. 3-5(b) and (c)]. If E_{dc} is -5 V , it appears at the output as a $+5\text{-V}$ dc offset voltage upon which rides the inverted E_{ac} . If E_{dc} is $+7\text{ V}$, then E_{ac} is shifted *down* by 7 V . Most function generators contain this type of circuit. We will return to this circuit in Section 3-12 to design a signal conditioning circuit that interfaces between a temperature sensor and a microcontroller.

3-3 MULTICCHANNEL AMPLIFIER

3-3.1 The Need for a Multichannel Amplifier

Suppose you had low-, medium-, and high-level signal sources. You need to combine them and make their relative amplitudes reasonably equal. You can use a three-input adder circuit to combine the signals. The versatile adder circuit will also allow you to equalize the signal amplitudes at its output. Simply design the required gain for each input channel by the selection of R_f and input resistors R_1 , R_2 , and R_3 as shown in Fig. 3-6.

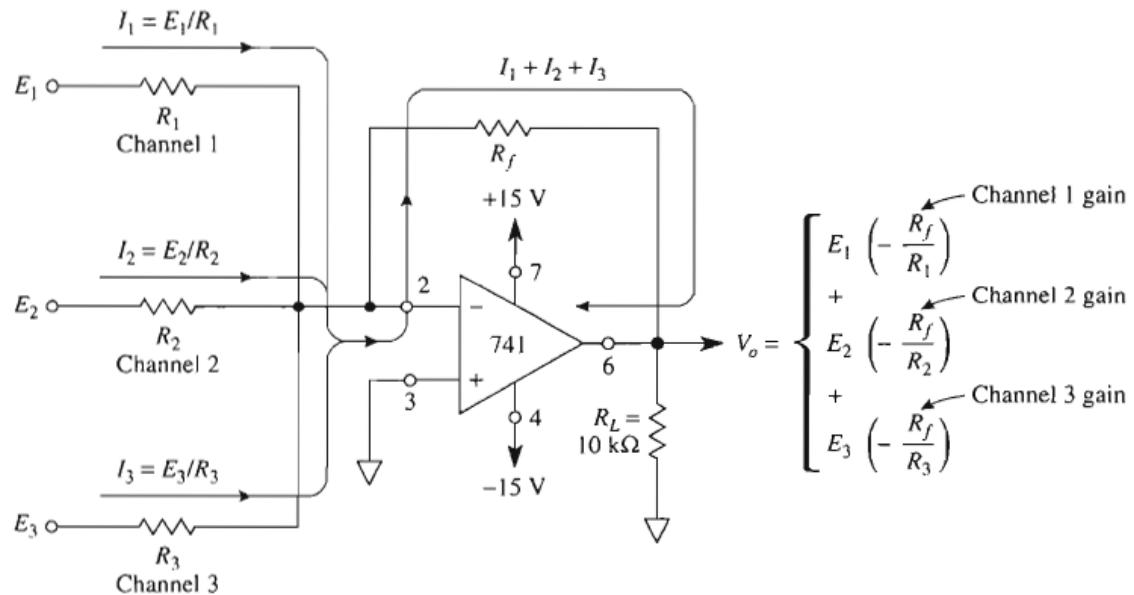


FIGURE 3-6 Multichannel amplifier. The inverting voltage gain of each channel depends on the values of its input resistor and R_f .

3-3.2 Circuit Analysis

As shown in Fig. 3-6, each channel input signal sees its associated input resistor connected to a virtual ground at the op amp's (−) input. Therefore, the input resistance of each channel is equal to the corresponding value selected for R_1 , R_2 , or R_3 .

Input currents I_1 , I_2 , and I_3 are added in feedback resistor R_f and then converted back to a voltage V_{R_f}

$$V_{R_f} = (I_1 + I_2 + I_3)R_f \quad (3-6a)$$

where

$$I_1 = \frac{E_1}{R_1}, \quad I_2 = \frac{E_2}{R_2}, \quad I_3 = \frac{E_3}{R_3} \quad (3-6b)$$

As was shown in Section 3-2.1, output voltage $V_o = -V_{R_f}$. Therefore,

$$V_o = - \left(E_1 \frac{R_f}{R_1} + E_2 \frac{R_f}{R_2} + E_3 \frac{R_f}{R_3} \right) \quad (3-7a)$$

Equation (3-7a) shows that the gain of each channel can be changed independently of the others by simply changing its input resistor.

$$A_{CL_1} = - \frac{R_f}{R_1}, \quad A_{CL_2} = - \frac{R_f}{R_2}, \quad A_{CL_3} = - \frac{R_f}{R_3} \quad (3-7b)$$

or

$$V_o = E_1 A_{CL_1} + E_2 A_{CL_2} + E_3 A_{CL_3}$$

3-3.3 Design Procedure

Following is an example of the design procedure for a multichannel amplifier.

Design Example 3-11

Design a three-channel inverting amplifier. The gains for each channel will be

Channel number	Voltage gain
1	-10
2	-5
3	-2

Design Procedure

1. Select a 10-k Ω resistor for the input resistance of the channel with the *highest* gain. Choose $R_1 = 10$ k Ω since A_{CL_1} is the largest.
2. Calculate feedback resistor R_f from Eq. (3-7b):

$$A_{CL_1} = - \frac{R_f}{R_1}, \quad -10 = - \frac{R_f}{10 \text{ k}\Omega}, \quad R_f = 100 \text{ k}\Omega$$

3. Calculate the remaining input resistors from Eq. (3-7b) to get $R_2 = 20$ k Ω and $R_3 = 50$ k Ω .

3-4 INVERTING AVERAGING AMPLIFIER

Suppose that you had to measure the average temperature at three locations in a dwelling. First make three temperature-to-voltage converters (shown in Section 5-14). Then connect their outputs to an *averaging* amplifier. An *averaging* amplifier gives an output voltage

proportional to the average of all the input voltages. If there are three input voltages, the averager should add the input voltages and divide the sum by 3. The averager is the same circuit arrangement as the inverting adder in Fig. 3-4 or the inverting adder with gain in Fig. 3-6. The difference is that the input resistors are made equal to some convenient value R and the feedback resistor is made equal to R divided by the number of inputs. Let n equal the number of inputs. Then for a three-input averager, $n = 3$ and $R_f = R/3$. Proof is found by substituting into Eq. (3-7a), for $R_f = R/3$ and $R_1 = R_2 = R_3 = R$ to show that

$$V_o = - \left(\frac{E_1 + E_2 + E_3}{n} \right) \quad (3-8)$$

Example 3-12

In Fig. 3-4, $R_1 = R_2 = R_3 = R = 100 \text{ k}\Omega$ and $R_f = 100 \text{ k}\Omega/3 \approx 33 \text{ k}\Omega$. If $E_1 = +5 \text{ V}$, $E_2 = +5 \text{ V}$, and $E_3 = -1 \text{ V}$, find V_o .

Solution Since $R_f = R/3$, the amplifier is an averager, and from Eq. (3-8) with $n = 3$, we have

$$V_o = - \left[\frac{5 \text{ V} + 5 \text{ V} + (-1 \text{ V})}{3} \right] = - \frac{9 \text{ V}}{3} = -3 \text{ V}$$

Up to now we have dealt with amplifiers whose input signals were applied via R_i to the op amp's inverting input. We turn our attention next to amplifiers in which E_i is applied directly to the op amp's noninverting input.

3-5 NONINVERTING AMPLIFIER

3-5.1 Circuit Analysis

Figure 3-7 is a noninverting amplifier; that is, the output voltage, V_o , is the same polarity as the input voltage, E_i . The input resistance of the inverting amplifier (Section 3-1) is R_i , but the input resistance of the noninverting amplifier is extremely large, typically exceeding $100 \text{ M}\Omega$. Since there is practically 0 voltage between the (+) and (-) pins of the op amp, both pins are at the same potential E_i . Therefore, E_i appears across R_1 . E_i causes current I to flow as given by

$$I = \frac{E_i}{R_1} \quad (3-9a)$$

The direction of I depends on the polarity of E_i . Compare Figs. 3-7(a) and (b). The input current to the op amp's (-) terminal is negligible. Therefore, I flows through R_f and the voltage drop across R_f is represented by V_{R_f} and expressed as

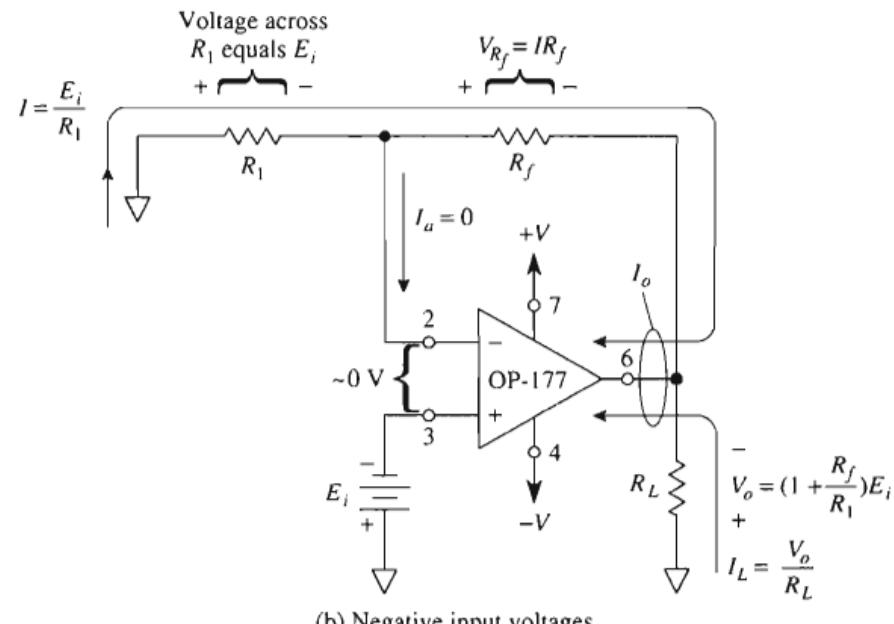
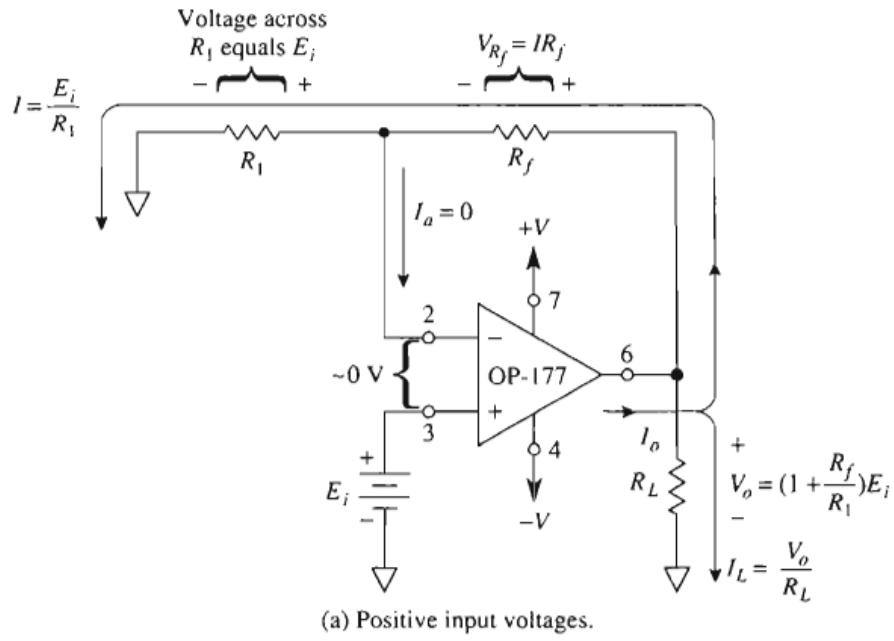


FIGURE 3-7 Voltage polarities and direction of currents for noninverting amplifiers.

$$V_{R_f} = I (R_f) = \frac{R_f}{R_1} E_i \quad (3-9b)$$

Equations (3-9a) and (3-9b) are similar to Eqs. (3-1a) and (3-1b).

The output voltage V_o is found by adding the voltage drop across R_1 , which is E_i , to the voltage across R_f , which is V_{R_f} :

$$V_o = E_i + \frac{R_f}{R_1} E_i$$

or

$$V_o = \left(1 + \frac{R_f}{R_1}\right) E_i \quad (3-10a)$$

Rearranging Eq. (3-10a) to express voltage gain, we get

$$A_{CL} = \frac{V_o}{E_i} = 1 + \frac{R_f}{R_1} = \frac{R_f + R_1}{R_1} \quad (3-10b)$$

Equation (3-10b) shows that the voltage gain of a noninverting amplifier is always greater than 1.

The load current I_L is given by V_o/R_L and therefore depends only on V_o and R_L . I_o is the op amp's output current and is given by Eq. (3-3).

Example 3-13

(a) Find the voltage gain for the noninverting amplifier of Fig. 3-8. If E_i is a 100-Hz triangle wave with a 2-V peak, plot (b) V_o vs. t ; (c) V_o vs. E_i .

Solution (a) From Eq. (3-10b),

$$A_{CL} = \frac{R_f + R_1}{R_1} = \frac{(40 + 10) \text{ k}\Omega}{10 \text{ k}\Omega} = 5$$

(b) See Fig. 3-8(b). These are the waveshapes that would be seen on a dc-coupled, dual-trace oscilloscope.

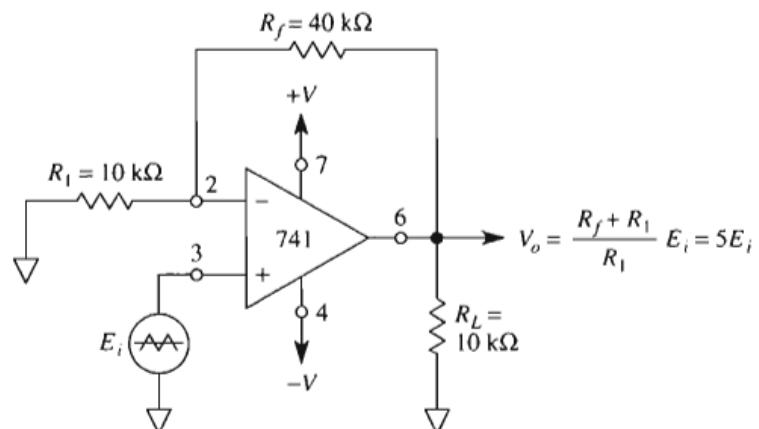
(c) See Fig. 3-8(c). Set an oscilloscope for an x - y display, vertical 5 V/div, horizontal 1 V/div. Note that the slope rises to the right and is positive. Rise over run gives you the gain magnitude of +5.

3-5.2 Design Procedure

Following is an example of the design procedure for a noninverting amplifier.

Design Example 3-14

Design an amplifier with a gain of +10.



(a) Noninverting amplifier circuit with gain of +5.

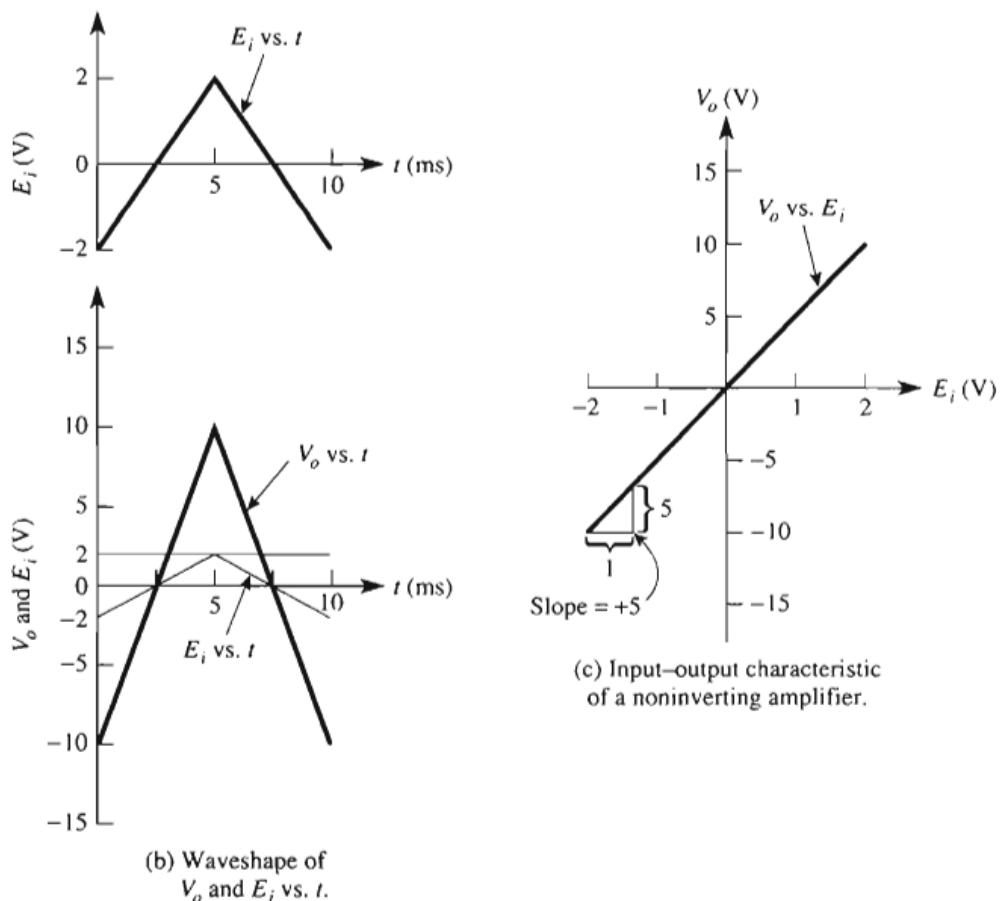


FIGURE 3-8 Noninverting amplifier circuit analysis for Example 3-13.

Design Procedure

1. Since the gain is positive, select a noninverting amplifier. That is, we apply E_i to the op amp's (+) input.
2. Choose $R_1 = 10 \text{ k}\Omega$.
3. Calculate R_f from Eq. (3-10b).

$$A_{CL} = 1 + \frac{R_f}{R_1}, \quad 10 = 1 + \frac{R_f}{10 \text{ k}\Omega}, \quad R_f = 9(10 \text{ k}\Omega) = 90 \text{ k}\Omega$$

3-6 VOLTAGE FOLLOWER

3-6.1 Introduction

The circuit of Fig. 3-9 is called a *voltage follower*, but it is also referred to as a *source follower*, *unity-gain amplifier*, *buffer amplifier*, or *isolation amplifier*. It is a special case of the noninverting amplifier. The input voltage, E_i , is applied directly to the (+) input. Since the voltage between (+) and (−) pins of the op amp can be considered 0,

$$V_o = E_i \quad (3-11a)$$

Note that the output voltage equals the input voltage in both magnitude and sign. Therefore, as the name of the circuit implies, the output voltage *follows* the input or source voltage. The voltage gain is 1 (or unity), as shown by

$$A_{CL} = \frac{V_o}{E_i} = 1 \quad (3-11b)$$

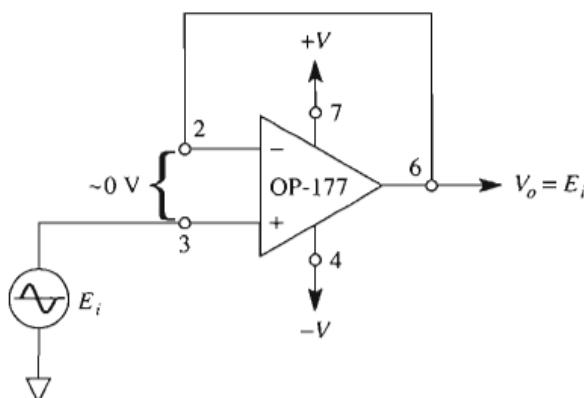


FIGURE 3-9 Voltage follower.

Example 3-15

For Fig. 3-10(a), determine (a) V_o ; (b) I_L ; (c) I_o .

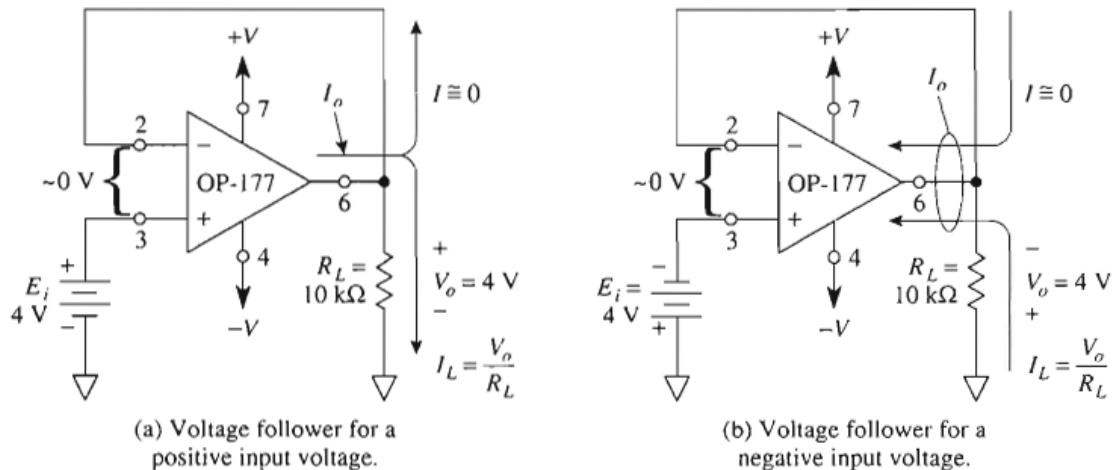


FIGURE 3-10 Circuits for Example 3-15.

Solution (a) From Eq. (3-11a),

$$V_o = E_i = 4 \text{ V}$$

(b) From Ohm's law,

$$I_L = \frac{V_o}{R_L} = \frac{4 \text{ V}}{10 \text{ k}\Omega} = 0.4 \text{ mA}$$

(c) From Eq. (3-3),

$$I_o = I + I_L$$

This circuit is still a negative-feedback amplifier because there is a connection between output and (−) input. Remember that it is negative feedback that forces E_d to be 0 V. Also $I \approx 0$, since input terminals of op amps draw negligible current; therefore,

$$I_o = 0 + 0.4 \text{ mA} = 0.4 \text{ mA}$$

If E_i were reversed, the polarity of V_o , the direction of currents would be reversed, as shown in Fig. 3-10(b).

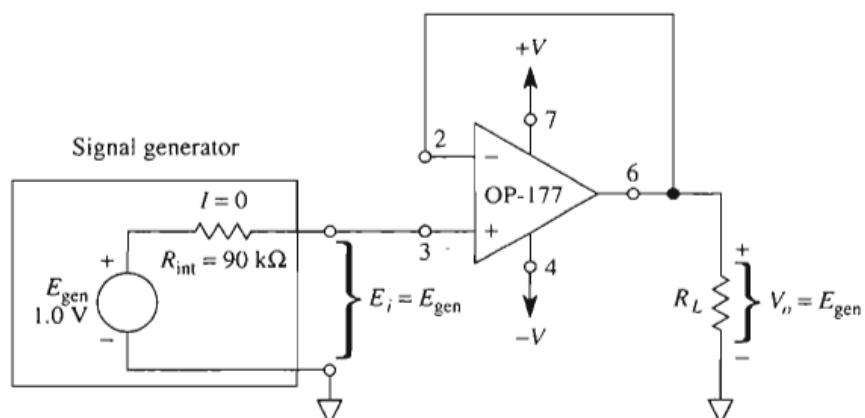
3-6.2 Using the Voltage Follower

A question that arises quite often is “Why bother to use an amplifier with a gain of 1?” The answer is best seen if we compare a voltage follower with an inverting amplifier. In

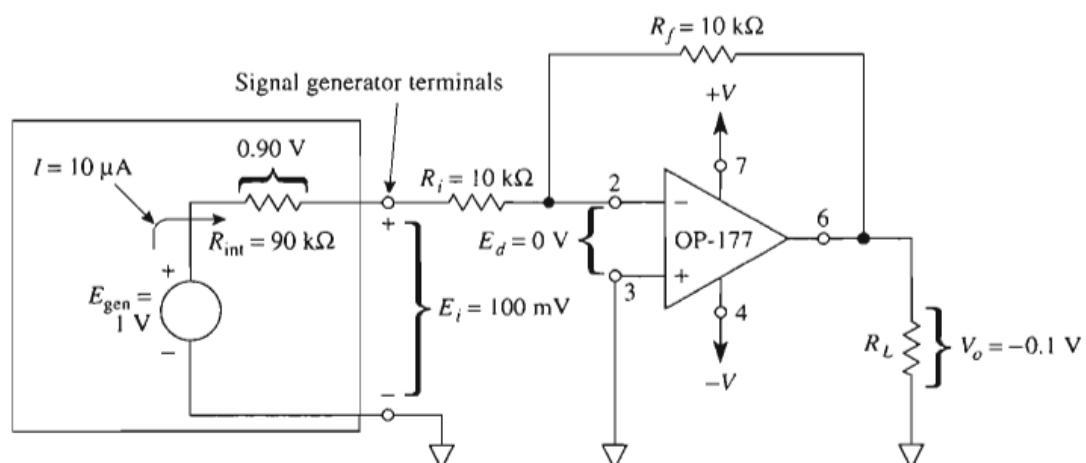
in this example, we are not primarily concerned with the polarity of voltage gain but rather with the input loading effect.

The voltage follower is used because its input resistance is high (many megohms). Therefore, it draws negligible current from a signal source. For example, in Fig. 3-11(a) the signal source has an open circuit or generator voltage, E_{gen} , of 1.0 V. The generator's internal resistance is $90 \text{ k}\Omega$. Since the input terminal of the op amp draws negligible current, the voltage drop across R_{int} is 0 V. The terminal voltage E_i of the signal source becomes the input voltage to the amplifier and equals E_{gen} . Thus

$$V_o = E_i = E_{\text{gen}}$$



(a) Essentially no current is drawn from E_{gen} .
The output terminal of the op amp can supply up to 5 mA with a voltage held constant at E_{gen} .



(b) E_{gen} divides between its own internal resistance and amplifier input resistance.

FIGURE 3-11 Comparison of loading effect between an inverting amplifier and a voltage follower on a high-resistance source.

Now let us consider the same signal source connected to an inverting amplifier whose gain is -1 [see Fig. 3-11(b)]. As stated in Section 3-1.3, the input resistance to an inverting amplifier is R_i . This causes the generator voltage E_{gen} to divide between R_{int} and R_i . Using the voltage division law to find the generator terminal voltage E_i yields

$$E_i = \frac{R_i}{R_{\text{int}} + R_i} \times E_{\text{gen}} = \frac{10 \text{ k}\Omega}{10 \text{ k}\Omega + 90 \text{ k}\Omega} \times (1.0 \text{ V}) = 0.1 \text{ V}$$

Thus it is this 0.1 V that becomes the input voltage to the inverting amplifier. If the inverting amplifier has a gain of only -1 , the output voltage V_o is -0.1 V .

In conclusion, if a high-impedance source is connected to an inverting amplifier, the voltage gain from V_o to E_{gen} is not set by R_f and R_i as given in Eq. (3-2b). The actual gain must include R_{int} , as

$$\frac{V_o}{E_{\text{gen}}} = - \frac{R_f}{R_i + R_{\text{int}}} = - \frac{10 \text{ k}\Omega}{100 \text{ k}\Omega} = - 0.1$$

If you must amplify and invert a signal from a high-impedance source and wish to draw no signal current, first *buffer* the source with a voltage follower. Then feed the follower's output into an inverter. If you need buffering and do not want to invert the input signal, use the noninverting amplifier.

3-7 THE "IDEAL" VOLTAGE SOURCE

3-7.1 Definition and Awareness

The ideal voltage source is first encountered in textbooks concerned with fundamentals. By definition, the voltage does not vary regardless of how much current is drawn from it. You may not be aware of the fact that you create a perfect voltage source when you measure the frequency response of an amplifier or filter. We explain how this apparently perfect performance comes about in the next section.

3-7.2 The Unrecognized Ideal Voltage Source

The lab or field procedure typically goes like this: Set the input signal amplitude at 0.2 V rms and frequency at the lowest limit. Measure output V_o . Hold E_{in} at 0.2 V rms for each measurement. Plot V_o or V_o/E_{in} versus frequency. As you dial higher frequencies, E_{in} begins to decrease (because of input capacitance loading). You automatically increase the function generator's volume control to hold E_{in} at 0.2 V . You have just, by definition, created an "ideal" voltage source. E_{in} never varied throughout the test sequence no matter how much current was drawn from it. This is an example of the unrecognized ideal voltage source.

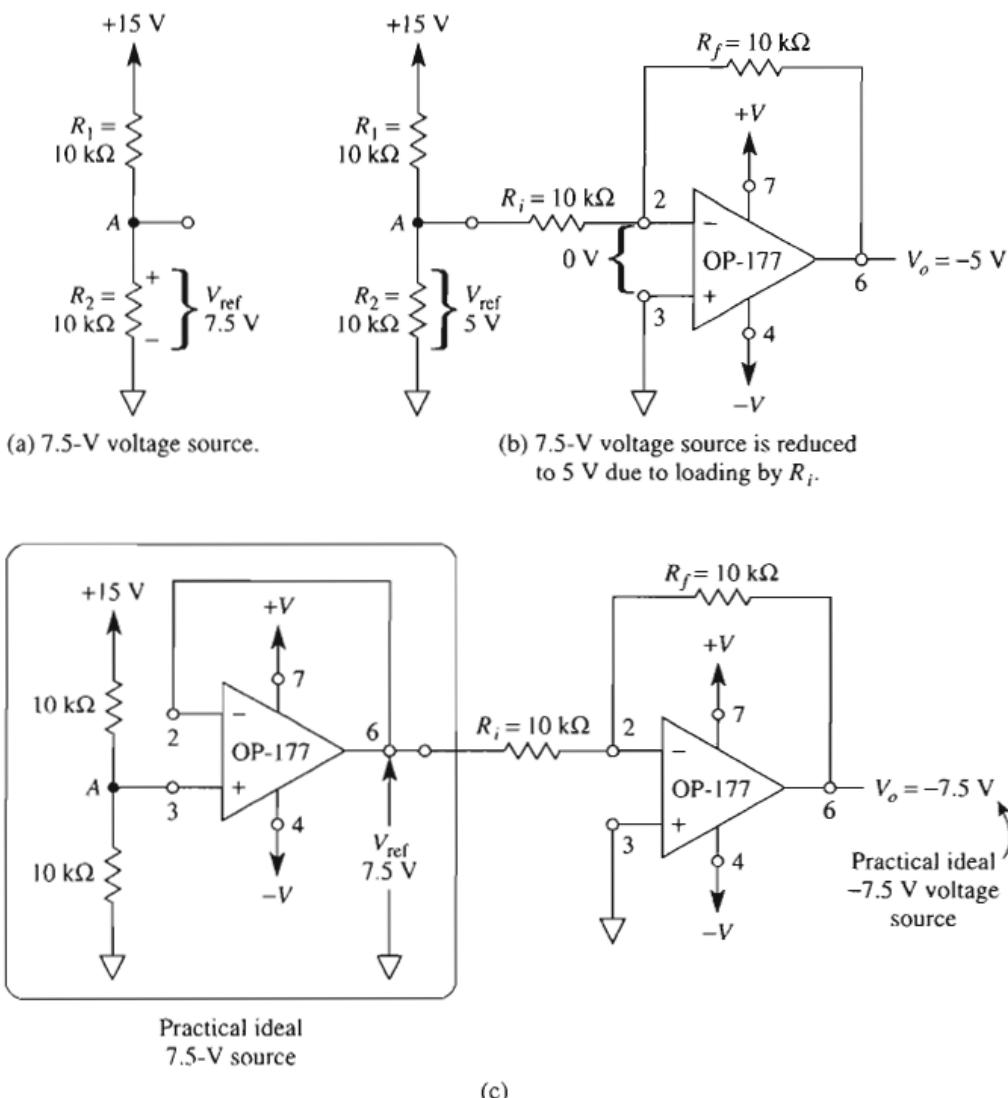


FIGURE 3-12 A voltage divider and (+) supply voltage gives a 7.5-V test or reference voltage in (a). V_{ref} drops to 5 V in (b) when connected to an inverter. A voltage follower converts the voltage divider into an ideal voltage source in (c).

3-7.3 The Practical Ideal Voltage Source

A circuit schematic shows a battery symbol labeled -7.5 V . Your job is to make one. The convenient $+15 \text{ V}$ supply voltage is available, and a simple voltage divider network gives 7.5 V as shown in Fig. 3-12(a). This 7.5 V source is fine as long as you never use it by connecting a load.

As shown in Fig. 3-12(b), R_i of the inverter appears in parallel with R_2 to form an equivalent resistance of $10 \text{ k}\Omega \parallel 10 \text{ k}\Omega = 5 \text{ k}\Omega$. The 15 V supply divides between $R_1 = 10 \text{ k}\Omega$ and $5 \text{ k}\Omega$, and V_{ref} drops to 5 V .

To preserve the value of any reference voltage, simply *buffer* it with a voltage follower. The 7.5-V reference voltage is connected to a voltage follower in Fig. 3-12(c). The output of the follower equals V_{ref} . You can extract up to 5 mA from the follower's output with no change in V_{ref} .

The buffer makes an excellent clandestine bug. You can monitor what is going on at any circuit point. Since a follower has a high input impedance, it draws negligible current from the circuit. Therefore, it is nearly impossible to detect.

3-7.4 Precise Voltage Sources

Section 2-6 introduced precision voltage reference ICs such as the REF-02 (a precision +5-V reference chip). You can use these voltage reference chips with an inverting amplifier to create precise negative voltages as well as positive and negative voltages. The circuit of Figure 3-13(a) shows how a negative voltage of -5 V can be created using the REF-02 and an inverting amplifier. This circuit has a lower parts count and more precision than the circuit of Figure 3-12(c). The parts count is obvious, and the precision is obtained by the REF-02 in place of R_i and R_f . Consider R_i and R_f to be 1% resistors. Then there is a possibility that one resistor could be $+1\%$ while the other is -1% . This will produce an output voltage with a 2% error, which may not be acceptable for your design.

Another application using the REF-02 with an inverting amplifier is shown in Figure 3-13(b). This circuit creates a ± 5 -V source from a single REF-02 chip and an inverting amplifier.

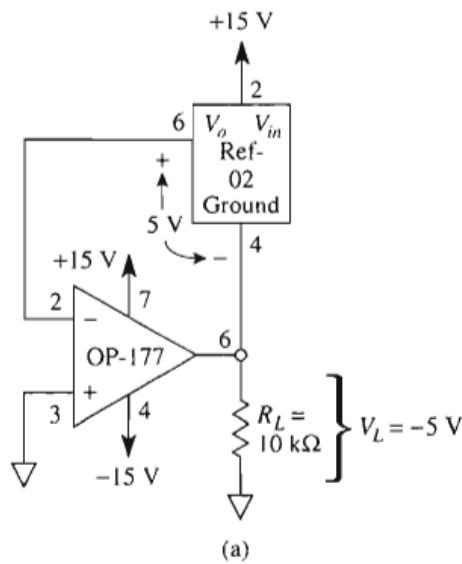
3-8 NONINVERTING ADDER

A three-input noninverting adder is constructed with a passive averager and noninverting amplifier as shown in Fig. 3-14(a). The passive averager circuit consists of three equal resistors R_A and the three voltages to be added. The output of the passive averager is E_{in} , where E_{in} is the average of E_1 , E_2 , and E_3 , or $E_{\text{in}} = (E_1 + E_2 + E_3)/3$. Connect a voltage follower to E_{in} if you need a noninverting averager (in contrast with Sec. 3-4).

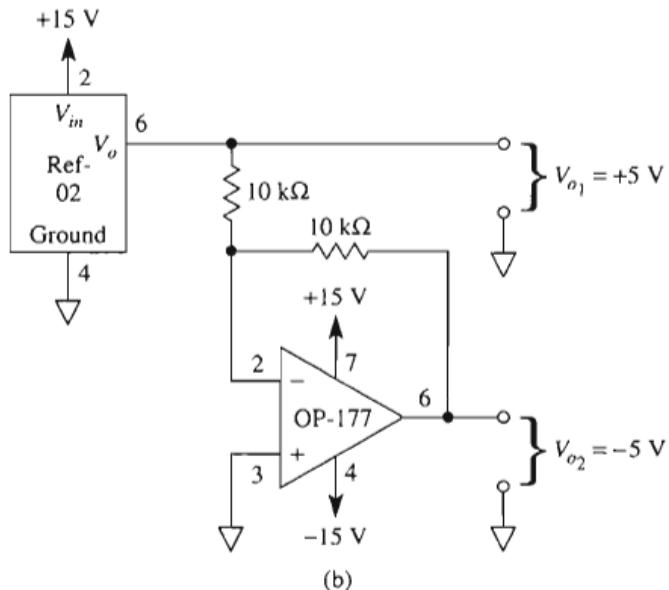
Output V_o results from amplifying E_{in} by a gain equal to the number of inputs n . In Fig. 3-14(a), $n = 3$. Design the amplifier by choosing a convenient value for resistor R . Then find R_f from

$$R_f = R(n - 1) \quad (3-12)$$

As shown in Fig. 3-14(a), the value for R_f should be $R_f = 10 \text{ k}\Omega(3 - 1) = 20 \text{ k}\Omega$. If E_1 , E_2 , and E_3 are not ideal voltage sources, such as a battery or output of an op amp, buffer them with followers as in Fig. 3-14(b).



(a)

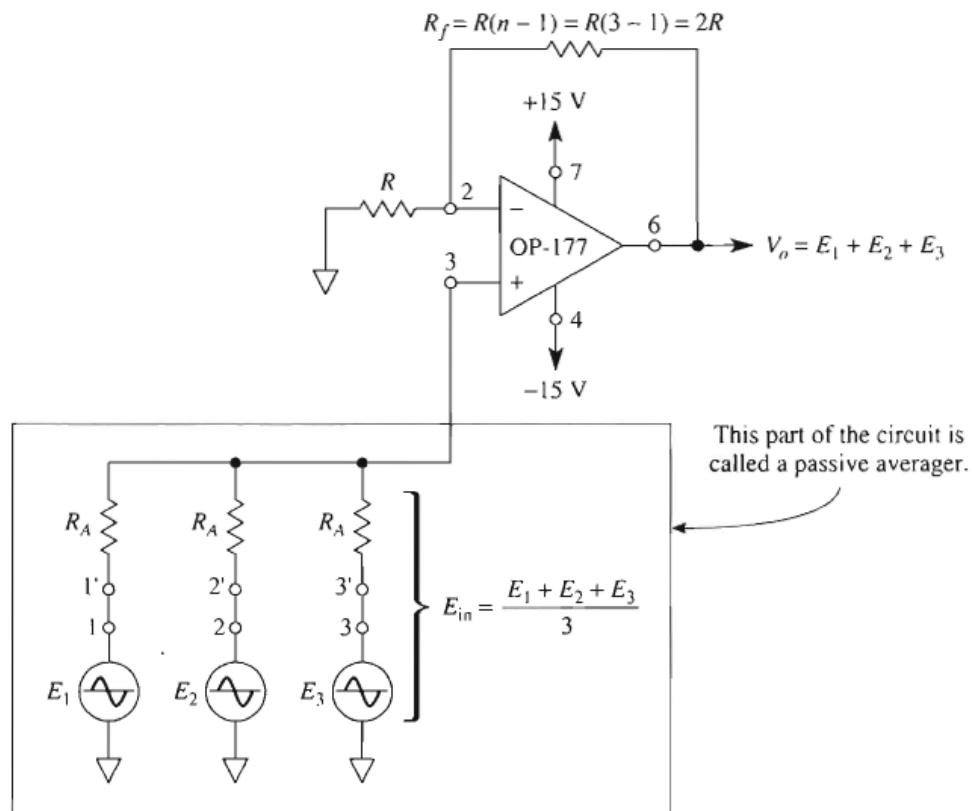


(b)

FIGURE 3-13 (a) A -5 V precision output voltage; (b) a $\pm 5\text{ V}$ output voltage.

3-9 SINGLE-SUPPLY OPERATION

Some amplifier designs require battery-powered operation and output voltage swings to within millivolts of the supply voltages. Thus, you want an op amp described by manufacturers as a device capable of single-supply and rail-to-rail operation. Two such devices are the AD820 and the OP-90 from Analog Devices. These op amps can operate from either a single or dual supply. For example, the AD820 can operate from a dual supply



(a) Noninverting adder.

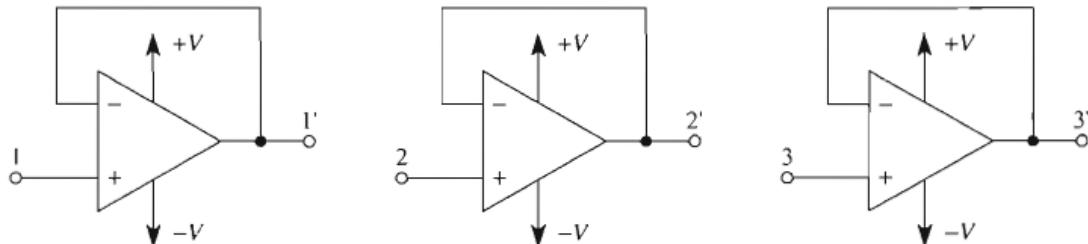
(b) If E_1 , E_2 , and E_3 are not ideal voltage sources, simply buffer each one with a voltage follower.

FIGURE 3-14 All resistors of an n -input noninverting adder are equal except the feedback resistor; choose $R = 10 \text{ k}\Omega$ and $R_A = 10 \text{ k}\Omega$. Then R_f equals R times the number of inputs minus one: $R_f = R(n - 1)$.

($\pm 1.5 \text{ V}$ to $\pm 18 \text{ V}$) or from a single supply ($+3 \text{ V}$ to $+36 \text{ V}$). The input signal applied to these devices can be brought to ground, and the output can swing to within 10 mV of either supply voltage. They are available in an 8-pin mini-DIP package with the same pinouts as the 741 or OP-177 op amps. Single-supply op amps are often used in battery-powered applications, portable instruments, medical instrumentation, and data acquisition units. Often they are used to amplify positive signals coming from sensors such as strain

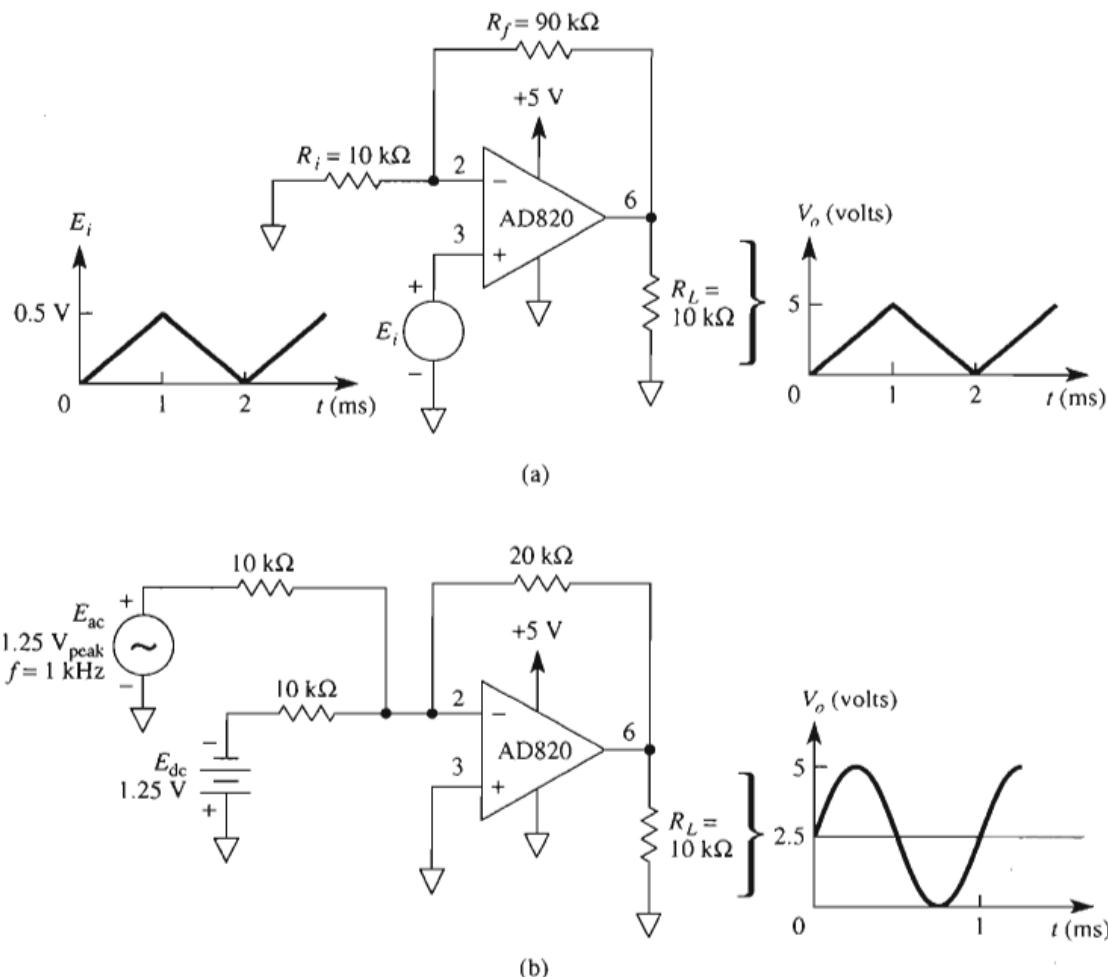


FIGURE 3-15 The AD820 can operate for single-supply applications as shown in (a) and (b).

gages or thermocouples. Figure 3-15(a) shows the AD820 wired as a noninverting amplifier with a gain of 10. If you are operating the AD820 from a single supply and want to amplify an ac signal, then the input ac signal has to have a dc offset or be combined with a dc voltage as shown in Figure 3-15(b). (Note: This circuit is similar to the inverting adder studied in Figure 3-5(a) but now operated from a single supply.)

3-10 DIFFERENCE AMPLIFIERS

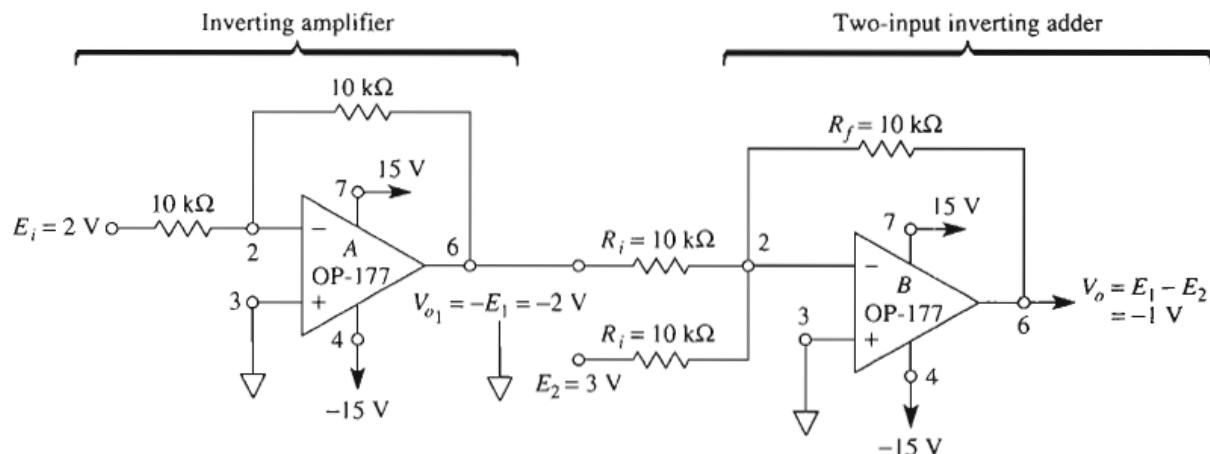
The differential amplifier and its more powerful relative, the instrumentation amplifier, will be studied in Chapter 8. However, as other applications of inverting and noninverting amplifiers, we offer two examples of the *difference* amplifier in this section and the design of a signal conditioning circuit for a temperature sensor in the next.

3-10.1 The Subtractor

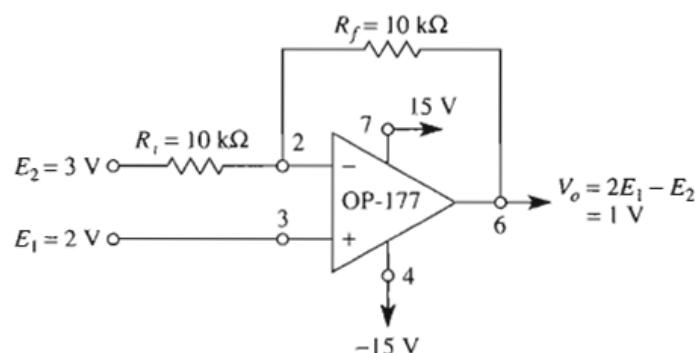
A circuit that takes the difference between two signals is called a *subtractor* [see Fig. 3-16(a)]. It is made by connecting an inverting amplifier to a two-input inverting averager. To analyze this circuit, note that E_i is transmitted through op amp A with a gain of -1 and appears as $V_{o_1} = -E_1$. V_{o_1} is then inverted (times -1) by the top channel of the inverting amplifier B . Thus E_1 is inverted once by op amp A and again by op amp B to appear at V_o as E_1 .

E_2 is inverted by the bottom channel of op amp B and drives V_o to $-E_2$. Thus V_o responds to the difference between E_1 and E_2 , or

$$V_o = E_1 - E_2 \quad (3-13a)$$



(a) An inverting amplifier and a two-input inverting adder make a subtractor. $V_o = E_1 - E_2$.



(b) Both amplifier inputs are used to make an amplifier that calculates the difference between $2E_1$ and E_2 .

optionally check this

FIGURE 3-16 Two examples of difference amplifiers are the subtractor in (a) and using the op amp as both an inverting and a noninverting amplifier in (b).

As shown in Fig. 3-16(a), for $E_1 = 2$ V and $E_2 = 3$ V, $V_o = 2 - 3 = -1$ V. If the value of R_f is made larger than R_i , the subtractor will have gain

$$V_o = \frac{R_f}{R_i} (E_1 - E_2) \quad (3-13b)$$

3-10.2 Inverting–Noninverting Amplifier

In Fig. 3-16(b), signal E_1 is applied to the amplifier's noninverting input and signal E_2 is applied to the inverting input. We will use superposition to analyze this circuit. First remove E_2 and replace it by a ground. E_1 sees a noninverting amplifier with a gain of $(R_f + R_i)/R_i$, or 2. Thus E_1 alone drives V_o to $2E_1$. Next reconnect E_2 and replace E_1 by a ground. E_2 sees an inverting amplifier with a gain of -1 . E_2 drives V_o to $-E_2$. When both E_1 and E_2 are connected, V_o is given by

$$V_o = 2E_1 - E_2 \quad (3-14)$$

As shown in Fig. 3-16(b), $V_o = 1$ V when $E_1 = 2$ V and $E_2 = 3$ V.

We will now show how to design the subtractor circuit of Fig. 3-16(a) to be the analog interface circuitry connected between a temperature sensor and the analog–digital converter of a microcontroller. This analog interface circuit is also known as a signal conditioning circuit.

3-11 DESIGNING A SIGNAL CONDITIONING CIRCUIT*

Another way of viewing the circuit in Fig. 3-5(a) (redrawn in Figure 3-17 for convenience) is that it allows us to design a signal conditioning circuit (SCC) for a microcontroller application that satisfies the equation of a straight line, $y = mx + b$. This equation occurs quite often when designing SCCs. Comparing the equation of $y = mx + b$ to the circuit of Fig. 3-17, the y term is the output voltage, V_o ; the x term is the input signal voltage, E_i ; the m term is the gain of the circuit, R_f/R_1 ; and the b term is R_f/R_2 times E_{dc} . Therefore, if your application uses a sensor that generates an output signal measured with respect to ground, which must be amplified and offset, then an SCC similar to Fig. 3-17 may be used. (Note: The outputs of some sensors generate a differential output, and these devices require an SCC capable of measuring a differential voltage. Such circuits are studied in Chapter 8.) The design of any SCC unit requires obtaining the equation of the circuit. This equation is obtained from what you've got (the output conditions of the sensor) to what you want (the input conditions of the microcontroller's A/D converter). Let us study this topic.

Statement of the problem. Design a signal conditioning circuit to interface between a temperature sensor and the A/D converter of a microcontroller. The tempera-

* For more examples of the linear circuit design procedure refer to *Data Acquisition and Process Control with the M68HC11 Microcontroller*, 2nd Ed. by F. Driscoll, R. Coughlin, and R. Villanucci, Prentice Hall (2000).

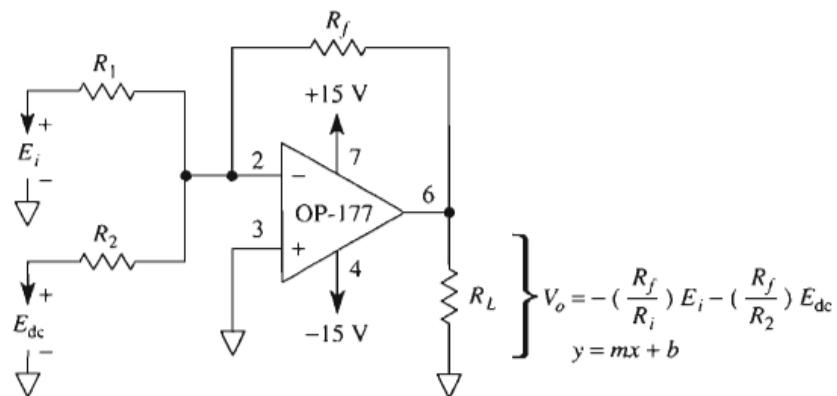


FIGURE 3-17 The inverting summer can be designed to satisfy the equation of a straight line, $y = mx + b$.

ture range to be measured is 0° to 50°C , and the range of the A/D converter is from 0 to 5 V. You want the output of the SCC to be linear; that is, when the sensor is measuring 0°C , the output of the SCC is 0 V; when the sensor is measuring 10°C , the SCC's output is to be 1 V; and so forth up to 50°C , at which temperature the SCC outputs 5 V.

Solution. Although our goal is to design the SCC, which is an op amp circuit, our starting point is the sensor and writing an equation for it, because the output of the sensor is the input to the SCC. Therefore, once the sensor is picked, this is what you've *got*. What you *want* is the output of the SCC to fit the range of the microcontroller's A/D converter. Therefore, the SCC design is being squeezed between what you've *got* and what you *want*. Let's first learn about one type of temperature sensor and how to write the equation for it.

Introduction to a temperature sensor. For this application, we shall choose the LM335, which is a solid-state temperature sensor that belongs to a family of devices that has a sensitivity of $10 \text{ mV}/^\circ\text{K}$. It is used in applications that require measuring temperatures from -10° to 100°C and is modeled as a two-terminal zener. The package style and model are shown in Figures 3-18(a) and (b), respectively. This device is capable of operating over a current range of from $400 \mu\text{A}$ to 5 mA . The data sheet for the LM335 gives the device's sensitivity as $10 \text{ mV}/^\circ\text{K}$. However, our application is to measure degrees Celsius. The relationship between degrees Kelvin and degrees Celsius is: A 1-degree rise in Kelvin equals a 1-degree rise in Celsius, and the freezing point of water is 0°C , which equals 273°K .

Writing an equation that describes the sensor. A plot of the output voltage of the LM335 versus temperature is given in Figure 3-18(c). The slope of the line is the device's sensitivity— $10 \text{ mV}/^\circ\text{K}$. Therefore, in terms of $^\circ\text{K}$ the output voltage is

$$V_T = (10 \text{ mV}/^\circ\text{K}) (T_{in^\circ\text{K}}) \quad (3-15)$$

where T is the temperature in $^\circ\text{K}$. At 273°K (0°C), the sensor's output voltage is

$$V_T = (10 \text{ mV}/^\circ\text{K}) (273^\circ\text{K}) = 2.73 \text{ V}$$

as shown in Figure 3-18(c).

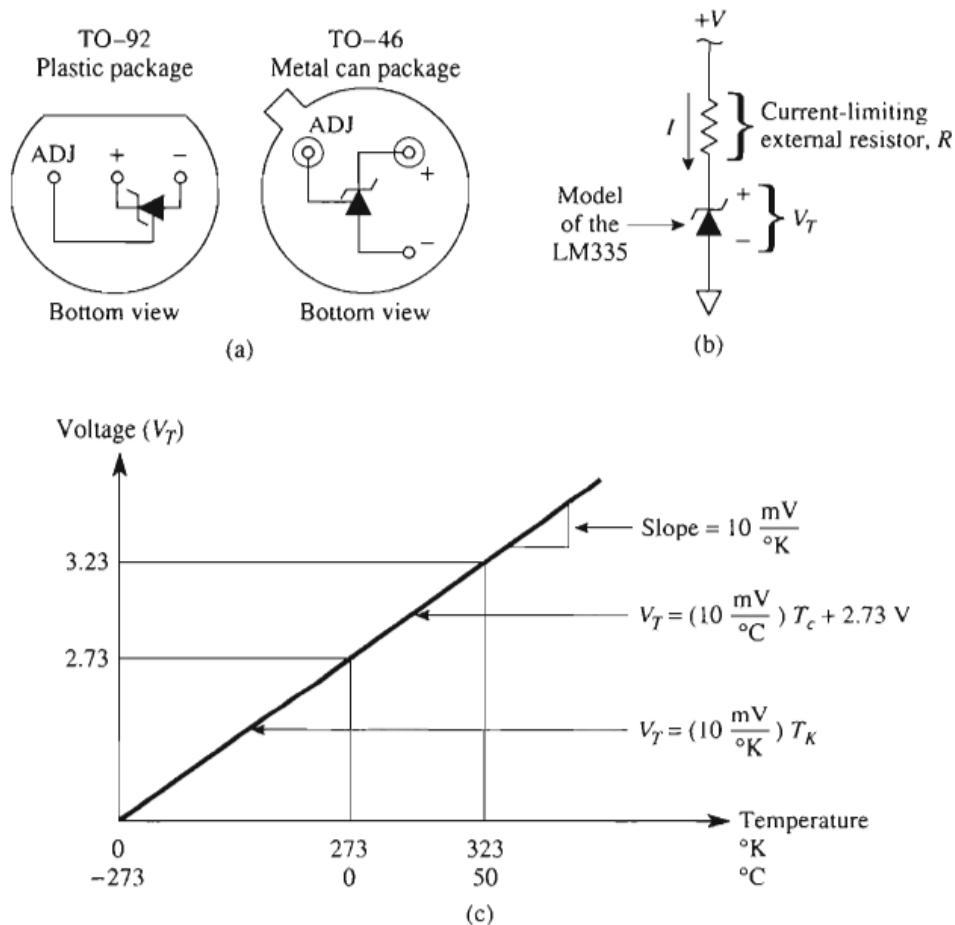


FIGURE 3-18 The LM335 (a) package styles, (b) model, and (c) voltage versus temperature characteristic.

Now the sensor's output voltage can be written in terms of degrees Celsius as

$$V_T = (10 \text{ mV/}^{\circ}\text{C}) (T_{\text{in}}^{\circ}\text{C}) + 2.73 \text{ V} \quad (3-16)$$

where T is the temperature in degrees Celsius. For our application, at 0°C $V_T = 2.73 \text{ V}$ and at 50°C $V_T = 3.23 \text{ V}$. This is the input voltage range for the SCC. The output range of the SCC is the input range of the A/D converter, which is 0 V to 5 V. Figure 3-19 shows a block diagram of this data acquisition system for measuring temperature.

Writing an equation that describes the SCC. From the information we know about the sensor and the A/D converter, we can plot the output/input characteristics of the SCC. Figure 3-19 includes such a plot. The output values of the SCC are plotted on the y-axis. Remember, these values are the voltage range of the A/D converter—0 V to 5 V. The input values to the SCC are plotted on the x-axis. These values are the voltage range of the sensor—2.73 V to 3.23 V for this application.

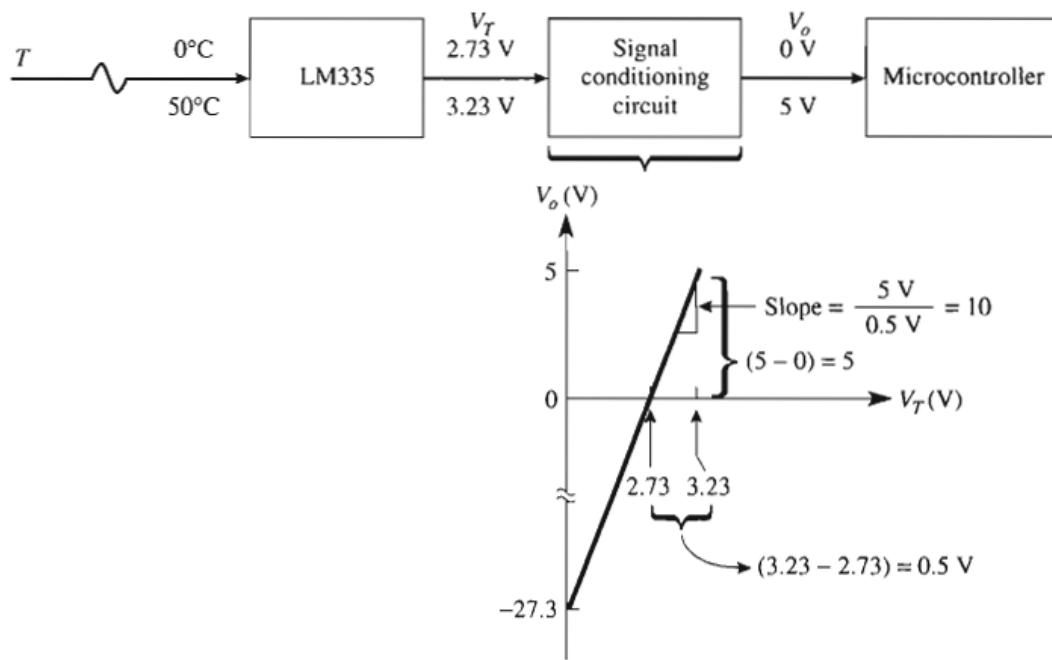


FIGURE 3-19 Block diagram of a temperature measuring system and the desired output–input characteristics of the SCC.

The slope of the line is

$$m = \frac{(5 - 0)\text{ V}}{(3.23 - 2.73)\text{ V}} = 10 = \frac{\Delta V_o}{\Delta V_T} \quad (3-17)$$

This value of 10 is the gain that V_T must be multiplied by. The dc offset is found from choosing a point on the line and substituting into the equation of a straight line— $y = mx + b$. Choosing the coordinate pair $(2.73, 0)$, we obtain

$$0 = (10)(2.73) + b$$

Solving for b yields

$$b = -27.3\text{ V}$$

Thus, the equation of the SCC's output voltage is

$$V_o = (10)(V_T) - 27.3\text{ V} \quad (3-18)$$

Note: Although the dc offset is -27.3 V , the output voltage, V_o , never goes to this value because the range of V_T is from 2.73 V to 3.23 V . This range of V_T limits V_o from 0 to 5 V .

Designing the signal conditioning circuit. Now that we know the equation for the SCC and it is in the form of $y = mx + b$, we want a circuit in which the gain of 10 and the offset of -27.3 V can be set independently. A noninverting summer is not the

answer because the gain and offset cannot be set independently. What is required is an op amp circuit as shown in Fig. 3-20—an inverting amplifier with a gain of -1 followed by an inverting adder. This circuit is similar to Fig. 3-16(a). The general equation for the output voltage of the adder is

$$V_o = -(R_f/R_1) (-V_T) - (R_f/R_2) E_{dc} \quad (3-19a)$$

$$y = mx + b$$

or

$$V_o = (R_f/R_1) V_T - (R_f/R_2) E_{dc} \quad (3-19b)$$

Matching the coefficients of V_T in Eq. (3-18) and Eq. (3-19b) yields

$$\frac{R_f}{R_1} = 10$$

choosing $R_1 = 10 \text{ k}\Omega$, then $R_f = 100 \text{ k}\Omega$. Matching the dc offset terms in Eq. (3-18) and Eq. (3-19b) yields

$$\frac{-R_f}{R_2} E_{dc} = -27.3 \text{ V}$$

Let E_{dc} be wired to the $+15\text{-V}$ supply. Since $R_f = 100 \text{ k}\Omega$, then $R_2 = 54.9 \text{ k}\Omega$. Note that E_{dc} is a positive voltage and V_T is a negative voltage at the input of inverting adder. Since the LM335 generates a positive voltage, V_T , the inverting amplifier with a gain of -1 is used to generate $-V_T$ as shown in the complete circuit of Fig. 3-20.

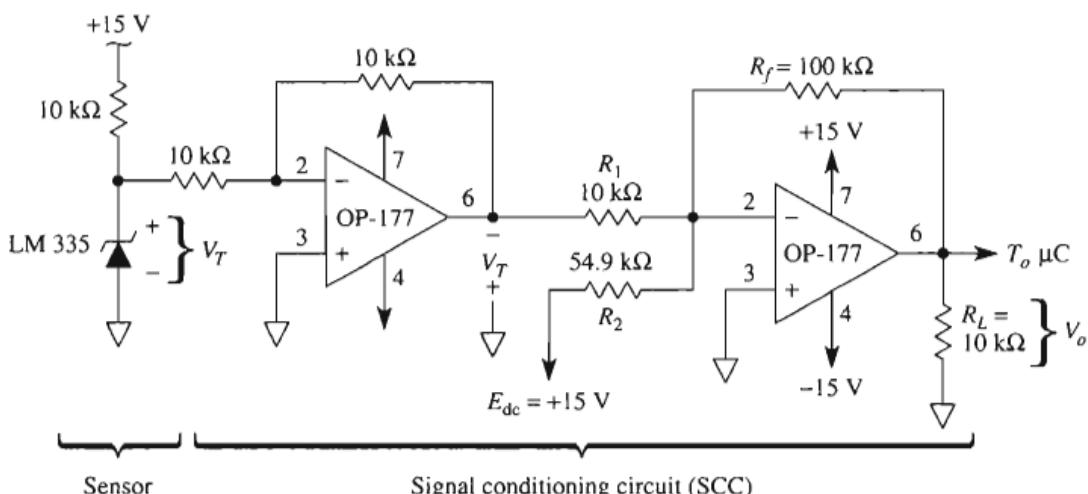


FIGURE 3-20 Design of the SCC for the temperature measuring system of Fig. 3-19. The SCC is an interface between the sensor and microcontroller.

3-12 PSPICE SIMULATION

In this section, we will use PSpice and simulate the performance of four circuits studied in this chapter.

3-12.1 Inverting Amplifier—DC Input

Create the PSpice model of the inverting amplifier of Fig. 3-2. Set the input voltage, E_i , to 0.5 V. Use **IPROBE** to measure currents, I , I_L , and I_o , and **VIEWPOINT** to measure, with respect to ground, the voltage at the inverting input and the op amp's output voltage. Use the procedure outlined in Chapter 2 to obtain and place the following parts on the right side of the work area.

Draw = > Get New Part

Part	Number	Library
=> uA741	1	eval.slb
=> VDC	3	source.slb
=> R	3	analog.slb
=> GLOBAL	4	port.slb
=> AGND	5	port.slb
=> IPROBE	3	special.slb
=> VIEWPOINT	2	special.slb

Arrange the parts as shown in the schematic of Fig. 3-2 but include the **IPROBE**s and **VIEWPOINT**s. Save the file with an **.SCH** extension and click **Analysis** => **Simulate**. The completed circuit with current and voltage values is shown in Fig. 3-21.

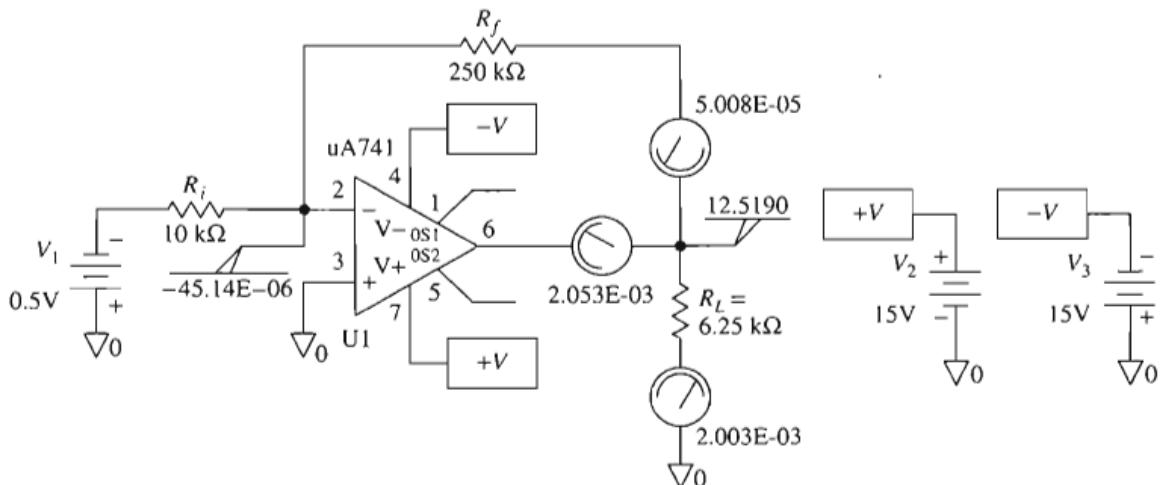


FIGURE 3-21 PSpice model of Fig. 3-2.

3-12.2 Inverting Amplifier—AC Input

Refer to Fig. 3-3 and create the PSpice model of the circuit. Set the input voltage to a sine wave with a peak value of 5 V and a frequency of 500 Hz. Obtain a plot of E_i and V_o versus time. To begin, place the following parts in the work area.

Draw = > Get New Part

Part	Number	Library
=> uA741	1	eval.slb
=> VSIN	1	source.slb
=> VDC	2	source.slb
=> R	3	analog.slb
=> GLOBAL	4	port.slb
=> AGND	5	port.slb

Note that we are using a sine wave as the input signal instead of a triangular wave as shown in Fig. 3-3. Arrange the parts as shown in Fig. 3-3. Change the attributes of the parts as given in Fig. 3-3. Set up the sine-wave attributes by double-clicking on the symbol. In the pop-up window change **VOFF**, **VAMPL**, and **FREQ**.

VOFF = > 0 = > Save Attr

VAMPL = > 5V = > Save Attr = > Change Display = > Both name and value

FREQ = > 500Hz = > Save Attr = > Change Display = > Both name and value

Double-click on the lead from the sine wave generator to **Ri** and label it **Ei**. Double-click on the lead from the output terminal of the op amp and label it **Vo**. See Fig. 3-22.

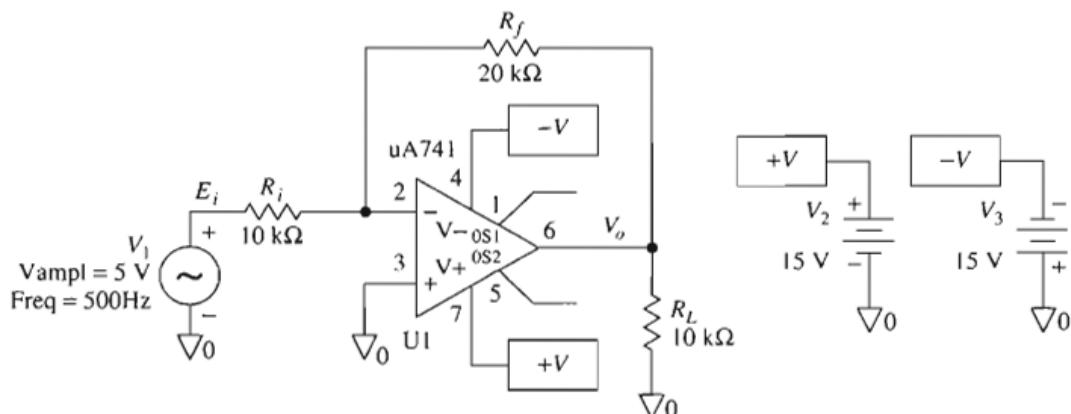


FIGURE 3-22 PSpice model for Fig. 3-3.

In order to obtain a plot of E_i and V_o versus time, we must initialize the Transient menu.

Select

Analysis = > Setup = > Transient
 Click Transient = > Print Step: = > $20\mu\text{s}$
 = > Final Time: = > 4ms

Save the circuit as a file with the **.SCH** extension. Run the simulation

Analysis = > Simulate

In the Probe window, select

Trace = > Add = > $\mathbf{V}[\mathbf{Ei}]$
Trace = > Add = > $\mathbf{V}[\mathbf{Vo}]$

Label the plots and obtain a printout as shown in Fig. 3-23.

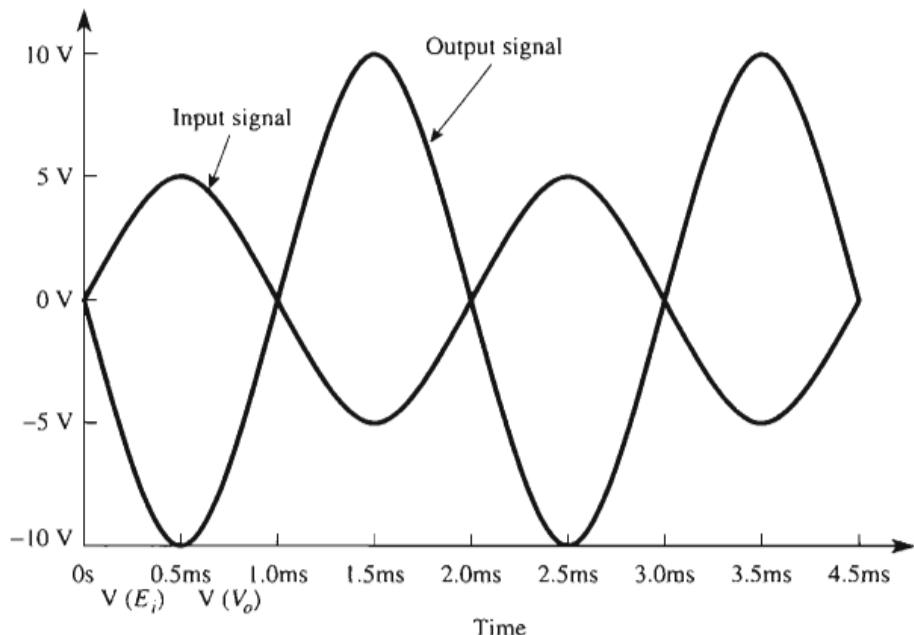


FIGURE 3-23 Plot of E_i and V_o versus time for the circuit of Figs. 3-22 and 3-3.

3-12.3 Inverting Adder

Create the PSpice model and simulate the inverting adder shown in Fig. 3-4. Use **IPROBE** to show $I_1 + I_2 + I_3 = I_f$. Measure the voltage at the summing node, $V(-)$, and V_L using **VIEWPOINT**.

Draw => Get New Part

Part	Number	Library
=> uA741	1	eval.slb
=> VDC	5	source.slb
=> R	5	analog.slb
=> GLOBAL	4	port.slb
=> AGND	7	port.slb
=> IPROBE	4	special.slb
=> VIEWPOINT	2	special.slb

Arrange and wire the parts as show in Fig. 3-4. Place the **IPROBES** to measure I_1 , I_2 , I_3 , and I_f , and place the **VIEWPOINT**s to measure the voltage at the summing point, S , and V_o . Change the parts attributes to correspond to Fig. 3-4. Save the circuit in a file and run the simulation **Analysis => Simulate**. The results are shown in Fig. 3-24.

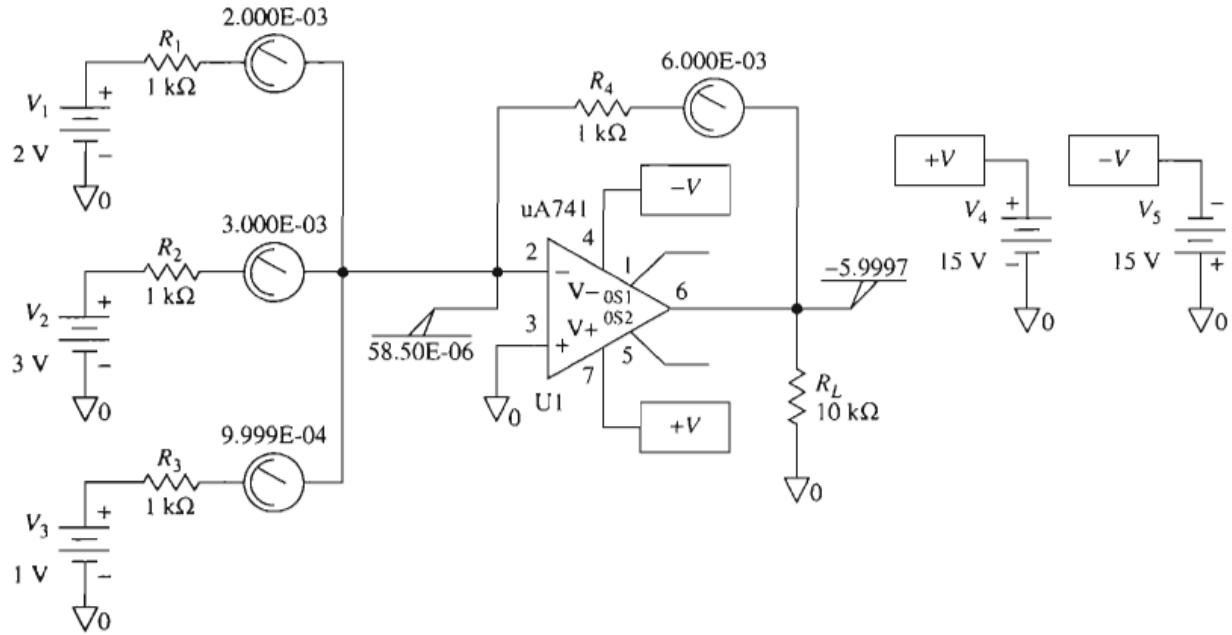


FIGURE 3-24 PSpice model of Fig. 3-4—the inverting adder.

3-12.4 Noninverting Amplifier

Create a PSpice model of the noninverting amplifier shown in Fig. 3-7(a) with $R_f = 20 \text{ k}\Omega$, $R_1 = 10 \text{ k}\Omega$, and $E_i = 2 \text{ V}$. Use **IPROBE** to measure I_o , I_f , I_L , and $I(-)$. Use **VIEWPOINT** to measure V_L and the voltage at the $(-)$ input. If you are using the

evaluation software package, build the circuit with a 741 op amp instead of the OP-177 as shown in Fig. 3-7(a). Place the following parts in the work area.

Draw => Get New Part

Part	Number	Library
=> uA741	1	eval.slb
=> VDC	3	source.slb
=> R	3	analog.slb
=> GLOBAL	4	port.slb
=> AGND	5	port.slb
=> IPROBE	4	special.slb
=> VIEWPOINT	2	special.slb

Arrange the parts and include the **IPROBE**s and **VIEWPOINT**s. Save the file and run the simulation **Analysis => Simulate**. The results are shown in Fig. 3-25.

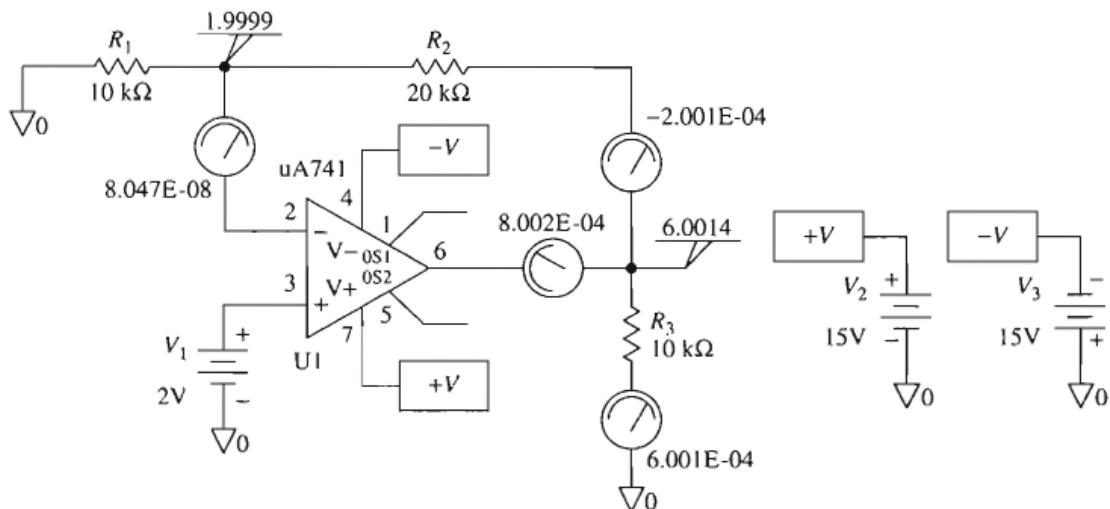


FIGURE 3-25 PSpice model for the noninverting amplifier of Fig. 3-7(a).

PROBLEMS

- 3-1. What type of feedback is applied to an op amp when an external component is connected between the output terminal and the inverting input?
- 3-2. If the open-loop gain is very large, does the closed-loop gain depend on the external components or the op amp?
- 3-3. What two assumptions have been used to analyze the circuits in this chapter?

- 3-4. Identify the circuit in Fig. P3-4.

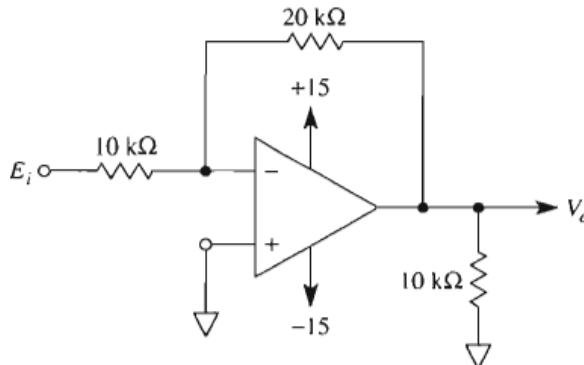


FIGURE P3-4

- 3-5. Calculate V_o and the op amp's output current in Fig. P3-4 if E_i equals (a) +5 V; (b) -2 V. For each situation, state if the op amp sources or sinks current.
- 3-6. Calculate E_i in Fig. P3-4 if V_o equals (a) +5 V; (b) -2 V.
- 3-7. Let E_i be a triangle wave with a frequency of 100 Hz and a peak value of 5 V in Fig. P3-4. (a) Plot E_i and V_o vs. time; (b) V_o vs. E_i .
- 3-8. Repeat Problem 3-7 but let E_i be increased in amplitude to 8 V. (Assume $\pm V_{sat} = \pm 15$ V for ease of plotting.)
- 3-9. Identify the circuit in Fig. P3-9 and calculate V_o if E_i equals (a) +5 V; (b) -2 V. Compare your results with Problem 3-5.

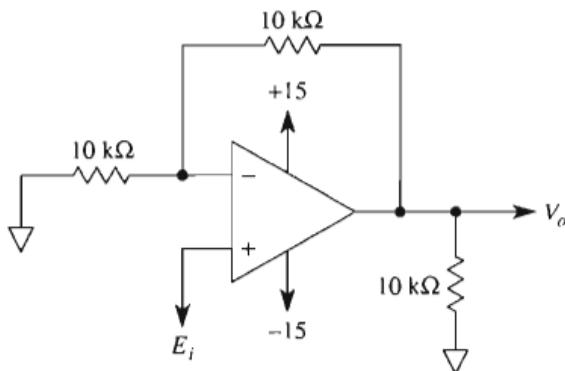


FIGURE P3-9

- 3-10. Repeat Problem 3-7 except apply it to Fig. P3-9. Compare solutions of both problems to distinguish between inverting and noninverting operation.
- 3-11. Design an inverting amplifier with a gain of -5 and an input resistance of 10 kΩ.
- 3-12. Design a noninverting amplifier with a gain of 5.

- 3-13. Input-output characteristics are shown for three different circuits in Fig. P3-13. Design circuits to re-create plots A, B, and C.

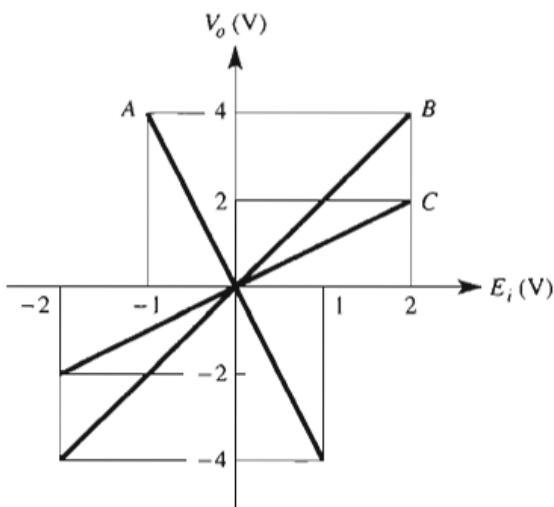


FIGURE P3-13

- 3-14. The circuit of Fig. P3-14 is called a “subtractor.” Is E_1 subtracted from E_2 , or vice versa?
 3-15. A 5-V peak-to-peak sine wave, E_2 , is applied to the summing node in Fig. P3-14. Plot V_o vs. E_1 if voltage E_1 is (a) +5 V; (b) -5 V.

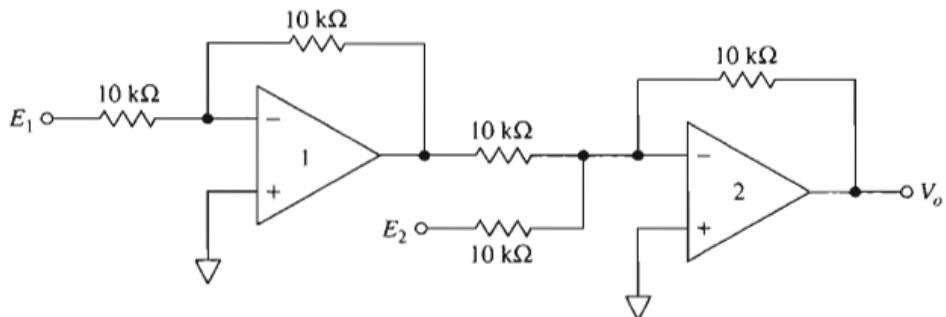


FIGURE P3-14

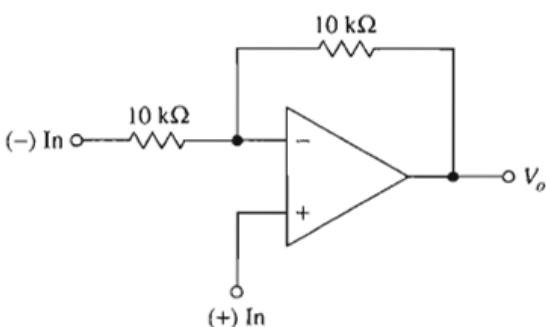


FIGURE P3-15

- 3-16. A 5-V peak-to-peak sine wave, E_i , is applied to (+) In of Fig. P3-15. Plot V_o vs. E_i if the voltage of (-) In is (a) +5 V; (b) -5 V. (Assume that $\pm V_{sat} = \pm 15$ V.)
- 3-17. Design a three-channel inverting amplifier. Gains are to be -1 for channel 1, -3 for channel 2, and -5 for channel 3 (refer to Section 3-3.2).
- 3-18. Design a two op amp circuit to subtract 1 V from 3 V. Show the output voltage present at each op amp.
- 3-19. Design a circuit to amplify the difference between E_1 and E_2 by 5. The inputs E_1 and E_2 should be buffered.
- 3-20. Redesign the system of Fig. 3-20 to measure a temperature range from 0° to 100°C.
- 3-21. Obtain the data sheet of the LM135/335 temperature sensor from National Semiconductor's Web site and determine
- (a) temperature range (continuous) of the LM135.
 - (b) temperature range (continuous) of the LM335.
 - (c) package styles of the LM335.
 - (d) operating current range.
 - (e) LM335 temperature accuracy (typical) at 25°C.