Mid Term Examination of B. Sc. Engg. (CSE) January-June 2022

Course Title: Computer Organization and Architecture Course Code : CIT-313

Time: 40 Min Marks: **15**

N.B. *Answer the following questions.* ***(Split answers are highly discouraged)***

1. Describe the structure of SRAM. Distinguish among PROM, EPROM, EEPROM and flash. **4**
2. Why RAM is so called? **1**
3. Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. **3**
   a. How is a 16-bit memory address divided into tag, line number, and byte number?
   b. Into what line would bytes with each of the following addresses be stored?

      1100 0011 0011 0100

   c. How many total bytes of memory can be stored in the cache?
   d. Why is tag stored in the cache?
4. Give the basic elements to design different buses. Describe PCI bus structure. **4**
5. Define interrupts. How do the multiple interrupts managed? **3**

Patuakhali Science and Technology University
Department of Computer Science and Information Technology
B.Sc. Engg. (CSE) 5th Semester (L-III, S-I), January-June/22
Course Code: CIT-313 Course Title: Computer Organization and Architecture
Credit Hour: 3.00 Session: 2019-2020 Full Marks:70 Duration: 3 Hours

*[Figure in the right margin indicates full marks. **Answer should be short, neat and clean.** Split answering of any question is not recommended.]*

Answer any 5 of the following questions.

1. a) Give the learning outcomes from this course with respect to your current and forthcoming professional perspective. 4
   b) i. What is computer family? 1
   ii. Find out the quotient and reminder by performing two's complement division operation where divisor = -4 and dividend = -7. 4
   c) i. Assume numbers are represented in 6-bit two's complemented representation. Show calculation of the following. 2
   -A+B (Hex)
   ii. Enlist the categories of computer's functions. What is the difference between arithmetic shift and logical shift? 1+2

2. a) Give the technological features for switching computer generation. Also mention the key technological development for any 2 consecutive generation in current era. 4
   b) i. Give the comparative discussion between 2's complement and sign magnitude representation. 2
   ii. Explain variable length instruction with example. Explain the issues regarding a instruction set design. 3
   c) Mention the advantages and disadvantages of condition codes. 2
   "Each operation needs operand"-justify this statement. Briefly describe various categories of operand. 3

3. a) Distinguish among direct, associative and set associative mapping of cache. 2
   b) i. For hexadecimal main memory addresses F000EE, FABCEF, show the following information in hexadecimal format. (Where cache size is 64 KBytes). 5
   a. Tag, Line and Word values for a direct mapped cache.
   b. Tag, Set and Word values for two-way set associative cache.
   ii. Explain different replacement algorithms with respect to cache memory.
   c) i. Why is SRAM so called? Distinguish between SRAM and DRAM. 2.5
   ii. Explain the SRAM structure. 2
   d) Distinguish between EPROM, EEPROM.

4. a) What is RAID? Explain error detection and error correction mechanisms in semiconductor memory. 4
   b) Give the technological features of the storage tape, CD, DVD, HDD, SSD, flash. 2
   c) Why input/output module is used in computer system? Describe the functions of I/O module. 2+2
   d) Shortly explain peripheral devices with its classification. Distinguish between program driven and interrupt driven I/O. 2+2

5. a) i. Describe pipelining. How can the pipeline be sustained in case of branch dealing? 1+2
   ii. "Pipeline processor with k stages is k time faster than non-pipeline processor" justify this statement. 2
   b) i. Why interrupts is used in computer system? Classify interrupts. 2.5
   ii. How does the processor handle multiple interrupts? 2.5
   c) i. Enlist different addressing mechanism. 1.5
   ii. Illustrate the effective address EA = (A) + (R) where, A = base value, R = register that holds displacement. 2.5

6. a) i. Determine the number of page table entries that are needed for the following combinations of virtual address size (n) and page size (P). 1+3

n	P=2^P	#PTE
32	4K	
64	8K	

   ii. How does the page fault handle in VM system.
   b) Distinguish between CISC and RISC. 3
   c) Explain the micro-operations for executing the following instruction with respect to IAS architecture. 3
   ADD AX, 3
   d) The following performance measures were recorded when executing a set of benchmark programs for a machine. 1+3

Instruction category	Percentage of occurrence	No. of cycles per instruction
ALU	40	2
Load & Store	17	3
Branch	40	5
Others	3	6

Assume that the execution of 350 instructions and the clock rate of the CPU is 1.2 GHz. Calculate CPU time, CPI and MIPS.

COA

Patuakhali Science and Technology University
Department of Computer Science and Information Technology

5th Semester (Level-3, Semester-I), Midterm Examination of B.Sc. Engg.(CSE), January-June/2021, Session: 2018-19

Course Code: CIT-313 Course Title: Computer Architecture

Full Marks: 15 Duration: 50 minutes

[Figures in the right margin indicate full marks]

Answer all the following questions.

1.	List and briefly define the possible states that define an instruction execution.	3
2.	Consider a hypothetical microprocessor generating a 16-bit address (for example, assume that the program counter and the address registers are 16 bits wide) and having a 16-bit data bus. i) What is the maximum memory address space that the processor can access directly if it is connected to a "16-bit memory"? 4096 ii) What is the maximum memory address space that the processor can access directly if it is connected to an "8-bit memory"? 32 iii) What architectural features will allow this microprocessor to access a separate "I/O space"? 32, 16 If an input and an output instruction can specify an 8-bit I/O port number, how many 8-bit I/O ports can the microprocessor support? How many 16-bit I/O ports? Explain.	3
3.	Give the elements for designing bus.	1.5
4.	Why study Computer Organization and architecture? Describe the structure and functions of a computer.	3
5.	Describe the evolution of DRAM and processor characteristics.	2
6.	Prepare a question on semiconductor main memory and answer it yourself?	2.5

Mid Term Examination of B. Sc. Engg. (CSE) January-June 2020

Course Title: Computer Organization and Architecture Course Code : CIT-313

Time: 40 Min Marks: 15

N.B. Answer the following questions. (Split answers are highly discouraged)

Give the basic elements to design different buses. Describe PCI bus structure. 5

Mention the characteristics of computer family. Distinguish among sequential, nested, time sequenced and priority interrupt. 5

Enlist the processors from 4 bit to 64 bit. Mention the categories of IAS instruction set with example (opcode, symbolic presentation and description). 5

Mid Term Examination of B. Sc. Engg. (CSE) January-June 2017

Course Title: Computer Organization and Architecture Course Code : CIT-313

Marks: 15

Consider a machine with a byte addressable main memory of 2^{16} bytes and block size 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. 10

How is 16-bit memory address divided into tag, line number and byte number?

Into what line would bytes with each of the following addresses be stored?

0001 0001 0001 1011

1100 0011 0011 0100

Suppose the byte with the address 0001 1010 0001 1010 is stored in the cache. What are the addresses of other bytes stored along with it?

Why is the tag also stored in the cache?

Why interconnection is needed in computer? Briefly describe the considering elements to design a computer. 5

Mid Term Examination of B. Sc. Engg. (CSE) January-June 2019

Course Title: Computer Organization and Architecture Course Code : CIT-313

Time: 35 Min Marks: 15

Find out the quotient and reminder by performing twos complement division operation where divisor = 3 and dividend = -7. 6

Explain Booth's algorithm with flowchart. Mention steps of interrupt driven I/O. 6

Describe peripheral devices. 3

Patuakhali Science and Technology University

5th Semester (Level-3, Semester-I) Final Examination of B.Sc. Engg. (CSE) (January-June 2021)

Course Code: CIT-313 Course Title : Computer Organization and Architecture

Credit Hour : 3.00 Session: 2018-2019 Full Marks:70 Duration: 3 Hours

[Figure in the right margin indicates full marks. Split answering of any question is not recommended.]

Answer any 5 of the following questions. Answer must be brief, relevant and neat.

1 a) Describe RAID working mechanism. 3

b) "If a large number of device are connected to the buses, performance will suffer"- explain this statement. Distinguish among local bus, system bus and expansion bus. 4

c) Give the characteristics of RISC and CISC. 3

d) Describe about set associative mapping. Give the replacement algorithms in cache memory. 4

2 a) Shortly explain the working mechanism of operating system to interact user with computer hardware. 3

b) Find out the quotient and reminder by performing twos complement division operation where divisor = -3 and dividend = -7. 4

c) Define random access memory. Distinguish between two's complement and sign magnitude representation. 3

d) Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

i) How is a 16-bit memory address divided into tag, line number, and byte number? 1

ii) Into what line would bytes with each of the following addresses be stored? 2

i. 0001 0001 0001 1011

ii. 1100 0011 0011 0100

iii) How many total bytes of memory can be stored in the cache? 1

3 a) Distinguish between program driven and interrupt driven I/O. 3

b) i) Illustrate and list the micro-operations to perform addition between two operands from memory. 4

ii) Assume numbers are represented in 6-bit two's complemented representation. Show calculation of the following.

-1A+2B (Hex)

c) Why I/O module is used in computer system? Classify the external devices. 3

d) Write short notes (any two) 4

i) Dual core.

ii) Pentium 4.

iii) Core i7.

4 a) What, in general terms, is the distinction between computer organization and computer architecture? List and briefly define the main structural components of a computer. 3

b) Explain Moore's law. On the IAS, describe the process that the CPU must undertake to read a value from memory and to write a value to memory in terms of what is put into the MAR, MBR, address bus, data bus, and control bus. 4

c) What are the key properties of semiconductor memory? What is the difference between DRAM and SRAM in terms of characteristics such as speed, size, and cost? 3

d) Define memory cell. Describe the structure of a typical Memory Cell. 4

5 a) What is chip logic? Describe a 16 Megabit DRAM (4M × 4) memory structure. 3

b) How Error-Correcting Code works? Describe the Hamming Error-Correcting Code procedure. 4

c) Write down the elements of a machine instruction. Draw and describe the Instruction Cycle State Diagram. 3

d) Describe about Nested Procedures. What is the difference between an arithmetic shift and a logical shift? 4

6 a) Define register addressing. Describe the x86 Instruction Formats. 3

b) What is user-visible registers? Draw the Internal Structure of the CPU. 4

c) Write down the control and status registers. Describe the data flow of fetch and indirect cycle. 3

d) What is instruction pipelining? Describe the Six-Stage CPU Instruction Pipelining with timing diagram. 4

example of a routing protocol that takes a centralized and a decentralized approach.

Patuakhali Science and Technology University

5th Semester (L-3, S-I) Final Examination of B.Sc. Engg. (CSE) January-June 20

Course Code: CIT-313 Course Title: Computer Organization and Architecture

Credit Hour : 3.00 Session: 2017-18 Full Marks:70 Duration: 3 Hours

(Figure in the right margin indicates full marks. Split answering of any question is not recommended.)

Answer any 7 of the following questions.

1 a) Why do you need to study computer organization and architecture? 2

b) A hypothetical machine has 5 instructions

0001=Load AC from memory	0011=Load AC from I/O
0010=Store AC to memory	0111=Store AC to I/O
0101=Add to AC from memory	0110=Sub memory from AC

In this case, the 12-bit address identifies a particular I/O device. Show the program execution (using 16 bit instruction format where prefix 4 bits for opcode) for the following program.

i) Load AC from device 6. 1

ii) Add contents of memory location 555 2

iii) Store AC to memory location 999 3

Assume that the next value retrieved from device 6 is 7 and that location 555 contains a value of 3.

c) i) "Interconnection is necessary in computer system" briefly describe this statement. 1.5

ii) Enlist the registers of IAS computer with its functionality 1.5

2 a) What are the difference among sequential, direct, and random access? 2

b) Describe about set associative mapping. Suppose FFFFF8 is an address of 16M memory. Find out the corresponding address of 16K line cache in associative mapping. 3+3

c) How does the cache speed up the computer performance? 2

3 a) How can you characterize the memory of your computer? 2

b) Explain Booth's algorithm for multiplicand Q=-3 and multiplier M= - 7. 5

c) What is computer system. Distinguish between synchronous and asynchronous timing bus operation. 3+2

4 a) Which issues are responsible for designing instruction set? 2

b) Explain two's complement division procedure for dividend Q=-19 and divisor M=7. 5

c) Give the classification of peripherial devices. Explain the function of an I/O module. 1+3

5 a) Assume numbers are represented in 8-bit two's complemented representation. Show calculation of the following. 1+1

i. -13+6 1+3

ii. -6-13

b) Define interrupts. How does the processor handle multiple interrupts? 2+2

c) Explain different types of operation. Perform arithematic left shift (10100110) for 3 bits and right rotate (10100110) for 3 bits.

6 a) Give the replacement algorithms in cache memory. 2

b) Distinguish between SRAM and DRAM. If an instruction contains four addresses, what might be the purposes of each address? 2+2

c) Explain error detection and error correction mechanisms in semiconductor memory. 2+2

7 a) What do you mean by variable length addressing? Why is it necessary? 1+1

b) Explain various different addressing techniques in computer programming. 4

OR

Describe about control signals of CPU

c) "Each operation needs operand"-justify this statement. Briefly describe various categories of operand. 2+2

8 a) What general roles are performed by processors? 1

b) What do you mean by user visible register in CPU? Also mention advantages and disadvantages of condition codes. 2+2

OR

What is the function of condition codes? What are the differences between the two's complement representation of a number and the two's complement of a number?

c) Describe pipelining. "Pipeline processor with k stages is k time faster than non pipeline processor" justify this statement. 2+2

Patuakhali Science and Technology University

3rd Semester (Level-3, Semester-I) Final Examination of B.Sc. Engg. (CSE) January-June 2018

Course Code: CSE-313 Course Title: Computer Organization and Architecture

Credit Hour: 3.00 Session: 2015-16 Full Marks: 70 Duration: 3 Hours

[Figure in the right margin indicates full marks. Split answering of any question is not recommended.]

There are 5 of the following questions. Answer must be brief, relevant and neat

1. a) A hypothetical machine has 8 instructions: 6

1010 = Load AC from memory	1011 = Sub memory from AC
0011 = Store AC to memory	0110 = Store AC to I/O
0100 = Add to AC from memory	0101 = Load AC from I/O

In this case, the 12-bit address identifies a particular I/O device. Show the program execution (using 16 bit instruction format where prefix 4 bits for opcode) for the following program.

i. Load AC from device 9

ii. Add contents of memory location 555

iii. Store AC to memory location 666.

Assume that the next value retrieved from device 9 is 23 and location 555 contains a value of 3

b) i. Distinguish between computer architecture and organization. 2+4

ii. Mention the computer generation with its corresponding technology. What general roles are performed by processor registers?

c) Why do we need to study computer organization and architecture? 2

2. a) Explain the distinction between the written sequence and time sequence of an instruction. Illustrate and list the micro-operations to perform addition between two operands from memory. 2+4

b) Differentiate between CISC and RISC architectures. What are their typical characteristics? Give some examples of processors of each category. 2+3

c) Why cache controller is needed in memory system? 2

3. a) Mention the key features of RAID-0 RAID-6. Is pipelining processor is inefficient for branch instruction. Explain its mechanism to deal the branches in pipelining. 3+3

b) Consider a pipeline with 4 stages, fetch instruction (FI), decode instruction and calculate address (DA), fetch operand (FO), and execute (EX). Draw a timing diagram for instruction pipeline operation for a sequence of 9 instructions, in which the fifth instruction is a branch that is taken and in which there is no data dependencies. 4+2

c) i. Mention data types for multimedia and give 2 multimedia instruction of Intel Pentium product.

ii. Mention the advantages and disadvantages of variable length addressing. 2

4. a) Describe the elements of a machine instruction. Assume numbers are represented in 6-bit two's complemented representation. Show calculation of as follows: 3+3

i) 9 - 5 (Hint: 9 + (-5))

ii) -13-4 (Hint: (-13) + (-4))

b) i. Find out the quotient and remainder by performing 2's complemented division operation where divisor = -3 and dividend = -7. 4+2

ii. Illustrate the arithmetic shift operation.

c) Enlist different addressing modes. 2

5. a) Why input output module is used in computer system? Describe the functions of I/O module. 2+4

b) Shortly explain peripheral devices with its classification. Distinguish between program driven and interrupt driven I/O.

c) Distinguish between SRAM and DRAM. 2+4

6. a) Compare direct, associative and set-associative mapping. Explain replacement algorithm of cache memory. 3+3

b) Mention the control signals among system modules. Explain multiple interrupts with example. 3+3

c) Give the characteristics of computer family. 2

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Patuakhali Science and Technology University

B.Sc. Engg. (CSE) Level-3, Semester-2 Final Examination-2016 (January-June)

Course Code: CIT-313 Course Title : Computer Organization and Architecture

Credit Hour : 3.0 Session: 2013-2014 Full Marks:70 Duration: 3 Hours

[Figure in the right margin indicates full marks. Split answering of any question is not recommended.]

Answer any 5 of the following questions. Answer must be brief, relevant and neat.

1 [A] Explain about the learning outcomes for studying the Computer Organization and Architecture course. 3

[B] Illustrate the basic elements of a digital computer. 2

[C] What are the roles of different register of control unit and the ALU? 3

[D] How are data read from a magnetic disk? 3

[E] List and briefly define three techniques for performing I/O. 3

2 [A] Four benchmark programs are executed on three Laptops with the following results: 3

	Laptop A	Laptop B	Laptop C
Program 1	10	10	20
Program 2	1000	100	20
Program 3	500	1000	50
Program 4	100	800	100

The table shows the execution time in seconds, with 200,000,000 instructions executed in each of the four programs. Calculate the MIPS values for each computer for each program. Then calculate the arithmetic and harmonic means assuming equal weights for the four programs, and rank the computers based on arithmetic mean and harmonic mean.

[B] Consider the below computer specification 5

- Pentium Intel® Core™ i7 4.7 GHz
- 2GB 1333 MHz DDR3 SoDIMM expandable Up to 4GB memory
- 32 KB L1 Cache, 256 KB L2 cache and 4MB L3 Cache
- 1TB 7200 RPM SATA8 Hard drive
- (6) High speed USB 2.0 (2 side/4 rear), (2) Side audio ports: headphone and microphone,(2) PS/2 ports2, Serial2
- 19'' Inches LCD Monitor, 0.25 mm AG, 1280×1024 at 80 MHz
- 48x DVD RW Optical
- 256 MB PCI express graphics card
- 56K data/fax Modem
- 64 bit PCI sound card
- Intel® 82578DM, 10M/100M/1000M Gigabit Ethernet
- What does it all mean?

[C] Discuss about cache/main memory structure with block diagram 3

[D] Your computer Hard disk drive with 8 surfaces, 512 tracks per surface, and 64 sectors per track. Sector size is 1 KB. The average seek time is 8 ms, the track-to-track access time is 1.5 ms, and the drive rotates at 3600 rpm. Successive tracks in a cylinder can be read without head movement. 3

i) What is the disk capacity?

ii) What is the average access time? Assume this file is stored in successive sectors and tracks of successive cylinders, starting at sector 0, track 0, of cylinder 1

iii) Estimate the time required to transfer a 5-MB file.

iv) What is the burst transfer rate?

3 [A] What are the basic elements of Cache Design? 2

P.T.O.

[B.] What is the general relationship among access time, memory cost, and capacity?
[C.] A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.
[D.] Explain Direct-Mapping Cache Organization with diagram
[E.] Distinguish between DRAM and SRAM in terms of characteristics such as application, speed, size, and cost. 5

4 [A.] Explain hardware implementation of unsigned binary multiplication for multiplicand=13 and multiplier=11. 4
[B.] Analyze the statement "CPU performs all arithmetic operation using addition" 3
[C.] i) Define instruction format. Why does the variable length instruction format used in CPU operation? 4
ii) Mention the concept of von Neumann architecture.
[D.] Justify the statement- "More dedicated interconnection produce faster computer". 3
Differentiate between system bus and local bus.

5 [A.] i) What is the difference between the twos complement representation of a number and twos complement of a number? 4
ii) If an instruction contains four address, what might be the purpose of each address? /10
[B.] i) What are the typical elements of machine instruction? 3
ii) What types of locations can hold source and destination operands?
[C.] A hypothetical machine has 6 instructions 4

0010=Load AC from memory	1011=Sub memory from AC
0011=Store AC to memory	0110=Store AC to I/O
0101=Add to AC from memory	1001= Load AC from I/O

In this case, the 12-bit address identifies a particular I/O device. Show the program execution (using 16 bit instruction format where prefix 4 bits for Opcode) for the following program.

i. Load AC from memory location 999
ii. Add contents of memory location 555
iii. Store AC to device 6.

Assume that the next value retrieved from memory location 999 is 2 and location 555 contains a value of 3.

[D.] List and explain the instruction set design issues. /10

[A.] Explain two's complement division procedure for dividend Q= - 7 and divisor M= -3
[B.] i) Analyze the relationship between instruction and micro-operation.
ii) Explain performance and performance penalty of instruction pipelining.
[C.] Explain RISC architecture. Differentiate between RISC and CISC.
[D.] i) Differentiate between arithmetic shift and logical shift.
ii) A given microprocessor has words of one byte. What is the smallest and largest integer that can be represented in the following representation?
a) Unsigned
b) Two's complement

Patuakhali Science and Technology University

B.Sc. Engg. (CSE) Level-3, Semester-2 Final Examination-2023 (January-June)

Course Code: CIT-313 Course Title : Computer Organization and Architecture

Credit Hour : 3.0 Session: 2020-2021 Full Marks:70 Duration: 3 Hours

[Figure in the right margin indicates full marks. Split answering of any question is not recommended.]

Answer any 5 of the following questions.

1 a) Define Computer Organization and Computer Architecture. What is the difference between the them? 2

b) What are the key concepts of Von Neumann architecture? Define hardware and software programming. 5

c) Define Interrupts. What are the approaches for handling multiple interrupts? Illustrate and explain. 5

d) What are the steps of the instruction cycle for the instruction "SUB B, A," which stores the difference of memory locations B and A into location A? 2

2 a) Define computer instructions and describe their types. 3

b) Where Zero-address instructions are applicable and how? Explain. 2

c) What are logical, arithmetic, and cyclic (rotate) shifts? Apply a 4-bit logical right shift, logical left shift, arithmetic right shift, arithmetic left shift, right rotate, and left rotate to the bits 10100110. 5

d) What is a procedure, and why is it necessary? Illustrate and explain the procedure mechanism. 4

3 a) What is an I/O module, and why is it necessary? 3

b) What are the differences among Programmed I/O, Interrupt-driven I/O and direct memory access (DMA)? Describe with flowcharts. 5

c) How does a DMA module transfer control to the processor after its task? Does it interrupt the processor? Define *cycle stealing* in DMA. 2

d) Give the features of CISC and Corei7 in the perspective of computer architecture and organization . 4

4 a) A hypothetical machine has 6 instructions 5

1110=Load AC from memory	1011=Sub memory from AC
0001=Store AC to memory	0110=Store AC to I/O
0101=Add to AC from memory	1101= Load AC from I/O

In this case, the 12-bit address identifies a particular I/O device. Show the program execution steps (using 16 bit instruction format where prefix 4 bits for opcode) for the following program.

i. Load AC from device 99.

ii. Add contents of memory location 555

Store AC to memory location 666.

b) Explain RAID 2. Mention the characteristics of semiconductor memories (4 types). 2+2

c) i. Enlist different addressing mode. 2+3

ii. Assume numbers are represented in 6-bit two's complemented representation. Show calculation of the following.

a) -A+B (Hex)

b) -33-17 (Decimal)

5 a) Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. 5

i. How is a 16-bit memory address divided into tag, line number. and byte number?

ii. Into what line would bytes with each of the following addresses be stored?

0001 0001 0001 1011

1101 0000 0001 1101

iii. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?

iv. How many total bytes of memory can be stored in the cache?

b) Calculate the multiplication operation using Booth's algorithm for Q = -17 (multiplicand) and M = 16 (multiplier). 4

c) i. Define access time and cycle time. 2+3

ii. Distinguish among sequential, direct and random memory access.

6 a) i. Explain the responsibility of memory management unit in computer system. 2+3

ii. Assume a pipeline with 4 stages: fetch instruction (FI), decode instruction and calculate address (DA), fetch operand (FO), and execute (EX). Draw a timing diagram for instruction pipeline operation for a sequence of 9 instructions, in which the fifth instruction is a branch that is taken and in which there is no data dependencies.

b) Describe the structure of SRAM. Give the features of SRAM and DRAM. 2+2

c) Define virtual address and physical address space. Explain page miss mechanism in virtual memeory system. 2+3