DLD viva preparatory questions

C O N T E N T S

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Revision 01

Digital Design Interview Questions and Answers

https://www.mytectra.com/interview-question/digital-design-interview-questions-and-answers

Q1. What is a multiplexer?

Ans: A multiplexer is a combinational circuit which selects one of many input signals and directs to the only output.

Q2. What is meant by LUT?

Ans: LUT: Look-Up Table. An n-bit look-up table can be implemented with a multiplexer whose select lines are the inputs of the LUT and whose inputs are constants. An n-bit LUT can encode any n-input Boolean function by modeling such functions as truth tables. This is an efficient way of encoding Boolean logic functions, and LUTs with 4-6 bits of input are in fact the key component of modern FPGAs.

Q3. What is meant by bit Binary multiplier?

Ans: Binary multiplication process: A Binary Multiplier is a digital circuit used in digital electronics to multiply two binary numbers and provide the result as output. The method used to multiply two binary numbers is similar to the method taught to school children for multiplying decimal numbers which is based on calculating partial product, shifting them and adding them together. Similar approach is used to multiply two binary numbers. Long multiplicand is multiplied by 0 or 1 which is much easier than decimal multiplication as product by 0 or 1 is 0 or same number respectively. Figure 1 below shows the block diagram of a 2-bit binary multiplier. The two numbers A1A0 and B1B0 are multiplied together to produce a 4-bit output P3P2P1P0. (The maximum product term can be 3 * 3 = 9, which is 1001, a 4-bit number).

Q4. What is a ring counter?

Ans: A ring counter is a type of counter composed of a circular shift register. The output of the last shift register is fed tothe input of the first register. For example, in a 4-register counter, with initial register values of 1100, the repeatingpattern is: 1100, 0110, 0011, 1001, 1100, so on.

Q5. What are PLA and PAL? Give the differences between them.

Ans: Programmable Logic Array is a programmable device used to implement combinational logic circuits. The PLA has a set of programmable AND planes, which link to a set of programmable OR planes, which can then be conditionally complemented to produce an output. PAL is programmable array logic, like PLA, it also has a wide, programmable AND plane. Unlike a PLA, the OR plane is fixed, limiting the number of terms that can be ORed together. Due to fixed OR plane PAL allows extra space, which is used for other basic logic devices,

such as multiplexers, exclusive-ORs, and latches. Most importantly, clocked elements, typically flip-flops, could be included in PALs. PALs are also extremely fast.

Q6. 16x1 mux using 4x1 muxes

Ans: Implementing 16:1 multiplexer with 4:1 multiplexers: A 16x1 mux can be implemented using 5 4x1 muxes. 4 of these multiplexers can be used as first stage to mux 4 inputs each with two least significant bits of select lines (S0 and S1), resulting in 4 intermediate outputs, which, then can be muxed again using a 4:1 mux. The implementation of 16x1 mux using 4x1 muxes is shown below in figure 1:

Q7. Compare and Contrast Synchronous and Asynchronous reset.

Ans: Synchronous reset logic will synthesize to smaller flip-flops, particularly if the reset is gated with the logicgenerating the d-input. But in such a case, the combinational logic gate count grows, so the overall gate countsavings may not be that significant. The clock works as a filter for small reset glitches; however, if these glitchesoccur near the active clock edge, the Flip-flop could go metastable. In some designs, the reset must be generated bya set of internal conditions. A synchronous reset is recommended for these types of designs because it will filter thelogic equation glitches between clock.Problem with synchronous resets is that the synthesis tool cannot easily distinguish the reset signal from any otherdata signal. Synchronous resets may need a pulse stretcher to guarantee a reset pulse width wide enough to ensurereset is present during an active edge of the clock, if you have a gated clock to save power, the clock may bedisabled coincident with the assertion of reset. Only an asynchronous reset will work in this situation, as the resetmight be removed prior to the resumption of the clock. Designs that are pushing the limit for data path timing, cannot afford to have added gates and additional net delays in the data path due to logic inserted to handle synchronousresets.

Q8. How can you convert a JK flip-flop to a D flip-flop?

Ans: Connect the inverted J input to K input.

Q9. What is the Reset basics?

Ans: Purpose of reset: We see that almost every electronic device has a reset button. Your video game has a reset button that resets the game and your unsaved progress is lost. Your laptop's reset button reboots it. Have you ever wondered why a system (or specifically a chip) has a reset? Well, the simple purpose of resets is to provide a known initial state to the system to start with. Another reason is, when the system accidentally goes into some unknown state (there may be many reasons for this), the system always knows how to get out of this and go into a known state by asserting a reset signal.

Reset design strategies:

Defining a reset is one of the most important decisions that needs to be taken for the good health of design. In general, following things need to be kept in mind during deciding reset strategy:

- **What flops to receive reset**: One of the easiest and safest approaches is to enable all the flip-flops in the design with a reset. However, there may be a some registers, whose initial state will not have any impact on the design state. In other words, it might not matter if the register's output is '0' or '1' when design goes in reset state. Such registers can be kept non-resettable after an analysis. Let us elaborate with the help of an example. Figure 1 shows a part of an FSM wherein two registers are feeding an AND gate. In figure 1(a), we have decided to initialize both to '0' during reset (**with an asynchronous reset, to be explained later**). However, given this scenario, if one of the flip-flops is provided with an initial state of '0', the output of the other will be gated. So, we may omit reset on one of the flip-flops. Figure 1(b) shows that omission of reset on one of the flip-flops does not have any impact on state machine design.

We may not always encounter such scenarios. If, instead of AND gate, we had an OR gate, we would not have been able to keep one of the flip-flops uninitialized during reset. Figure 2 shows such an example. In figure 2(b), if we remove reset from second flip-flop, output of OR gate goes 'X'; thus, impacting the state machine.

Another popular scenario wherein we can skip a few registers from having a reset pin is shift registers. If the first stage of a shift register is you give more than one clock pulses when in reset state, subsequent stages will get reset. If you have four stages, you need to give at least three clock pulses while in reset. The same is shown in figure below.

- **Synchronous vs asynchronous reset**: There are two kinds of reset assertion/deassertion strategies - synchronous vs asynchronous reset. Although each of the two can be used to effective implementation of reset, each of these has its own advantages/disadvantages. Designer may decide upon the desired strategy by considering the pros and cons.
    - Synchronous reset means that the reset will affect the state of the design only on the active edge of the clock.
    - Asynchronous reset resets the design asynchronously. For this purpose, flip-flops have a special pin that resets the output to '0' or '1' based upon the need.

Q10. What is a Johnson counter?

Ans: Johnson counter connects the complement of the output of the last shift register to its input and circulates a streamof ones followed by zeros around the ring. For example, in a 4-register counter, the repeating pattern is: 0000, 1000,1100, 1110, 1111, 0111, 0011, 0001, so on.

Q11. How to build an XOR gate using NAND gates?

Ans: We can build a 2-input XOR gate using only 3 NAND gates. Sound interesting, isn't it? Let us see hos.
As we know, the logical equation of a 2-input XOR gate is given as below:

Y = A (xor) B = (A' B + A B')

Let us take an approach where we consider **A** and **A'** as different variables for now (optimizations related to this, if any, will consider later). Thus, the logic equation, now, becomes:

Y = (CB + A D) ----- (i)

where

C = A' and D = B'

De-Morgan's law states that

m + n = (m'n')'

Taking this into account,

Y = ((CB)'(AD)')' = ((A' B)' (A B')')'

Thus, Y is equal to **((A' nand B) nand (A nand B')).** No further optimizations to the logic seem possible to this logic. Figure 1 below shows the implementation of XOR gate using 2-input NAND gates.

Q12. In a 4-bit Johnson counter How many unused states are present?

Ans: 4-bit Johnson counter: 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000.8 unused states are present.

Q13. Delay line based Time to digital converter.

Ans: A time to digital converter is a circuit that digitizes time; i.e., it converts time into digital number. In other words, a time-to-digital converter measures the time interval between two events and represents that interval in the form of a digital number.

TDCs are used in places where the time interval between two events needs to be determined. These two events may, for example, be represented by rising edges of two signals. Some applications of TDCs include time-of-flight measurement circuits and All-Digital PLLs.

Delay line based time-to-digital converter: This is a very primitive TDC and involves a delay-line which is used to delay the reference signal. The other signal is used to sample the state of delay chain. Each stage of delay chain outputs to a flip-flop or a latch which is clocked by the sample signal. Thus, the output of the TDC forms a thermometer code as the stage will show a '1' if the reference signal has passed it, otherwise it will show a zero.

Q14. What are the differences between a flip-flop and a latch?

Ans: Flip-flops are edge-sensitive devices where as latches are level sensitive devices.Flip-flops are immune to glitches where are latches are sensitive to glitches.Latches require less number of gates (and hence less power) than flip-flops.Latches are faster than flip-flops.

Q15. What is the difference between Mealy and Moore FSM?

Ans: Mealy FSM uses only input actions, i.e. output depends on input and state. The use of a Mealy FSM leads often to areduction of the number of states.Moore FSM uses only entry

actions, i.e. output depends only on the state. The advantage of the Moore model is asimplification of the behavior.

400+ TOP Digital Logic Design VIVA Questions and Answers

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Digital Logic Design VIVA Questions :-

1) Explain about setup time and hold time, what will happen if there is setup time and hold tine violation, how to overcome this?

- Set up time is the amount of time before the clock edge that the input signal needs to be stable to guarantee it is accepted properly on the clock edge.
- Hold time is the amount of time after the clock edge that same input signal has to be held before changing it to make sure it is sensed properly at the clock edge.
- Whenever there are setup and hold time violations in any flip-flop, it enters a state where its output is unpredictable: this state is known as metastable state (quasi stable state); at the end of metastable state, the flip-flop settles down to either '1' or '0'. This whole process is known as metastability

2) What is skew, what are problems associated with it and how to minimize it?

- In circuit design, clock skew is a phenomenon in synchronous circuits in which the clock signal (sent from the clock circuit) arrives at different components at different times.
- This is typically due to two causes. The first is a material flaw, which causes a signal to travel faster or slower than expected. The second is distance: if the signal has to travel the entire length of a circuit, it will likely (depending on the circuit's size) arrive at different parts of the circuit at different times. Clock skew can cause harm in two ways. Suppose that a logic path travels through combinational logic from a source flip-flop to a destination flip-flop. If the destination flip-flop receives the clock tick later than the source flip-flop, and if the logic path delay is short enough, then the data signal might arrive at the destination flip-flop before the clock tick, destroying there the previous data that should have been clocked through. This is called a hold violation because the previous data is not held long enough at the destination flip-flop to be properly clocked through. If the destination flip-flop receives the clock tick earlier than the source flip-flop, then the data signal has that much less time to reach the destination flip-flop before the next clock tick. If it fails to do so, a setup violation occurs, so-called because the new data was not set up and stable before the next clock tick arrived. A hold violation is more serious than a setup violation because it cannot be fixed by increasing the clock period.
- Clock skew, if done right, can also benefit a circuit. It can be intentionally introduced to decrease the clock period at which the circuit will operate correctly, and/or to increase the setup or hold safety margins. The optimal set of clock delays is deter-

mined by a linear program, in which a setup and a hold constraint appears for each logic path. In this linear program, zero clock skew is merely a feasible point.
Clock skew can be minimized by proper routing of clock signal (clock distribution tree) or putting variable delay buffer so that all clock inputs arrive at the same time

3) What is slack?

- 'Slack' is the amount of time you have that is measured from when an event 'actually happens' and when it 'must happen'.. The term 'actually happens' can also be taken as being a predicted time for when the event will 'actually happen'.
- When something 'must happen' can also be called a 'deadline' so another definition of slack would be the time from when something 'actually happens' (call this Tact) until the deadline (call this Tdead).
  Slack = Tdead – Tact.
- Negative slack implies that the 'actually happen' time is later than the 'deadline' time…in other words it's too late and a timing violation….you have a timing problem that needs some attention.

4) What is glitch? What causes it (explain with waveform)? How to overcome it?

The following figure shows a synchronous alternative to the gated clock using a data path. The flip-flop is clocked at every clock cycle and the data path is controlled by an enable. When the enable is Low, the multiplexer feeds the output of the register back on itself. When the enable is High, new data is fed to the flip-flop and the register changes its state

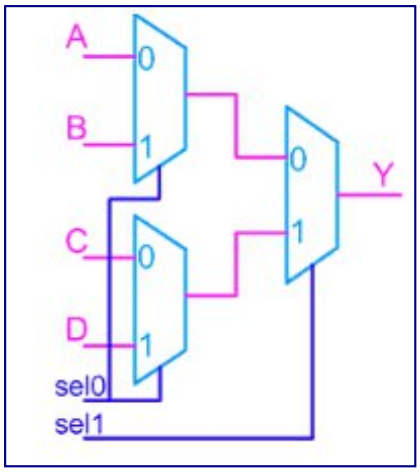
5) Given only two xor gates one must function as buffer and another as inverter?

1. Tie one of xor gates input to 1 it will act as inverter.
2. Tie one of xor gates input to 0 it will act as buffer.

6) What is difference between latch and flipflop?

The main difference between latch and FF is that latches are level sensitive while FF are edge sensitive. They both require the use of clock signal and are used in sequential logic. For a latch, the output tracks the input when the clock signal is high, so as long as the clock is logic 1, the output can change if the input also changes. FF on the other hand, will store the input only when there is a rising/falling edge of the clock.

7) Build a 4:1 mux using only 2:1 mux?



8.Difference between heap and stack?

The Stack is more or less responsible for keeping track of what's executing in our code (or what's been "called"). The Heap is more or less responsible for keeping track of our objects (our data, well… most of it – we'll get to that later.).
Think of the Stack as a series of boxes stacked one on top of the next. We keep track of what's going on in our application by stacking another box on top every time we call a method (called a Frame). We can only use what's in the top box on the stack. When we're done with the top box (the method is done executing) we throw it away and proceed to use the stuff in the previous box on the top of the stack. The Heap is similar except that its purpose is to hold information (not keep track of execution most of the time) so anything in our Heap can be accessed at any time. With the Heap, there are no constraints as to what can be accessed like in the stack. The Heap is like the heap of clean laundry on our bed that we have not taken the time to put away yet – we can grab what we need quickly. The Stack is like the stack of shoe boxes in the closet where we have to take off the top one to get to the one underneath it.

9) Difference between mealy and moore state machine?

A) Mealy and Moore models are the basic models of state machines. A state machine which uses only Entry Actions, so that its output depends on the state, is called a Moore model. A state machine which uses only Input Actions, so that the output depends on the state and also on inputs, is called a Mealy model. The models selected will influence a design but there are no general indications as to which model is better. Choice of a model depends on the application, execution means (for instance, hardware systems are usually best realized as Moore models) and personal preferences of a designer or programmer

B) Mealy machine has outputs that depend on the state and input (thus, the FSM has the output written on edges)
Moore machine has outputs that depend on state only (thus, the FSM has the output written in the state itself.

Adv and Disadv
In Mealy as the output variable is a function both input and state, changes of state of the

state variables will be delayed with respect to changes of signal level in the input variables, there are possibilities of glitches appearing in the output variables. Moore overcomes glitches as output dependent on only states and not the input signal level.
All of the concepts can be applied to Moore-model state machines because any Moore state machine can be implemented as a Mealy state machine, although the converse is not true.
Moore machine: the outputs are properties of states themselves… which means that you get the output after the machine reaches a particular state, or to get some output your machine has to be taken to a state which provides you the output.The outputs are held until you go to some other state Mealy machine:
Mealy machines give you outputs instantly, that is immediately upon receiving input, but the output is not held after that clock cycle.

10) Difference between onehot and binary encoding?

Common classifications used to describe the state encoding of an FSM are Binary (or highly encoded) and One hot.
A binary-encoded FSM design only requires as many flip-flops as are needed to uniquely encode the number of states in the state machine. The actual number of flip-flops required is equal to the ceiling of the log-base-2 of the number of states in the FSM.
A onehot FSM design requires a flip-flop for each state in the design and only one flip-flop (the flip-flop representing the current or “hot” state) is set at a time in a one hot FSM design. For a state machine with 9- 16 states, a binary FSM only requires 4 flip-flops while a onehot FSM requires a flip-flop for each state in the design
FPGA vendors frequently recommend using a onehot state encoding style because flip-flops are plentiful in an FPGA and the combinational logic required to implement a onehot FSM design is typically smaller than most binary encoding styles. Since FPGA performance is typically related to the combinational logic size of the FPGA design, onehot FSMs typically run faster than a binary encoded FSM with larger combinational logic blocks

11) How to achieve 180 degree exact phase shift?

Never tell using inverter
a) dcm’s an inbuilt resource in most of fpga can be configured to get 180 degree phase shift.
b) Bufgds that is differential signaling buffers which are also inbuilt resource of most of FPGA can be used.

12) What is significance of ras and cas in SDRAM?

- SDRAM receives its address command in two address words.
- It uses a multiplex scheme to save input pins. The first address word is latched into the DRAM chip with the row address strobe (RAS).
- Following the RAS command is the column address strobe (CAS) for latching the second address word.
- Shortly after the RAS and CAS strobes, the stored data is valid for reading.

13) Tell some of applications of buffer?

a)They are used to introduce small delays
b)They are used to eliminate cross talk caused due to inter electrode capacitance due to close routing.
c)They are used to support high fanout,eg:bufg

14) Implement an AND gate using mux?

This is the basic question that many interviewers ask. for and gate, give one input as select line,incase if u r giving b as select line, connect one input to logic '0' and other input to a.

15) What will happen if contents of register are shifter left, right?

- It is well known that in left shift all bits will be shifted left and LSB will be appended with 0 and in right shift all bits will be shifted right and MSB will be appended with 0 this is a straightforward answer
- What is expected is in a left shift value gets Multiplied by 2 eg:consider 0000_1110=14 a left shift will make it 0001_110=28, it the same fashion right shift will Divide the value by 2.

16)Given the following FIFO and rules, how deep does the FIFO need to be to prevent underflow or overflow?

RULES:
1) frequency(clk_A) = frequency(clk_B) / 4
2) period(en_B) = period(clk_A) * 100
3) duty_cycle(en_B) = 25%

Assume clk_B = 100MHz (10ns)
From (1), clk_A = 25MHz (40ns)
From (2), period(en_B) = 40ns * 400 = 4000ns, but we only output for 1000ns,due to (3), so 3000ns of the enable we are doing no output work. Therefore, FIFO size = 3000ns/40ns = 75 entries.

Digital Circuits Interview Questions and Answers

https://electronicspost.com/digital-circuits-interview-questions-and-answers/

Q.1. What do you mean by word 'digital'?

Answer: Digital means sequence of numbers having finite precision.

Q.2. What is the difference between digital system and analog system?

Answer: A digital system is a combination of devices designed to manipulate logical information or physical quantities that are represented in digital form that is the quantities can take only discrete values.

Example of digital systems includes digital computers and calculators, digital audio and video equipments etc.

An analog system contains devices that manipulate physical quantities that are represented in analog forms. In an analog system, the quantities can vary over a continuous range of values.

Q.3. What is the difference between digital signal and binary signal?

Answer: A digital signal is defined as a signal which has only a finite number of distinct values. Digital signals are not continuous signal, they are discrete signals. If a digital signal has only two distinct values, i.e. 0 and 1 then it is called as a binary signal.

Q.4. What are the advantages of digital signal?

Answer: Advantages of digital signal are: Digital signals can be processed and transmitted more efficiently and reliably than analog signals. It is possible to store the digital data. Play back or further processing of the digital data is possible. The effect of noise (unwanted voltage fluctuations) is less. So digital data does not get corrupt.

Q.5. Define number system.

Answer: A number system defines a set of values used to represent quantity. Examples of number system are binary, octal, decimal, duodecimal, hexadecimal etc.

Q.6. How the resolution can be increased in floating point representation of numbers?
Answer: More the number of bits used in fraction part better will be the resolution.

Q.7. What is the size of bit, nibble, byte, word and double word in terms of number of bits?

Answer: Bit = 1 bits, Nibble = 4 bits, Byte = 8 bits, word = 16 bits, double word = 32 bits.

Q.8. Which code is called as minimum change code and why?

Answer: Gray code is called as minimum change code because it has a very special feature that only one bit will change, each time the decimal number is incremented.

Q.9. What is a INHIBIT gate?

Answer: It is basically an AND gate with one of its input negated by an inverter. In INHIBIT operation output is zero when blocking input is one.

Q.10. What is the advantage of fixed point representation compared to floating point representation?

Answer: Complexity and the cost of algorithm is less in fixed point representation, so it is suitable for time domain filtering.

Q.11. What is the advantage of floating point representation compared to fixed point representation?

Answer: Quantization error is small and dynamic range is high for floating point representation so it is suitable for frequency domain algorithm.

Q.12. What are ASCII codes?

Answer: ASCII is the abbreviation of American Standard Code for Information Interchange. It is a universally accepted alphanumeric code. It is used in most computers and other electronic equipment. Most computer keyboards are standardized with ASCII. When we press a key, the corresponding ASCII code is generated which goes in to the computer. ASCII has 128 characters and symbols. We need 7 bits to represent 128 characters. So ASCII is a 7 bit code.

Q.13. Which gate is known as coincidence detector?

Answer: XNOR gate is known as coincidence detector.

Q.14. Which gates are used in parity checking and parity generation of binary numbers?

Answer: XOR and XNOR gates.

Q.15. What are degenerated functions?

Answer: Degenerated functions are those which generate single operation.

Q.16. What do you mean by sampling jitter?

Answer: Sampling jitter is the error in placement of each block edge controlling the point when sampling begins.

Q.17. What do you mean by aperture jitter?

Answer: The RMS variation in time of the sampling instant caused by jitter in the sample-hold command signal is known as aperture jitter. It is associated with sample and hold circuit.

Q.18. What are universal gates?

Answer: Universal gates are those gates with the help of which any gates can be designed. NAND and NOR gates are universal gates.

Q.19. What is the difference between static logic circuits and dynamic logic circuits?

Answer: Static logic circuits perform the logical operations with voltage levels while dynamic logic circuits are based on the capacitive nature of input of MOSFET, working by transferring stored charges corresponding to logic levels from one circuit to another with the help of clock signals.

Q.20. Why look ahead carry adder is faster than ripple adder?

Answer: Look ahead carry adder is faster; since carry is generated in parallel at all the stages of addition rather than sequentially as in ripple adder.

Q.21. What will be the number of possible combinations with n variables?

Answer: The number of possible combinations with n variables is 2^n.

Q.22. What will be the number of possible Boolean function with n variables?

Answer: The number of possible Boolean function with n variables is 2^{2n}.

Q.23. What is the difference between compiler and interpreter?

Answer: Compiler- Programs that converts English like words of a high level language into the machine language of a computer. It needs a given program called source code and translates the program into the machine language, called object code.

Interpreter- It translates one statement at a time from a source code to an object code.

Q.24. What is the difference between simulator and emulator?

Answer: Simulator is just software which acts like hardware inside which we can see all electronic components and connect them in different manner to get the output while emulator is actual hardware.

Q.25. What is the difference between assembler and cross assembler?

Answer: Assembler- The program that translates an assembly language program from mnemonics to the binary machine code of the computer is called Assembler.

Cross Assembler- The program that translates the mnemonics of a particular microprocessor into the mnemonics of other microprocessor is called a Cross Assembler.

Q.26. How microprocessor works without internal memory?

Answer: Microprocessor consists of address, data and control buses with some internal registers to process the task through external memory.

Q.27. Define memory word.

Answer: Memory word is a group of bits in a memory that represents instructions of some type. For example, a register consisting of 8 flip flops can be used as a memory for storing an 8 bit word.

Q.28. What is direct memory access (DMA)?

Answer: DMA interface is used for transferring data directly between an external device and memory. The bus buffers in the microprocessor are disabled and go into a high impedance state during DMA transfer.

Q.29. What is PLD?

Answer: Programmable logic device (PLD) is an IC that contains a large number of interconnected logic functions. The user can program the IC for a specific function by selective breaking the appropriate interconnections.

Q.30. Define PAL and PLA.

Answer: Programmable array logic (PAL) –

- It is a class of programmable logic devices.
- Its AND array is programmable while its OR array is hard wired.

Programmable logic array (PLA) –

- It is a class of programmable logic devices.
- Both its AND and OR arrays are programmable.
- It is also called as field programmable logic array (FLPA).

Q.31. What are the requirements of a logic family?

Answer: The requirements of a logic family are-

- Propagation delay time is minimum.
- Losses should be minimum.
- It should be highly immune to noise.
- The size should be minimum.

Q.32. What are the characteristics of Resistor Transistor logic (RTL)?

Answer: The characteristics of Resistor Transistor logic (RTL)are-

- Very much compatible with other logic families.
- It is very economical. Its design is easy.
- It has poor noise immunity.
- Its speed is low.
- Power dissipation is low.
- It has low threshold and fan out is also less.

Q.33. What are the characteristics of Diode Transistor logic (DTL)?

Answer: The characteristics of Diode Transistor logic (DTL) are-

- In this transistor acts as inverting amplifier.
- It possesses high speed.
- It has low power dissipation.
- Logic is performed by diodes.
- Noise immunity and fan out is poor.

Q.34. What are the characteristics of Integrated Injection logic (IIL)?

Answer: The characteristics of Integrated Injection logic (IIL) are-

- Its power consumption is low.
- It has only one output per gate.
- It has good packing density.
- Speed is low.
- Noise margin is poor.
- One transistor is grown for each gate.

Q.35. What are the characteristics of Transistor Transistor logic (TTL)?

Answer: The characteristics of Transistor Transistor logic (TTL) are-

- It has good current capability.
- It is very economical.
- Its switching speed is good.
- It is compatible with DTL and CMOS.
- Schottky type has very high switching speed and low power consumption.

Q.36. What are the characteristics of Emitter Coupled logic (ECL)?

Answer: The characteristics of Emitter Coupled logic (ECL) are-

- It has low noise.
- It has got fastest speed among all logic devices.
- It needs good heat sinking.
- Its cost is high. Both normal and inverted outputs are obtained.
- Its power consumption is high.

Q.37. What are the characteristics of Metal Oxide Semiconductor logic (MOS)?

Answer: The characteristics of Metal Oxide Semiconductor logic (MOS) are-

- MOS family uses negative logic for its operation.
- It is very economical.
- It is easier to make large complex chips.
- It needs both positive and negative supplies.
- Its speed is very low.

Q.38. What are the characteristics of complementary metal oxide semiconductor (CMOS)?

Answer: The characteristics of complementary metal oxide semiconductor (CMOS) are-

- Noise margin is high.
- Its power dissipation is very low.
- Area used is more than MOS.
- Processing is very complicated.
- Its speed is very low.

Q.39. What do you mean by current hogging and which logic family has this problem?

Answer: Current hogging problem is due to different characteristics of transistor. Owing to these differences, the saturation voltages of the load transistors may be different. So when one transistor enters into saturation it will not allow other transistors to enter saturation and will take whole of the current supplied from the driver gate. This is known as current hogging. DCTL has the problem of current hogging.

Q.40. What is Fanout?

Answer: It is the maximum number of similar logic gate input that can be driven by a logic gate output without affecting the logic gate performance. High fanout is advantageous because it reduces the need for additional drivers to drive more gates.

Q.41. What are combinational circuits?

Answer: A combinational circuit is a logic circuit the output of which depends only on the combination of the inputs. The output does not depend on the past values of inputs or outputs. Hence combinational circuits do not require any memory.

Q.42. What is magnitude comparator?

Answer: A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitudes. The outcome of comparison is specified by three variables that indicates whether A>B, A<B or A=B.

Q.43. What is the range of temperature over which logic families works satisfactorily?

Answer:The temperature range is 0 to 70∘c.

Q.44. Which saturated logic family is suitable for large scale integration (LSI)?

Answer: Integrated Injection logic (IIL) is the only saturated bipolar logic suitable for large scale integration because of small silicon chip area required and low power consumption.

Q.45. What is the use of schottky TTL?

Answer: Schottky TTL removes the storage time of transistors by preventing them from going into saturation. This version increases the speed of operation without an excessive increase in power dissipation. This is the most popular version in new designs.

Q.46. What is the advantage of using open collector output in TTL logic gates rather than using totem pole output?

Answer: With Totem pole output wired-And operation is not possible in TTL gates which may lead to transistor burning. With open collector output wired-AND operation is possible.

Q.47. What are sequential circuits?

Answer: In the sequential circuit, the timing parameter comes into picture. The output of a sequential circuit depends on the present time inputs, the previous output and the sequence in which the inputs are applied. In order to provide the previous input or output, a memory element is required to be used. Thus a sequential circuit needs a memory element.

Q.48. How will you define the present state and next state of sequential circuit?

Answer: Present state- The data stored by the memory element at any given instant of time is called as the present state of the sequential circuit.

Next state- The combinational circuit operates on the external inputs and the present state to produce new outputs. Some of these new outputs are stored in the memory element and called as the next state of the sequential circuit.

Q.49. Define clock skew.

Answer: Clock skew is defined as the difference in time between the clock edges arriving at a pair of clock inputs.

Q.50. What is a flip flop?

Answer: Flip flop is also known as the basic digital memory circuit or in other words it is the basic memory element. It has two stable states namely logic 1 state and logic 0 state. It can store one bit of digital information therefore it is also called as 1-bit memory cell. We can design it by using NOR gates or NAND gates.

Logic Gates Questions and Answers

https://instrumentationtools.com/logic-gates-questions-answers/

1. Explain what is a combinational circuit?

In a combinational circuit, the output depends upon present input(s) only i.e, not dependant on the previous input(s). The combinational circuit has no memory element. It consists of logic gates only.

2. Write two characteristics of combinational circuits.

The two characteristics of combinational circuits are:

In combinational circuits, the output exists as long as the input exists.

A combinational circuit will always respond in the same fashion to the input function, when we apply signal to the input terminal of the combinational logic circuit.

3. Explain what is a half-adder?

A logic circuit, that can add two 1-bit numbers and produce outputs for sum and carry, is called a half-adder.

4. Explain what is a full-adder?

A binary adder, which can add two 1-bit binary numbers along with a carry bit and produces outputs for sum and carry is called a full-adder.

5. Explain what is a flip-flop?

A flip-flop is a basic memory element that is made of an assembly of logic gates and is used to store 1-bit of information.

6. Explain what is a latch?

It is a D-type of flip-flop and stores one bit of data.

7. Explain what is an excitation table?

Excitation table gives an information about Explain what should be the flip-flop inputs if the outputs are specified before and after the clock pulses.

8. Explain what is a state table?

State table consists of complete information about present state, next state, and outputs of a sequential circuit.

9. Explain what is Boolean Algebra?

Boolean algebra is a mathematic system of logic in which truth functions are expresses as symbols and then these symbols are manipulated to arrive at conclusion.

10. Explain what are the basic logic elements?

Basic logic elements are NOT gate, AND gate, OR gate and the flip-flop.

11. Explain what is a truth table?

Truth table is a table that gives outputs for all possible combinations of inputs to a logic circuit.

12. Define positive logic and negative logic.

If the higher of the two voltages represents a 1 and the lower voltage represents a 0, then the logic is called a positive logic. On the other hand, if the lower voltage represents a 1 and the higher voltage a 0, we have a negative logic.

13. Explain what is pulse logic system?

A logic system in which a bit is recognized by the presence or absence of a pulse is called a pulse or dynamic logic system.

14. Explain what is an inverter?

An inverter is a logic gate whose output is the inverse or complement of its input.

15. Explain what are the universal logic gates?

Universal gate is a gate that can perform all the basic logical operations such as NAND and NOR gates.

16. Explain what is the specialty of NAND and NOR gates?

The specialty of NAND and NOR gates is that they are universal gates and can perform all the basic logical operations.

17. Explain why NAND-NAND realization is preferred over AND-OR realization?

NAND-NAND realization needs only one type of gate(NAND), that minimizes IC package counter.

18. Explain why is a two-input NAND gate called universal gate?

NAND gate is called universal gate because any digital system can be implemented with the NAND gate. Sequential and combinational circuits can be constructed with these gates because element circuits like flip-flop can be constructed from two NAND gates connected back-to-back. NAND gates are common in hardware because they are easily available in the ICs form. A NAND gate is in fact a NOT-AND gate. It can be obtained by connecting a NOT gate in the output of an AND gate.

19. Explain what is associate law?

Associate law is a low of addition and multiplication and according to this law grouping of the variable is the ORing or ANDing of several variables is immaterial and the results obtained are the same.

Digital Electronics Interview Questions

https://www.tpointtech.com/digital-electronics-interview-questions
(this is the new domain of javatpoint – though I am not sure Sir will figure this link or not!)

1) What is the difference between Latch And Flip-flop?

The difference between latches and Flip-flop is that the latches are level triggered and flip-flops are edge triggered. In latches level triggered means that the output of the latches changes as we change the input and edge triggered means that control signal only changes its state when goes from low to high or high to low.

Latches are fast whereas flip-flop is slow.

---

2) What is the binary number system?

The system which has a base 2 is known as the binary system and it consists of only two digits 0 and 1.

For Example: Take decimal number 625
625 = 600 + 20 + 5
That means,
6 100 + 2 10 + 5
$6\ 10^2 + 2\ 10^1 + 5\ 10^0$

In this 625 consist of three bits, we start writing the numbers from the rightmost bit power as 0 then the second bit as power 1 and the last as power 2. So, we can represent a decimal number as

$\sum$digit $10^{\text{corresponding position or bit}}$

Here 10 is the total number of digits from 0 to 9.

---

3) State the De Morgan's Theorem?

De Morgan's Theorem stated two theorems:

1.The complement of a product of two numbers is the sum of the complements of those numbers.

(A. B)' = A' + B'

Truth Table:

A	B	(AB)'	A' + B'
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

2. The complement of the sum of two numbers is equal to the product of the complement of two numbers.

(A + B)' = A'B'

Truth Table:

A	B	(A+B)'	A'B'
0	0	1	1
0	1	0	0
1	0	0	0
1	1	0	0

---

4) Define Digital System?

Digital systems are the system that processes a discrete or digital signal.

---

5) What is meant by a bit?

Bits are the binary digits like 0 and 1.

---

6) What is the best Example of Digital system?

Digital Computer.

---

7) How many types of number system are there?

There are four types of number system:

1. Decimal Number System.

2. Binary Number System.
3. Octal Number System.
4. Hexadecimal Number System.

---

8) What is a Logic gate?

The basic gates that make up the digital system are called a logic gate. The circuit that can operate on many binary inputs to perform a particular logic function is called an electronic circuit.

---

9) What are the basic Logic gates?

There are three basic logic gates-

1. AND gate.
2. OR gate.
3. NOT gate.

---

10) Which gates are called as Universal gate and what are its advantages?

The Universal gates are NAND and NOR. The advantages of these gates are that they can be used for any logic calculation.

---

11) What are the applications of the octal number system?

The applications of the octal number system are as follows:

1. For the efficient use of microprocessors.
2. For the efficient use of digital circuits.
3. It is used to enter binary data and display of information.

---

12) What are the fundamental properties of Boolean algebra?

The basic properties of Boolean algebra are:

1. Commutative Property.
2. Associative Property.
3. Distributive Property.

---

13) What are Boolean algebra and Boolean expression?

---

14) What is meant by K-Map or Karnaugh Map?

K-Map is a pictorial representation of truth table in which the map is made up of cells, and each term in this represents the min term or max term of the function. By this method, we can directly minimize the Boolean function without following various steps.

---

15) Name the two forms of Boolean expression?

The two forms of Boolean expression are:

1. Sum of products (SOP) form.
2. The Product of sum (POS) form.

---

16) What are Minterm and Maxterm?

A minterm is called Product of sum because they are the logical AND of the set of variables and Maxterm are called sum of product because they are the logical OR of the set of variables.

---

17) Write down the Characteristics of Digital ICs?

The characteristics of digital ICs are -

1. Propagation delay.
2. Power Dissipation.
3. Fan-in.
4. Fan-out.
5. Noise Margin.

---

18) What are the limitations of the Karnaugh Map?

The limitations of Karnaugh Map are as follows:

1. It is limited to six variable maps which means more than six variable involving expressions are not reduced.
2. These are useful for only simplifying Boolean expression which is represented I standard form.

---

19) What are the advantages and disadvantages of the K-Map Method?

The advantages of the K-Map method are as follows-

1. It is an excellent method for simplifying expression up to four variables.
2. For the logical simplification, it gives us a visual method.

3. It is suitable for both SOP and POS forms of reduction.
4. It is more suitable for classroom teachings on logic simplification.

The disadvantages of the K-Map method are as follows:

1. It is not suitable when the number of variables exceeds more than four.
2. For Computer reduction, it is not suitable.
3. We have to take while entering the numbers in the cell-like 0, 1 and don't care terms.

---

20) What are the advantages and disadvantages of Quine-MC Cluskey method?

---

21) Define Pair, Quad, and Octet?

Pair: Two adjacent cell of karnaugh map is called as Pair. It cancels one variable in a K-Map simplification.

Quad: A Pair of Four adjacent pairs in a karnaugh map is called a quad. It cancels two variables in a K-Map simplification.

Octet: A Pair of eight adjacent pair in a karnaugh map is called an octet. It cancels four variables in a K-map simplification.

---

22) Define Fan-in and Fan-out?

Fan-in- The Fan-in of the gate means that the number of inputs that are connected to the gate without the degradation of the voltage level of the system.

Fan-out- The Fan-out is the maximum number of same inputs of the same IC family that a gate can drive maintaining its output levels within the specified limits.

---

23) Write the definition of the Duality Theorem?

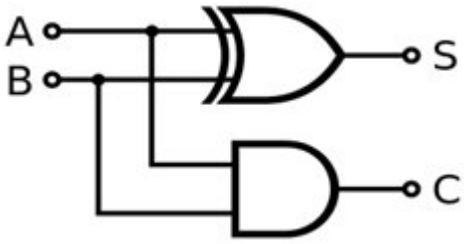
Duality Theorem states that we can derive another Boolean expression with the existing Boolean expression by:

1. Changing OR operation (+ Sign) to AND operation (. Dot Sign) and vice versa.
2. Complimenting 0 and 1 in the expression by changing 0 to 1 and 1 to 0 respectively.

---

24) What is Half-Adder?

Half-adder is the circuits that perform the addition of two bits. It has two inputs A and B and two outputs S (sum) and C (carry). It is represented by XOR logic gate and an AND logic gate.



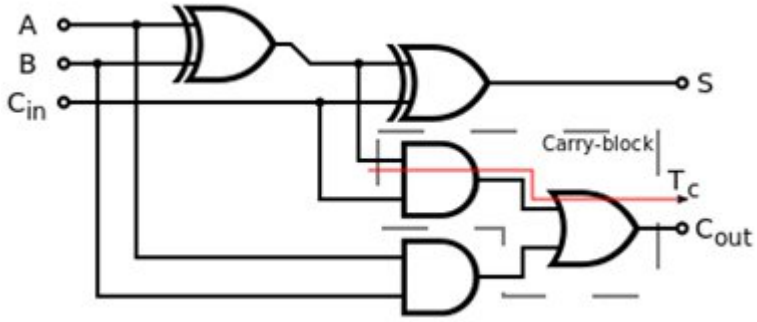
Truth Table of Half adder:

A (Input)	B (Input)	S (Output)	C (Output)
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

---

25) What is Full-Adder?

Full-adder is the circuits that perform the addition of three bits. It has three inputs A, B and a carry bit. Full adders are represented with AND, OR and XOR logic gate.



Truth Table of Full-Adder

Input			Output	
A	B	C_i	C_0	S
0	0	0	0	0
0	1	0	0	1
1	0	0	0	1
1	1	0	1	0
0	0	1	0	1
0	1	1	1	0
1	0	1	1	0
1	1	1	1	1

---

26) What is power dissipation?

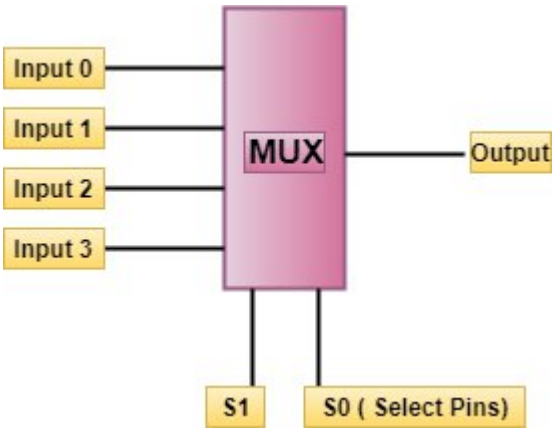
Period time is the electrical energy used by the logic circuits. It is expressed in milliwatts or nanowatts.

*Power dissipation = Supply voltage * mean current taken from the supply.*

---

27) What is a Multiplexer?

The multiplexer is a digital switch which combines all the digital information from several sources and gives one output.



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28) What are the applications of Multiplexer (MUX)?

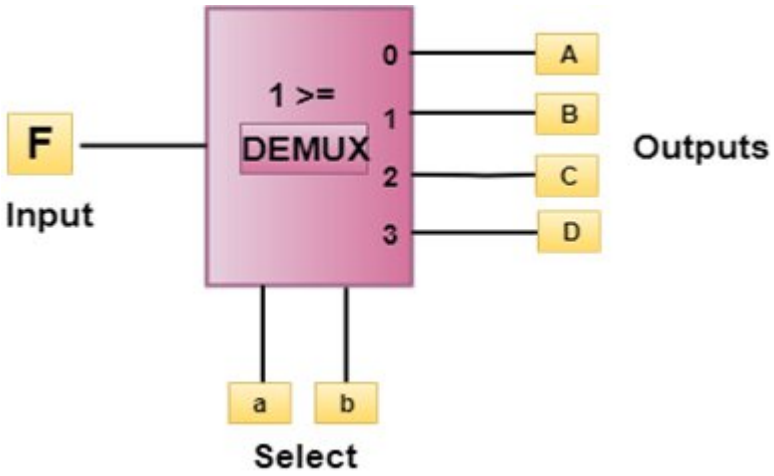
The applications of the multiplexer are as follows:

1. It is used as a data selector from many inputs to get one output.
2. It is used as A/D to D/A Converter.
3. These are used in the data acquisition system.
4. These are used in time multiplexing system.

---

29) What is a Demultiplexer?

The demultiplexer is a circuit that receives the input on a single line and transmits this onto 2n possible output line. A Demultiplexer of 2n outputs has n select lines, which are used to select which output line is to be sent to the input. The demultiplexer is also called as Data Distributor.



---

30) What are the applications of Demultiplexer?

The applications of the demultiplexer are as follows:

1. It is used in the data transmission system with error detection.
2. It is used as a decoder for the conversion of binary to decimal.
3. It is used as a serial to parallel converter.

---

31) What are the differences between Combinational Circuits and Sequential Circuits?

The differences between combinational and sequential circuits are as follows:

S.No	Combinational Circuits	Sequential Circuits
1.	These are faster in speed.	These are slower.
2.	These are easy to design.	These are difficult to design.
3.	The clock input is not required.	The clock input is required.
4.	In this, the memory units are not required.	In this, the memory units are required to store the previous values of inputs.

5.	**Example:** Mux, Demux, encoder, decoder, adders, subtractors.	**Example:** Shift registers, counters.

32) Define Rise Time?

Rise time is the time that is required to change the voltage level from 10% to 90%.

33) Define fall time?

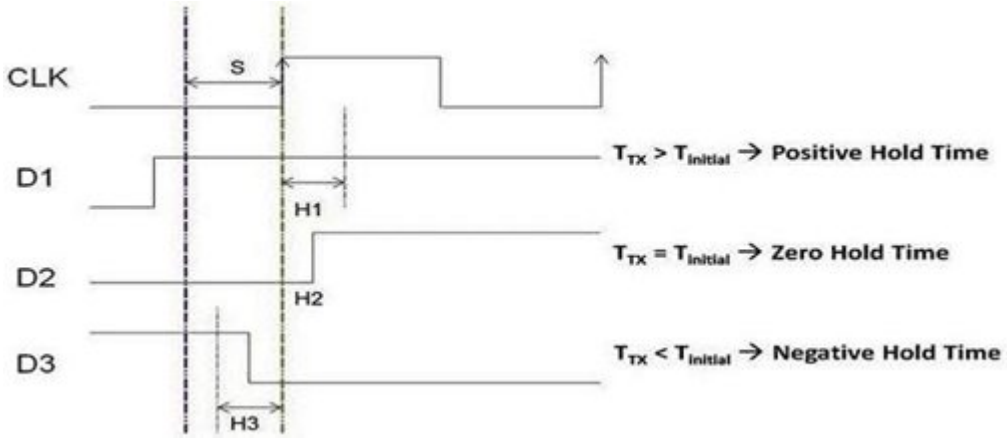
Fall time is the time that is required to change the voltage level from 90% to 10%.

34) Define Setup time?

The minimum time that is required to maintain the constant voltage levels at the excitation inputs of the flip-flop device before the triggering edge of the clock pulse for the levels to be reliably clocked in the flip flop is called the Setup time. It is denoted as tsetup.

35) Define Hold time?

The minimum time at which the voltage level becomes constant after triggering the clock pulse in order to reliably clock into the flip flop is called the Hold time. It is denoted by thold.



36) What is the difference between Synchronous and Asynchronous Counters?

The difference between Synchronous and Asynchronous Counters are as follows:

S.No	Asynchronous Counters	Synchronous Counters
1.	These are low-speed Counters.	These are high-speed Counters.
2.	The Flip flops of these counters are not clocked simultaneously.	In these counters, the flip-flops are clocked simultaneously.

3.	Simple logic circuits are there for more number of states.	Complex logic circuits are there when the number of states increases.

---

37) What are the applications of Flip-Flops?

The applications of flip-flops are:

1. Flip-flops are used as the delay element.
2. These are used for Data transfer.
3. Flip-flops are used in Frequency Division and Counting.
4. Flip-Flops are used as the memory element.

---

38) What is the difference between D-latch and D Flip-flop?

D-latch is level sensitive whereas flip-flop is edge sensitive. Flip-flops are made up of latches.

---

39) What are the applications of Buffer?

Applications of buffer are as follows:

1. Buffer helps to introduce small delays.
2. Buffer helps for high Fan-out.
3. Buffer are used to eliminate cross talks.

Digital Electronics Viva Questions and Answers

https://www.scribd.com/document/503041541/DIgital-Electronics-Lab-Exam-Viva-Questions

1. Define gates ?
Ans. Gates are the digital circuits, which perform a specific type of logical operation.
2 Define IC?
Ans. IC means integrated circuit. It is the integration of no. of components on a common substrate.
3. Define Universal gates.
Ans. Universal gates are those gates by using which we can design any type of logical expression.
4. Write the logical equation for AND gate.
Ans. Y=A.B
5. How many no. of input variables can a NOT Gate have?
Ans. One.
6. Under what conditions the output of a two input AND gate is one?
Ans. Both the inputs are one.
7. 1+0=?
Ans. 1
8. When will the output of a NAND Gate be 0?
Ans. When all the inputs are 1.
9. Define K-map ?
Ans. It is a method of simplifying Boolean Functions in a systematic mathematical way.
10. What are combinational circuits?
Ans. These are those circuits whose output depends upon the inputs present at that instant of time.
11. What are sequential circuits?
Ans. These are those circuits whose output depends upon the input present at that time as well as the
previous output.
12. If there are four variables how many cells the K-map will have?
Ans. 16.
13. When two min-terms can be adjacent?
Ans. 2 to the power n.
14. Which code is used for the identification of cells?
Ans8. Gray Code.
15. Define Byte?
Ans. Byte is a combination of 8 bits.
16. Flip flop is Astable or Bistable?
Ans. Bistable.
17. What are the I/Ps of JK flip–flop where this race round condition occurs?
Ans. Both the inputs are 1.
18. When RS flip-flop is said to be in a SET state?
Ans. When the output is 1.

19.When RS flip-flop is said to be in a RESET state?
Ans. When the output is 0.
20.What is the truth table of JK flip-flop?
21.What is the function of clock signal in flip-flop?
Ans. To get the output at known time.
22.What is the advantage of JK flip-flop over RS flip-flop?
Ans. In RS flip-flop when both the inputs are 1 output is undetermined.
23.In D flip-flop I/P = 0 what is O/P?
Ans.0
24.In D flip-flop I/P = 1 what is O/P?
Ans.1
25. In T flip-flop I/P = 1 what is O/P?
Ans. Qn
26. What do you understand by decoder?
Ans. A decoder is a combinational circuit that converts binary information from n input lines to a
maximum of 2n unique output lines. Most IC decoders include one or more enable inputs to control the
circuit operation.
27. What is demultiplexer?
Ans. The demultiplexer is the inverse of the multiplexer, in that it takes a single data input input and n
address inputs. It has 2n outputs. The address input determine which data output is going to have the
same value as the data input. The other data outputs will have the value 0.
28. What do you understand by encoder?
Ans. An encoder or multiplexer is therefore a digital IC that outputs a digital code based on which of its
several digital inputs is enabled.
29. What is the main difference between decoder and demultiplexer?
Ans. In decoder we have n input lines as in demultiplexer we have n select lines.
30. Why Binary is different from Gray code?
Ans. Gray code has a unique property that any two adjacent gray codes differ by only a single bit.
31. Write down the method of Binary to Gray conversion.
Ans. Using the Ex-Or gates.
32. Write the full form of ASCII Codes?
Ans. American Standard Code for Information Interchange.
33.Binary code is a weighted code or not?
Ans. Yes
34 Why is MUX called as "Data Selector"?
Ans. This selects one out of many inputs.
35. What do you mean by Multiplexing?
Ans. Multiplexing means selecting only a single input out of many inputs.
36. What is Digital Multiplexer?
Ans. The multiplexer which acts on digital data.
37 What is the function of Enable input to any IC?
Ans. When this enable signal is activated.
38 What is demultiplexer?

Ans. A demultiplexer transmits the data from a single source to various sources.

39 Can a decoder function as a D'MUX?

Ans. Yes

40. What is the role of select lines in a Demultiplexer?

Ans. Select line selects the output line.

41. Differentiate between functions of MUX & D'MUX?

Ans. Multiplexer has only single output but demultiplexer has many outputs.

42.The number of control lines required for a 1:8 demultiplexer will be

Ans. 3

43. How many 4:1 multiplexers will be required to design 8:1 multiplexer?

Ans. 2

44. What do you understand by parallel adder?

Ans. If we place full adders in parallel, we can add two- or four-digit numbers or any other size desired
i.e. known as parallel adder.

45. What happens when an N-bit adder adds two numbers whose sum is greater than N or equal to 2

Ans. Overflow.

46. Is Excess-3 code is weighted code or not?

Ans. Excess-3 is not a weighted code.

47 What is IC no. of parallel adder?

Ans. IC 7483.

48. What is the difference between Excess-3 & Natural BCD code?

Ans. Natural BCD code is weighted code but Excess-3 code is not weighted code.

49. What is the Excess-3 code for (396) 10

Ans. (396) 10 = (011011001001) EX-3

50 Can we obtain 1's complement using parallel adder?

Ans. Yes

51 Can we obtain 2's complement using parallel adder?

Ans. Yes

52 How many bits can be added using IC7483 parallel adder?

Ans. 4 bits.

53 Can you obtain subtractor using parallel adder?

Ans. Yes

54 Give the basic rules for binary addition?

Ans. 0+0 = 0; 0+1 = 1; 1+1 = 1 0 ; 1+0 = 1.

55 Specify the no. of I/P and O/P of Half adder?

Ans2. Two inputs & one output.

56 What is the drawback of half adder?

Ans. We can't add carry bit from previous stage

57.Write the equation for sum & carry of half adder?

Ans. Sum = A XOR B; carry = A.B.

58 Write the equation for sum & carry of full adder?

Ans. SUM= A'B'C+A'BC'+AB'C'+ABC; CARRY=AB+BC+AC.

59.How many half adders will be required for Implementing full adder?

Ans. Two half adders and a OR gate.

60. Define Bit?

Ans. Bit is an abbreviation for binary digit.

61. What is the difference b/w half adder& half sub tractor?

Ans. Half adder can add two bits & half sub tractor can subtract two bits.

62. Half subtractor logic circuit has one extra logic element. Name the element?

Ans. Inverter.

63. Define Nibble?

Ans. Combination of four bits.

64 What is half subs tractor?

Ans. Performs subs traction of two bits.

65 For implementing half subs tractor how many EX-OR, AND gates and Not gates are required?

Ans. One EX-OR, one –AND gate, one- Not gate.

66. What are the logical equations for difference & borrow?

Ans. $D = \bar{A}B + A\,B$

$B = \bar{A}.B$

67. How full subtractor is different from half subs tractor.

Ans. Full sub tractor performs subtraction of three bits but half subs tractor Performs subtraction of two
bits.

68. If inputs of half subs tractor are A=0, and B=1 then Borrow will be?

Ans. B=1

69. Is 2's complement method appropriate for subtraction?

Ans. 2's complement method is appropriate method for subtraction.

70. How many bits we use in half subtractor for subtraction?

Ans. only two bits.

71. Can we use parallel adder for subtraction?

Ans. We can use parallel adder using 2's complement method.

72. Which one is better subtractor or parallel adder for subtraction?

Ans. Parallel adder is the best option using 1's complement or 2's complement

73. Which adder is used for addition of BCD numbers?

Ans. BCD adder.

74.What is comparator?

Ans. Comparator compares the inputs (bits).

75. What are universal gates?

Ans. NAND, NOR

76. What is the full form of BCD?

Ans. Binary Coded decimal.

77. What is the base of binary number system? Ans. 2

78. How many bits are there in one byte?

Ans. 8

79. How many digits are there in octal number system?

Ans. 8

80. What is the binary no. equivalent to decimal no. 20?

Ans. 10100

81.A binary digit is called?

Ans. Bit.

81 Define Gates.

Ans. Gates are digital circuit, which perform a specific type of logical operation.

82 Define IC?

Ans. IC means Integrated Circuit It is the integration of no. of components on a common substrate.

83 (A+A), A=?
Ans. A.
84. Define universal gates
Ans. We can design any type of logical expression by using universal gates.
85 Will the output of a NAND Gate be 0.
Ans. When all the inputs are1.
86 Which IC is used for NAND GATE?
Ans. IC 7400.
87 Why NAND is called as universal gate?
Ans.Because all gates can be made using circuits.
88 Name any other universal gate?
Ans. NOR Gate.
89 Which type of TTL gates can drive CMOS Gate?
Ans. TTL with open collector can derive CMOS.
90 What is meant by literal?
Ans. A logical variable in a complemented or Un-complemented form is called a literal.

Dead Links

- https://vivaquestions.com/logic-gates-viva-questions/
- https://vivaquestions.com/digital-electronics-viva-questions/
- https://www.wisdomjobs.com/e-university/digital-logic-design-interview-questions.html