PSoC® Creator™
Project Datasheet for notoriOS

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1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C58LP series member PSoC 5LP device. For details on all the systems listed above, please refer to the PSoC 5LP Technical Reference Manual.

Figure 1. CY8C58LP Device Series Block Diagram

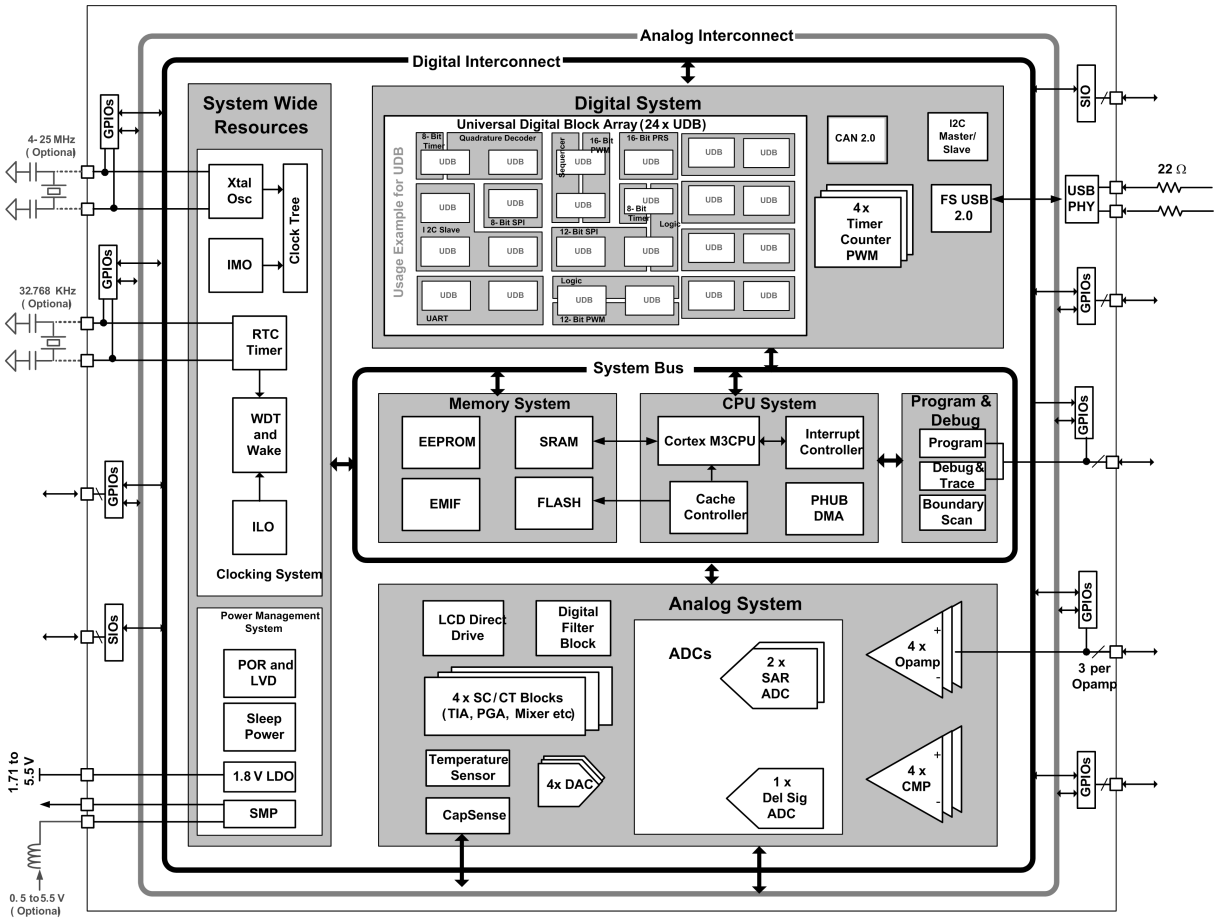


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C5888LTI-LP097
Package Name	68-QFN
Family	PSoC 5LP
Series	CY8C58LP
Max CPU speed (MHz)	0
Flash size (kB)	256
SRAM size (kB)	64
EEPROM size (bytes)	2048
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85
JTAG ID	0x2E161069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

Table 2. Device Resources

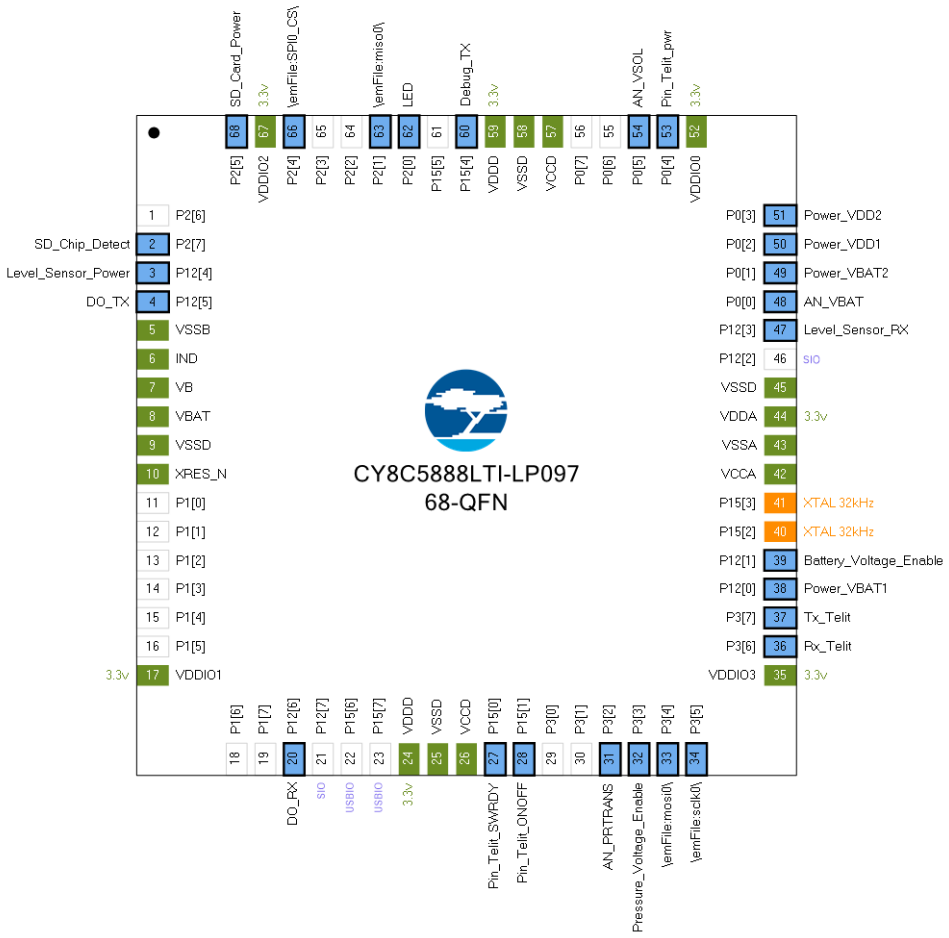
Resource Type	Used	Free	Max	% Used
Digital Clocks	6	2	8	75.00 %
Analog Clocks	1	3	4	25.00 %
CapSense Buffers	0	2	2	0.00 %
Digital Filter Block	0	1	1	0.00 %
Interrupts	6	26	32	18.75 %
IO	28	20	48	58.33 %
Segment LCD	0	1	1	0.00 %
CAN 2.0b	0	1	1	0.00 %
I2C	0	1	1	0.00 %
USB	0	1	1	0.00 %
DMA Channels	0	24	24	0.00 %
Timer	0	4	4	0.00 %
UDB				
Macrocells	91	101	192	47.40 %
Unique P-terms	179	205	384	46.61 %
Total P-terms	212			
Datapath Cells	10	14	24	41.67 %
Status Cells	12	12	24	50.00 %
StatusI Registers	8			
Routed Count7 Load/Enable	4			
Control Cells	6	18	24	25.00 %
Control Registers	2			
Count7 Cells	4			
Opamp	0	4	4	0.00 %
Comparator	1	3	4	25.00 %
Delta-Sigma ADC	1	0	1	100.00 %
LPF	0	2	2	0.00 %
SAR ADC	0	2	2	0.00 %
Analog (SC/CT) Blocks	0	4	4	0.00 %
DAC				

Resource Type	Used	Free	Max	% Used
VIDAC	0	4	4	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[6]	GPIO [unused]			HiZ Analog Unb
2	P2[7]	SD_Chip_Detect	Software In/Out	Strong drive	HiZ Analog Unb
3	P12[4]	Level_Sensor_Power	Software In/Out	Strong drive	HiZ Analog Unb
4	P12[5]	DO_TX	Dgtl Out	Strong drive	HiZ Analog Unb
5	VSSB	VSSB	Dedicated		
6	IND	IND	Dedicated		
7	VB	VB	Dedicated		
8	VBAT	VBAT	Dedicated		
9	VSSD	VSSD	Power		
10	XRES_N	XRES_N	Dedicated		
11	P1[0]	GPIO [unused]			HiZ Analog Unb
12	P1[1]	GPIO [unused]			HiZ Analog Unb
13	P1[2]	GPIO [unused]			HiZ Analog Unb
14	P1[3]	GPIO [unused]			HiZ Analog Unb
15	P1[4]	GPIO [unused]			HiZ Analog Unb
16	P1[5]	GPIO [unused]			HiZ Analog Unb
17	VDDIO1	VDDIO1	Power		
18	P1[6]	GPIO [unused]			HiZ Analog Unb
19	P1[7]	GPIO [unused]			HiZ Analog Unb
20	P12[6]	DO_RX	Dgtl In	HiZ digital	HiZ Analog Unb
21	P12[7]	SIO [unused]			HiZ Analog Unb
22	P15[6]	USB IO [unused]			HiZ Analog Unb
23	P15[7]	USB IO [unused]			HiZ Analog Unb
24	VDDD	VDDD	Power		
25	VSSD	VSSD	Power		
26	VCCD	VCCD	Power		
27	P15[0]	Pin_Telit_SWRDY	Software In/Out	Strong drive	HiZ Analog Unb
28	P15[1]	Pin_Telit_ONOFF	Software In/Out	Strong drive	HiZ Analog Unb
29	P3[0]	GPIO [unused]			HiZ Analog Unb
30	P3[1]	GPIO [unused]			HiZ Analog Unb
31	P3[2]	AN_PRTRANS	Analog	HiZ analog	HiZ Analog Unb
32	P3[3]	Pressure_Voltage_Enable	Software In/Out	Strong drive	HiZ Analog Unb
33	P3[4]	\emFile:mosi0\	Dgtl Out	Strong drive	HiZ Analog Unb
34	P3[5]	\emFile:sclk0\	Dgtl Out	Strong drive	HiZ Analog Unb
35	VDDIO3	VDDIO3	Power		
36	P3[6]	Rx_Telit	Dgtl In	HiZ digital	HiZ Analog Unb
37	P3[7]	Tx_Telit	Dgtl Out	Strong drive	HiZ Analog Unb
38	P12[0]	Power_VBAT1	Software In/Out	Strong drive	HiZ Analog Unb
39	P12[1]	Battery_Voltage_Enable	Software In/Out	Strong drive	HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
40	P15[2]	XTAL 32kHz:Xi	Reserved		
41	P15[3]	XTAL 32kHz:Xi	Reserved		
42	VCCA	VCCA	Power		
43	VSSA	VSSA	Power		
44	VDDA	VDDA	Power		
45	VSSD	VSSD	Power		
46	P12[2]	SIO [unused]			HiZ Analog Unb
47	P12[3]	Level_Sensor_RX	Dgtl In	Strong drive	HiZ Analog Unb
48	P0[0]	AN_VBAT	Analog	HiZ analog	HiZ Analog Unb
49	P0[1]	Power_VBAT2	Software In/Out	Strong drive	HiZ Analog Unb
50	P0[2]	Power_VDD1	Software In/Out	Strong drive	HiZ Analog Unb
51	P0[3]	Power_VDD2	Software In/Out	Strong drive	HiZ Analog Unb
52	VDDIO0	VDDIO0	Power		
53	P0[4]	Pin_Telit_pwr	Software In/Out	Strong drive	HiZ Analog Unb
54	P0[5]	AN_VSOL	Analog	HiZ analog	HiZ Analog Unb
55	P0[6]	GPIO [unused]			HiZ Analog Unb
56	P0[7]	GPIO [unused]			HiZ Analog Unb
57	VCCD	VCCD	Power		
58	VSSD	VSSD	Power		
59	VDDD	VDDD	Power		
60	P15[4]	Debug_TX	Dgtl Out	Strong drive	HiZ Analog Unb
61	P15[5]	GPIO [unused]			HiZ Analog Unb
62	P2[0]	LED	Software In/Out	Strong drive	HiZ Analog Unb
63	P2[1]	\emFile:miso0\	Dgtl In	HiZ digital	HiZ Analog Unb
64	P2[2]	GPIO [unused]			HiZ Analog Unb
65	P2[3]	GPIO [unused]			HiZ Analog Unb
66	P2[4]	\emFile:SPI0_CS\	Software In/Out	Strong drive	HiZ Analog Unb
67	VDDIO2	VDDIO2	Power		
68	P2[5]	SD_Card_Power	Software In/Out	Strong drive	HiZ Analog Unb

Abbreviations used in Table 3 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- HiZ analog = High impedance analog

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode	Reset State
P0[0]	48	AN_VBAT	Analog	HiZ analog	HiZ Analog Unb
P0[1]	49	Power_VBAT2	Software In/Out	Strong drive	HiZ Analog Unb
P0[2]	50	Power_VDD1	Software In/Out	Strong drive	HiZ Analog Unb
P0[3]	51	Power_VDD2	Software In/Out	Strong drive	HiZ Analog Unb
P0[4]	53	Pin_Telit_pwr	Software In/Out	Strong drive	HiZ Analog Unb
P0[5]	54	AN_VSOL	Analog	HiZ analog	HiZ Analog Unb
P0[6]	55	GPIO [unused]			HiZ Analog Unb
P0[7]	56	GPIO [unused]			HiZ Analog Unb
P1[0]	11	GPIO [unused]			HiZ Analog Unb
P1[1]	12	GPIO [unused]			HiZ Analog Unb
P1[2]	13	GPIO [unused]			HiZ Analog Unb
P1[3]	14	GPIO [unused]			HiZ Analog Unb
P1[4]	15	GPIO [unused]			HiZ Analog Unb
P1[5]	16	GPIO [unused]			HiZ Analog Unb
P1[6]	18	GPIO [unused]			HiZ Analog Unb
P1[7]	19	GPIO [unused]			HiZ Analog Unb
P12[0]	38	Power_VBAT1	Software In/Out	Strong drive	HiZ Analog Unb
P12[1]	39	Battery_Voltage_Enable	Software In/Out	Strong drive	HiZ Analog Unb
P12[2]	46	SIO [unused]			HiZ Analog Unb
P12[3]	47	Level_Sensor_RX	Dgtl In	Strong drive	HiZ Analog Unb
P12[4]	3	Level_Sensor_Power	Software In/Out	Strong drive	HiZ Analog Unb
P12[5]	4	DO_TX	Dgtl Out	Strong drive	HiZ Analog Unb
P12[6]	20	DO_RX	Dgtl In	HiZ digital	HiZ Analog Unb
P12[7]	21	SIO [unused]			HiZ Analog Unb
P15[0]	27	Pin_Telit_SWRDY	Software In/Out	Strong drive	HiZ Analog Unb
P15[1]	28	Pin_Telit_ONOFF	Software In/Out	Strong drive	HiZ Analog Unb
P15[2]	40	XTAL 32kHz:Xi	Reserved		
P15[3]	41	XTAL 32kHz:Xi	Reserved		
P15[4]	60	Debug_TX	Dgtl Out	Strong drive	HiZ Analog Unb
P15[5]	61	GPIO [unused]			HiZ Analog Unb
P15[6]	22	USB IO [unused]			HiZ Analog Unb
P15[7]	23	USB IO [unused]			HiZ Analog Unb
P2[0]	62	LED	Software In/Out	Strong drive	HiZ Analog Unb
P2[1]	63	\emFile:miso0\	Dgtl In	HiZ digital	HiZ Analog Unb
P2[2]	64	GPIO [unused]			HiZ Analog Unb
P2[3]	65	GPIO [unused]			HiZ Analog Unb

Port	Pin	Name	Type	Drive Mode	Reset State
P2[4]	66	\emFile:SPI0_CS\	Software In/Out	Strong drive	HiZ Analog Unb
P2[5]	68	SD_Card_Power	Software In/Out	Strong drive	HiZ Analog Unb
P2[6]	1	GPIO [unused]			HiZ Analog Unb
P2[7]	2	SD_Chip_Detect	Software In/Out	Strong drive	HiZ Analog Unb
P3[0]	29	GPIO [unused]			HiZ Analog Unb
P3[1]	30	GPIO [unused]			HiZ Analog Unb
P3[2]	31	AN_PRTRANS	Analog	HiZ analog	HiZ Analog Unb
P3[3]	32	Pressure_Voltage_Enable	Software In/Out	Strong drive	HiZ Analog Unb
P3[4]	33	\emFile:mosi0\	Dgtl Out	Strong drive	HiZ Analog Unb
P3[5]	34	\emFile:sclk0\	Dgtl Out	Strong drive	HiZ Analog Unb
P3[6]	36	Rx_Telit	Dgtl In	HiZ digital	HiZ Analog Unb
P3[7]	37	Tx_Telit	Dgtl Out	Strong drive	HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- HiZ analog = High impedance analog
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- Dgtl Out = Digital Output
- HiZ digital = High impedance digital

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type	Reset State
\emFile:miso0\	P2[1]	Dgtl In	HiZ Analog Unb
\emFile:mosi0\	P3[4]	Dgtl Out	HiZ Analog Unb
\emFile:sclk0\	P3[5]	Dgtl Out	HiZ Analog Unb
\emFile:SPI0_CS\	P2[4]	Software In/Out	HiZ Analog Unb
AN_PRTRANS	P3[2]	Analog	HiZ Analog Unb
AN_VBAT	P0[0]	Analog	HiZ Analog Unb
AN_VSOL	P0[5]	Analog	HiZ Analog Unb
Battery_Voltage_Enable	P12[1]	Software In/Out	HiZ Analog Unb
Debug_TX	P15[4]	Dgtl Out	HiZ Analog Unb
DO_RX	P12[6]	Dgtl In	HiZ Analog Unb
DO_TX	P12[5]	Dgtl Out	HiZ Analog Unb
GPIO [unused]	P3[1]		HiZ Analog Unb
GPIO [unused]	P3[0]		HiZ Analog Unb
GPIO [unused]	P2[6]		HiZ Analog Unb
GPIO [unused]	P2[2]		HiZ Analog Unb
GPIO [unused]	P2[3]		HiZ Analog Unb
GPIO [unused]	P15[5]		HiZ Analog Unb
GPIO [unused]	P0[6]		HiZ Analog Unb
GPIO [unused]	P0[7]		HiZ Analog Unb
GPIO [unused]	P1[5]		HiZ Analog Unb
GPIO [unused]	P1[4]		HiZ Analog Unb
GPIO [unused]	P1[1]		HiZ Analog Unb
GPIO [unused]	P1[6]		HiZ Analog Unb
GPIO [unused]	P1[0]		HiZ Analog Unb
GPIO [unused]	P1[3]		HiZ Analog Unb
GPIO [unused]	P1[2]		HiZ Analog Unb
GPIO [unused]	P1[7]		HiZ Analog Unb
LED	P2[0]	Software In/Out	HiZ Analog Unb
Level_Sensor_Power	P12[4]	Software In/Out	HiZ Analog Unb
Level_Sensor_RX	P12[3]	Dgtl In	HiZ Analog Unb
Pin_Telit_ONOFF	P15[1]	Software In/Out	HiZ Analog Unb
Pin_Telit_pwr	P0[4]	Software In/Out	HiZ Analog Unb
Pin_Telit_SWRDY	P15[0]	Software In/Out	HiZ Analog Unb
Power_VBAT1	P12[0]	Software In/Out	HiZ Analog Unb
Power_VBAT2	P0[1]	Software In/Out	HiZ Analog Unb
Power_VDD1	P0[2]	Software In/Out	HiZ Analog Unb

Name	Port	Type	Reset State
Power_VDD2	P0[3]	Software In/Out	HiZ Analog Unb
Pressure_Voltage_Enable	P3[3]	Software In/Out	HiZ Analog Unb
Rx_Telit	P3[6]	Dgtl In	HiZ Analog Unb
SD_Card_Power	P2[5]	Software In/Out	HiZ Analog Unb
SD_Chip_Detect	P2[7]	Software In/Out	HiZ Analog Unb
SIO [unused]	P12[7]		HiZ Analog Unb
SIO [unused]	P12[2]		HiZ Analog Unb
Tx_Telit	P3[7]	Dgtl Out	HiZ Analog Unb
USB IO [unused]	P15[7]		HiZ Analog Unb
USB IO [unused]	P15[6]		HiZ Analog Unb
XTAL 32kHz:Xi	P15[3]	Reserved	
XTAL 32kHz:Xi	P15[2]	Reserved	

Abbreviations used in Table 5 have the following meanings:

- Dgtl In = Digital Input
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x4000
Stack Size (bytes)	0x1000
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	GPIO
Enable Device Protection	False
Embedded Trace (ETM)	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

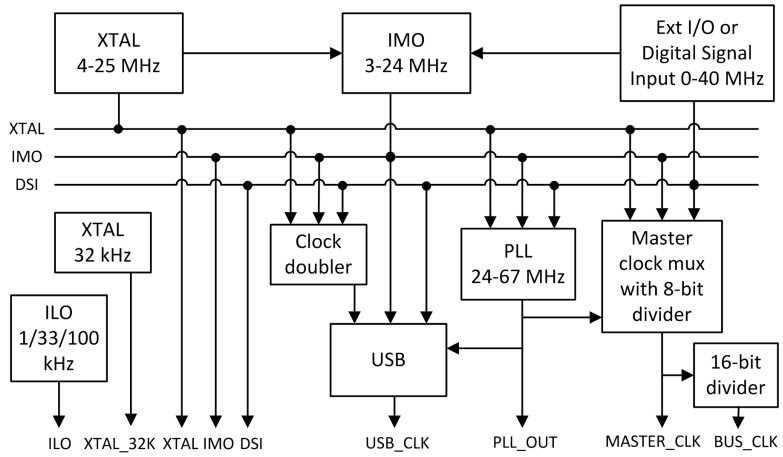
Name	Value
VDDA (V)	3.3
VDDD (V)	3.3
VDDIO0 (V)	3.3
VDDIO1 (V)	3.3
VDDIO2 (V)	3.3
VDDIO3 (V)	3.3
Variable VDDA	False
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 74.7 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 80 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 80 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
BUS_CLK	DIGITAL	MASTER_CLK	? MHz	24 MHz	±4	True	True
MASTER_CLK	DIGITAL	PLL_OUT	? MHz	24 MHz	±4	True	True
IMO	DIGITAL		24 MHz	24 MHz	±4	True	True
PLL_OUT	DIGITAL	IMO	24 MHz	24 MHz	±4	True	True
XTAL 32kHz	DIGITAL		32.768 kHz	32.768 kHz	±0	False	True
ILO	DIGITAL		? MHz	1 kHz	-50,+100	True	True
USB_CLK	DIGITAL	IMO	48 MHz	? MHz	±0	False	False
Digital Signal	DIGITAL		? MHz	? MHz	±0	False	False
XTAL	DIGITAL		24 MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

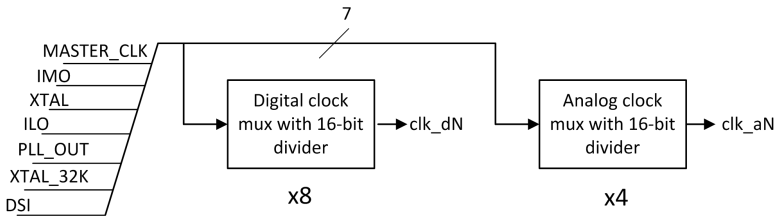


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
emFile_Clock_1	DIGITAL	MASTER_CLK	? MHz	24 MHz	±4	True	True
ADC_Ext_CP_-Clk	DIGITAL	MASTER_CLK	? MHz	24 MHz	±4	True	True
Debug_UART_-IntClock	DIGITAL	IMO	921.6 kHz	923.077 kHz	±4	True	True
UART_Telit_-IntClock	DIGITAL	IMO	921.6 kHz	923.077 kHz	±4	True	True
ADC_theACLK	ANALOG	MASTER_CLK	172 kHz	171.429 kHz	±4	True	True
DO_UART_-IntClock	DIGITAL	IMO	76.8 kHz	76.677 kHz	±4	True	True
Clock_IMO	DIGITAL	MASTER_CLK	76.8 kHz	76.677 kHz	±4	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 5LP Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CyPLL API routines
  - CyIMO API routines
  - CyILO API routines
  - CyMaster API routines
  - CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	Vector	Priority
DO_ISR	0	0	7
Level_Sensor_ISR	1	1	7
RTC_isr	2	2	7
isr_SleepTimer	3	3	7
isr_telit_rx	4	4	7
ADC_IRQ	29	29	7

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 5LP Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 5LP devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x3FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

For more information on Flash memory and protection, please refer to:

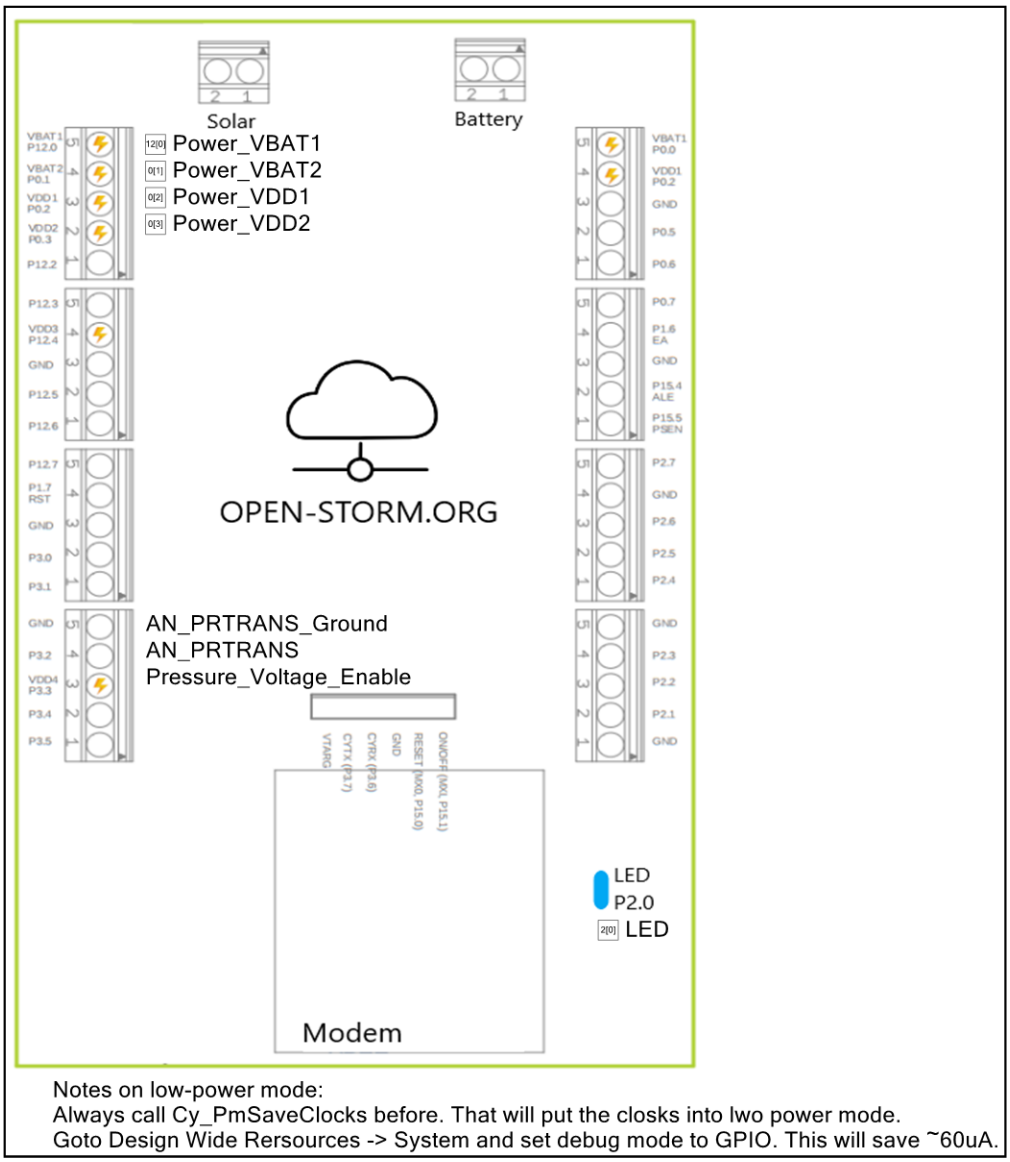
- Flash Protection chapter in the PSoC 5LP Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyWrite API routines
  - CyFlash API routines

7 Design Contents

This design's schematic content consists of the following 2 schematic sheets:

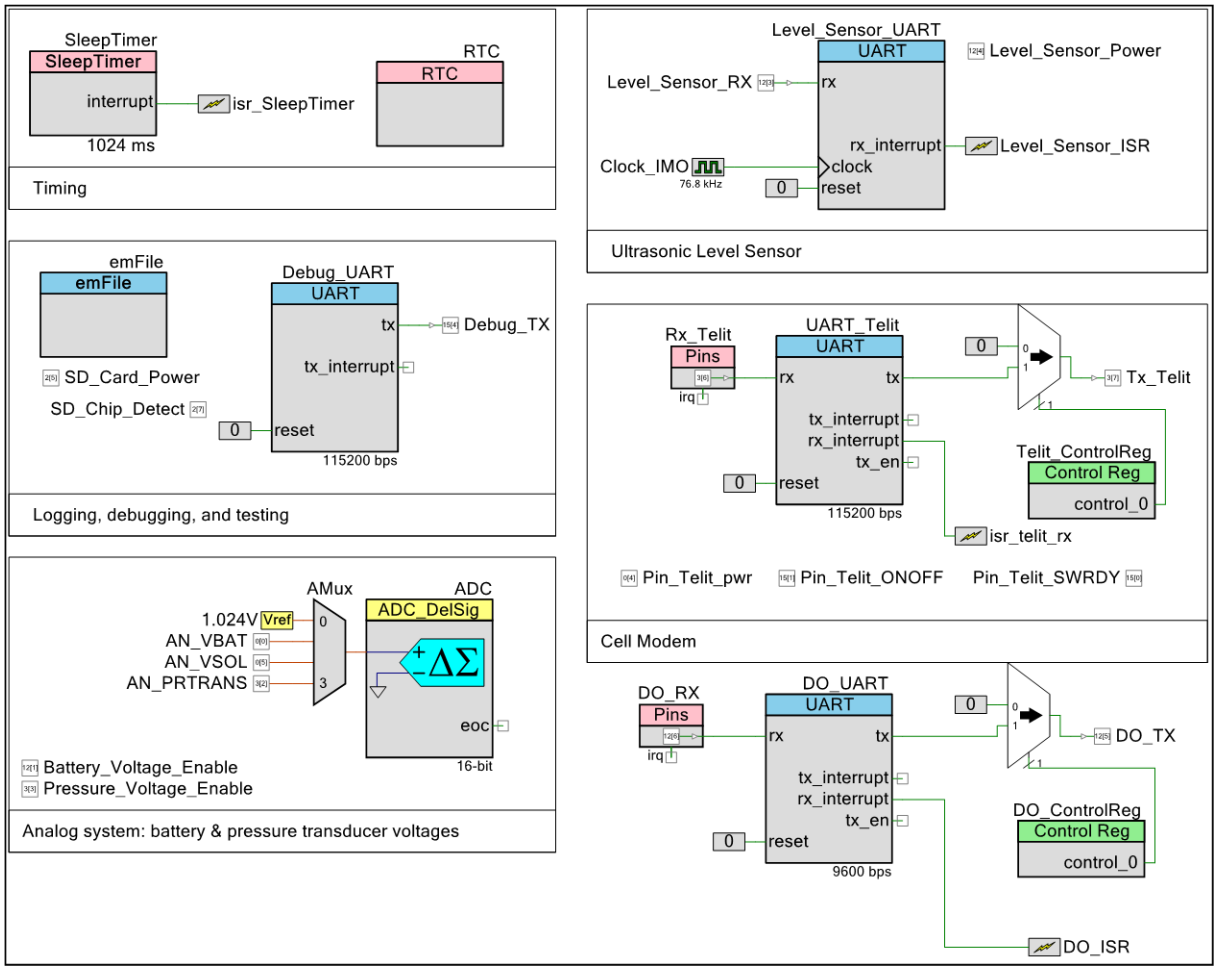
7.1 Schematic Sheet: Board Overview

Figure 5. Schematic Sheet: Board Overview



7.2 Schematic Sheet: Core

Figure 6. Schematic Sheet: Core



This schematic sheet contains the following component instances:

- Instance ADC (type: ADC_DelSig_v3_30)
- Instance AMux (type: AMux_v1_80)
- Instance Debug_UART (type: UART_v2_50)
- Instance DO_ControlReg (type: CyControlReg_v1_80)
- Instance DO_UART (type: UART_v2_50)
- Instance emFile (type: emFile_v1_20)
- Instance Level_Sensor_UART (type: UART_v2_50)
- Instance RTC (type: RTC_v2_0)
- Instance SleepTimer (type: SleepTimer_v3_20)
- Instance Telit_ControlReg (type: CyControlReg_v1_80)
- Instance telit_mux (type: mux_v1_10)
- Instance telit_mux_1 (type: mux_v1_10)
- Instance UART_Telit (type: UART_v2_50)

8 Components

8.1 Component type: ADC_DelSig [v3.30]

8.1.1 Instance ADC

Description: Delta-Sigma ADC
Instance type: ADC_DelSig [v3.30]
Datasheet: online component datasheet for ADC_DelSig

Table 13. Component Parameters for ADC

Parameter Name	Value	Description
ADC_Alignment	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config2	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config3	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config4	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Charge_Pump_Clock	false	Low power charge pump clock selection
ADC_Clock	Internal	Parameter for selecting the ADC clock type.
ADC_Input_Mode	Single	Differential or Single ended input mode
ADC_Input_Range	0.0 to 6*Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config2	0.0 to Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config3	0.0 to Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config4	0.0 to Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Power	Medium Power	Sets power level of ADC.
ADC_Reference	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config2	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config3	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config4	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Resolution	16	ADC Resolution in bits
ADC_Resolution_Config2	16	ADC Resolution in bits
ADC_Resolution_Config3	16	ADC Resolution in bits
ADC_Resolution_Config4	16	ADC Resolution in bits

Parameter Name	Value	Description
Clock_Frequency	64000	Determines the ADC clock frequency.
Comment_Config1	Default Config	Parameter which holds the user comment for the config1.
Comment_Config2	Second Config	Parameter which holds the user comment for the config2.
Comment_Config3	Third Config	Parameter which holds the user comment for the config3.
Comment_Config4	Fourth Config	Parameter which holds the user comment for the config4.
Config1_Name	CFG1	This parameter is used to create constants in the header file for config 1.
Config2_Name	CFG2	This parameter is used to create constants in the header file for config 2.
Config3_Name	CFG3	This parameter is used to create constants in the header file for config 3.
Config4_Name	CFG4	This parameter is used to create constants in the header file for config 4.
Configs	4	Number of active configurations
Conversion_Mode	0 - Single Sample	ADC conversion mode
Conversion_Mode_Config2	2 - Continuous	ADC conversion mode
Conversion_Mode_Config3	2 - Continuous	ADC conversion mode
Conversion_Mode_Config4	2 - Continuous	ADC conversion mode
Enable_Vref_Vss	false	Determines whether or not to connect ADC's reference Vssa to AGL[6].
EnableModulatorInput	false	When this parameter is enabled, the modulator input terminal will be enabled on the symbol.
Input_Buffer_Gain	1	Gain of input amplifier
Input_Buffer_Gain_Config2	1	Gain of input amplifier
Input_Buffer_Gain_Config3	1	Gain of input amplifier
Input_Buffer_Gain_Config4	1	Gain of input amplifier
Input_Buffer_Mode	Bypass Buffer	Buffer Mode type selection
Input_Buffer_Mode_Config2	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config3	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config4	Rail to Rail	Buffer Mode type selection
Ref_Voltage	1.024	Set reference voltage
Ref_Voltage_Config2	1.024	Set reference voltage
Ref_Voltage_Config3	1.024	Set reference voltage
Ref_Voltage_Config4	1.024	Set reference voltage
rm_int	false	Removes internal interrupt (IRQ)
Sample_Rate	616	Sample Rate in Hz
Sample_Rate_Config2	10000	Sample Rate in Hz
Sample_Rate_Config3	10000	Sample Rate in Hz
Sample_Rate_Config4	10000	Sample Rate in Hz
Start_of_Conversion	Software	Continuous conversions or hardware controlled
User Comments		Instance-specific comments.

8.2 Component type: AMux [v1.80]

8.2.1 Instance AMux

Description: Multiplexer used to route analog signals.
Instance type: AMux [v1.80]
Datasheet: online component datasheet for AMux

Table 14. Component Parameters for AMux

Parameter Name	Value	Description
AtMostOneActive	false	Limit to at most one active channel.
Channels	4	Channel count.
Isolation	Maximum	Specify minimum, medium, or maximum switch control; affects channel isolation and switching time.
MuxType	Single	Select between single or differential inputs.
User Comments		Instance-specific comments.

8.3 Component type: CyControlReg [v1.80]

8.3.1 Instance DO_ControlReg

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 15. Component Parameters for DO_ControlReg

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)
User Comments		Instance-specific comments.

8.3.2 Instance Telit_ControlReg

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 16. Component Parameters for Telit_ControlReg

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)
User Comments		Instance-specific comments.

8.4 Component type: emFile [v1.20]

8.4.1 Instance emFile

Description: emFile file system for SD card in SPI mode
Instance type: emFile [v1.20]
Datasheet: online component datasheet for emFile

Table 17. Component Parameters for emFile

Parameter Name	Value	Description
Max_SPI_Frequency	4000	Maximum frequency (in kHz) of the SPI Master serial clock (sclk). See the SPI Master data sheet for details.
NumberSDCards	1	The number of SD cards in the system. The maximum is four (4).
User Comments		Instance-specific comments.
WP0_En	false	Enable write protect signal for SD card #1. If disabled the SD card isn't write protected.
WP1_En	false	Enable write protect signal for SD card #2. If disabled the SD card is not write protected.
WP2_En	false	Enable write protect signal for SD card #3. If disabled the SD card is not write protected.
WP3_En	false	Enable write protect signal for SD card #4. If disabled the SD card is not write protected.

8.5 Component type: mux [v1.10]

8.5.1 Instance telit_mux

Description: Multiplexer with configurable number of input terminals and terminal width.
Instance type: mux [v1.10]

Datasheet: online component datasheet for mux

Table 18. Component Parameters for telit_mux

Parameter Name	Value	Description
NumInputTerminals	2	Number of inputs required for the Multiplexer. Acceptable values are 2, 4, 8, and 16.
TerminalWidth	1	Width of each terminal
User Comments		Instance-specific comments.

8.5.2 Instance telit_mux_1

Description: Multiplexer with configurable number of input terminals and terminal width.
Instance type: mux [v1.10]
Datasheet: online component datasheet for mux

Table 19. Component Parameters for telit_mux_1

Parameter Name	Value	Description
NumInputTerminals	2	Number of inputs required for the Multiplexer. Acceptable values are 2, 4, 8, and 16.
TerminalWidth	1	Width of each terminal
User Comments		Instance-specific comments.

8.6 Component type: RTC [v2.0]

8.6.1 Instance RTC

Description: Real Time Clock
Instance type: RTC [v2.0]
Datasheet: online component datasheet for RTC

Table 20. Component Parameters for RTC

Parameter Name	Value	Description
DstEnable	false	Enable Data Saving Time
StartOfWeek	Sunday	Start of new week
User Comments		Instance-specific comments.

8.7 Component type: SleepTimer [v3.20]

8.7.1 Instance SleepTimer

Description: The Sleep Timer component
Instance type: SleepTimer [v3.20]
Datasheet: online component datasheet for SleepTimer

Table 21. Component Parameters for SleepTimer

Parameter Name	Value	Description
EnableInt	true	Determines whether the sleep timer interrupt is enabled or disabled.
Interval	CTW_1024_MS	Parameter that defines the wake up interval in milliseconds.
User Comments		Instance-specific comments.

8.8 Component type: UART [v2.50]

8.8.1 Instance Debug_UART

Description: Universal Asynchronous Receiver Transmitter
Instance type: UART [v2.50]
Datasheet: online component datasheet for UART

Table 22. Component Parameters for Debug_UART

Parameter Name	Value	Description
Address1	0	This parameter specifies the RX Hardware Address #1.
Address2	0	This parameter specifies the RX Hardware Address #2.
BaudRate	115200	Sets the target baud rate.
BreakBitsRX	13	Specifies the break signal length for the RX (detection) channel.
BreakBitsTX	13	Specifies the break signal length for the TX channel.
BreakDetect	false	Enables the break detect hardware.
CRCoutputsEn	false	Enables the CRC outputs.
EnIntRXInterrupt	false	Enables the internal RX interrupt configuration and the ISR.
EnIntTXInterrupt	false	Enables the internal TX interrupt configuration and the ISR.
FlowControl	None	Enable the flow control signals.
HalfDuplexEn	false	Enables half duplex mode on the RX Half of the UART module.
HwTXEnSignal	false	Enables the external TX enable signal output.
InternalClock	true	Enables the internal clock. This parameter removes the clock input pin.
InterruptOnTXComplete	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event.
InterruptOnTXFifoEmpty	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event.
InterruptOnTXFifoFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event.
InterruptOnTXFifoNotFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event.
IntOnAddressDetect	false	Enables the interrupt on hardware address detected event by default
IntOnAddressMatch	false	Enables the interrupt on hardware address match detected event by default
IntOnBreak	false	Enables the interrupt on break signal detected event by default

Parameter Name	Value	Description
IntOnByteRcvd	false	Enables the interrupt on RX byte received event by default
IntOnOverrunError	false	Enables the interrupt on overrun error event by default
IntOnParityError	false	Enables the interrupt on parity error event by default
IntOnStopError	false	Enables the interrupt on stop error event by default
NumDataBits	8	Defines the number of data bits. Values can be 5, 6, 7 or 8 bits.
NumStopBits	1	Defines the number of stop bits. Values can be 1 or 2 bits.
OverSamplingRate	8	This parameter defines the over sampling rate.
ParityType	None	Sets the parity type as Odd, Even or Mark/Space
ParityTypeSw	false	This parameter allows the parity type to be changed through software by using the WriteControlRegister API
RXAddressMode	None	Configures the RX hardware address detection mode
RXBufferSize	4	The size of the RAM space allocated for the RX input buffer.
RXEnable	false	Enables the RX in the UART
TXBitClkGenDP	true	When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7.
TXBufferSize	4	The size of the RAM space allocated for the TX output buffer.
TXEnable	true	Enables the TX in the UART
Use23Polling	true	Allows the use of 2 out of 3 polling resources on the RX UART sampler.
User Comments		Instance-specific comments.

8.8.2 Instance DO_UART

Description: Universal Asynchronous Receiver Transmitter
Instance type: UART [v2.50]
Datasheet: online component datasheet for UART

Table 23. Component Parameters for DO_UART

Parameter Name	Value	Description
Address1	0	This parameter specifies the RX Hardware Address #1.
Address2	0	This parameter specifies the RX Hardware Address #2.
BaudRate	9600	Sets the target baud rate.
BreakBitsRX	13	Specifies the break signal length for the RX (detection) channel.

Parameter Name	Value	Description
BreakBitsTX	13	Specifies the break signal length for the TX channel.
BreakDetect	false	Enables the break detect hardware.
CRCoutputsEn	false	Enables the CRC outputs.
EnIntRXInterrupt	false	Enables the internal RX interrupt configuration and the ISR.
EnIntTXInterrupt	false	Enables the internal TX interrupt configuration and the ISR.
FlowControl	None	Enable the flow control signals.
HalfDuplexEn	false	Enables half duplex mode on the RX Half of the UART module.
HwTXEnSignal	true	Enables the external TX enable signal output.
InternalClock	true	Enables the internal clock. This parameter removes the clock input pin.
InterruptOnTXComplete	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event.
InterruptOnTXFifoEmpty	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event.
InterruptOnTXFifoFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event.
InterruptOnTXFifoNotFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event.
IntOnAddressDetect	false	Enables the interrupt on hardware address detected event by default
IntOnAddressMatch	false	Enables the interrupt on hardware address match detected event by default
IntOnBreak	false	Enables the interrupt on break signal detected event by default
IntOnByteRcvd	true	Enables the interrupt on RX byte received event by default
IntOnOverrunError	false	Enables the interrupt on overrun error event by default
IntOnParityError	false	Enables the interrupt on parity error event by default
IntOnStopError	false	Enables the interrupt on stop error event by default
NumDataBits	8	Defines the number of data bits. Values can be 5, 6, 7 or 8 bits.
NumStopBits	1	Defines the number of stop bits. Values can be 1 or 2 bits.
OverSamplingRate	8	This parameter defines the over sampling rate.
ParityType	None	Sets the parity type as Odd, Even or Mark/Space

Parameter Name	Value	Description
ParityTypeSw	false	This parameter allows the parity type to be changed through software by using the WriteControlRegister API
RXAddressMode	None	Configures the RX hardware address detection mode
RXBufferSize	4	The size of the RAM space allocated for the RX input buffer.
RXEnable	true	Enables the RX in the UART
TXBitClkGenDP	true	When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7.
TXBufferSize	4	The size of the RAM space allocated for the TX output buffer.
TXEnable	true	Enables the TX in the UART
Use23Polling	true	Allows the use of 2 out of 3 polling resources on the RX UART sampler.
User Comments		Instance-specific comments.

8.8.3 Instance Level_Sensor_UART

Description: Universal Asynchronous Receiver Transmitter
Instance type: UART [v2.50]
Datasheet: online component datasheet for UART

Table 24. Component Parameters for Level_Sensor_UART

Parameter Name	Value	Description
Address1	0	This parameter specifies the RX Hardware Address #1.
Address2	0	This parameter specifies the RX Hardware Address #2.
BaudRate	9600	Sets the target baud rate.
BreakBitsRX	13	Specifies the break signal length for the RX (detection) channel.
BreakBitsTX	13	Specifies the break signal length for the TX channel.
BreakDetect	false	Enables the break detect hardware.
CRCoutputsEn	false	Enables the CRC outputs.
EnIntRXInterrupt	false	Enables the internal RX interrupt configuration and the ISR.
EnIntTXInterrupt	false	Enables the internal TX interrupt configuration and the ISR.
FlowControl	None	Enable the flow control signals.
HalfDuplexEn	false	Enables half duplex mode on the RX Half of the UART module.
HwTXEnSignal	true	Enables the external TX enable signal output.

Parameter Name	Value	Description
InternalClock	false	Enables the internal clock. This parameter removes the clock input pin.
InterruptOnTXComplete	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event.
InterruptOnTXFifoEmpty	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event.
InterruptOnTXFifoFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event.
InterruptOnTXFifoNotFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event.
IntOnAddressDetect	false	Enables the interrupt on hardware address detected event by default
IntOnAddressMatch	false	Enables the interrupt on hardware address match detected event by default
IntOnBreak	false	Enables the interrupt on break signal detected event by default
IntOnByteRcvd	true	Enables the interrupt on RX byte received event by default
IntOnOverrunError	false	Enables the interrupt on overrun error event by default
IntOnParityError	false	Enables the interrupt on parity error event by default
IntOnStopError	false	Enables the interrupt on stop error event by default
NumDataBits	8	Defines the number of data bits. Values can be 5, 6, 7 or 8 bits.
NumStopBits	1	Defines the number of stop bits. Values can be 1 or 2 bits.
OverSamplingRate	8	This parameter defines the over sampling rate.
ParityType	None	Sets the parity type as Odd, Even or Mark/Space
ParityTypeSw	false	This parameter allows the parity type to be changed through software by using the WriteControlRegister API
RXAddressMode	None	Configures the RX hardware address detection mode
RXBufferSize	4	The size of the RAM space allocated for the RX input buffer.
RXEnable	true	Enables the RX in the UART
TXBitClkGenDP	true	When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7.
TXBufferSize	4	The size of the RAM space allocated for the TX output buffer.
TXEnable	false	Enables the TX in the UART

Parameter Name	Value	Description
Use23Polling	true	Allows the use of 2 out of 3 polling resources on the RX UART sampler.
User Comments		Instance-specific comments.

8.8.4 Instance UART_Telit

Description: Universal Asynchronous Receiver Transmitter
Instance type: UART [v2.50]
Datasheet: online component datasheet for UART

Table 25. Component Parameters for UART_Telit

Parameter Name	Value	Description
Address1	0	This parameter specifies the RX Hardware Address #1.
Address2	0	This parameter specifies the RX Hardware Address #2.
BaudRate	115200	Sets the target baud rate.
BreakBitsRX	13	Specifies the break signal length for the RX (detection) channel.
BreakBitsTX	13	Specifies the break signal length for the TX channel.
BreakDetect	false	Enables the break detect hardware.
CRCoutputsEn	false	Enables the CRC outputs.
EnIntRXInterrupt	false	Enables the internal RX interrupt configuration and the ISR.
EnIntTXInterrupt	false	Enables the internal TX interrupt configuration and the ISR.
FlowControl	None	Enable the flow control signals.
HalfDuplexEn	false	Enables half duplex mode on the RX Half of the UART module.
HwTXEnSignal	true	Enables the external TX enable signal output.
InternalClock	true	Enables the internal clock. This parameter removes the clock input pin.
InterruptOnTXComplete	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event.
InterruptOnTXFifoEmpty	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event.
InterruptOnTXFifoFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event.
InterruptOnTXFifoNotFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event.
IntOnAddressDetect	false	Enables the interrupt on hardware address detected event by default

Parameter Name	Value	Description
IntOnAddressMatch	false	Enables the interrupt on hardware address match detected event by default
IntOnBreak	false	Enables the interrupt on break signal detected event by default
IntOnByteRcvd	true	Enables the interrupt on RX byte received event by default
IntOnOverrunError	false	Enables the interrupt on overrun error event by default
IntOnParityError	false	Enables the interrupt on parity error event by default
IntOnStopError	false	Enables the interrupt on stop error event by default
NumDataBits	8	Defines the number of data bits. Values can be 5, 6, 7 or 8 bits.
NumStopBits	1	Defines the number of stop bits. Values can be 1 or 2 bits.
OverSamplingRate	8	This parameter defines the over sampling rate.
ParityType	None	Sets the parity type as Odd, Even or Mark/Space
ParityTypeSw	false	This parameter allows the parity type to be changed through software by using the WriteControlRegister API
RXAddressMode	None	Configures the RX hardware address detection mode
RXBufferSize	4	The size of the RAM space allocated for the RX input buffer.
RXEnable	true	Enables the RX in the UART
TXBitClkGenDP	true	When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7.
TXBufferSize	4	The size of the RAM space allocated for the TX output buffer.
TXEnable	true	Enables the TX in the UART
Use23Polling	true	Allows the use of 2 out of 3 polling resources on the RX UART sampler.
User Comments		Instance-specific comments.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5LP register map is covered in the PSoC 5LP Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 5LP Technical Reference Manual
  - Low Power Modes chapter in the PSoC 5LP Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 5LP Technical Reference Manual
  - Cache chapter in the System Reference Guide
    - CyFlushCache() API routine