RAMAIAH Institute of Technology

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(Autonomous Institute, Affiliated to VTU)
(Approved by AICTE, New Delhi & Govt. of Karnataka)
Accredited by NBA & NAAC with 'A+' Grade

SUPPLEMENTARY SEMESTER EXAMINATIONS – SEPTEMBER 2022

Program	:	**B.E. : Computer Science and Engineering**	**Semester**	:	**IV**
Course Name	:	**Microprocessor and Microcontrollers**	**Max. Marks**	:	**100**
Course Code	:	**CS43**	**Duration**	:	**3 Hrs**

Instructions to the Candidates:

- Answer one full question from each unit.
- Write a program in C or Assembly.

UNIT- I

1.	a)	Explain the different abstraction levels in a processor design.	CO1	(06)
	b)	Examine the MU0 simple microprocessor architecture with a neat diagram showing its various registers, and data operations.	CO1	(08)
	c)	List the implementations features of CortexM0 that support low power applications.	CO1	(06)
2.	a)	State the different addressing methods for access data from the memory with examples.	CO1	(08)
	b)	Compare the RISC and CISC instruction set processors and state their advantages and disadvantages.	CO1	(06)
	c)	Discuss the salient system features of CortexM0 processors.	CO1	(06)

UNIT – II

3.	a)	Differentiate between Main stack pointer and Process stack pointer.	CO2	(06)
	b)	Explain memory-remapping implementation with the boot loader and SRAM for fast program accesses.	CO2	(06)
	c)	Discuss the different ways of structuring the embedded programs.	CO2	(08)
4.	a)	Explain the Various programming models employed for embedded system applications examine the critical differences between them.	CO2	(10)
	b)	Discuss the utility of APSR,IPSR, EPSR, Control register and Primask registers.	CO2	(06)
	c)	Discuss the interrupt features available with NVIC support.	CO2	(04)

UNIT – III

5.	a)	Write a program Assembly program to implement Switch case.	CO3	(06)
	b)	Write a neat program to discuss nested loop and stack utility for nested functions.	CO3	(08)
	c)	Find the output of following code i) LDR r2,=0x08000080; LSRS r0,r2,#05;	CO3	(06)

ii) LDR r2,=0x80000080;
ASRS r0,r2,#05;
iii) LDR r2,=0x80000080;
RORS r0,r2,#05;

6.	a)	Write a program to transfer 100 bytes of data from one memory location to another using LDMIA and STMIA instructions.	CO3	(08)
	b)	Write a program to implement for loop and add a array of 10 nos.	CO3	(06)

	c)	Find the output of following code:
		i) LDR r2,=0x80000080;
		SXTB r0,r0
		ii) LDR r2,=0x80000080;
		SXTH r0,r0;
		iii) LDR r2,=0x80000080;
		UXTB r0,r0;
			CO3	(06)

UNIT – IV

7.	a)	List any six available exceptions in Cortex M0 processor with its priority levels?	CO4	(06)
	b)	Illustrate the usage of each region in the memory map of a Cortex M0 Processor. With a neat sketch.	CO4	(10)
	c)	Write the differences between APB and AHB.	CO4	(04)
8.	a)	Explain the following: i) Program Memory ii) Boot Loader.	CO4	(08)
	b)	Write an assembly code to set the priority level of interrupt#2 to 0xC0.	CO4	(07)
	c)	Write a note on Late Arrival with Exception sequences.	CO4	(05)

UNIT – V

9.	a)	List the general features of 8266 Nodemcu microcontroller.	CO5	(08)
	b)	Examine the scarcity of runtime resources of Nodemcu.	CO5	(06)
	c)	Examine the various control pins of LCD 16x2 which are read write and enable data transfer and check if LCD is busy.	CO5	(06)
10.	a)	Explain the Boot process of Nodemcu.	CO5	(05)
	b)	Elaborate on Micropython interpreter its, auto intent and auto completion and soft reset.	CO5	(05)
	c)	Analyse the shortcomings of Nodemcu 8266 in terms of RTC, socket and buffer overflow and SSL/TLS limitations.	CO5	(10)

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