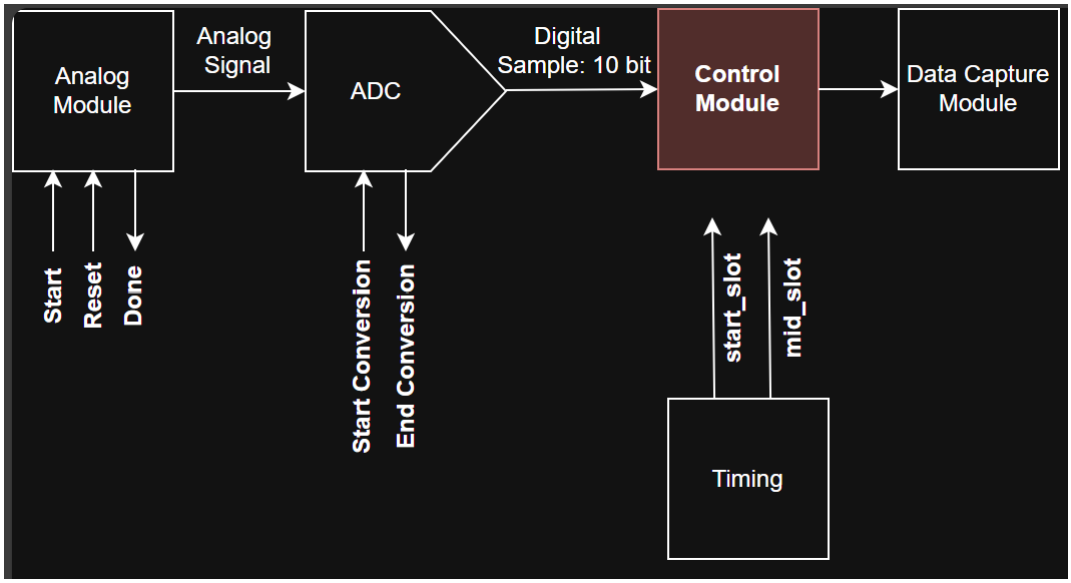
You are tasked with designing a control module that interfaces with multiple modules for data acquisition and storage. The control module works on clock, with clock period T_{ctrl}

Here are the system requirements:



System Components:

1. An analog measurement module
    - Has an active high 'start' signal to trigger a capture
    - Has an active low reset input, which resets the module to start a new capture.
    - Outputs an active high 'done' signal after a variable, unpredictable time period.

2. An ADC which
    - Takes the output from the analog measurement module and converts it to a 10 bit digital value.
    - Requires a trigger signal to start conversion
    - Provides an active high 'end_of_conversion' signal with deterministic timing. The end of 'end_of_conversion' signal is high for a duration $5*T_{ctrl}$
    - Holds the sample value until while the 'end_of_conversion' signal is high

3. A timing module that keeps track of slots
    - Provides an active high 'start_slot' signal to indicate the start of slot
    - Provides an active high 'mid_slot' to indicate a certain point of interest within the slot
    - The slots keep on repeating over time

4. An external module that

- Reads stored data from the control module
- The data is read asynchronously in bursts

Functional Requirements:

1. **Dual Sampling Protocol:** Within each time slot, the control module captures exactly two ADC samples and store them as a correlated pair/tuple

2. **Trigger Management:** The first data capture process is triggered after a programmable delay from the 'start-slot' signal. The second data capture is also triggered after a programmable delay from the 'mid-slot' signal.

3. **Data Integrity:** The correspondence between the two samples in each pair is critical and must be maintained. As in, the samples are treated as pairs for external processing.

4. Storage Management: The system must monitor internal storage capacity and send a trigger signal to the external reading module when storage is running low

5. Continuous Operation: The system runs continuously, capturing sample pairs in each time slot

Please draw a timing diagram, high level RTL design and explain the design considerations (safeguards, bus widths, data integrity guarantee, etc.)