SHARAT HIREMATH

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EDUCATION

Master of Science in Electrical and Electronics Engineering | 3.66 GPA Jan 2024 - Dec 2025
San Jose State University, San Jose, CA
Relevant Courses: Advanced Computer Architectures, Digital System Design and Synthesis, SoC Design & Verification with System Verilog, Logic Verification with UVM, Embedded SoC Design, Computer Vision with Artificial Intelligence Applications, ASIC CMOS Design

Bachelor of Engineering in Electronics and Communication Engineering Aug 2019 - Jun 2023
Visvesvaraya Technological University, Bengaluru, India

TECHNICAL SKILLS

Programming Skills: Verilog HDL, SystemVerilog, UVM, C/C++, Python, Perl Scripting, OOP, Data Structures & Algorithms
Core Skills: Digital Logic Design, Assertions-Based Verification, Scoreboarding & Reference Models, RTL-to-GDSII basics, VLSI design, FPGA design, Constrained Randomization Verification, STA, FSMs, ALUs, Linux, Computer Architecture, GPU Architecture
EDA Tools: Synopsys VCS, Synopsys Design Compiler, Xilinx Vivado, Cadence Virtuoso, Cadence Xcelium, MATLAB
Bus Protocols: AMBA AHB, APB, AXI, PCIe, RISC-V, UART
Soft Skills: Strong communication skills, Team player, Goal oriented, Ability to work independently and in team

ACADEMIC PROJECTS

RTL-to-GDSII Implementation and Verification of AI Accelerator using UVM and OpenROAD (In Progress) Jan 2025 - Present
- Developing a UVM-based testbench to verify AI accelerator functionality, focusing on **constrained-random testing, assertion-based verification**, and coverage-driven validation.
- Implementing full ASIC flow from RTL to GDSII using OpenROAD and Cadence tools, optimizing timing, power, and area to meet industry standards for AI hardware acceleration.

AI Calculation Engine with Custom S-Bus and UVM Verification Oct 2024 - Dec 2024
- Designed a **high-speed 352-bit read and 176-bit write bus with 16-cycle burst transfers**, ensuring efficient memory bandwidth and arbitration for AI engines.
- Developed a UVM-based testbench to verify bus functionality and system performance, **reducing verification time by 25%** and ensuring robust operation across edge cases.

Real-Time Edge Detection on ARM Cortex-A9 Oct 2024 - Nov 2024
- Designed and implemented **Sobel, Roberts Cross, and Prewitt edge detection algorithms** on ARM Cortex-A9 processor integrated with the Zybo Z7 FPGA for real-time image processing.
- Developed a video processing pipeline using **dual frame buffers, AXI Video DMA, and HDMI input/output interfaces**, improving data transfer efficiency by 35%.

Design and Verification of UART to I2C-Bus bridge using UVM Jun 2024 - Jul 2024
- Deployed a test plan from scratch to verify UART to I2C Bus Bridge with standard UVM workflow.
- Developed a testbench with two agents for respective interfaces, including a scoreboard to validate transactions.
- Executed a **Virtual sequencer to send and receive data** simultaneously on UART and I2C.

4-Stage Pipelined Half-Precision Floating-Point Adder Jun 2023 - Aug 2023
- Developed a 4-stage pipelined half-precision floating-point adder in Verilog, attaining a **30% raise in computational speed** compared to a non-pipelined design by enabling parallel execution stages.
- Accomplished a **20% reduction in simulation processing time** and memory usage through pipelining and efficient Verilog coding techniques, verified using Synopsys VCS for high-speed arithmetic operations in a simulation environments.

EXPERIENCE

Bharat Electronics Limited, Bengaluru, India Jan 2023 - Mar 2023
Application Engineer Intern
- Designed and developed embedded software for fighter jet pilot mask testing using LabView and Python.
- Optimized data acquisition with I2C and RS485 protocols, troubleshooting hardware/software issues with a 90% success rate.

Indian Institute of Science (L2M Rail), Bengaluru, India Jun 2022 - Sept 2022
Intern Railway Scientist
- Designed a real-time temperature monitoring system for railway axle boxes, implementing FPGA-based signal processing and sensor interfacing using Fiber Bragg Grating (FBG) sensors.
- Designed and deployed real-time Cyber Signalling Systems for railway sidings, integrating FPGA-based processing, IoT sensors, and AI-driven predictive maintenance for enhanced railway safety and efficiency.

PUBLICATIONS

- S. Hiremath, B. Yamini, T. M. N and P. K, "**Automation of Library Management System using Autonomous Robot**," 2023 4th International Conference for Emerging Technology (INCET), Belgaum, India, 2023, pp. 1-5, doi: 10.1109/INCET57972.2023.10169902
- G S, Pavithra & Muniswamy, Venkatesha & Sarvepalli, Srikrishna & B M, Chaya & Hiremath, Sharat. (2023). **Optical and Electrical Performance Analysis of New Polymer Layer in Organic Solar Cell**. 9. 170-174

CERTIFICATIONS

- VLSI System On Chip Design (Maven Silicon)
- SystemVerilog Essentials (Udemy)
- Computer Architecture (Coursera)