APB SLAVE
VERIFICATION DOCUMENT

CHAPTER 1: INTRODUCTION AND OBJECTIVES

1.1 Introduction:

APB is low bandwidth and low performance bus. So, the components requiring lower bandwidth like the peripheral devices such as UART, Keypad, Timer and PIO (Peripheral Input Output) devices are connected to the APB. The bridge connects the high performance AHB or ASB bus to the APB bus. So, for APB the bridge acts as the master and all the devices connected on the APB bus acts as the slave.

1.2 Specification

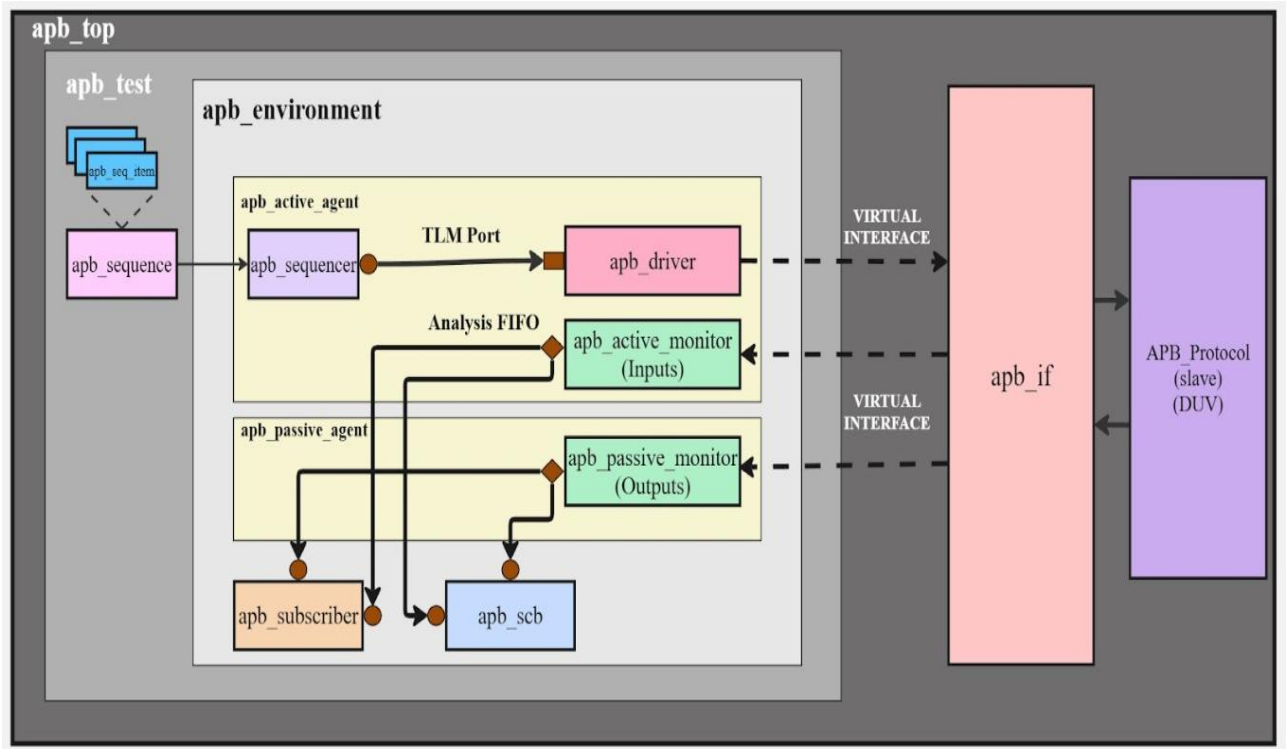
- The DUT is a single APB slave, receiving signals from an APB master.
- **Signal priority**:
    1. PRESETn (active low reset)
    2. PSEL
    3. PENABLE
    4. PREADY
    5. PWRITE
- **Data width**: 32 bits
- **Address width**: 8 bits

Write: PWRITE=1, PWDATA sent from master to slave

Read: PWRITE=0, PRDATA sent from slave to master

SIGNAL	SOURCE	DESCRIPTION	WIDTH
PCLK	Clock Source	All APB functionality occurs at rising edge	1
PRESETn	System Bus	Active low reset	1
PADDR	APB Master	Address bus	8
PSEL	APB Master	Slave select signal, active high	1
PENABLE	APB Master	Indicates the second cycle of a data transfer, active high	1
PWRITE	APB Master	Direction of transfer (1=write, 0=read)	1
PREADY	Slave	Indicates slave is ready for data transfer	1
PSLVERR	Slave	Indicates a transfer failure	1
PRDATA	Slave	Read data output from the slave	32
PWDATA	APB Master	Write data input to the slave	32

CHAPTER 2 - VERIFICATION ARCHITECTURE



The figure shows the verification architecture for an APB slave built using a UVM testbench approach.

Key Components:

- **Sequence Item** – A user-defined transaction class that holds all the required fields for a single APB operation, such as address, data, and control information.

- **Sequence** – Produces a stream of sequence items that serve as stimulus for the DUT. The test triggers the sequence to start generating transactions.

- **Sequencer** – Serves as the communication channel between the sequence and the driver. It forwards sequence items to the driver using a TLM interface and ensures proper handshaking.

- **Driver** – Receives transactions from the sequencer and translates them into pin-level APB signal activities. It drives the DUT through the APB interface

- **Monitor** – Observes DUT signal activity using the virtual interface.

  The **active monitor** captures the APB inputs driven to the DUT.

  The **passive monitor** captures the DUT's output responses.

  Both convert observed signal activity back into transaction objects and publish them through TLM analysis ports.

- **Agent** – A modular UVM component that groups related verification elements.

  The **active agent** contains the sequencer, driver, and an input monitor.

  The **passive agent** contains only the monitor that tracks output responses.

- **Scoreboard** – Receives monitored transactions and compares the DUT’s output with expected results to detect mismatches.

- **Subscriber** – Collects functional coverage information. It connects to analysis ports from both active and passive monitors to ensure all required scenarios are covered.

- **Environment** – A higher-level container that instantiates and connects all verification components, including agents, the scoreboard, and subscriber.

- **Test** – The top-level UVM class that builds the environment, configures components, and launches sequences that generate stimulus.

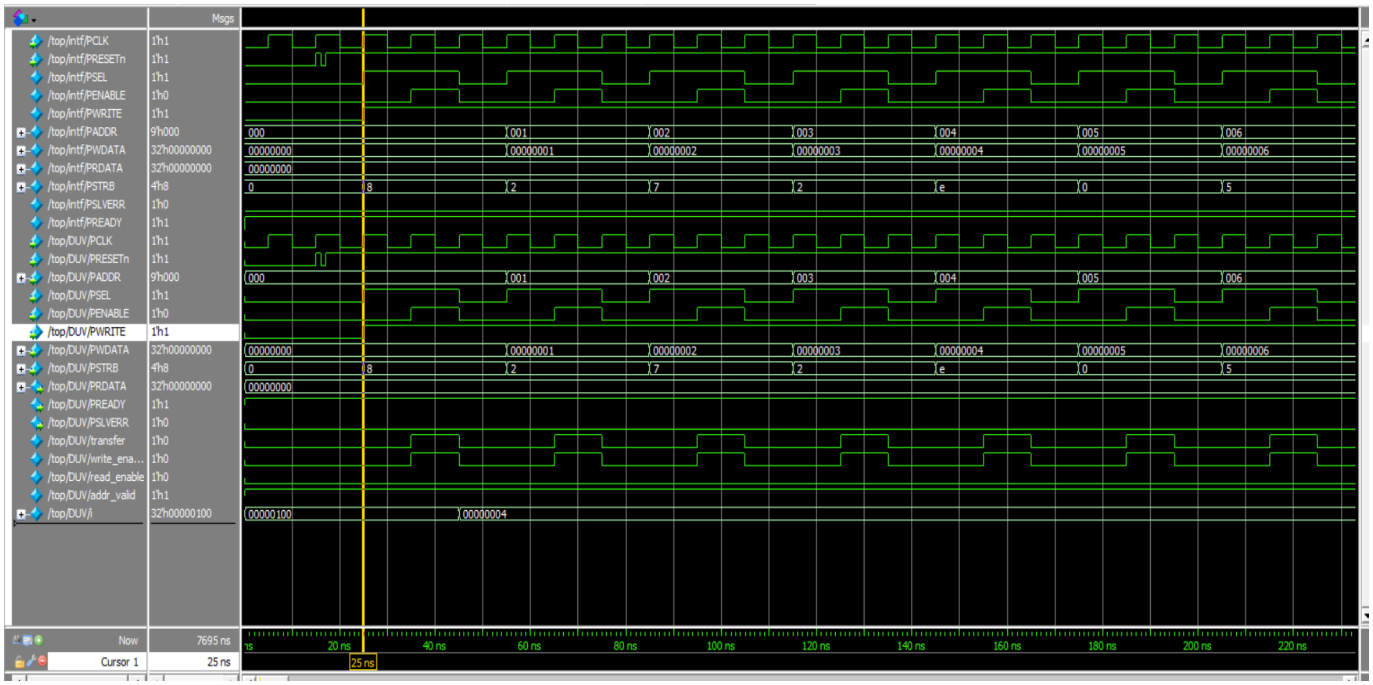
- **Top Module** – Instantiates the DUT and interface, connects everything to the UVM testbench, and starts the UVM phase flow.

- **Interface** – Provides the connection between the DUT and the testbench elements, exposing the APB signals to the driver and monitors via the virtual interface.

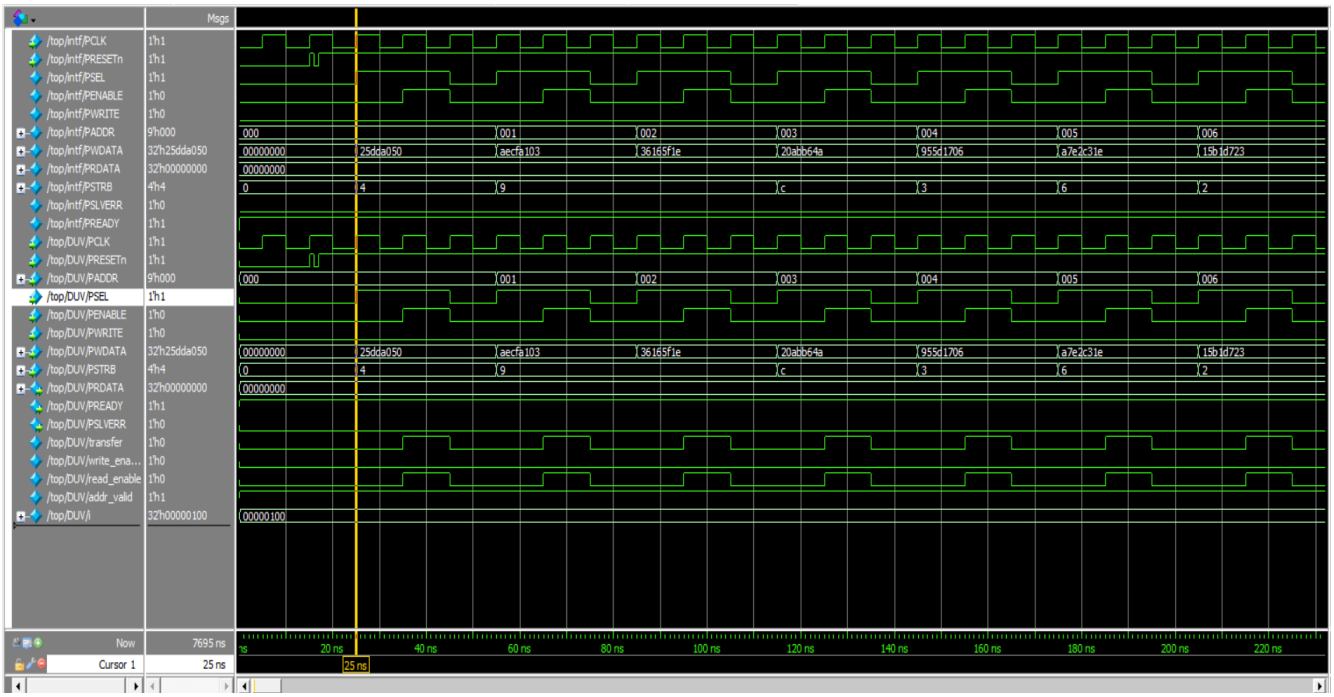
CHAPTER 3 - RESULT

Waveforms:

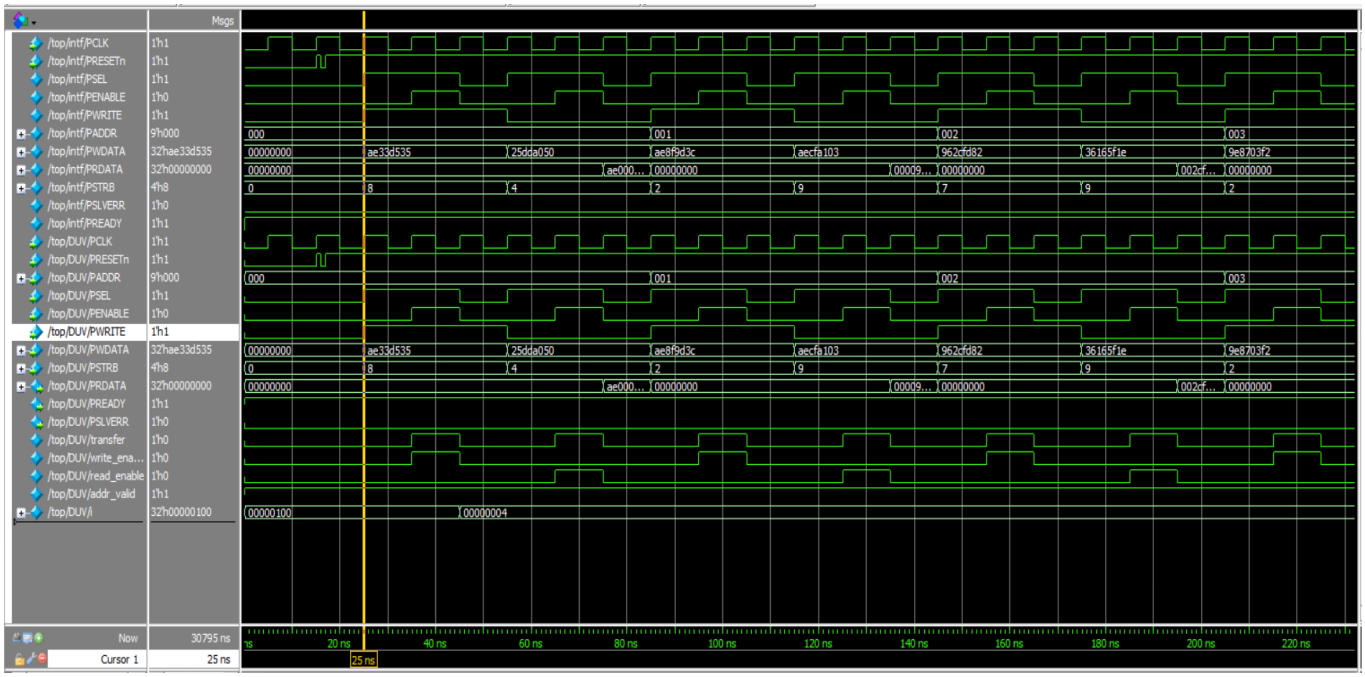
Write



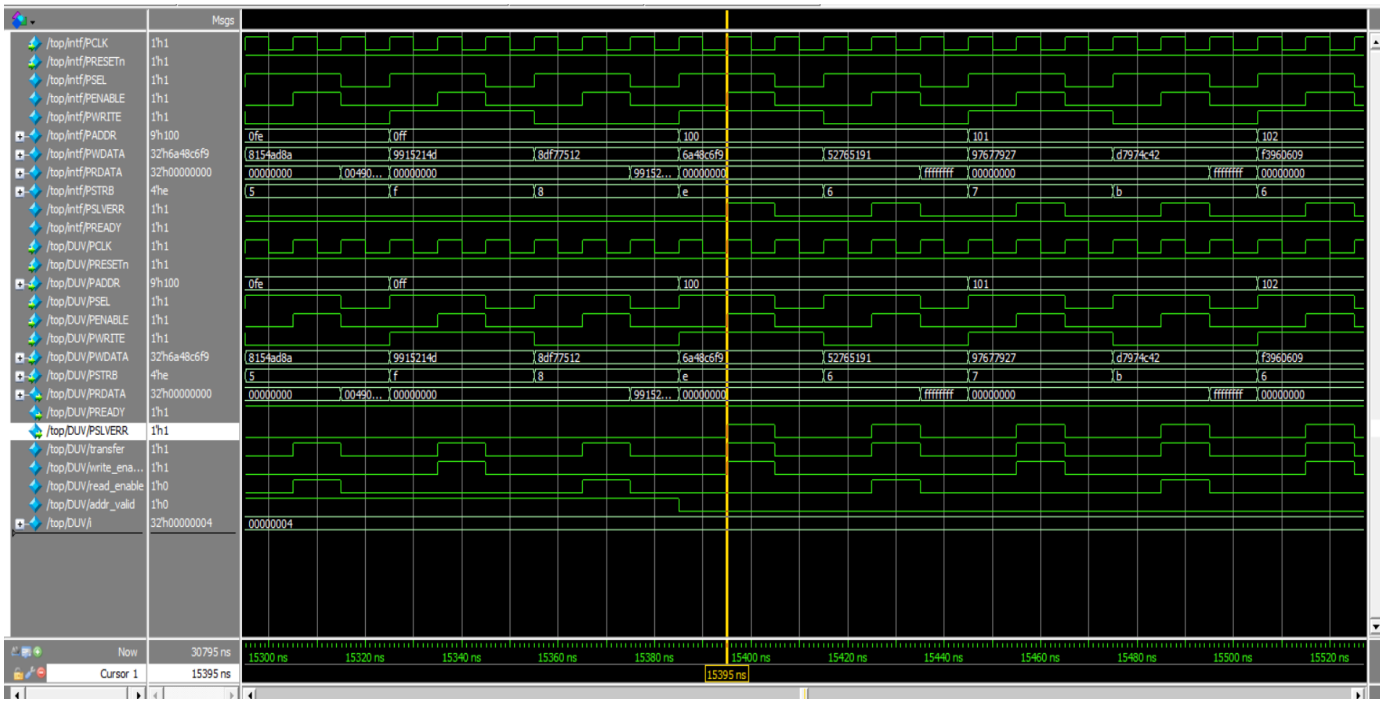
Read



Write_Read



Slave_err



Coverage Report:

Assertions

Assertions	Failure Count	Pass Count	Attempt Count	Vacuous Count	Disable Count	Active Count	Peak Active Count	Status
assert_pclk_valid	0	3080	3080	0	0	0	1	Covered
assert_presetn_valid	0	3080	3080	0	0	0	1	Covered
assert_psel_valid	0	3079	3080	0	1	0	1	Covered
assert_penable_valid	0	3079	3080	0	1	0	1	Covered
assert_pwrite_valid	0	3079	3080	0	1	0	1	Covered
assert_paddr_valid	0	3079	3080	0	1	0	1	Covered
assert_pwdata_valid	0	3079	3080	0	1	0	1	Covered
assert_pstrb_valid	0	3079	3080	0	1	0	1	Covered
setup_access_phase	0	1024	3080	2055	1	0	1	Covered
no_wait_states	0	1024	3080	2055	1	0	1	Covered
psel_stable	0	1024	3080	2055	1	0	1	Covered
prdata_valid	0	512	3080	2567	1	0	1	Covered
pslverr_valid	0	1024	3080	2055	1	0	1	Covered
no_new_input_during_access	0	1024	3080	2055	1	0	1	Covered

Questa Coverage Report

Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...

List of global attributes included in report...

List of Design Units included in report...

Coverage Summary by Structure:

Design Scope	Hits %	Coverage %
top	89.61%	97.46%
intf	98.93%	99.60%
DUV	77.22%	94.66%
apb_pkg	98.52%	91.66%
apb_subscriber	98.52%	91.66%

Coverage Summary by Type:

Total Coverage:					90.43%	96.63%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Covergroups	68	67	1	1	98.52%	91.66%
Statements	57	55	2	1	96.49%	96.49%
Branches	10	10	0	1	100.00%	100.00%
FEC Expressions	9	9	0	1	100.00%	100.00%
FEC Conditions	4	4	0	1	100.00%	100.00%
Toggles	580	512	68	1	88.27%	88.27%
Assertions	14	14	0	1	100.00%	100.00%

DUT Coverage:

Local Instance Coverage Details:

Total Coverage:					77.22%	94.66%
Coverage Type	**Bins**	**Hits**	**Misses**	**Weight**	**% Hit**	**Coverage**
Statements	18	18	0	1	100.00%	**100.00%**
Branches	10	10	0	1	100.00%	**100.00%**
FEC Expressions	9	9	0	1	100.00%	**100.00%**
FEC Conditions	4	4	0	1	100.00%	**100.00%**
Toggles	240	176	64	1	73.33%	**73.33%**

Input coverage:

Covergroup type:

input_cov

Summary	Total Bins	Hits	Hit %
Coverpoints	20	20	**100.00%**
Crosses	39	39	**100.00%**

Search:

CoverPoints	Total Bins	Hits	Misses	Hit %	Goal %	Coverage %
APB_ADDR	5	5	0	100.00%	**100.00%**	**100.00%**
APB_WRITE_DATA	5	5	0	100.00%	**100.00%**	**100.00%**
ENABLE	1	1	0	100.00%	**100.00%**	**100.00%**
SLAVE	1	1	0	100.00%	**100.00%**	**100.00%**
STRB	6	6	0	100.00%	**100.00%**	**100.00%**
WRITE_READ	2	2	0	100.00%	**100.00%**	**100.00%**

Search:

Crosses	Total Bins	Hits	Misses	Hit %	Goal %	Coverage %
ADDR_X_APB_WRITE_DATA	25	25	0	100.00%	**100.00%**	**100.00%**
WRITE_READ_X_ADDR	10	10	0	100.00%	**100.00%**	**100.00%**
WRITE_READ_X_ENABLE	2	2	0	100.00%	**100.00%**	**100.00%**
WRITE_READ_X_SLAVE	2	2	0	100.00%	**100.00%**	**100.00%**

Covergroup type:

output_cov

Summary	Total Bins	Hits	Hit %
Coverpoints	9	8	**88.88%**
Crosses	0	0	**0.00%**

Search:

CoverPoints	Total Bins	Hits	Misses	Hit %	Goal %	Coverage %
APB_READ_DATA_OUT	5	5	0	100.00%	**100.00%**	**100.00%**
APB_SLVERR	2	2	0	100.00%	**100.00%**	**100.00%**
READY	2	1	1	50.00%	**50.00%**	**50.00%**