SHARATH G

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EDUCATION

BMS College of Engineering, Bengaluru CGPA**: 8.30**
B.E. in Electronics and Communication 2022- Present (2025)
MEI Polytechnic, Bangalore Percentage**: 92%**
Diploma in ECE 2019-2022
Gandhi Vidya Shala, Bangalore Percentage**: 89.6%**
10th Grade 2018-2019

PROJECTS

- **32-Bit Pipelined MIPS Processor:** Designed & implemented a MIPS-based 32-bit RISC processor in Verilog with 16 instructions, multiple addressing modes and branch prediction.

  Design and Verified using Verilog:
  - **5 stage instruction cycle with pipeline**: IF, ID, EX, MEM, WB
  - **Address modes**: RR, RM, JMP
  - **Instruction set**: Arithmetic, Logical, Branch, Load/Store
  - **Instruction blocks**: Instruction memory, main memory and program counter
  - **Error handling**: Halt and Branch taken bit
  - **Data Hazard Handling**: Insertion of Dummy instructions

- **UART Communication Protocol:** Designed & implemented UART in Verilog, verified its functionality using System Verilog.

  Design using Verilog:
  - Transmitter and receiver design
  - FSM and Baud rate generator
  - Shift registers: PISO and SIPO

  Verification using System Verilog:
  - Developed SV Based environment to verify UART Design
  - Developed System Verilog assertions to check its violations
  - Checked the error scenarios
  - Written coverage to check the functionality

- **AMBA-APB Protocol:** Designed & implemented AMBA- APB BUS in Verilog, verified its functionality using System Verilog.

  Design using Verilog:
  - APB master
  - APB slave
  - FSM

  Verification using System Verilog:
  - Developed SV Based environment to verify APB bus protocol
  - Done System Verilog assertions to check its violations
  - Written coverage to check the functionality

- **CMOS Power Amplifier**: Designed a two-stage CMOS amplifier in Cadence Virtuoso, optimizing gain & power consumption using 45nm & 90nm technology nodes.
  - **Design using Cadence Virtuoso**
  - Optimizing gain & power consumption
  - Verified using Spectre tool

- **Physical Design of LFSR (RTL-to-GDSII):** Designed an LFSR circuit in Verilog, implemented physical design using OpenLane.

  Implementation using OpenLane:
  - **Synthesis using Yosys:** Generated Power, time and Area report
  - **Magic tool:** Floorplan and Placement, checking of DRC/LVS Violations
  - **OpenSTA:** Done Clock tree synthesis
  - **Final output:** Generated GDSII file

TECHNICAL SKILLS

- **Hardware Design & Verification:**
  - Digital Electronics, ASIC Design, Functional Verification (UVM), RTL Design, PLL & ADC/DAC Designs.
  - Synthesis & Place-and-Route (PnR), Static Timing Analysis (STA), Power & Performance Optimization
- **Programming & Scripting:**
  - System Verilog, Verilog HDL, Python, Embedded C, TCL
  - SVA, Coverage-Driven Verification (CDV)
- **EDA Tools & Simulators:**
  - Cadence Virtuoso, Cadence Xcelium, QuestaSim, Xilinx Vivado, OpenLANE, Yosys, OpenSTA
  - DRC/LVS Verification (Magic, Assura), SpectreRF, SPICE Simulation
- **Other Tools & Software:**
  - MATLAB, Proteus, Qualnet Simulator, Keil µVision, Fusion 360

INTERNSHIPS

- Embedded Design Intern, Einweit Technologies – **Present**
  - Leading a team in hardware-software co-design for ESL technology and IoT gateways.
  - Exploring digital system optimization and GenAI integration for efficient AI inference.

- VSD SoC Design & Planning Intern (Google- Skywater 130nm PDK)
  - Designed & implemented a RISC-V based SoC from RTL-to-GDSII using OpenLane & SKY130. Performed Synthesis, Floorplanning, Placement & Routing, STA, and DRC/LVS verification. Contributed to design closure & power-performance optimization for final chip tape-out.
- BMS College Of Engineering
  - **Practical IC design intern**: Hands-on internship in Practical Analog IC Design focusing on designing analog blocks, conducting analyses, and characterizing circuits. Utilized Cadence Virtuoso for practical training.

ACHIEVEMENTS & LEADERSHIP

- **Achievements:** Secured 267th state rank in the DCET Exam (2022)
- **Community Involvement:** Actively engaged in teaching Government School students through the Rotaract Club of BMSCE, fostering educational development and mentorship.
- **National level Hardware Hackathon Runner Up:** Held in SMVIT Udupi, Hackothsava in 2024.