INTRODUCTION TO COMPUTER ENGINEERING

WINTER 2014

ASSIGNMENT 3: SEQUENTIAL LOGIC
DUE DATE: MONDAY MARCH 17TH, 2014 AT 5:00PM

Please submit this assignment by 5:00 pm on the due date via *MyCourses*. Your assignment must be packaged as follows: one compressed file (.zip) containing the following files:

- Answers to all questions as well as discussions (including schematic circuit diagrams and timing printouts) in **one single** Microsoft Word (doc/docx) or portable document format (pdf) file. Note that scanned handwritten solutions are accepted.
- All files related to your Logicworks design. This includes: circuit files (`.cct`), timing files (`.tim`) and library files (`.clf`). All files should be named according to the following convention:

  `LAST_FIRST_QX_DESC.xxx`

  where "`LAST`" and "`FIRST`" are you last and first name respectively (no spaces), "`QX`" should be replaced by Q1, Q2 or Q3 depending on the question in the assignment to which your file belongs, "`DESC`" is an optional short description and "`xxx`" is the file extension.

A penalty of 10% will be applied if you do not follow these guidelines.

This assignment will be marked out of 100 points. **Late submissions will NOT be accepted.**

QUESTION 1 (50 POINTS) – 5-BIT SHIFT REGISTER

- The following table (generalized from the course notes) summarizes the function of a shift register that can shift right, shift left, hold a value or load a new value from inputs.

	Inputs		Next State				
Functions	**S1**	**S0**	$\widetilde{QA}$	$\widetilde{QB}$	$\widetilde{QC}$	$\widetilde{QD}$	$\widetilde{QE}$
HOLD	0	0	QA	QB	QC	QD	QE
S. RIGHT	0	1	RSI	QA	QB	QC	QD
S. LEFT	1	0	QB	QC	QD	QE	LSI
LOAD	1	1	A	B	C	D	E

The 5-bit register has inputs:

- S0 and S1, for mode selection

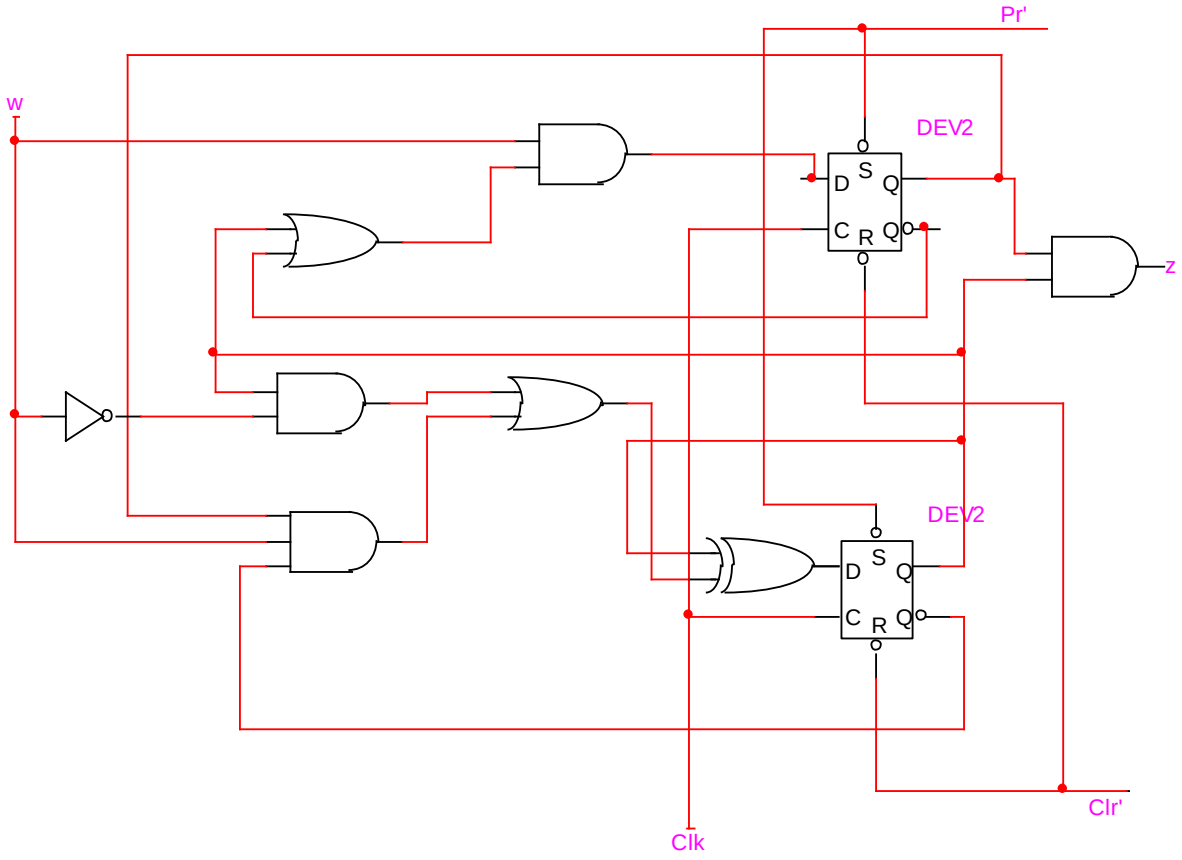
- A, B, C, D and E, as inputs in the load mode
- LSI as new bit input for left shift
- RSI as new bit input for the right shift
- A clock signal
- An asynchronous “clr” signal to reset the register

The five outputs re the 5 register bits QA, QB, QC, QD and QE.

(a) Implement this shift register in LogicWorks, using only combinational logic gates and JK flip-flops.
(b) Carry out a timing analysis of your circuit, assuming default LogicWorks delay values for the gates you have used. Determine the maximum operating frequency of the circuit.
(c) Carry out a LogicWorks simulation of the circuit to verify that the circuit does not function for frequencies above the value determined in (c).

QUESTION 2 (50 POINTS) – CIRCUIT ANALYSIS

You are given the following sequential circuit diagram.



Analyze this circuit in detail (show all you work) and write the corresponding state transition table

Verify your results through LogicWorks simulations of the circuit, and by devising a series of tests to ensure that your analysis corresponds to the actual circuit behaviour.