CPSC 359 – Spring 2018
Assignment 3 – Digital Logic
Arithmetic Logic Unit
Due Jun 19th @11:59 PM

Objective: In this assignment, you will design a small ALU with memory and registers.

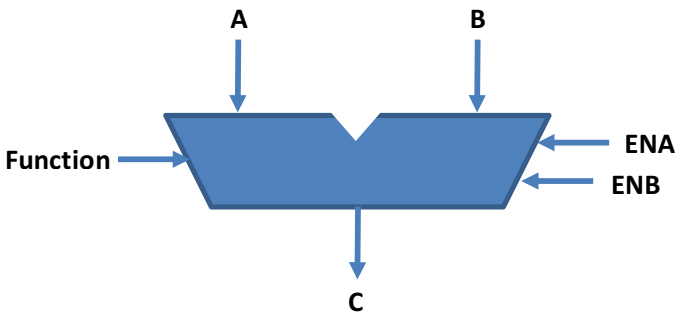
Background: An arithmetic logic unit (ALU) is a digital circuit used to perform arithmetic and logic operations. It represents the fundamental building block of a Central Processing Unit (CPU) of a computer.

In this assignment you will design an ALU with 4x4 Memory Unit and a number of registers as discussed below:

Components:

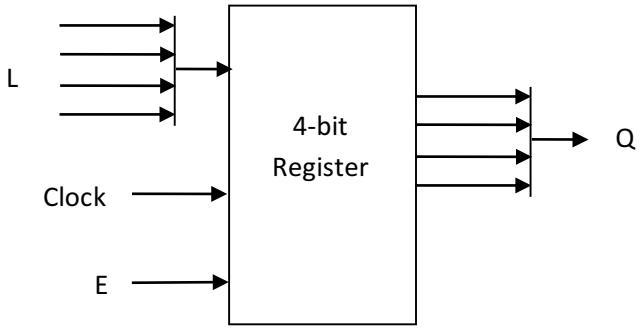
- **ALU**: It has 3 inputs: A (4 bits), B (4 bits) & Function (3 bits) and 1 output C (4 bits) where:

Function	C
000	A AND B
001	A OR B
010	NOT A
011	NOT B
100	A + B
101	A - B
110	-A
111	-B



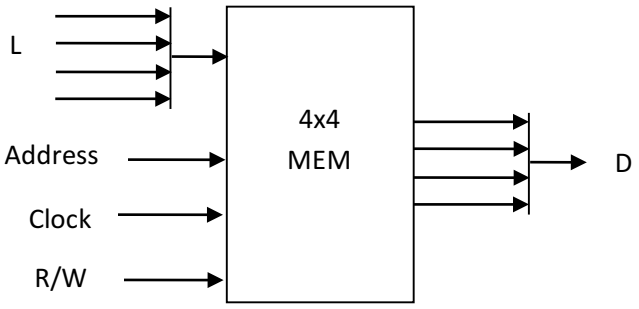
In addition, the ALU must have 2 additional signals ENA (1 bit) and ENB (1 bit) to enable/disable the A and B inputs, respectively. So, if ENA = 0, the A input is 0, If ENA = 1, the A input is A. The same applies for B.

- **4-bit register**: Stores 4 bits of data on the rising edge of a clock. If the Enable (E) is 0, clock triggers are ineffective.



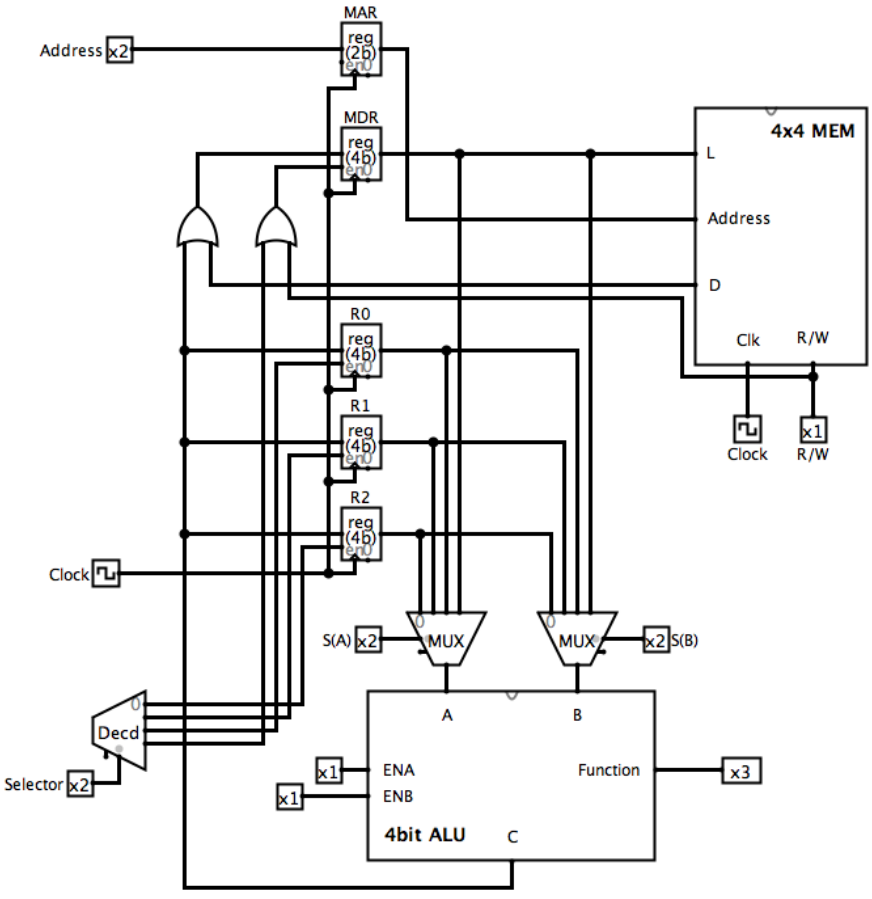
- **4x4 Memory Unit:** four (4-bit words) available memory locations for reading/writing. A write or read can be performed at a rising edge of the clock.

R/W	Function
0	Read from Address at D
1	Write L to Address



- **Other Components:** 2-bit register, 2-bit Decoder, two 4-bit 4x1 Multiplexer**.**

Circuit:



In the circuit above: there are four ***4-bit registers*** one of which is called **MDR**. **MDR** is a memory data register, it is connected to the ***4x4 MEM*** and can read and write from/to it, it is connected to the inputs/output of the ***ALU*** as well. ***MAR*** is a ***2-bit register*** used to store the address to be used for reading/writing from the ***4x4 MEM***.

Note: Using the available components in Logisim is not permitted except wiring, gates, and D-flip-flops.

Deliverables:

1. Design and implement the corresponding circuit in Logisim.
2. Use building blocks to create the corresponding components.
3. ALU, memory & registers' data, function & output lines of more than 1-bit must be bundled to a single 4-bit/3-bit/2-bit lines inside the block of the circuit (use splitters).

Marking Guide:

ALU	10 points
4x4 MEM	5
4-bit/2bit registers	2
Using building blocks	3
Labeling	2
Overall circuit function	3
Total	**25**

Teams: You are advised to work with another student in class in order to complete the assignment, but you are not required to do so. Peer evaluation in teams may be conducted. Teams for this assignment cannot exceed 2 students.

Submission: Submit your .circuit file to the dropbox on D2L.

Late Submission Policy: Late submissions will be penalized as follows:
-12.5% for each late day or portion of a day for the first two days
-25% for each additional day or portion of a day after the first two days
Hence, no submissions will be accepted after 5 days (including weekend days) of the announced deadline

Academic Misconduct: Any similarities between assignments will be further investigated for academic misconduct. While you are encouraged to discuss the assignment with your colleagues, your final submission must be your own original work.