19ECE341 VLSI System Design

Wallace Tree Multiplier using Kogge Stone Adder in VLSI circuit design

Term Project

Report

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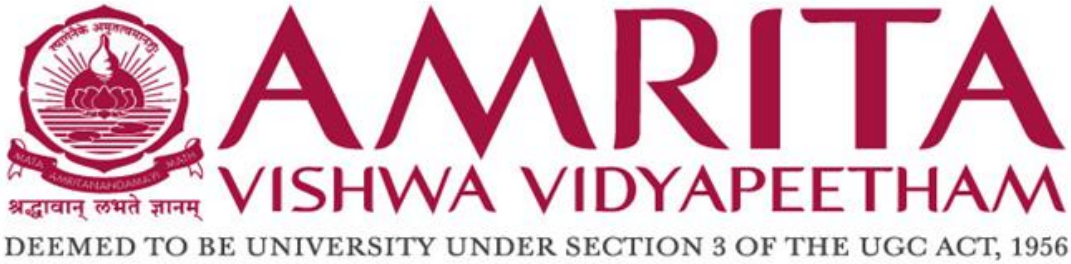

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Abstract:

Advancement of VLSI circuits with billions of logic element performing high-speed applications, with low area, consumption of power are important parameters for the design. As progressive as it seems in a very short time, the optimization of circuits is the only factor that will remain unchanged. An arithmetic operation is a foundation for processors which was used to solve complex problems and allows the computation of mathematical operations on binary numbers. A separate unit to contribute to the applications, a multiplier logic block come in handy. Processors are used mostly in digital applications, which make the multiplier a crucial need. Wallace tree multiplier is a hardware implementation of a binary multiplier that multiplies two integer values. It is much more efficient in speed and area comparatively, therefore it is vital for high-speed applications. Its ease and efficient implementation of hardware can improve manufacturing production.

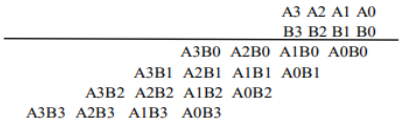
The process of the Wallace tree multiplier has two major phases: to produce partial products and summation of partial products is done in an iterative process by using full adders and half adders. To get the idea of why adders play a crucial role, here we try to implement 4-bit Wallace tree multiplier. In the second phase, the first three rows are added then it is added again with 4th partial products and remaining carry bits are added again in the final stage to give us the final product term. Since there are abundant usage of adders in this Wallace tree multiplier circuit. By improvising the summation speed, we can reduce the multiplier's overall delay.

Traditionally Carry select adder is used which is prone to carry propagation delay. To overcome the drawback, our proposed work is to alter the basic structure of the Wallace tree multiplier by replacing Full and Half adders in the final stage by a Parallel prefix adder (PPA) which can optimize the speed of over overall circuit of the multiplier. The term parallel prefix means that it uses the prefix operation to do addition efficiently. These adders are mostly suitable for binary-wide word applications. These are derived from carry look-ahead adders. Partial prefix adders can generate and propagate the carry bits for all input parallelly with the help of the carry generation tree which improves the performance of the Wallace tree multiplier by increasing the speed.

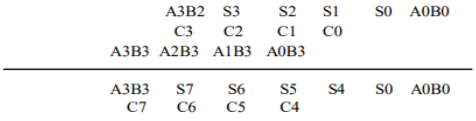
PPA performs by having 3 stages: Propagation and generating signal block, Parallel carry generation tree, and sum generation block which will be discussed in the methodology section. Though the concept of PPA remain same, there are options of prefix adders which are segregated based on its architecture. In our proposed work, the choice of implementation is by using a Kogge stone architecture-based parallel prefix adder, since it is best suitable for high-speed applications but with a trade-off in the area and power consumption. Our multiplier structures are designed and simulated using Verilog HDL, the tool used is ModelSim - Intel FPGA starter edition 10.5b. This report contains the architecture of Kogge stone adder, an elaborate on the methodology used, and then proposed designs are analyzed with respect to traditional multiplier design in terms of area (No. of LUTs) and delay (ns).

Methodology / Block diagram:

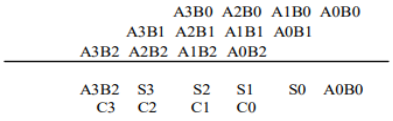
Wallace Tree:



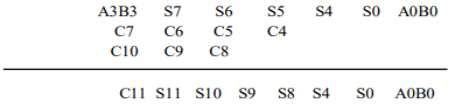
Phase 1 Partial products generation



Phase 2.2 Performing Addition of row 4 partial products with phase 2.1 result



Phase 2.1 Performing Addition of first three rows of partial products



Phase 2.3 Performing Addition of phase 2.2 result to obtain final product

Wallace tree structure is the most widely utilised multiplier design in various processors and memory units. The Wallace tree multiplication process is divided into two stages. The input numbers are applied to the AND gate in phase 1 to produce partial products. In phase 2, these partial products are added step by step utilising half and full adders to generate the final product output. The first phase consists of generating partial products by multiplying each bit of the specified input numbers with each other. As the input size is four bits, four rows of partial products are created. Phase 2 is made up of multiple sub-phases of adding the partial products obtained in phase 1. Half and full adders are used to perform the addition function. In phase 2, the addition operation is performed on the first three rows of partial products obtained in phase 1, resulting in two rows with sum terms in the first row and carry terms in the second row.The final row of partial products from phase 1 is then added with the sum and carry row, which results in two rows consisting of a sum row and a carry row to obtain. The sum, final product, and carry row are added. The major disadvantage of this existing methodology is the longer carry propagation time delay. To overcome this limitation, parallel prefix adders are deployed in phase 2 of this multiplier in place of half and full adders in the last step of addition.

Kogge Stone Adder:

Due to its high-speed performance and low fanout, the Kogge stone adder is regarded as one of the main adders among parallel prefix adders.

Three different stages during computation:

- Pre-Processing stage:

  Pi = Ai XOR Bi Gi = Ai AND Bi
- Generation of carry:

  Gi = (Pi AND Gi-1) + Gi Pi = (Pi AND Pi-1)
- Final processing stage:

  Ci = Gi Si = Pi XOR Ci-1

Wallace Tree Multiplier using Kogge stone Adder:

Fig 1: Methodological diagram of implemented wallace adder

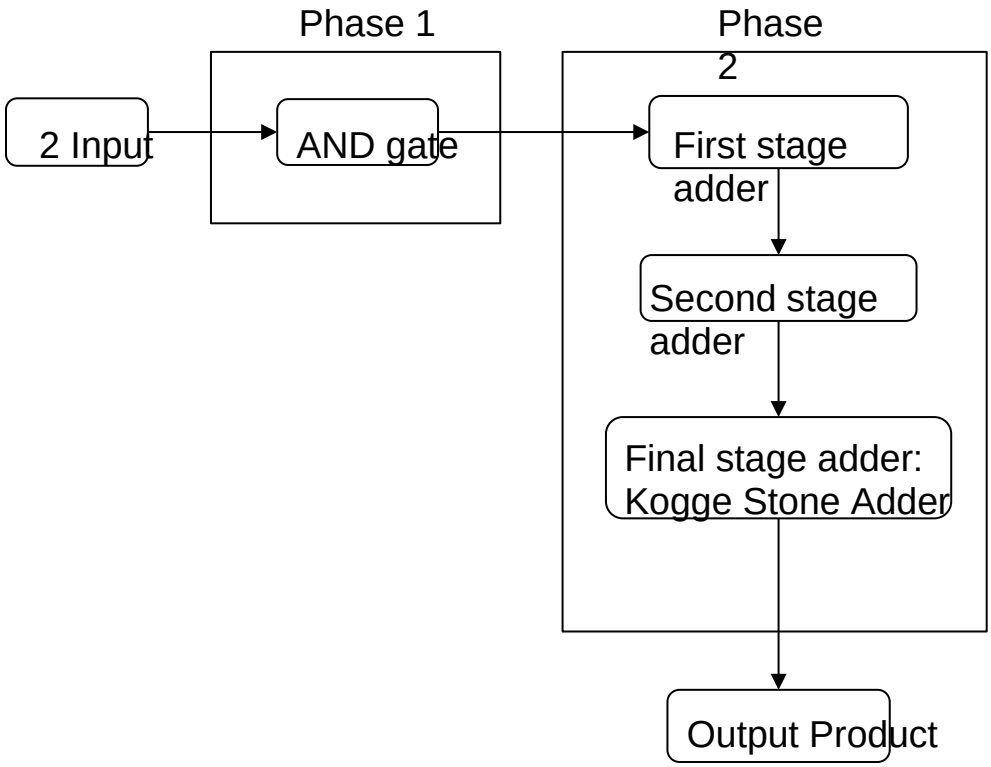


Fig 2: Procedural diagram of implemented wallace adder

Inference:

Compared to other multipliers, Wallace tree multipliers are considered to be fast. A novel Wallace tree multiplier structure that uses parallel prefix adders is built in order to increase the speed of the Wallace tree multiplier. Additionally, it is discovered that adding a compressor results in a smaller design than the standard Wallace Tree Multiplier Design.

Wallace tree multipliers employing Kogge stone adders can be utilised for high-speed application circuits, although they require a little bit more space than alternative parallel prefix adder designs.

Results:

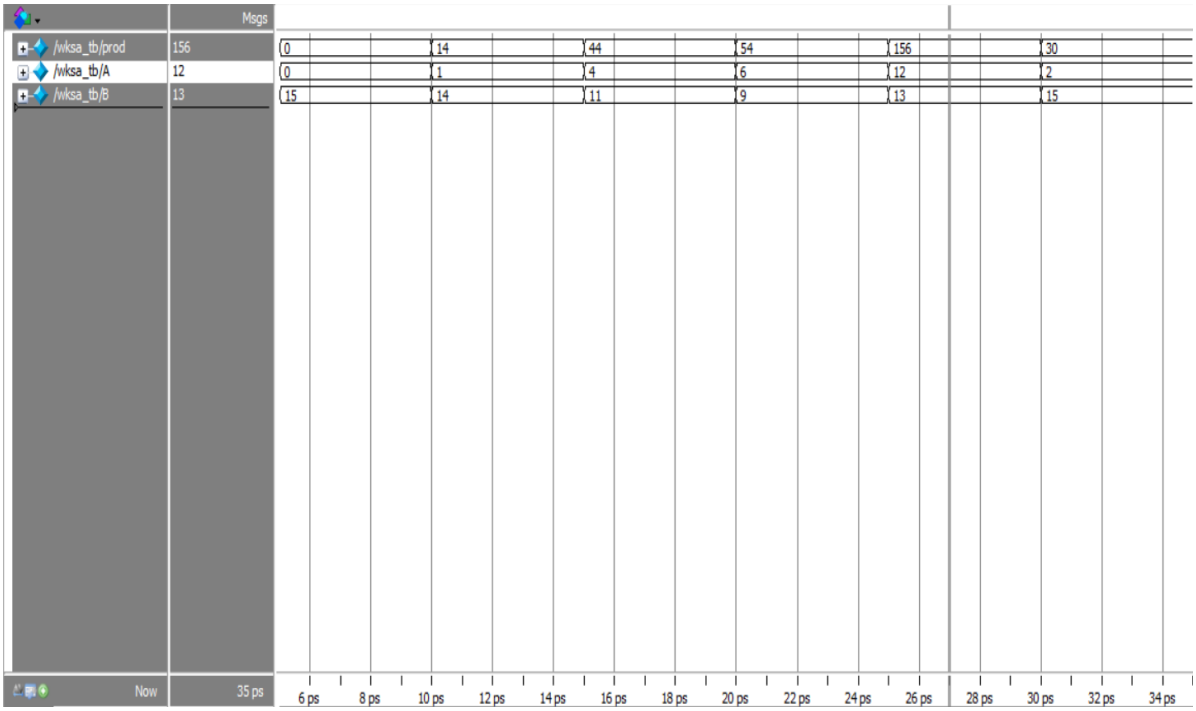


Fig 3: Waveform of the implemented wallace tree multiplier (unsigned)

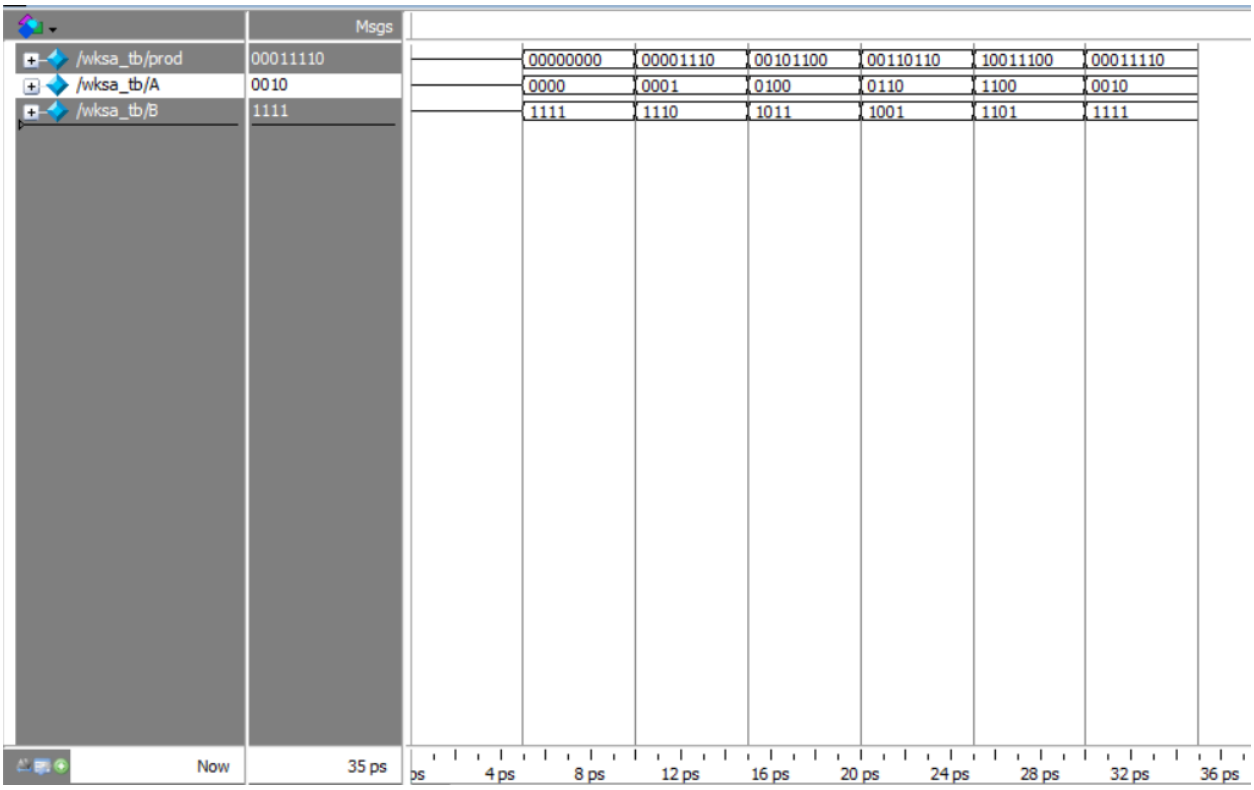


Fig 3: Waveform of the implemented wallace tree multiplier (binary)