CSE251: Electronic Devices and Circuits

Lecture: 14 - 16 – MOSFET

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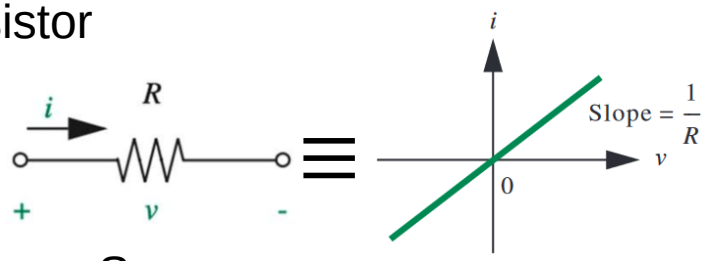
Outline

- Introduction to Electronic Switches
- Basic Inverter
- Introduction to Controlled Sources
- Introduction to MOSFET
- MOSFET as digital switch
- Designing Logic gates with MOSFETs

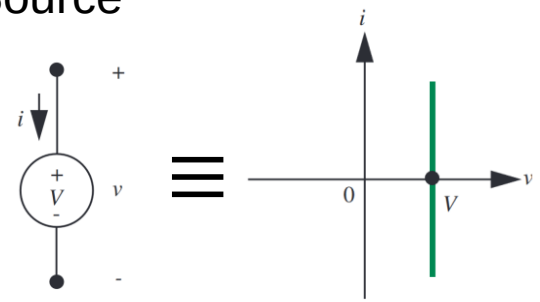
Two terminal Devices

Linear Devices

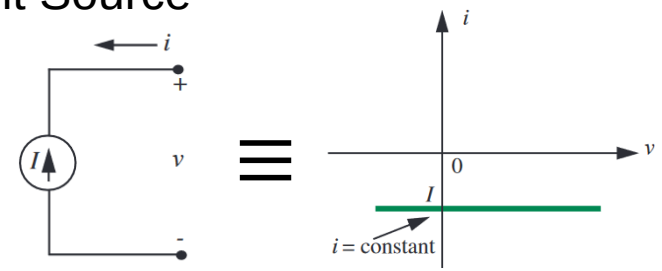
Resistor



Voltage Source



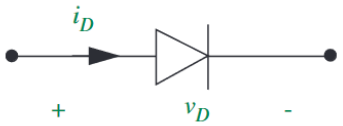
Current Source



IV characteristics of two terminal devices are fixed.

Non-linear Devices

Diode



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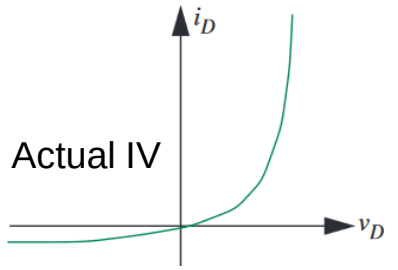
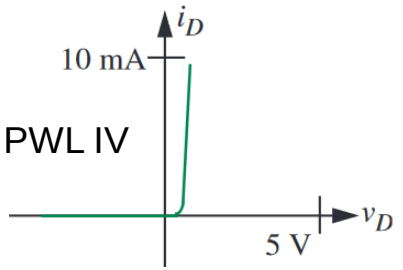


PWL: Piecewise Linear



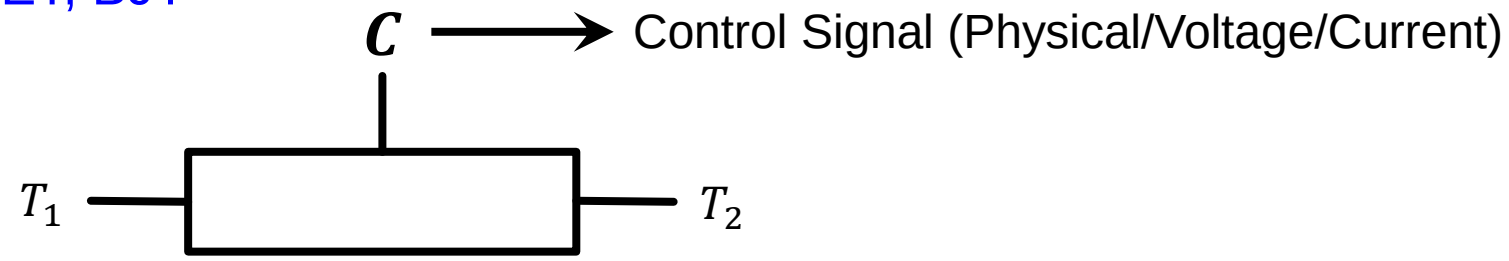
IV characteristics of **three terminal devices** can be changed

Three terminal Devices

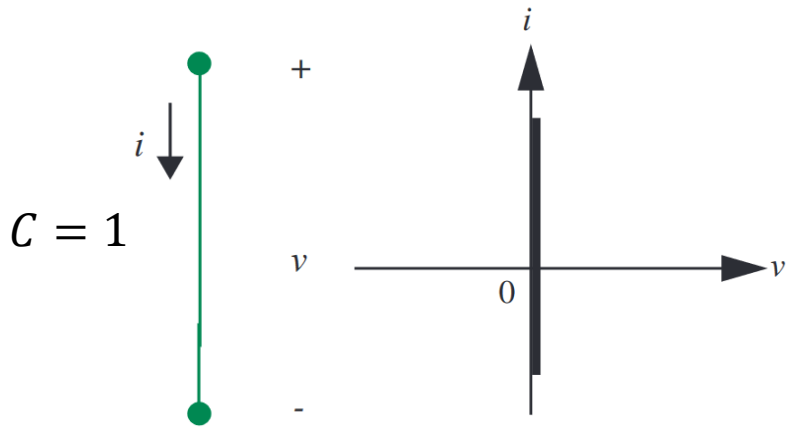
IV of two terminal can be controlled using a third terminal.

Example: Switch, MOSFET, BJT

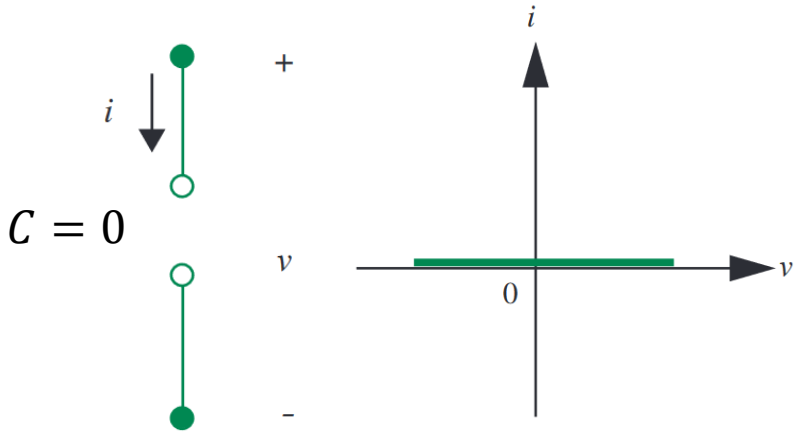
Switch



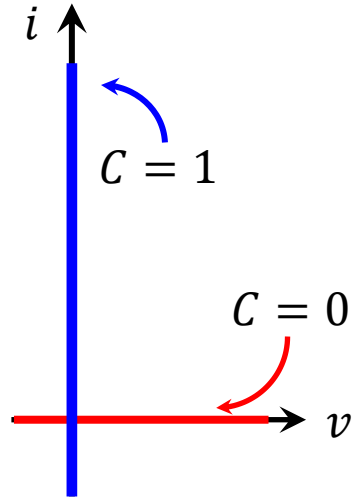
IV characteristics between T_1 and T_2 can be controlled by C



Switch **ON**

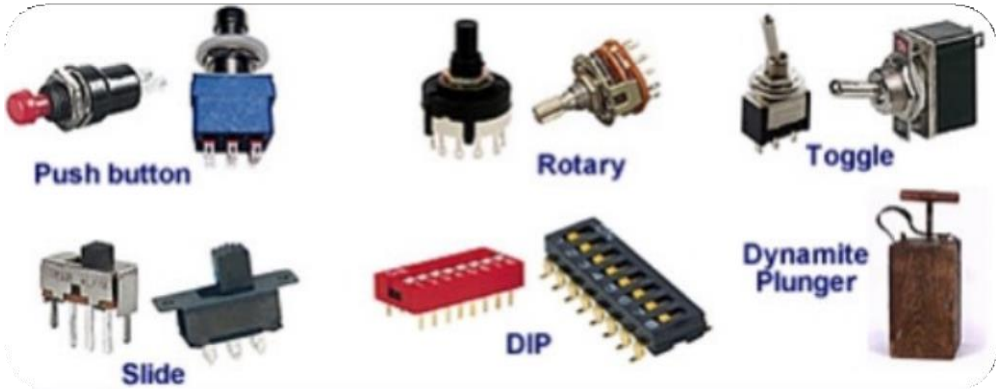


Switch **OFF**

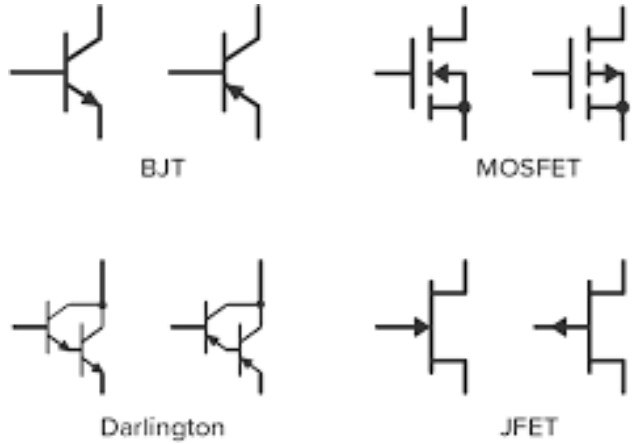


Switch – Types

- Depending on the control, the switch can be
  - **Analog**: Controlled using physical toggle/button
  - **Digital**: Controlled using voltage or current. Example – MOSFET (voltage controlled), BJT (current controlled)



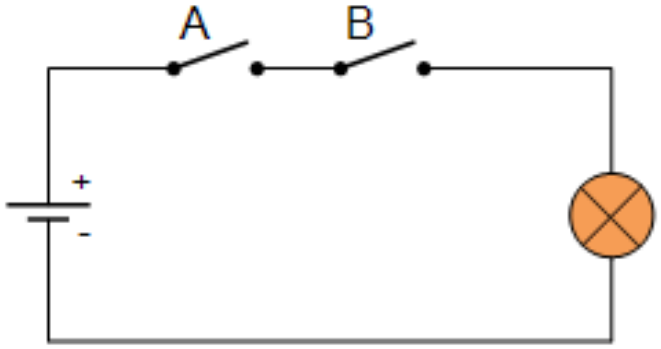
Analog switches



Digital switches (Transistors)

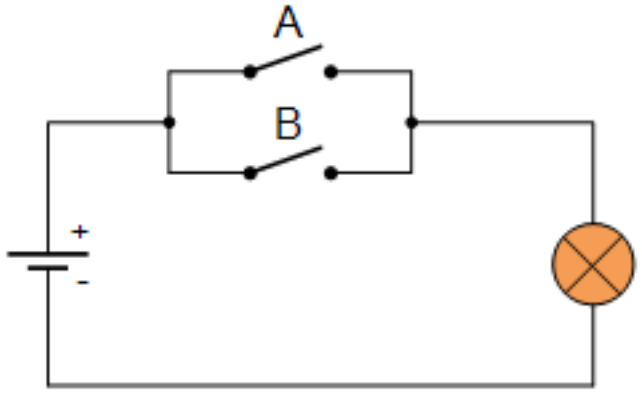
Switch Application – Logic Gates

- We can use switches to build logic gates



A	B	Bulb
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

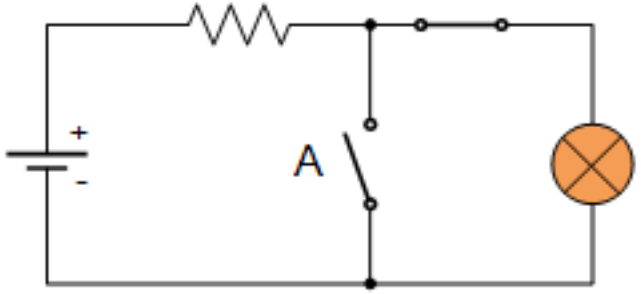
AND operation



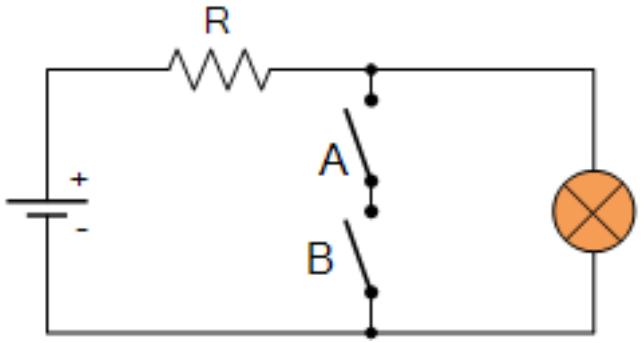
A	B	Bulb
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

OR operation

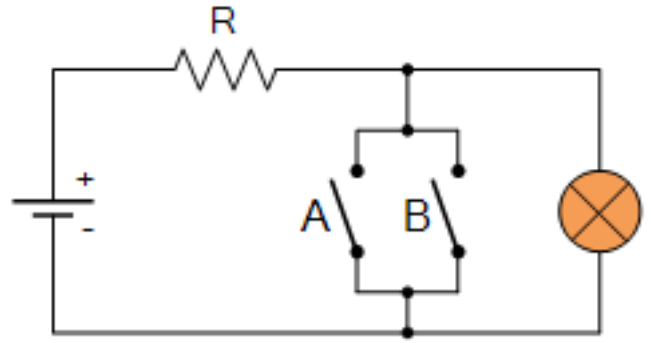
Switch Application – Logic Gates



A	Bulb
0	
1	



A	B	Bulb
0	0	
0	1	
1	0	
1	1	



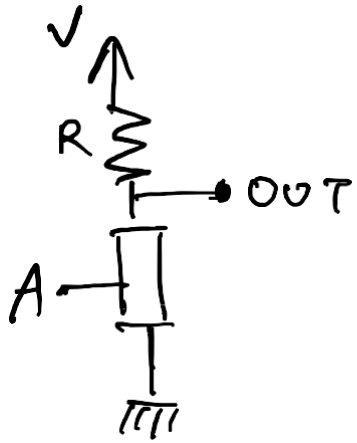
A	B	Bulb
0	0	
0	1	
1	0	
1	1	

These circuits are “preferred” – because they can be cascaded to build combinational logic circuits

-> if we remove the bulb and use the voltage across instead to cascade and drive the next gate

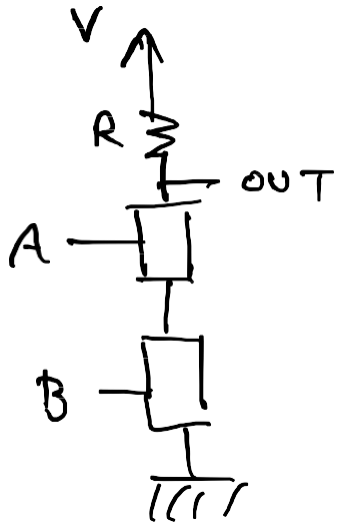
Switch Application – Logic Gates

Alternative representations:



Switch Application – Logic Gates

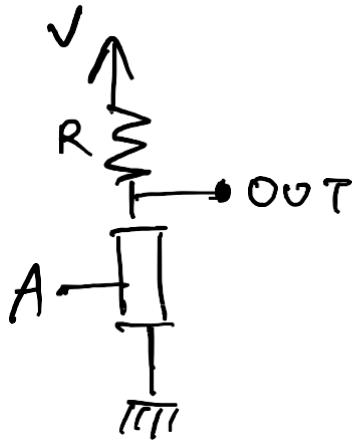
Alternative representations:



$OUT = \overline{AB}$

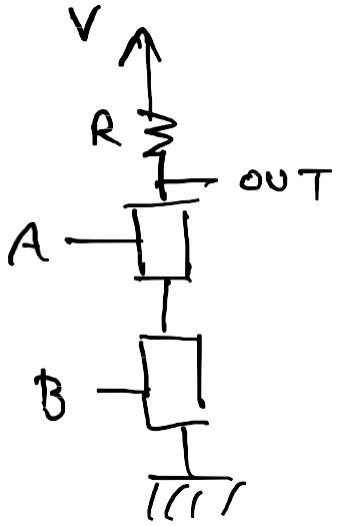
(NAND)

Switch Application – Logic Gates



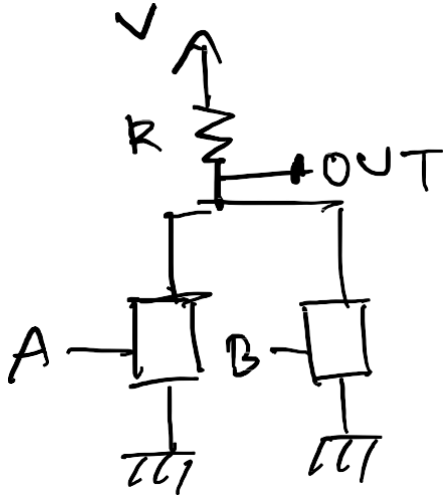
$OUT = \overline{A}$

A	V_{OUT}
0	5V
1	0V



$OUT = \overline{AB}$

A	B	V_{OUT}
0	0	5V
0	1	5V
1	0	5V
1	1	0V

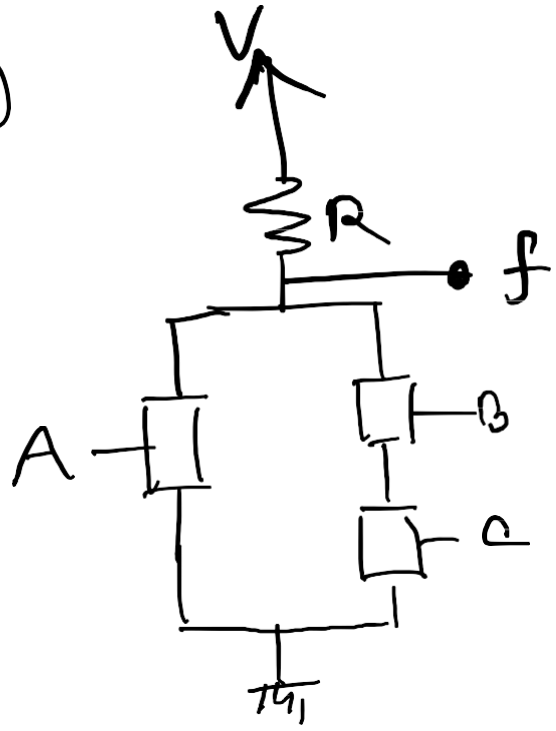


$OUT = \overline{A+B}$

A	B	V_{OUT}
0	0	5V
0	1	0V
1	0	0V
1	1	0V

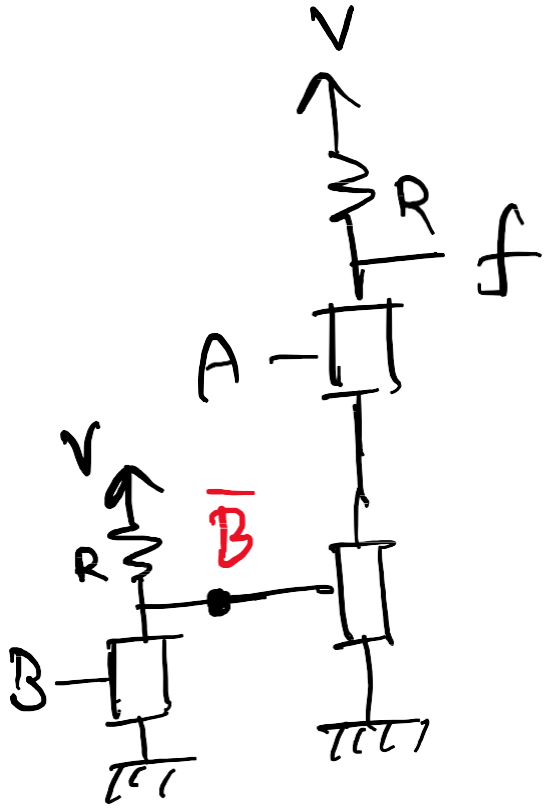
Examples

(1)



$$f = \overline{A + B.C}$$

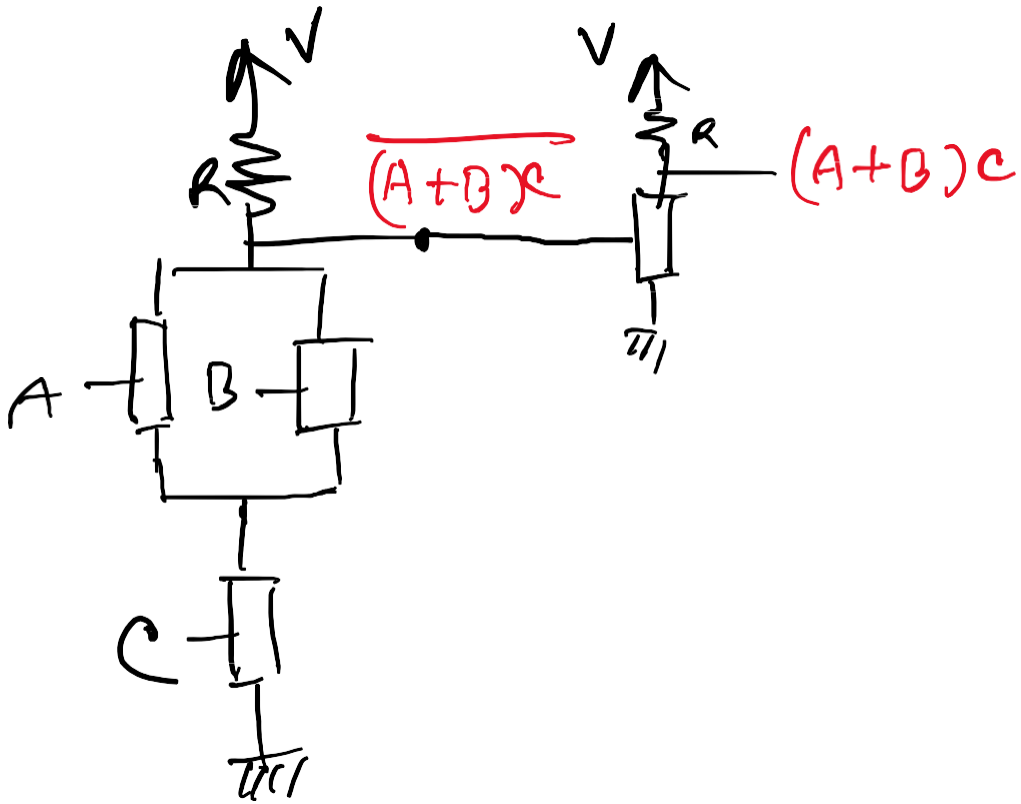
(2)



$$f = \overline{A\overline{B}}$$

Example

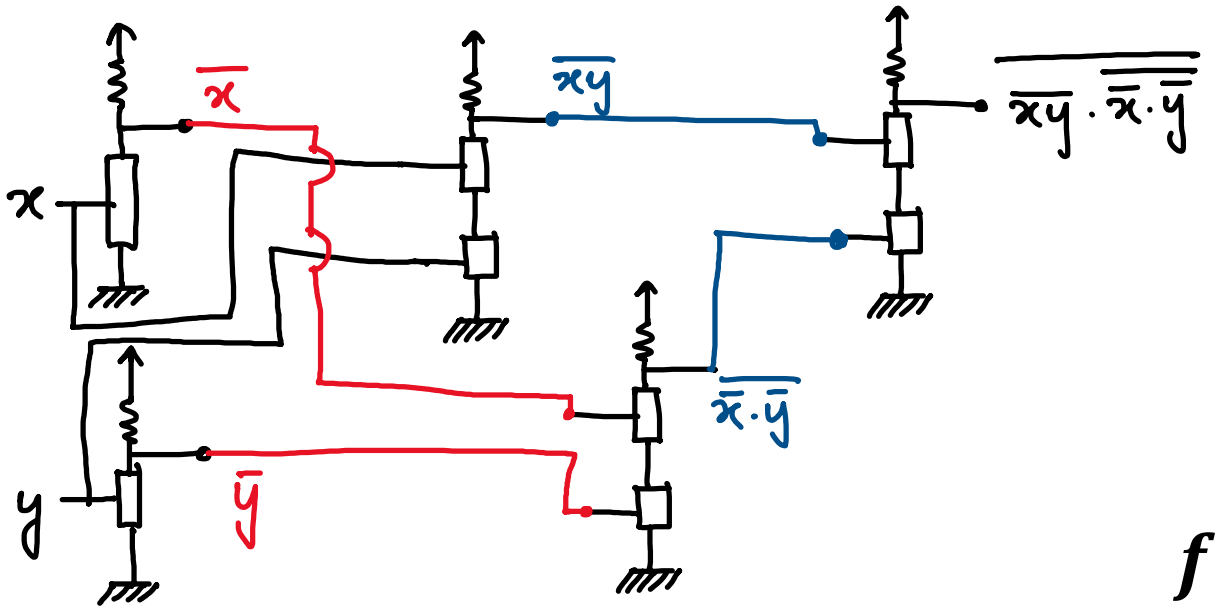
Implement using switches: $f = (A + B)C$



Practice Problem 1

In digital systems, binary data may be subjected to noise that can alter a 0 to a 1 or a 1 to a 0.

A simple way to check if any error has occurred is to use an **even parity checker**. If there are two input bits x and y, the output of the even parity checker (denoted as f) will be **HIGH** if there are even number of 1s, i.e., if both x and y are 0 or if both of them are 1.



x	y	f
0	0	
0	1	
1	0	
1	1	

$$f = x \cdot y + \overline{x} \cdot \overline{y} = \overline{\overline{x \cdot y + \overline{x} \cdot \overline{y}}}$$
$$= \overline{\overline{x.y} \cdot \overline{\overline{x}} \cdot \overline{\overline{y}}}$$

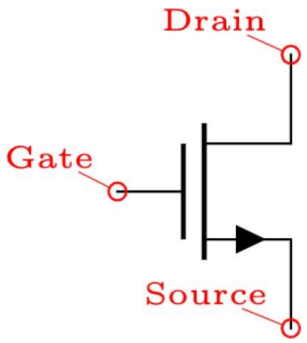
Digital Representation

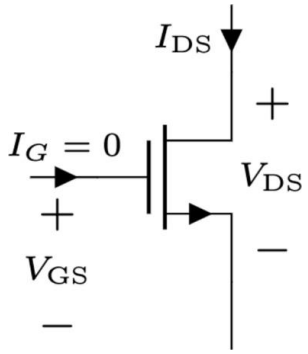
- Binary → Two states (0/False, 1/True)
- Binary variables in circuit, need to use two states of device/parameters

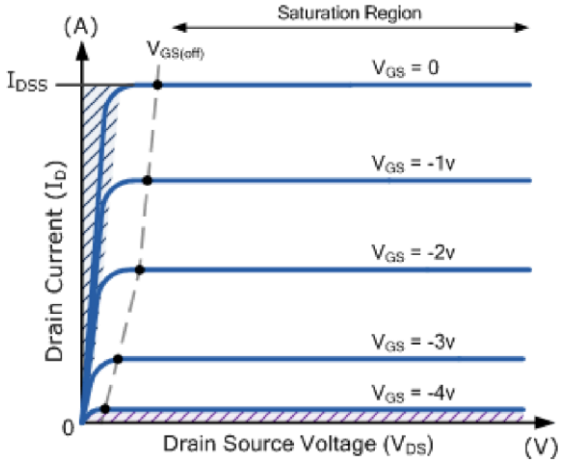
Voltage	Current	State

Transistors as Digital Switch

- Transistors are 3 terminal non-linear devices, can be used as switch
- 2 types – **Voltage Controlled**, **Current Controlled**
- **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor (**MOSFET**) are voltage controlled
- Control, $\boldsymbol{C = V_{GS}}$. The IV characteristics ($\boldsymbol{I_{DS}}$ vs $\boldsymbol{V_{DS}}$) depends on $\boldsymbol{V_{GS}}$
- Actual dependency is complex.
- Will start with a simple (but approximate) one – **S-Model** (Switch Model)

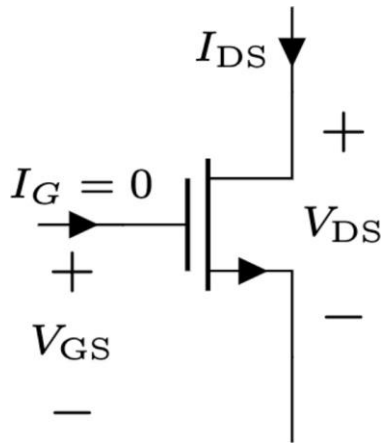


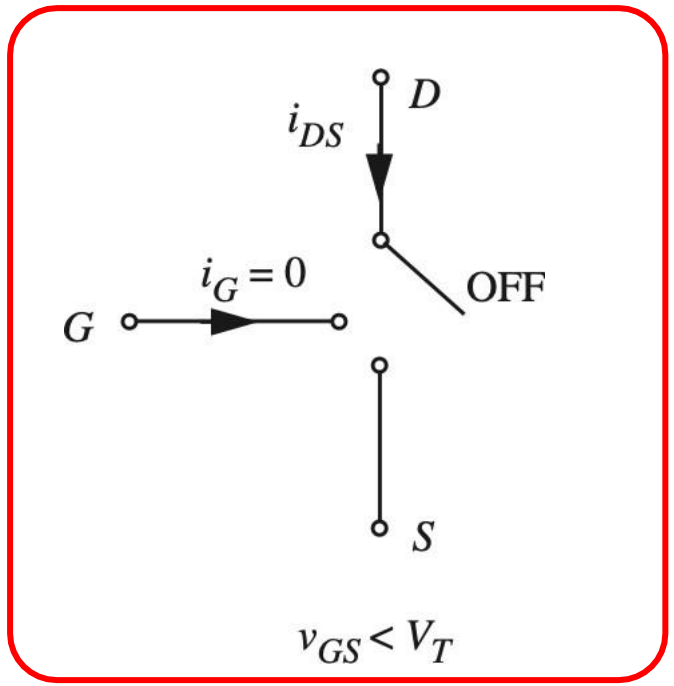


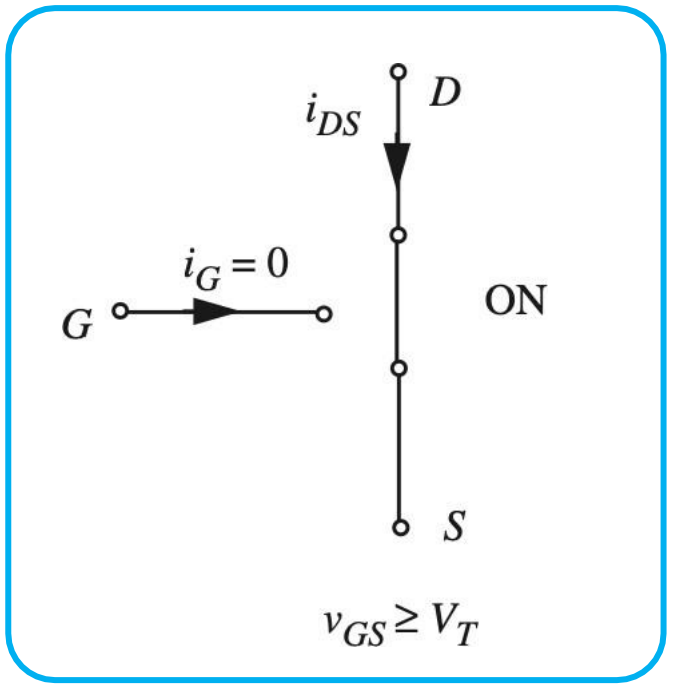


MOSFET S-Model

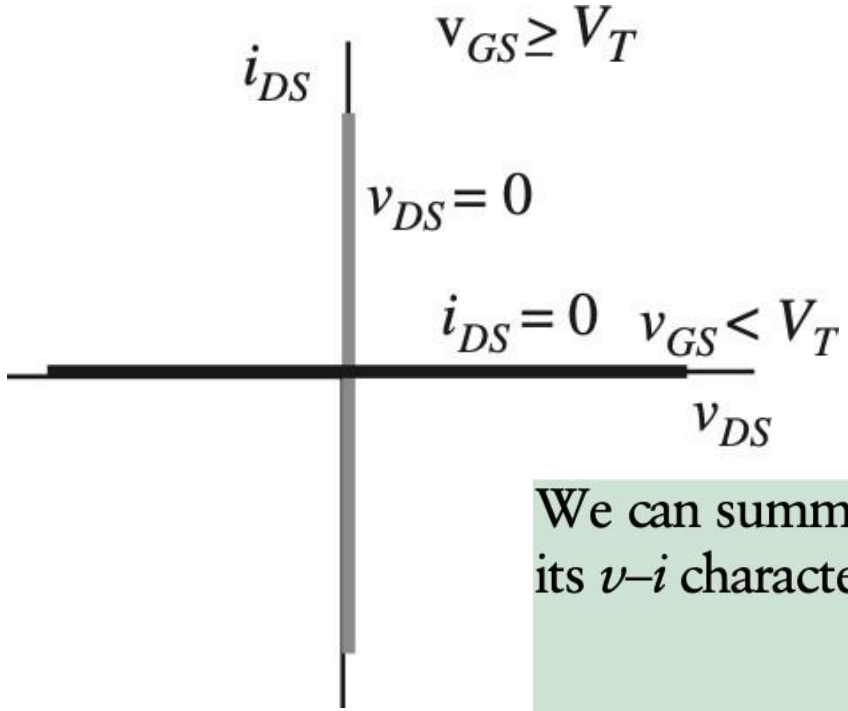
- The MOSFET (approximately) behaves like a switch
- C = V_{GS}. Here, $C = \text{“0”} \Rightarrow \boldsymbol{V_{GS} < V_T}$, and $C = \text{“1”} \Rightarrow \boldsymbol{V_{GS} < V_T}$







MOSFET S-Model



We can summarize the S model for the MOSFET in algebraic form by stating its v–i characteristics as follows:

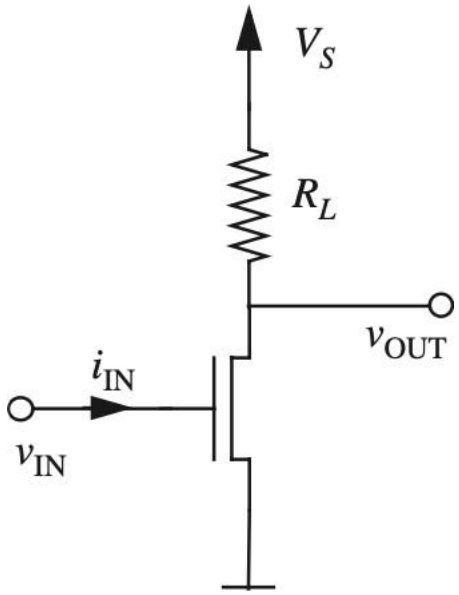
$$\text{for } v_{GS} < V_T, \quad i_{DS} = 0$$

and

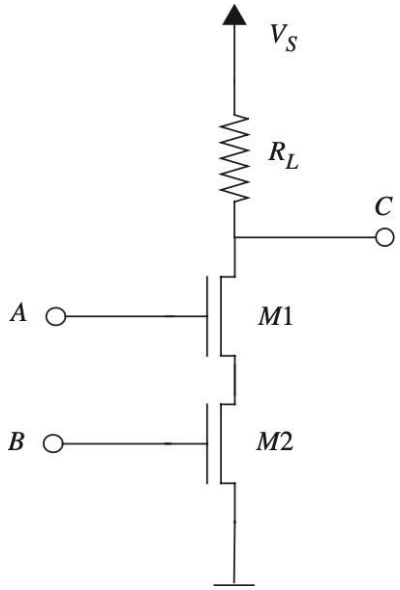
$$\text{for } v_{GS} \geq V_T, \quad v_{DS} = 0 \tag{6.2}$$

Logic Gates using MOSFET

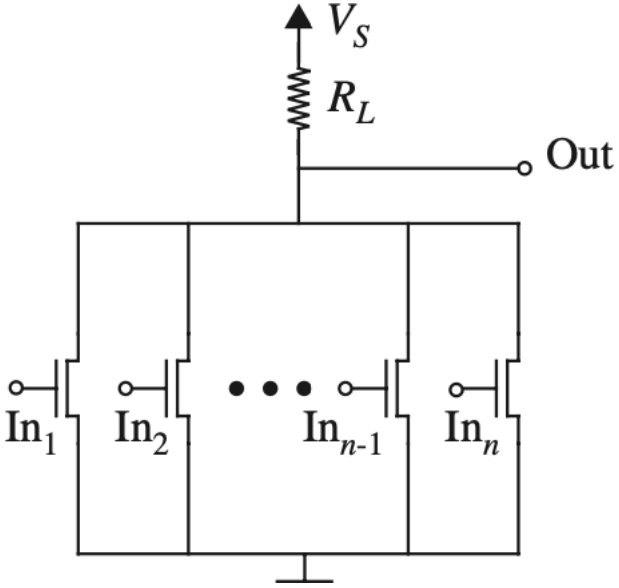
Just replace the switches with MOSFETs!



NOT Gate (Inverter)

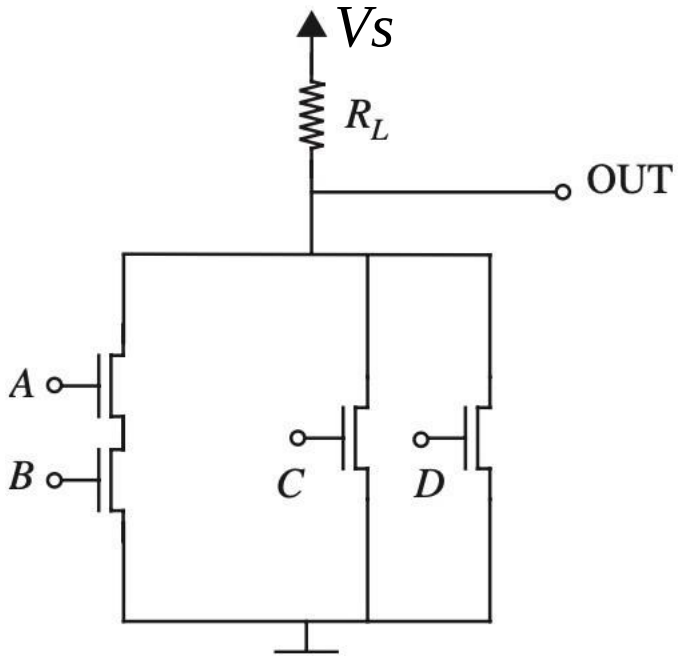


NAND Gate (Inverter)

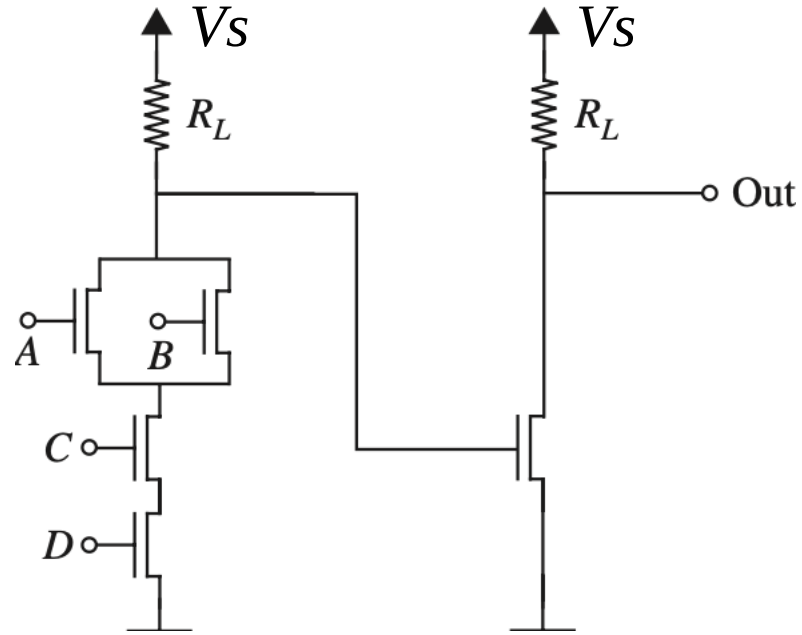


NOR Gate (Inverter)

MOSFET Logic Gates – More Examples



$$OUT = \overline{AB + C + D}$$



$$Out = \overline{\overline{(A + B)CD}} = (A + B)CD$$

Practice Problem 2

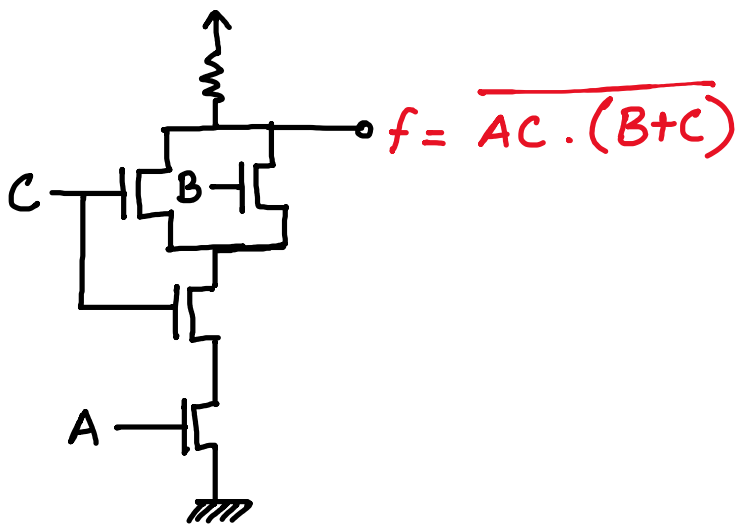
- **Design** a circuit using ideal MOSFETs (S-model) to implement the logic function

$$f = \overline{AC} + \overline{(B+C)}$$

$$= \overline{\overline{\overline{AC}} + \overline{(B+C)}}$$

$$= \overline{\overline{\overline{AC}} \cdot \overline{(B+C)}} \quad \text{[De Morgan's Theorem]}$$

$$= \overline{AC \cdot (B+C)}$$



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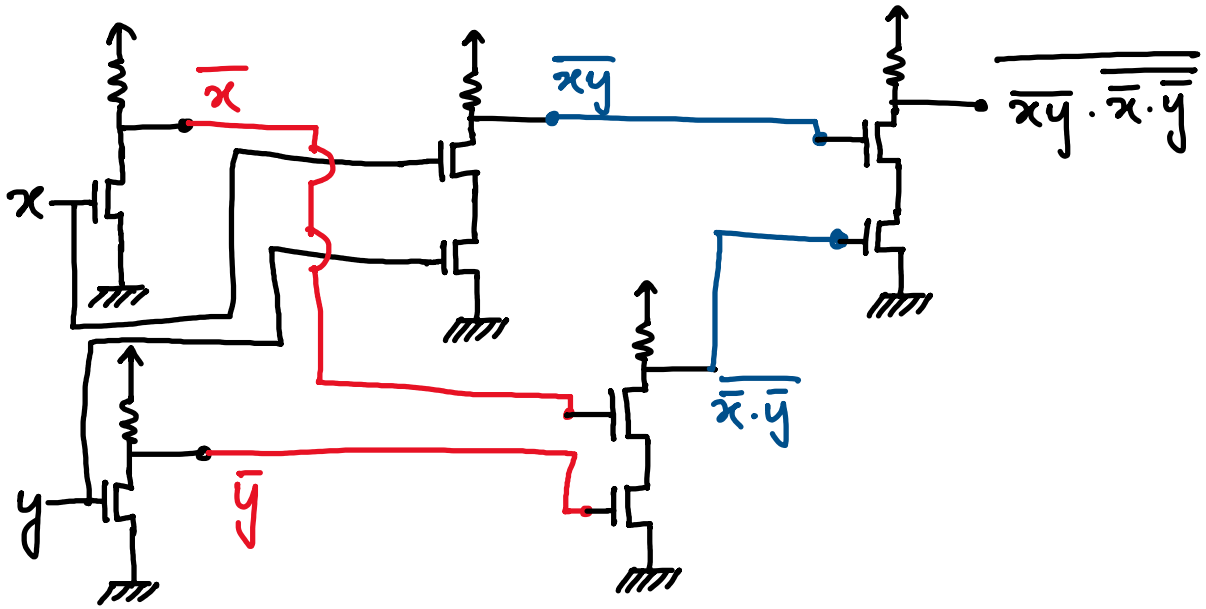
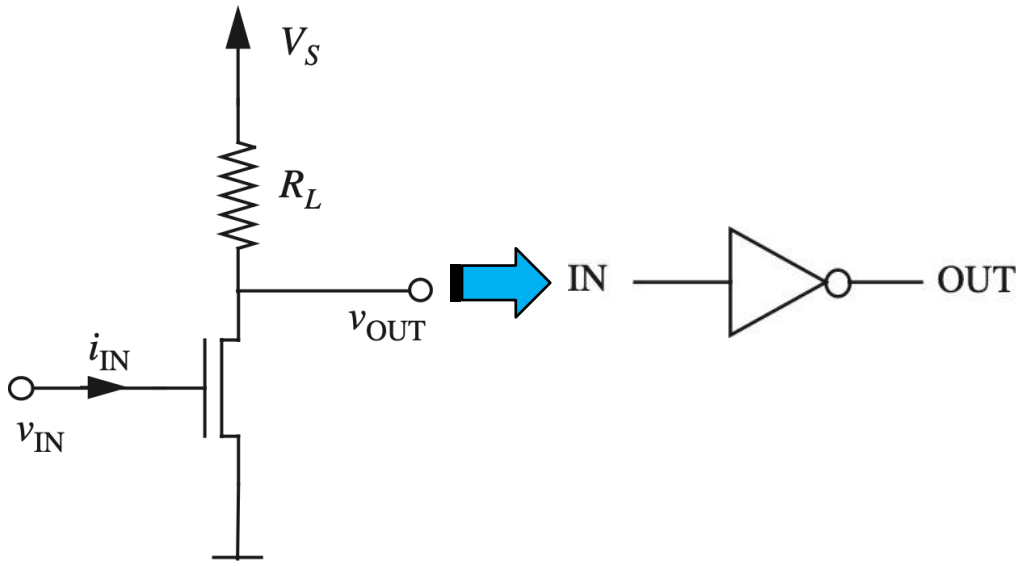


x	y	f
0	0	
0	1	
1	0	
1	1	

$$f = x \cdot y + \overline{x} \cdot \overline{y} = \overline{\overline{x \cdot y + \overline{x} \cdot \overline{y}}}$$
$$= \overline{\overline{x.y} \cdot \overline{\overline{x} \cdot \overline{y}}}$$

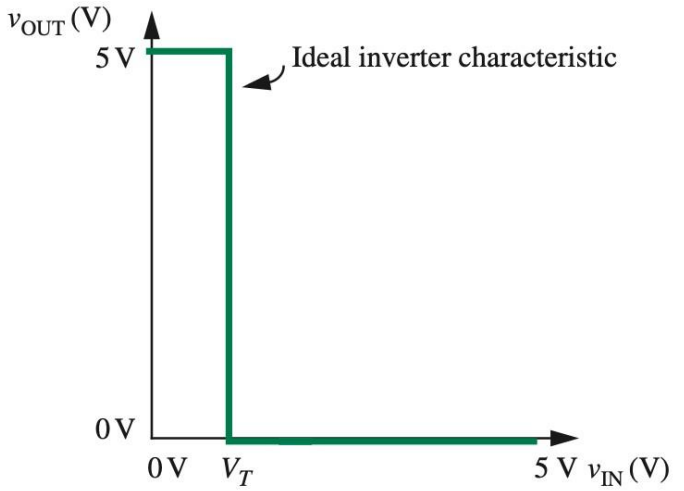
Voltage Transfer Characteristics (VTC)

- **Reminder:** VTC is a graph where $\boldsymbol{x}$ −axis = input voltage, $\boldsymbol{y}$-axis = output voltage
- **Why?** Design logic gates to follow a given static discipline



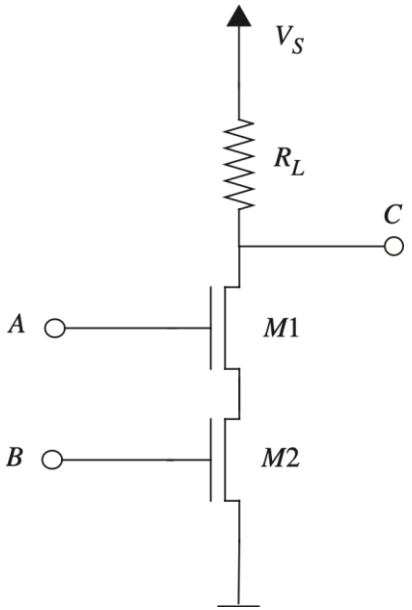
When $v_{IN} < V_T$ (Logical 0) $v_{OUT} = V_S = 5$ V (Logical 1)

When $v_{IN} \geq V_T$ (Logical 1) $v_{OUT} = 0$ V (Logical 0)

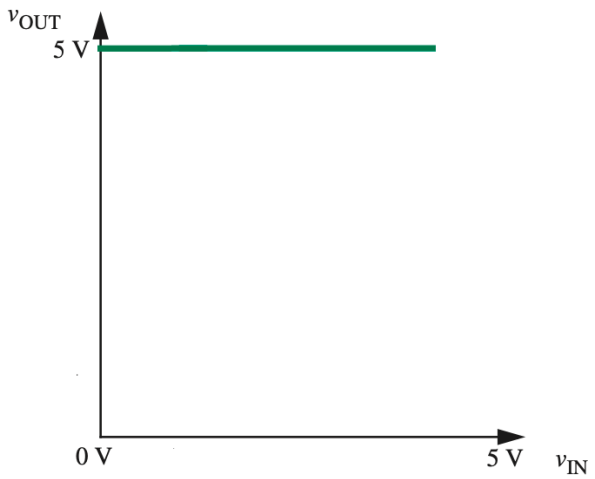


VTC of NAND gate

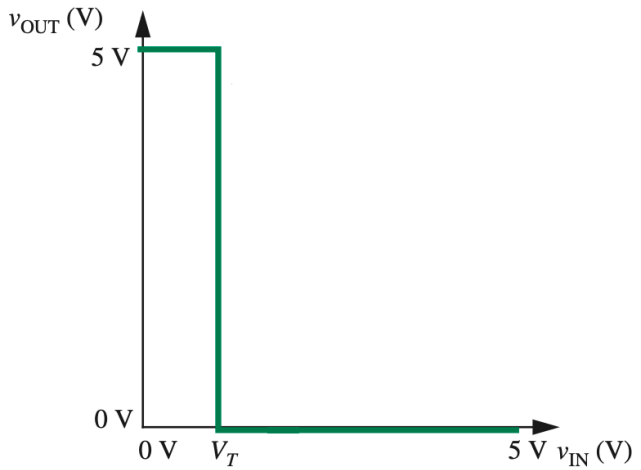
- We only have one $\boldsymbol{x}$ –axis, but two inputs
- **Solution:** Draw two VTC, one considering $V_A = 0$ one considering $V_A = 1$



When $V_A = 0$



When $V_A = 1$

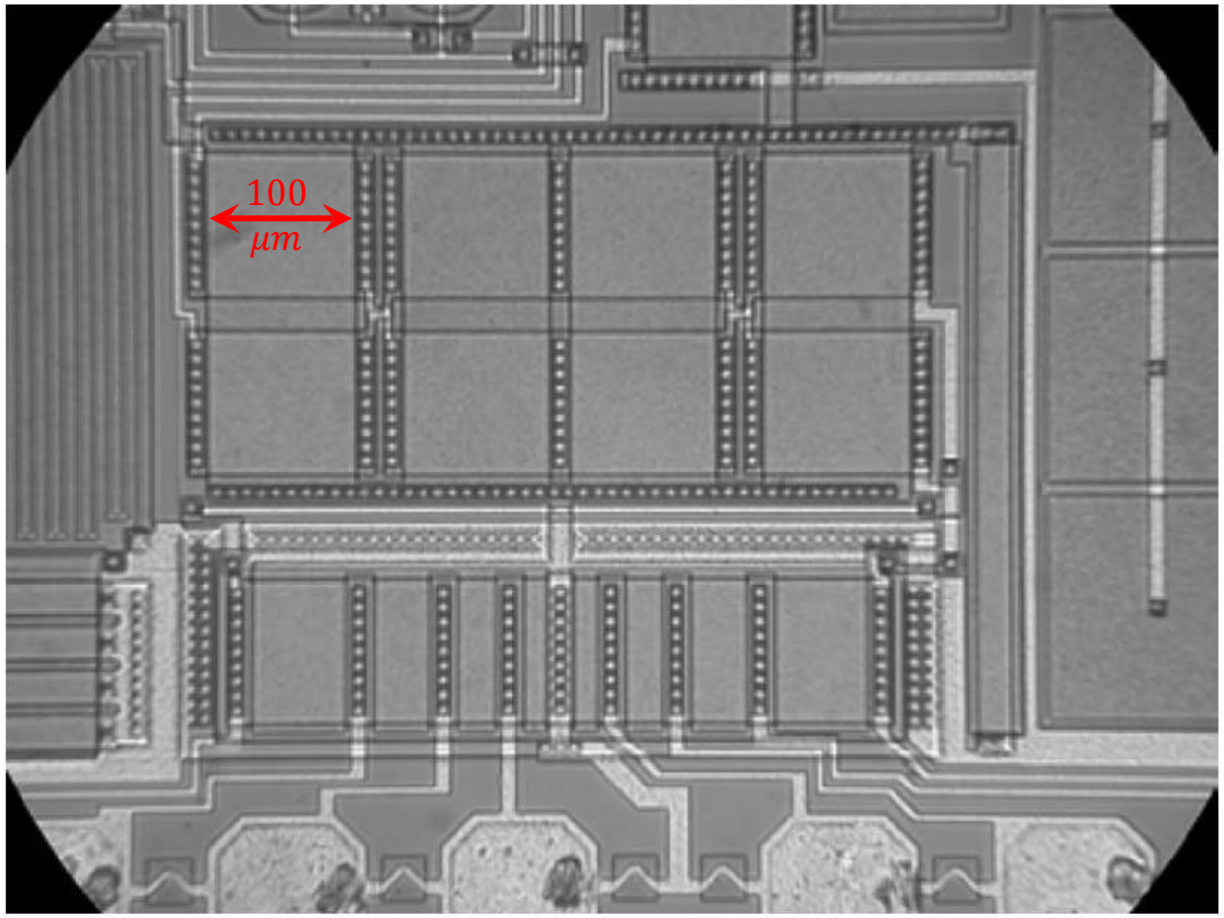


Homework: Find VTC for NOR gate

Outline

- Constructing a *real* MOSFET – n/p-channel
- **Operation of an MOSFET-**
  1. Cut-Off
  2. Saturation
  3. Triode Mode
- Output Characteristics
- PWL Model and Non-ideal Analysis: **SR model**
- Real MOSFET equations
- Introduction to Static analysis

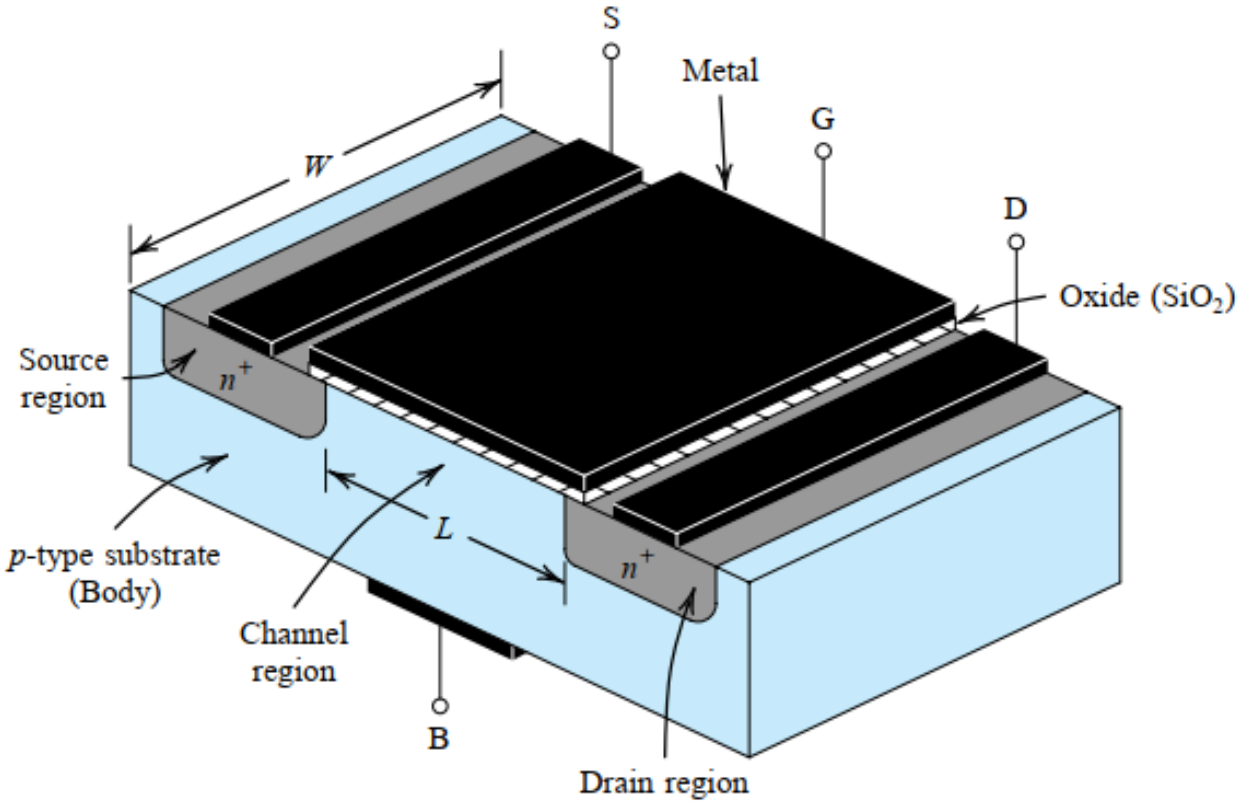
Construction of Real MOSFET

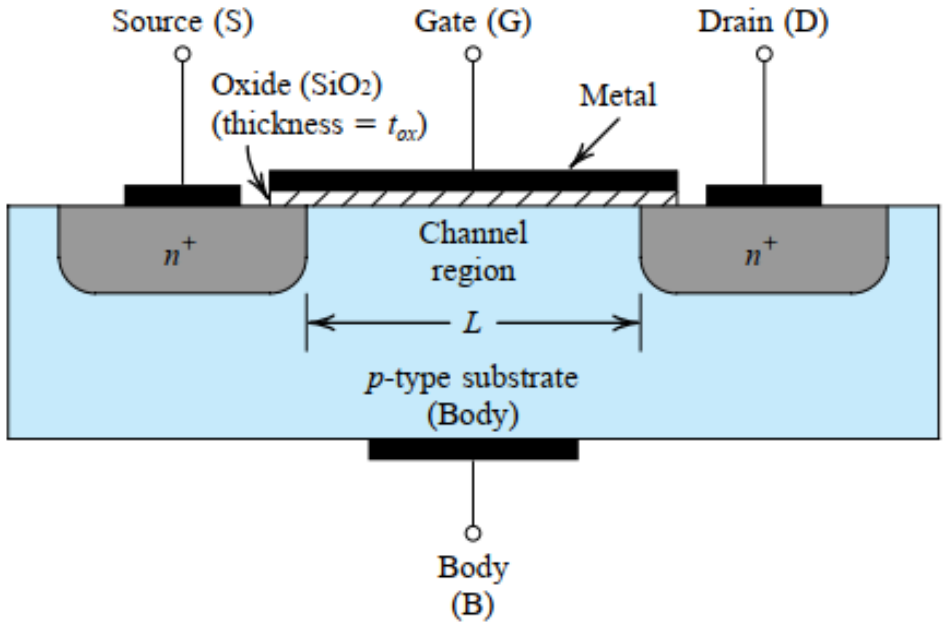


Top view of several n-channel MOSFETs fabricated on a chip. The square MOSFETs in the center of the photograph have a width and length of 100 μm. (Photograph Courtesy of Maxim Integrated Products.)

Real MOSFET – Enhancement Type

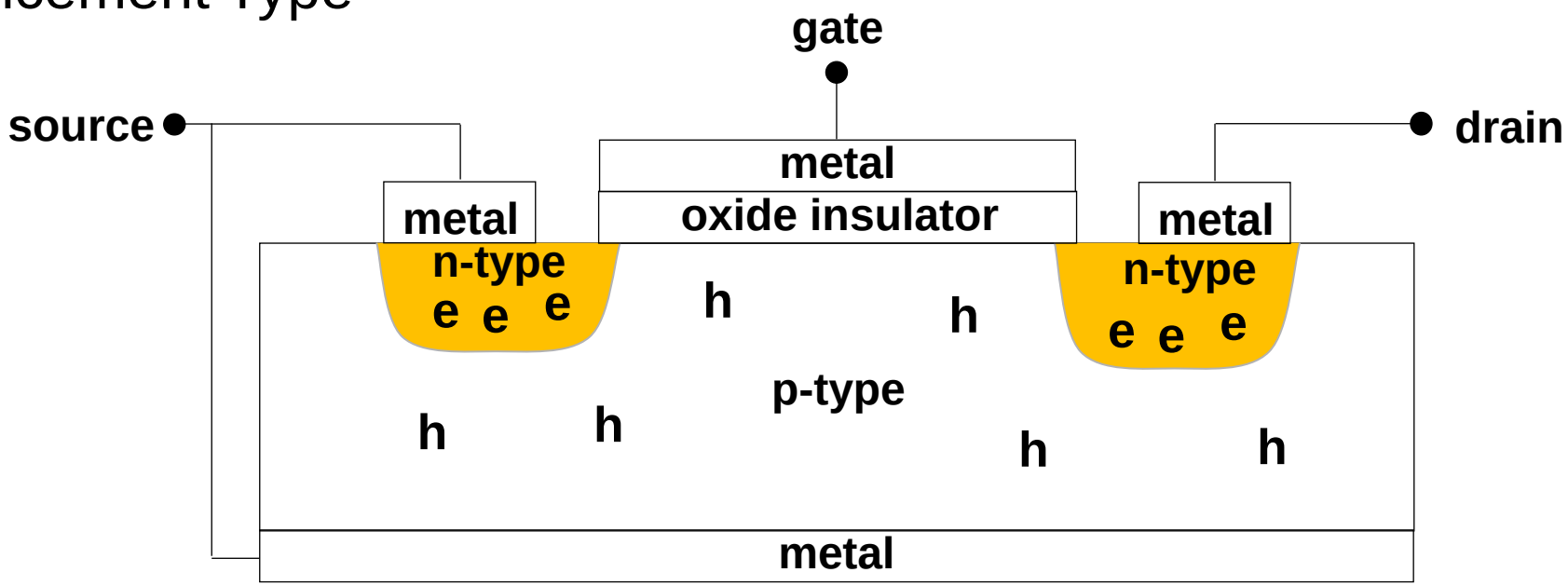
Device Structure (*n*-channel MOSFET)



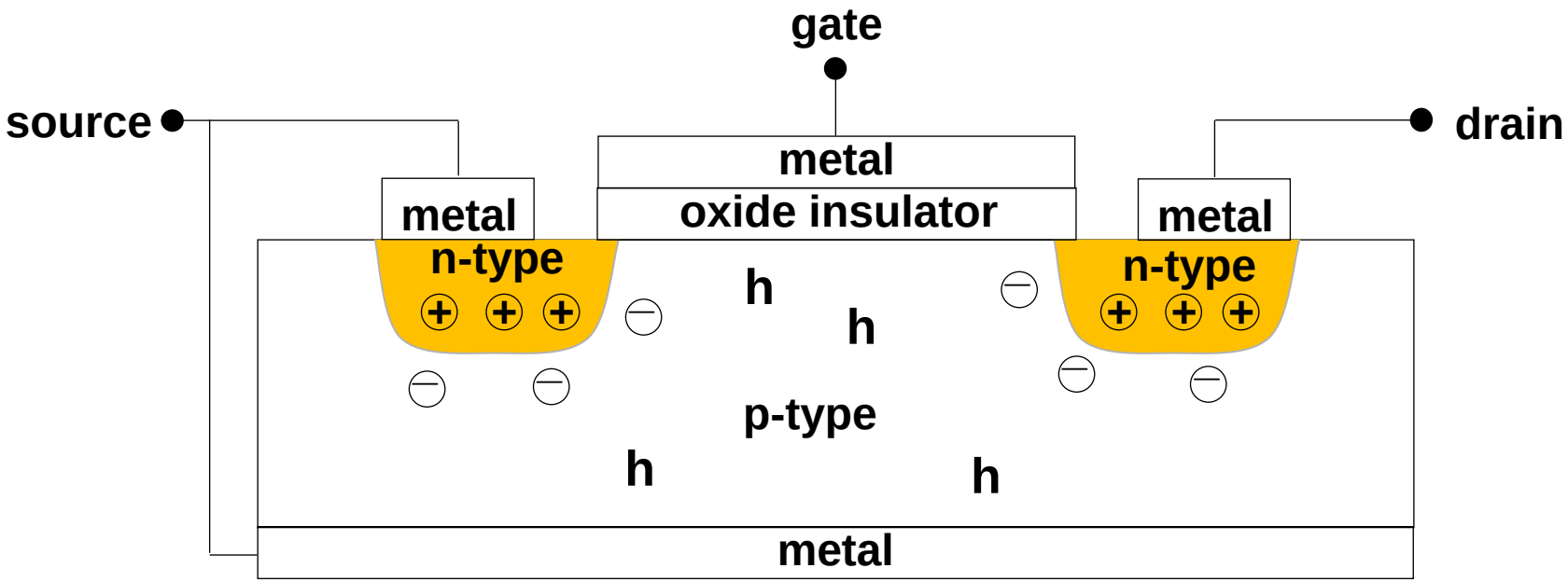


n-channel **MOS**FET (NMOS) Physical Structure

Enhancement Type



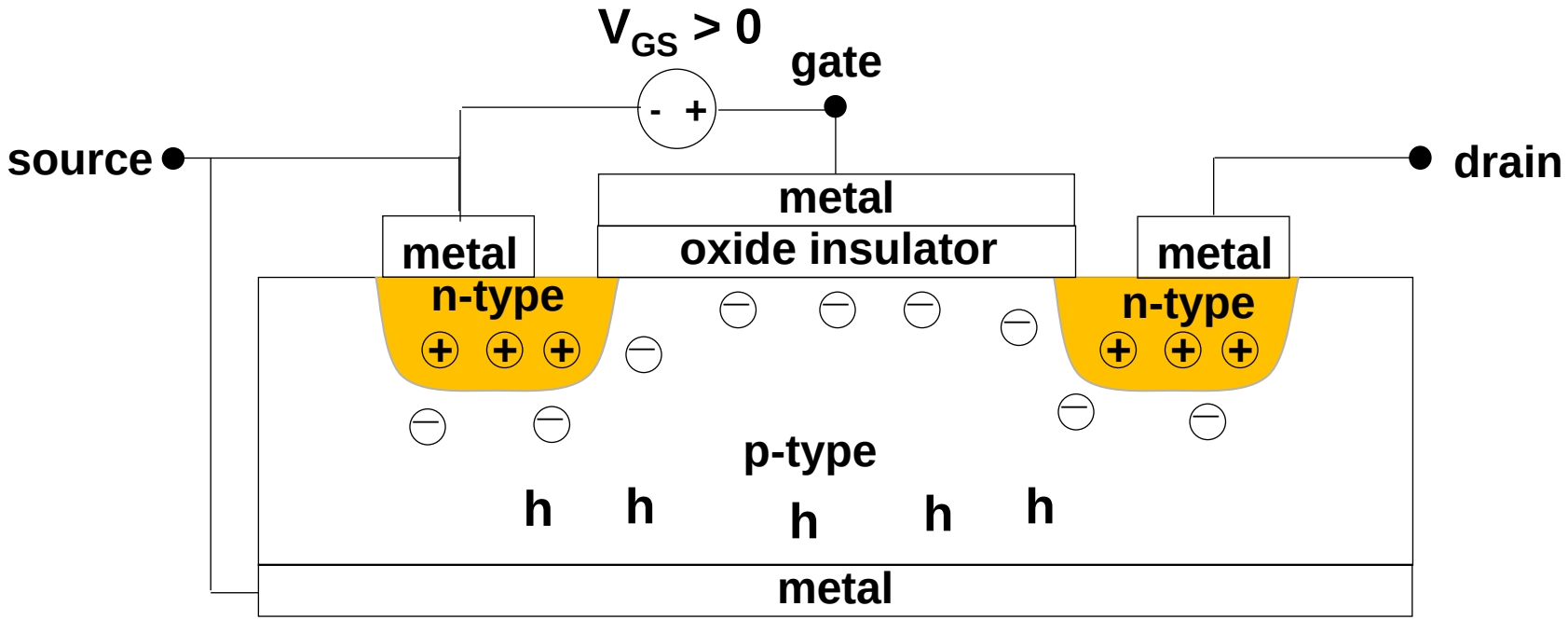
NMOS in Equilibrium



When the transistor is left alone, some electrons from the n-type wells diffuse into the p-type material to fill holes.

This creates negative ions in the p-type material and positive ions are left behind in the n-type material.

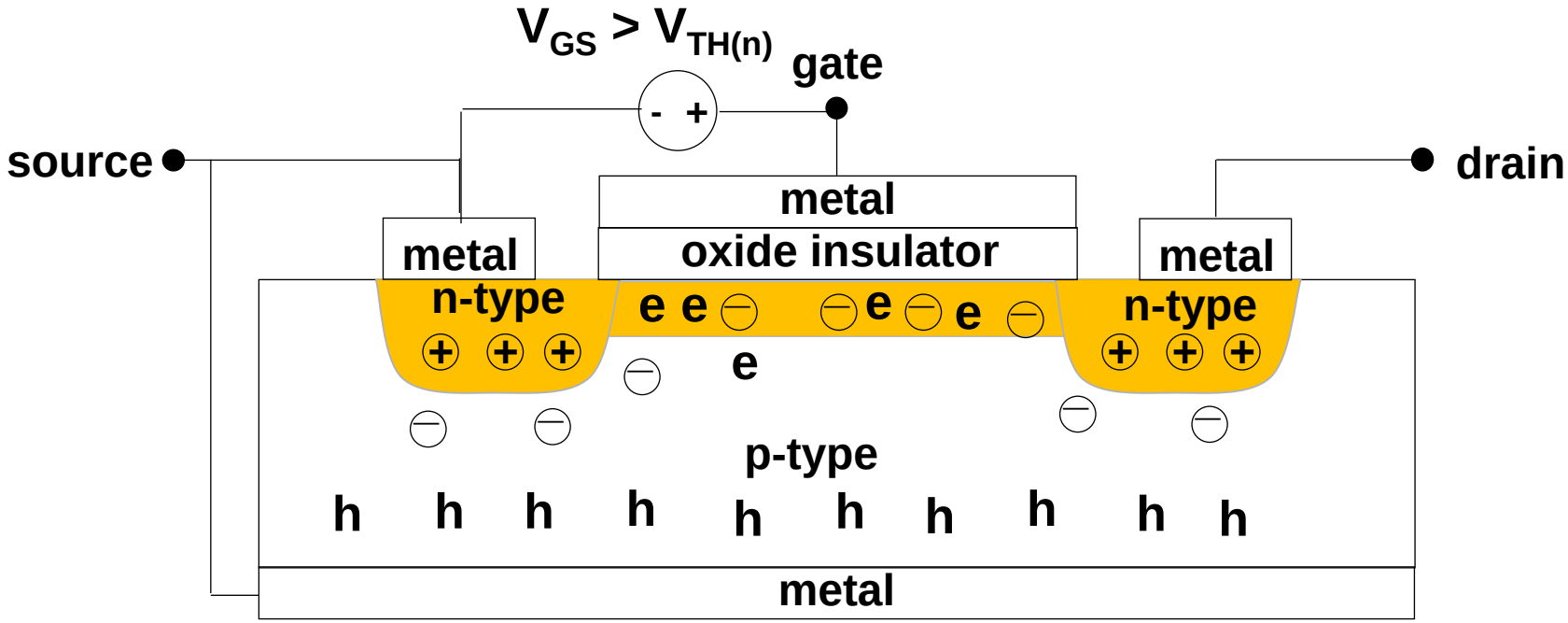
NMOS in Cutoff



When a small, positive V_{GS} is applied, holes “move away” from the gate.

Electrons from complete atoms elsewhere in the p-type material move to fill holes near the gate instead.

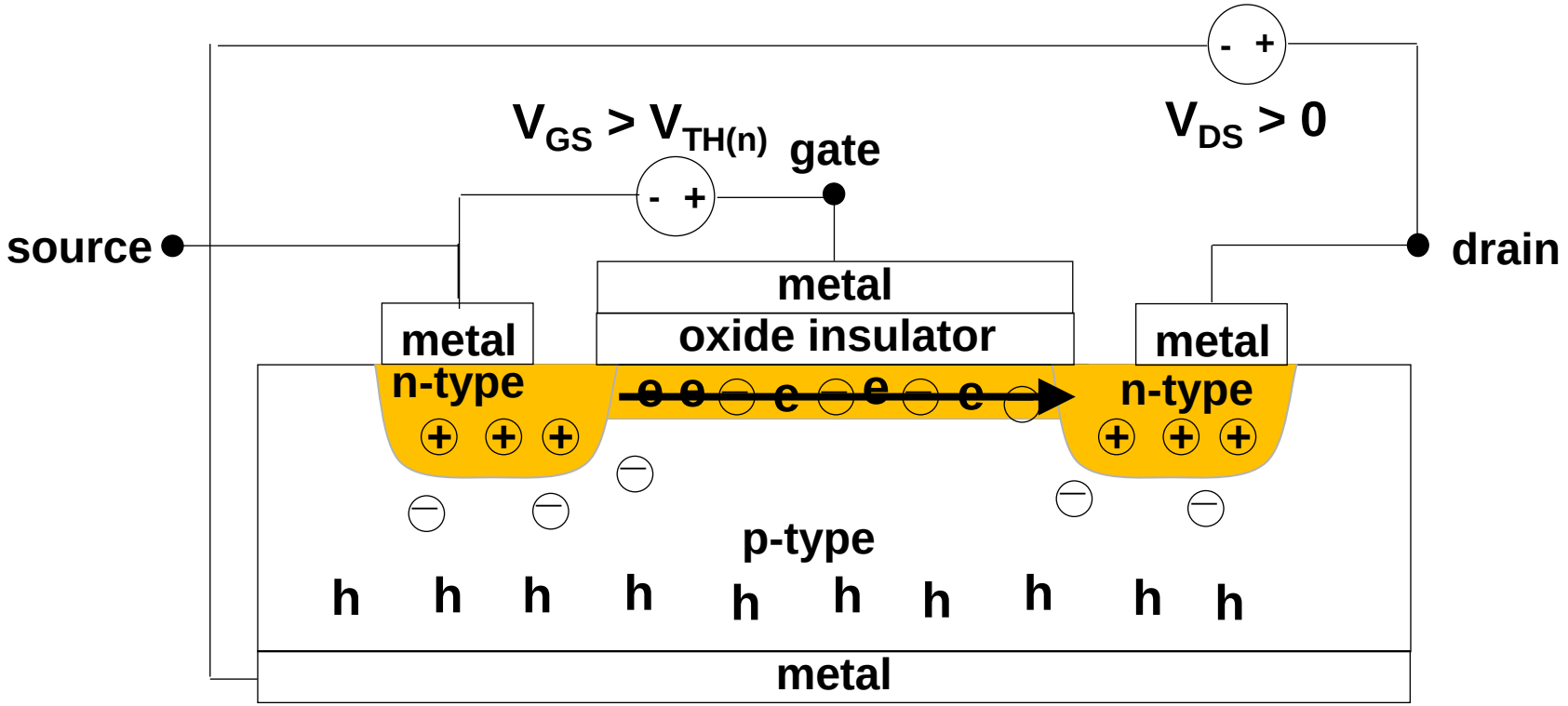
NMOS Transistor channel



When V_{GS} is larger than a **threshold** voltage $V_{TH(n)}$, the attraction to the gate is so great that free electrons collect there.

The applied V_{GS} creates an **induced n-type channel** under the gate (an area with free electrons).

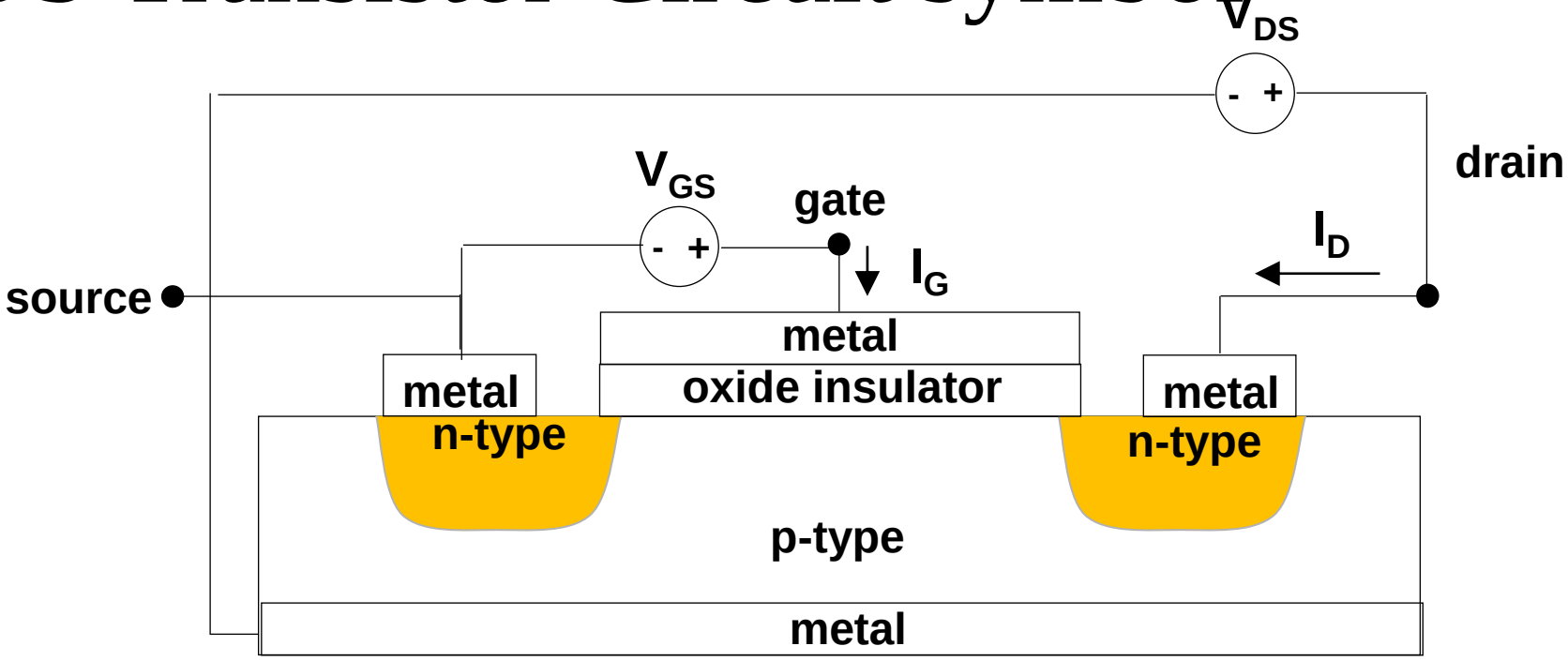
NMOS Transistor Drain Current

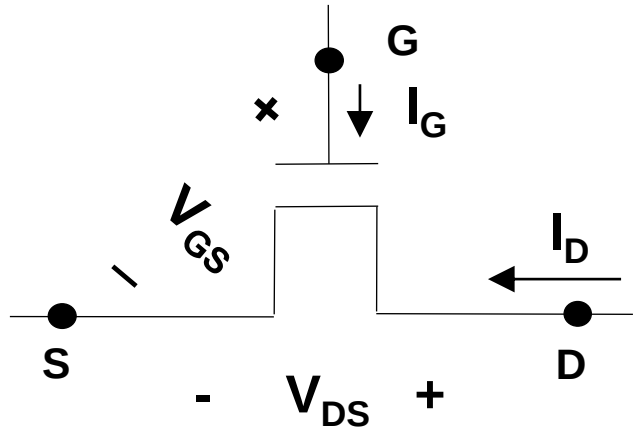


When a positive V_{DS} is applied, the free electrons flow from the source to the drain. (Positive current flows from drain to source).

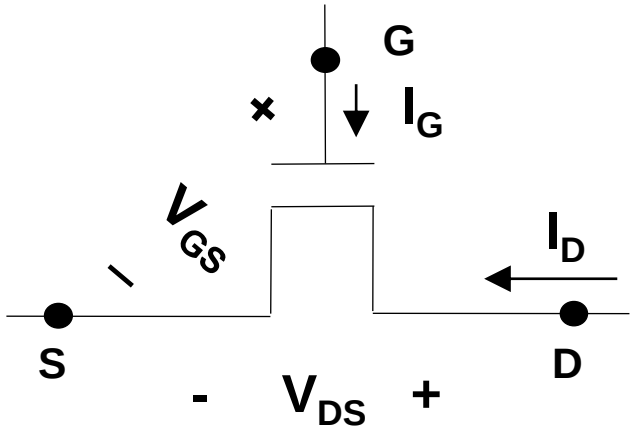
The amount of current depends on V_{DS}, as well as the number of electrons in the channel, channel dimensions, and material.

NMOS Transistor Circuit symbol





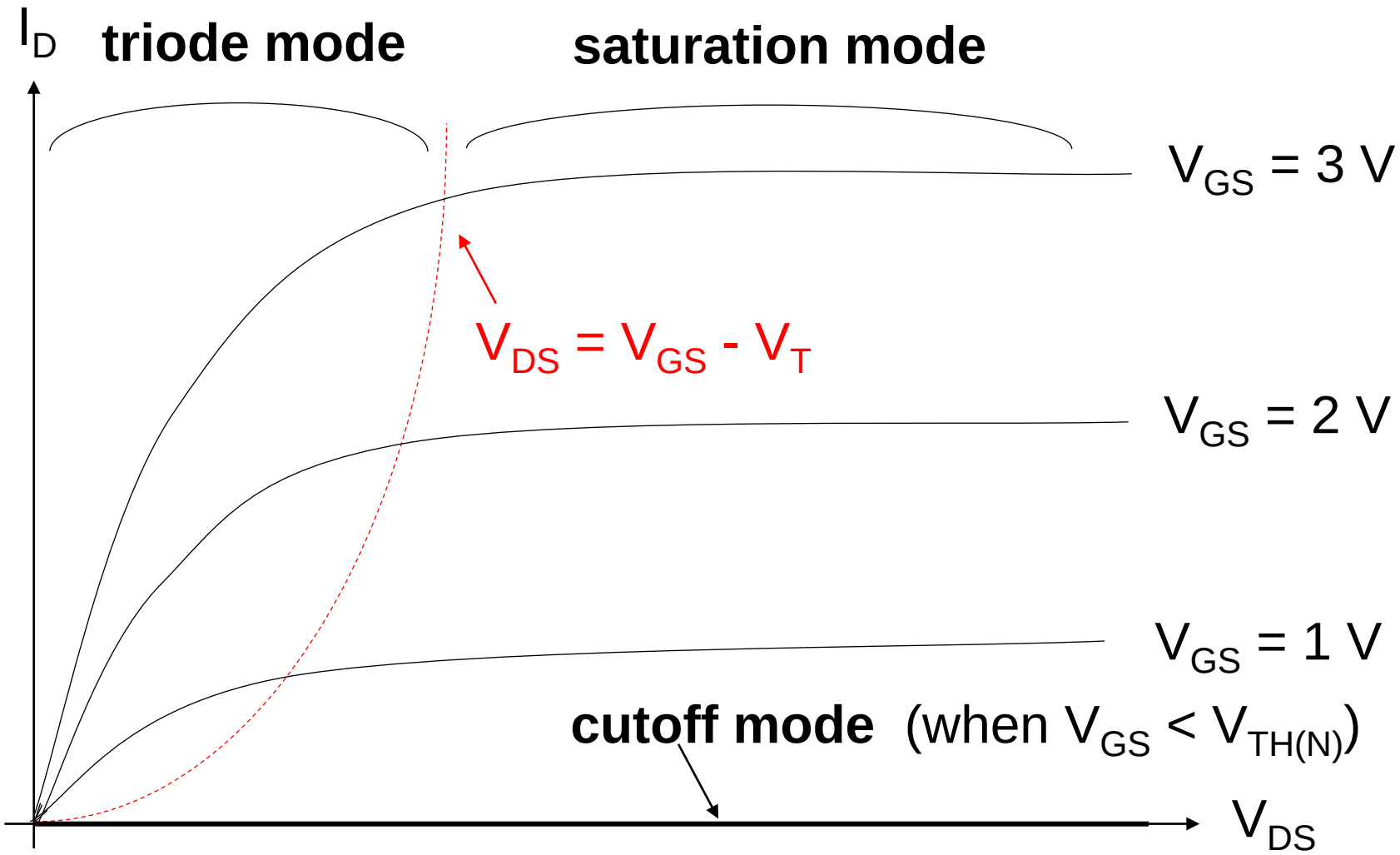
NMOS I-V Characteristic



- Since the transistor is a 3-terminal device, there is no single I-V characteristic.
- Note that because of the insulator, $I_G = 0$ A.
- We typically define the MOS I-V characteristic as

  I_D vs. V_{DS} for a fixed V_{GS}.
- The I-V characteristic changes as V_{GS} changes.

NMOS I-V Characteristic



Modes of Operation

- For small values of V_{GS}, $V_{GS} \leq V_{TH(n)}$, the n-type channel is not formed. No current flows. This is **cutoff mode**.
- When $V_{GS} > V_{TH(n)}$, current I_D may flow from drain to source, and the following modes of current flow are possible.
  - The mode of current flow depends on the propelling voltage, V_{DS}, and the channel-inducing voltage,

    $V_{GS} - V_{TH(n)}$.
  - When $V_{DS} < V_{GS} - V_{TH(n)}$, current is starting to flow. I_D increases rapidly with increased V_{DS}. This is **triode mode**.
  - When $V_{DS} \geq V_{GS} - V_{TH(n)}$, current is reaching its maximum value. I_D does not increase much with increased V_{DS}. This is called **saturation mode**.

Water Tap Analogy

Imagine the water tap on your kitchen sink.

- To make water flow, the water supply has to be connected to the water tap. This establishes a path for water to flow.
- Setting V_{GS} above the threshold voltage is like connecting the water supply.
- **Cutoff = water supply disconnected (no path for current flow)**
- Setting V_{GS} to a larger value is like connecting a high-pressure water supply—more flow can potentially occur.

Water Tap Analogy

- The water tap itself is used to adjust water flow. You can turn the flow up and down.
- V_{DS} is like the water tap. It controls the amount of flow.
- There is, of course, a saturation point. If you keep turning the water tap control, eventually you won't get any more flow.
- **Triode = water tap in "normal range", controls flow**
- **Saturation = water tap turned up to (or past) point for maximum flow**

NMOS Equations

Cutoff Mode

Occurs when $v_{GS} < V_T$

$$I_D = 0$$

Triode Mode

Occurs when $v_{GS} \geq V_T$ and $v_{DS} < v_{GS} - V_T$

$$I_{DS} = k'_n \frac{W}{L}\left(v_{GS} - V_T - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Mode

Occurs when $v_{GS} > V_T$ and $v_{DS} \geq v_{GS} - V_T$

$$I_{DS} = \frac{1}{2}k'_n \frac{W}{L}(v_{GS} - V_T)^2$$

$v_{GS} - V_T = V_{OV}$: Overdrive Voltage

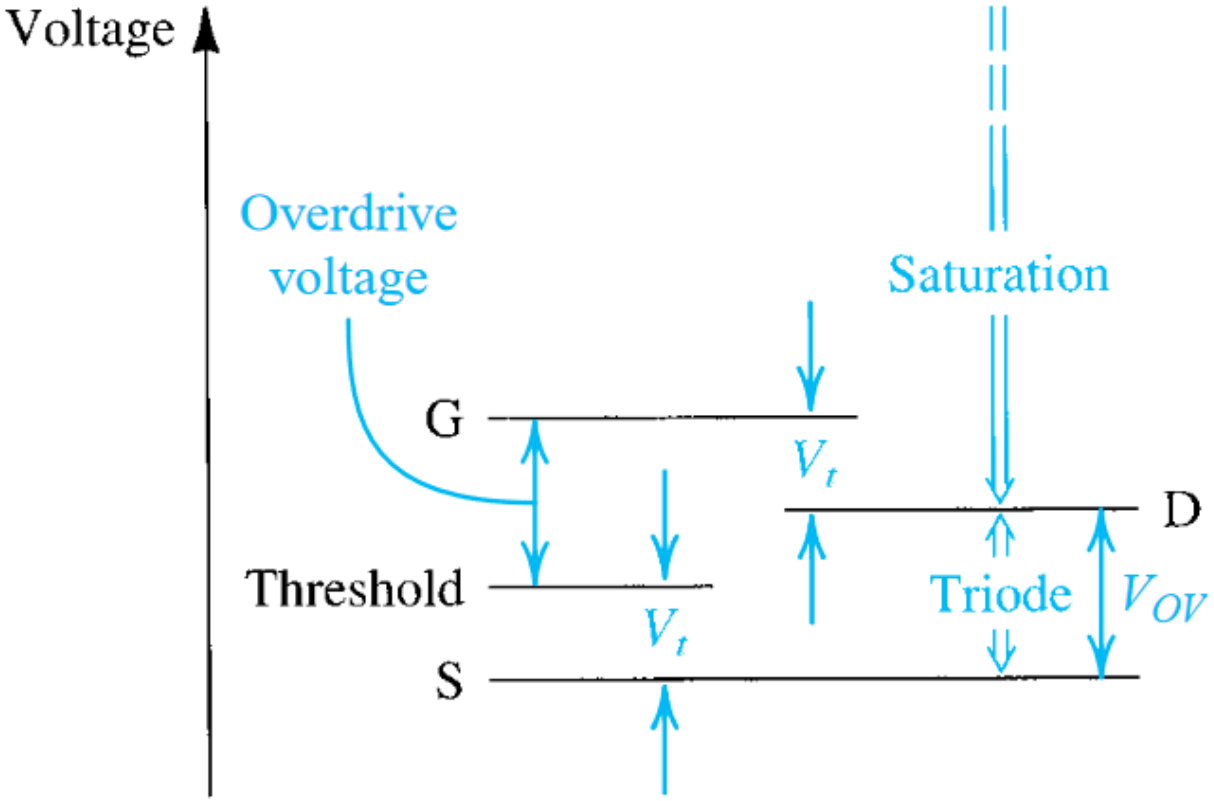
V_{OV}

Indicates the available excess voltage at **gate** after forming the n-channel.

V_T

The minimum voltage necessary at the **gate** terminal to form a channel.

Real MOSFET



$k_n = k'_n \frac{W}{L}$ MOSFET transconductance

v_{GS}: Gate Voltage

v_{DS}: Drain to Source Voltage

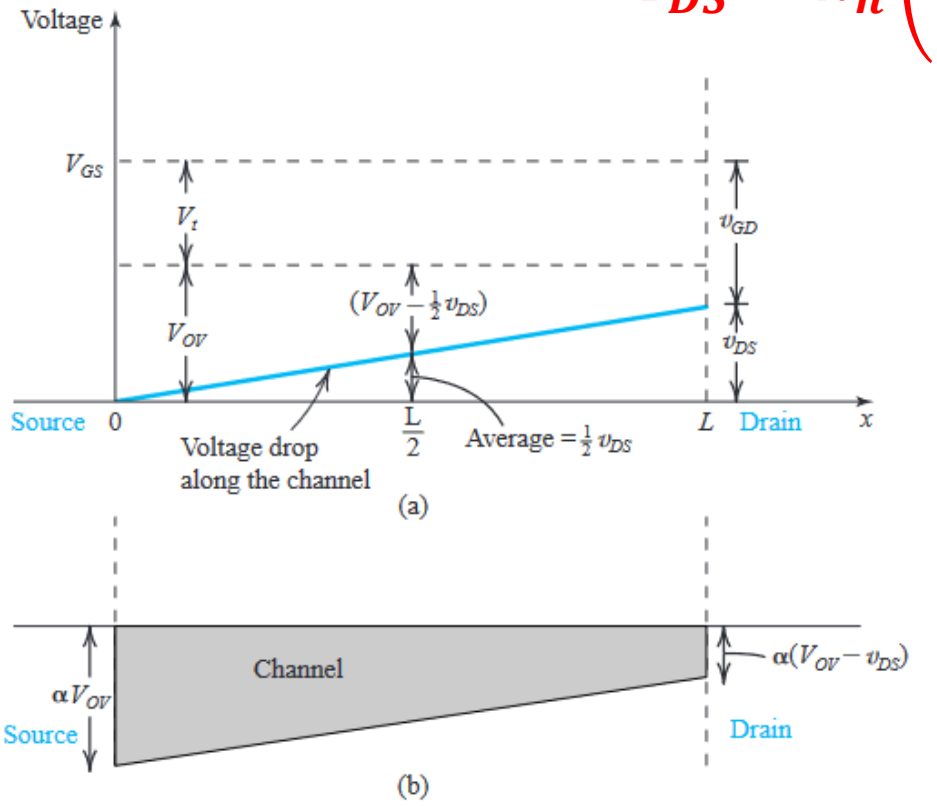
V_T: Threshold Voltage

$V_{OV} = v_{GS} - V_T$: Overdrive voltage

NMOS Triode Mode

Occurs when $v_{GS} \geq V_T$ and $v_{DS} < v_{GS} - V_T$

$$I_{DS} = k_n \left(v_{GS} - V_T - \frac{1}{2} v_{DS} \right) v_{DS}$$



$$I_{DS} \propto k_n'$$

$$I_{DS} \propto \frac{W}{L}$$

$$I_{DS} \propto (V_{OV} - \frac{1}{2} v_{DS})$$

Overdrive Voltage is defined as:

$$V_{OV} = v_{GS} - V_T$$

In triode mode, average voltage across channel is actually:

$$(V_{OV} - \frac{1}{2} v_{DS})$$

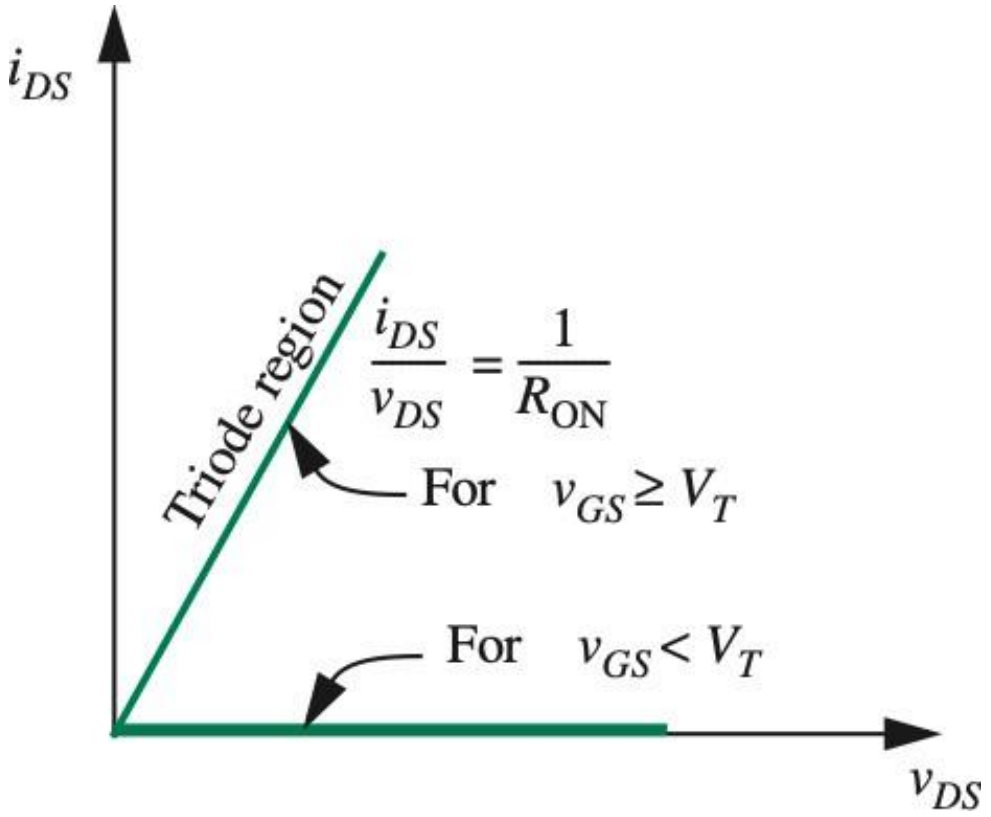
NMOS Triode Mode

$$I_{DS} = k_n' \frac{W}{L}\left(v_{GS} - V_T - \frac{1}{2}v_{DS}\right)v_{DS}$$

$$I_{DS} = \frac{1}{R_{ON}}v_{DS}$$

$$R_{ON} = \frac{1}{k_n' \frac{W}{L}(v_{GS} - V_T - \frac{1}{2}v_{DS})}$$

$$= \frac{1}{k_n(V_{OV} - \frac{1}{2}v_{DS})}$$



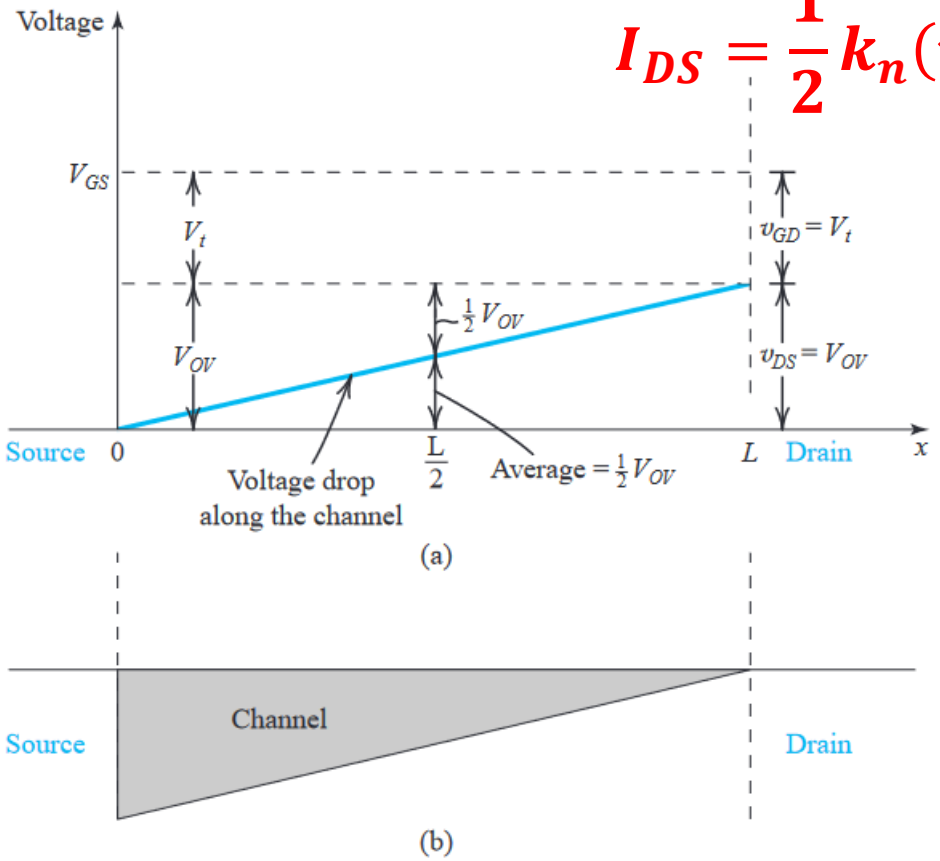
NMOS Saturation mode

Occurs when $v_{GS} > V_T$ and $v_{DS} \geq v_{GS} - V_T$

$$I_{DS} = \frac{1}{2} k_n (v_{GS} - V_T)^2 = \frac{1}{2} k_n V_{OV}^2$$

$$I_{DS} \propto k_n'$$

$$I_{DS} \propto \frac{W}{L}$$



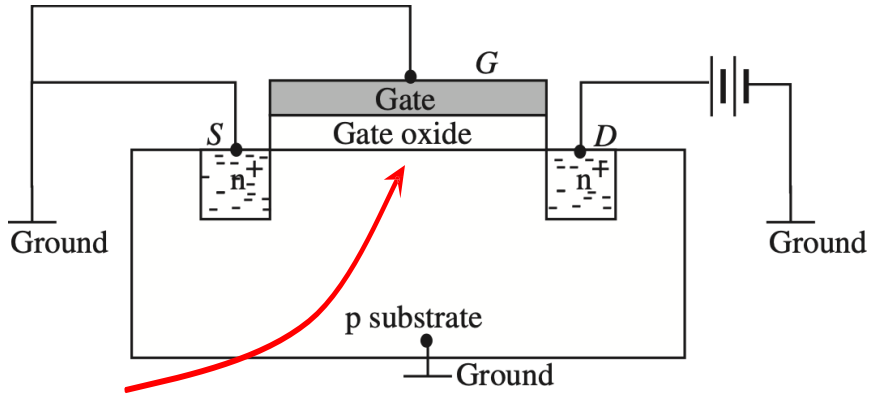
Overdrive Voltage is defined as:

$$V_{OV} = v_{GS} - V_T$$

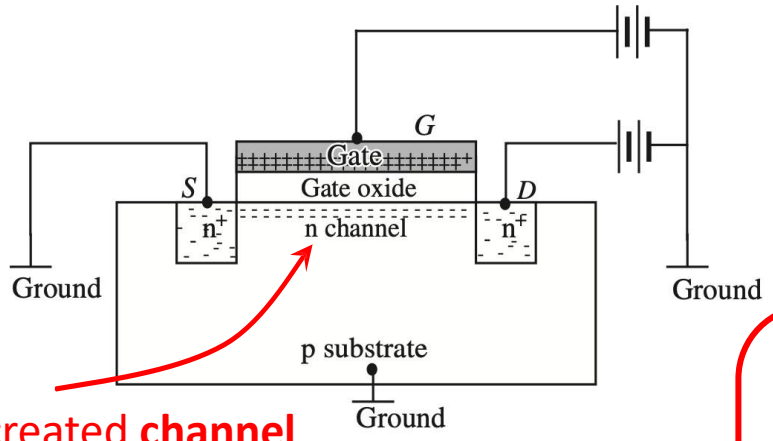
In **Saturation** mode, average voltage across channel fixed at:

$$\frac{1}{2} V_{OV}$$

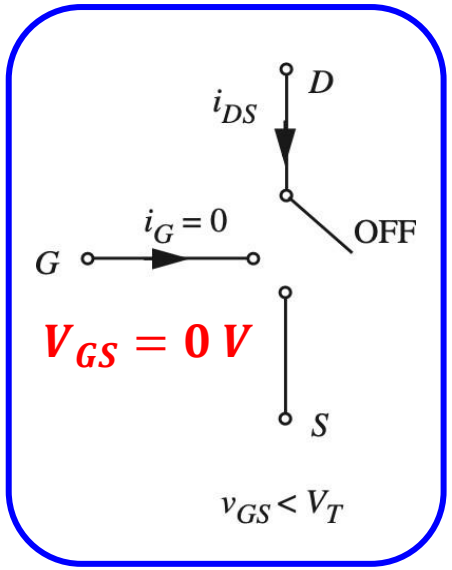
n-channel MOSFET - Summary



No channel, open ckt

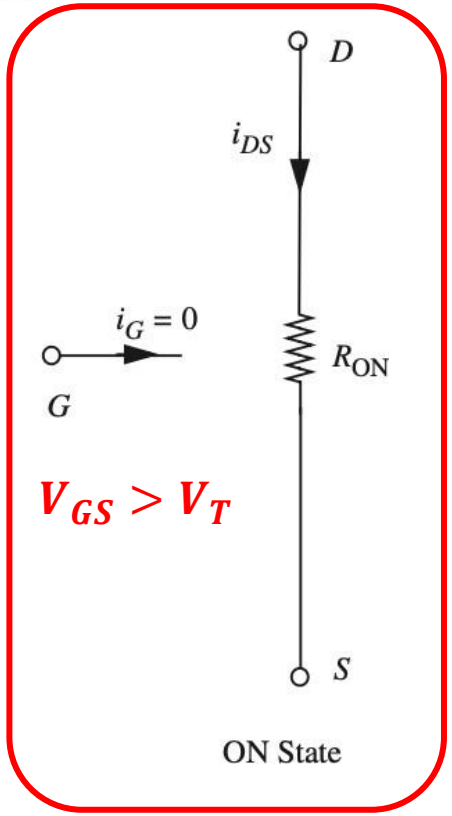


The created **channel** will have some R
-> SR model



Cut off mode

G – Gate: Trigger terminal
S – Source: Charge carrier reservoir
D – Drain: Charge carrier sink

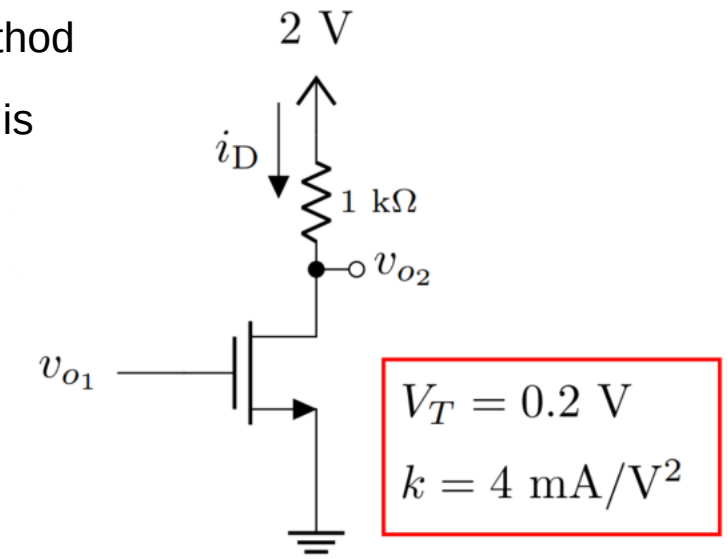


Small v_{DS}: Triode Mode
Large v_{DS}: Saturation Mode

Solving Circuits with MOSFET

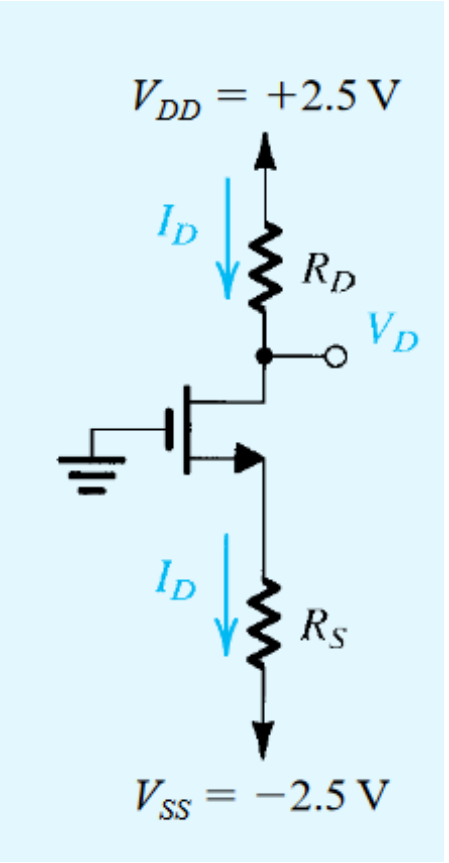
- Use **Method of Assumed State**!
- Three steps:
  - **Assume**: One of the modes (Cutoff, Triode, Saturation)
  - **Solve**: Use corresponding equation and KCL+KVL
  - **Verify**: Check if the conditions of V_{DS} and V_{GS} are satisfied. If not, repeat.
- Might need to solve quadratic equation $(ax^2 + bx + c = 0)$.
- If we get two roots, choose the one that's ***favorable*** to your assumption

Analyze the circuit to find $\boldsymbol{i_D}$ and $\boldsymbol{v_{O2}}$ using the Method of Assumed State. Here, the input of the MOSFET is $\boldsymbol{v_{o1} = 1\,V}$. You must validate your assumptions.



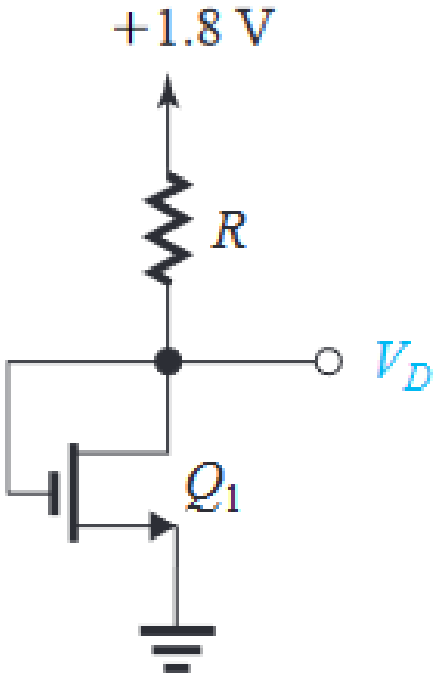
- Design the circuit, that is, determine the values of R_D and R, so that the transistor operates at $\boldsymbol{I_D} = 0.4\,\text{mA}$ and $\boldsymbol{V_D} = +0.5\,\text{V}$. The NMOS transistor has $\boldsymbol{V_T} = 0.7\,\text{V}$, $\boldsymbol{k} = 3.2\,\text{mA/V}^2$.

What is the mode of this transistor?

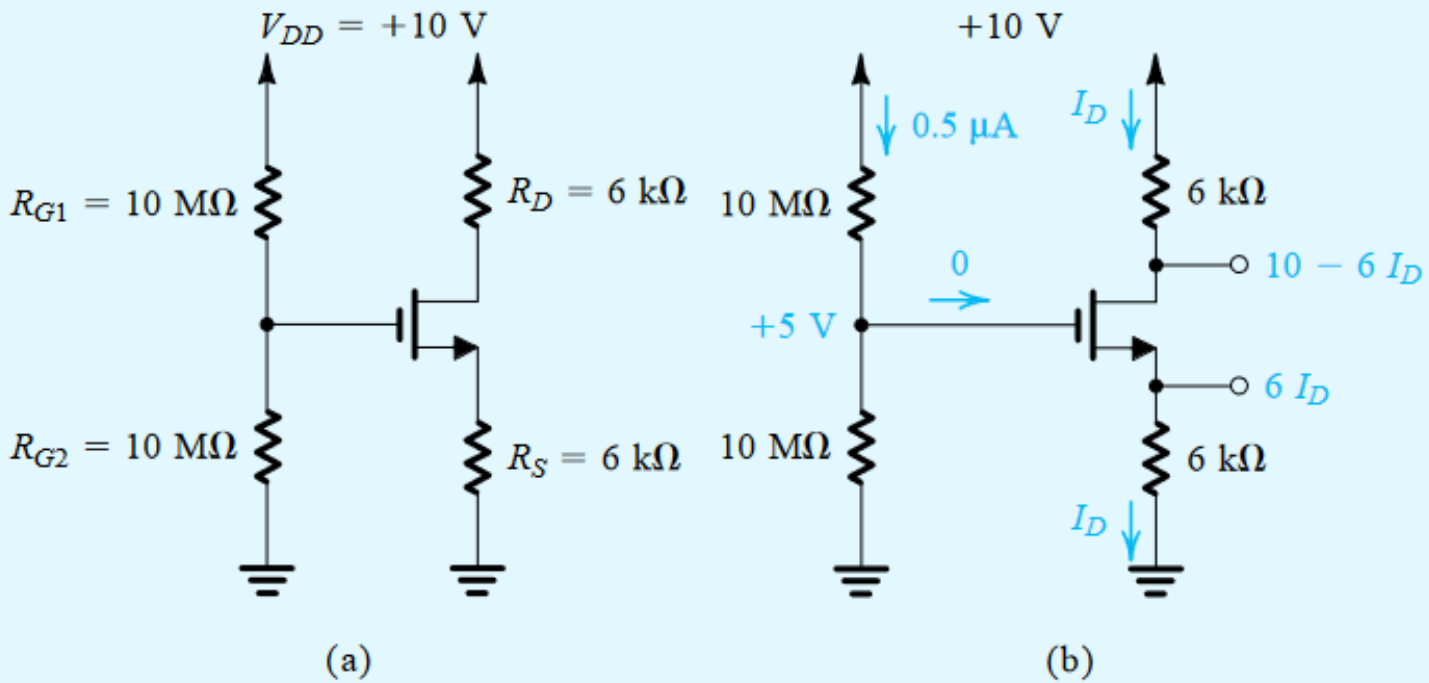


- For the circuit, find the value of R that results in $V_D = 0.8\ \text{V}$. The MOSFET has $V_T = 0.5\ \text{V}$, $k_n' = \mu_n C_{OX} = 0.4\ \text{mA/V}^2$, $\frac{W}{L} = \frac{0.72\ \mu\text{m}}{0.18\ \mu\text{m}}$

$$k_n = k_n' \frac{W}{L} = 1.6\ \text{mA/V}^2$$

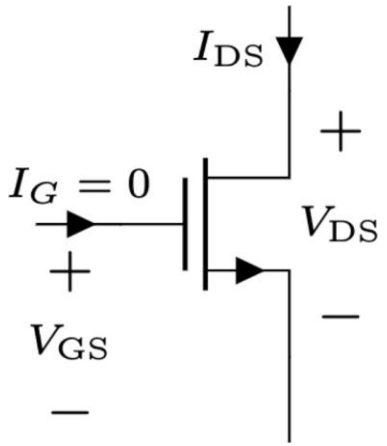


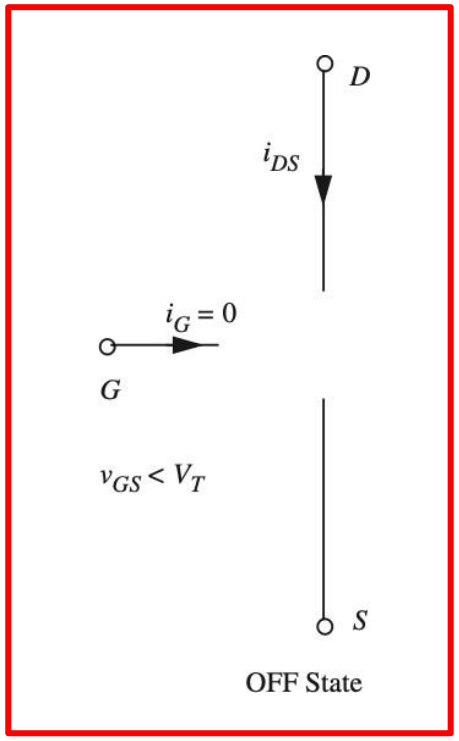
Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

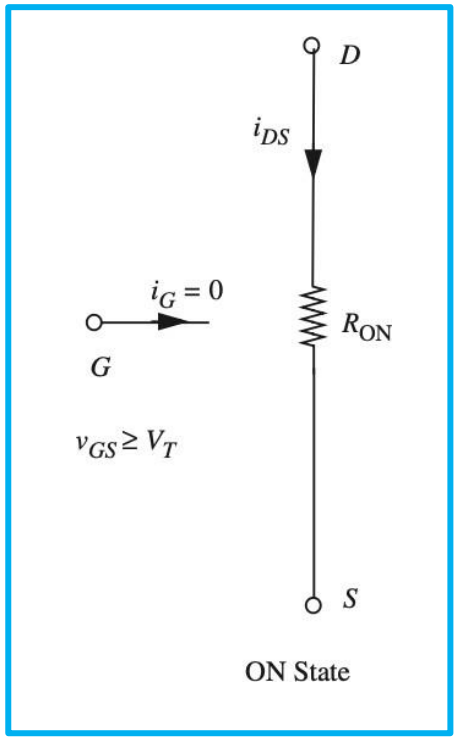


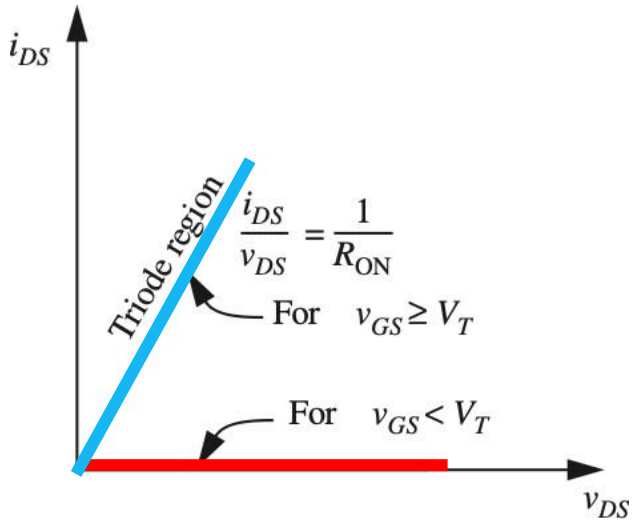
n-channel MOSFET - Summary

SR Model:









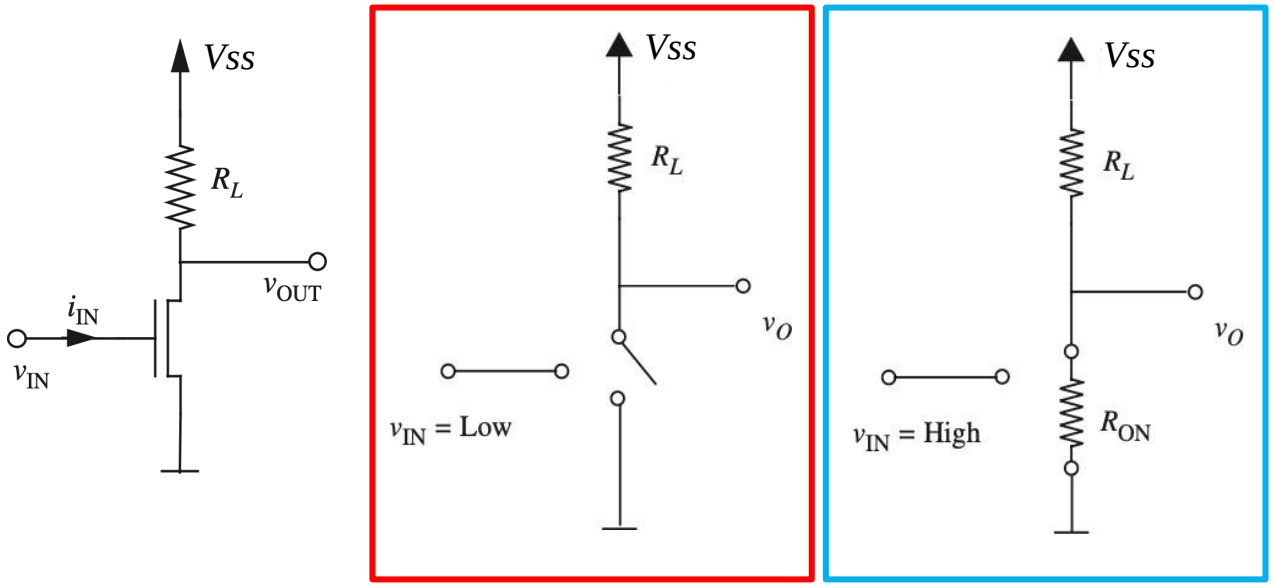
$$R_{ON} = \frac{1}{k_n(V_{OV} - \frac{1}{2}v_{DS})}$$

- SR model is a better approximation than S model.
- **Triode Mode exists until:** v_{DS} <=$(v_{GS} - V_T)$

V_{OV}

Indicates the available excess voltage at **gate** after forming the n-channel.

SR Model - Inverter



$v_{o,HI} = V_{SS}$

$v_{o,LO} = \frac{R_{ON}}{R_{ON} + R_L} V_{SS}$

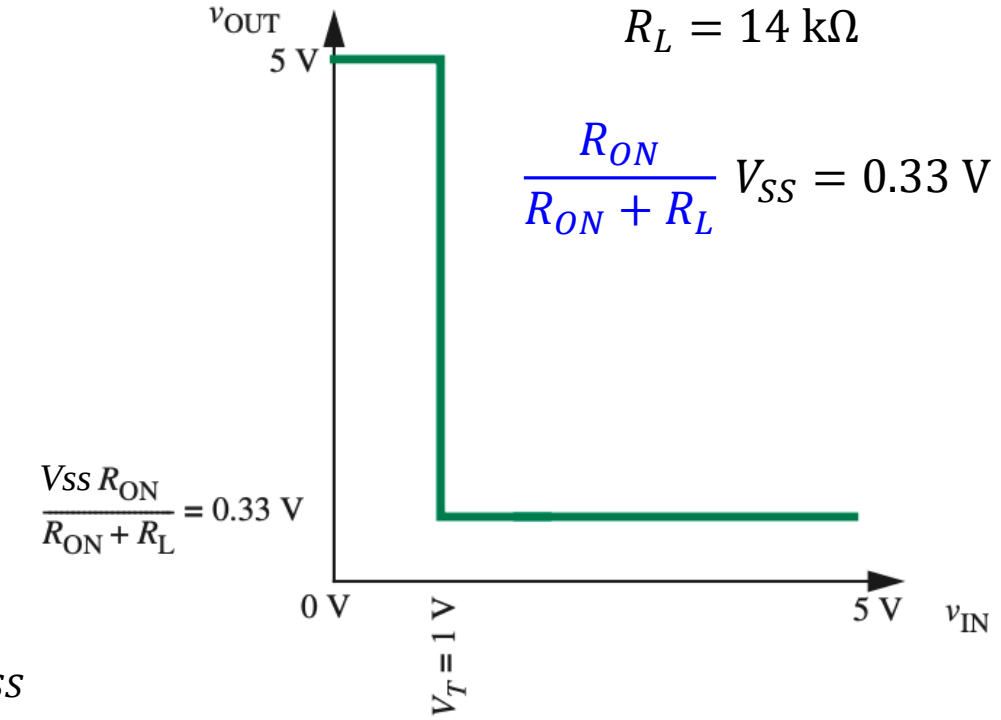
For example, If

$V_{SS} = 5$ V,

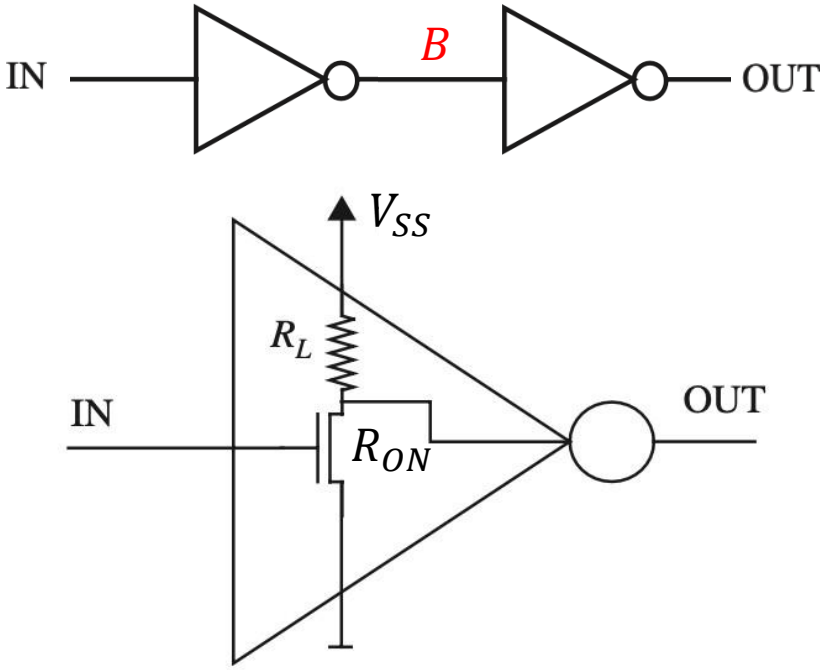
$R_{ON} = 1$ kΩ,

$R_L = 14$ kΩ

$\frac{R_{ON}}{R_{ON} + R_L} V_{SS} = 0.33$ V



Design of logic gates



Expected

IN	B	OUT
Low ($V_{IN} < V_T$)	High ($5V$)	Low ($V_{OUT} = V_{OUT,Low}$)
High ($V_{IN} > V_T$)	Low ($V_{OUT,Low}$)	High (5V)

Actual

IN	B	OUT
Low ($V_{IN} < V_T$)	High ($5V$)	Low ($V_{OUT} = V_{OUT,Low}$)
High ($V_{IN} > V_T$)	Low($V_{OUT,Low} = 0.5$ V $\not< V_T$)	Low($V_{OUT,Low} = 0.5\ V$)

$V_T = 0.4$ V

$V_{SS} = 5$ V, $R_{ON} = 1$ kΩ, $R_L = 9$kΩ

Therefore, need to design logic gates properly such that

$V_{OUT,HI} = V_{SS}$

$$V_{OUT,LOW} = \frac{R_{ON}}{R_{ON} + R_L} V_S = 5 \cdot \frac{1}{1+9} = 0.5 \text{ V} \not< V_T$$

$$\frac{R_{ON}}{R_{ON} + R_L} V_{SS} < V_T$$

Design of logic gates - Example

Assume the following values for the inverter circuit parameters: $V_{SS} = 5$ V, $V_T = 1$ V, and $R_L = 10$ kΩ. Assume, further, that $\frac{1}{k_n' V_{OV}} = \mathbf{5}$ for the MOSFET. Determine a $(\frac{W}{L})$ sizing for the MOSFET so that the inverter gate output for a logical 0 is able to switch OFF the MOSFET of another inverter.

Solution:

[Assume $R_{ON} = \frac{1}{k_n V_{OV}}$ if v_{DS} is not given or low]

$$V_{SS} \cdot \frac{R_{ON}}{R_{ON} + R_L} < V_T$$

$$\Rightarrow 5 \frac{R_{ON}}{R_{ON} + R_L} < 1$$

$$\Rightarrow 5R_{ON} < R_{ON} + 10$$

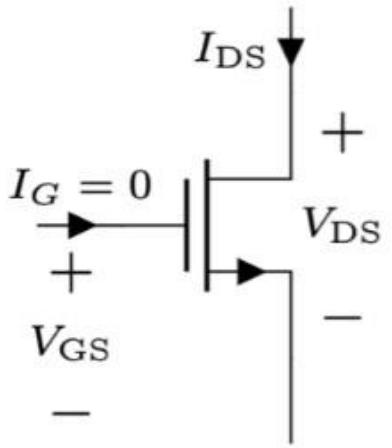
$$\Rightarrow R_{ON} < \frac{10}{4} \text{ kΩ} = 2.5 \text{ kΩ}$$

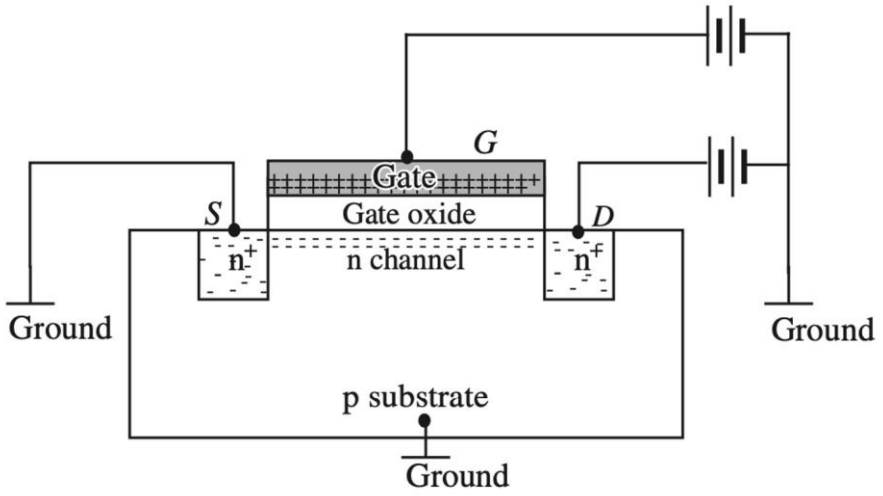
Now, $$R_{ON} = \frac{1}{k_n V_{OV}} = \frac{1}{k_n' \frac{W}{L} V_{OV}} = \frac{1}{5} \times \frac{1}{W/L}$$

Hence $$\frac{5}{W/L} < 2.5$$

$$\Rightarrow \frac{W}{L} > \frac{5}{2.5} = 2$$

Review – MOSFET





Control = $V_{GS} = V_G - V_S$ controls the IV between drain-source (I_{DS} vs V_{DS})

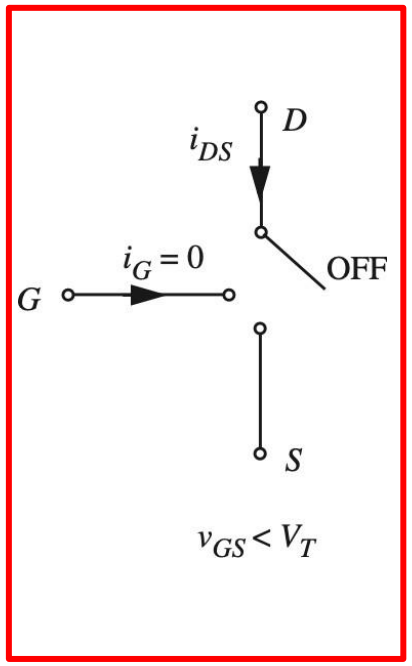
Threshold voltage = V_T, minimum voltage required to create the channel

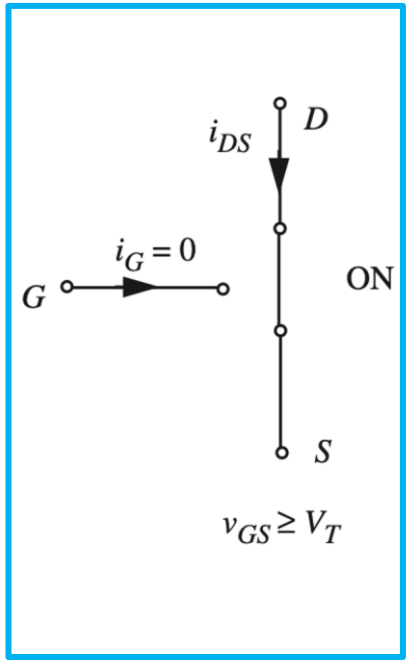
Models

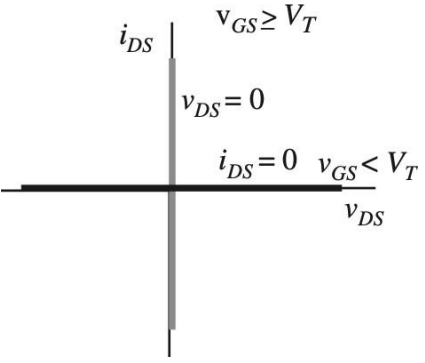
1. **S Mode**: Assumes an ideal channel with zero resistance
2. **SR Model**: Assumes finite channel resistance, R_{ON}, depends on $V_{GS} - V_T = V_{OV}$

MOSFET Linear Models

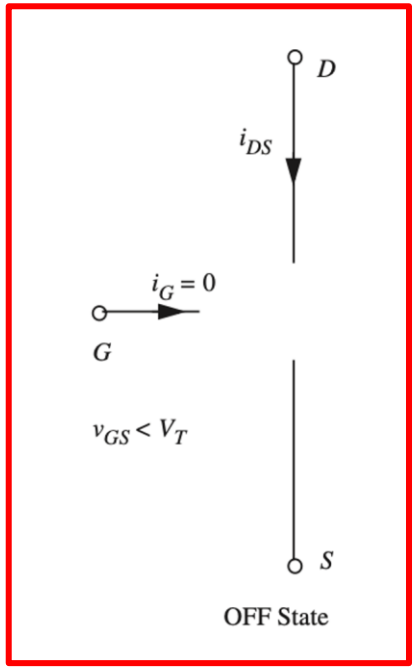
S Model

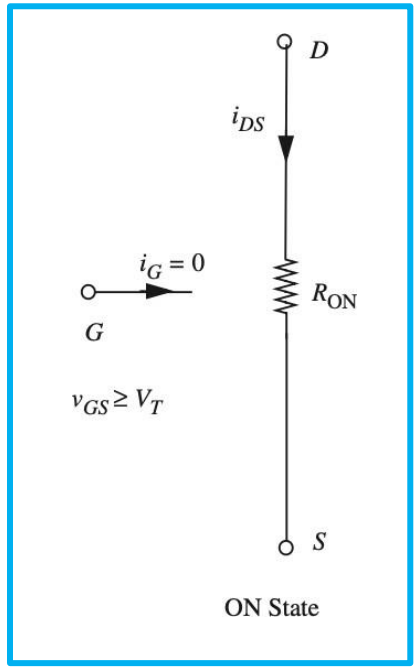


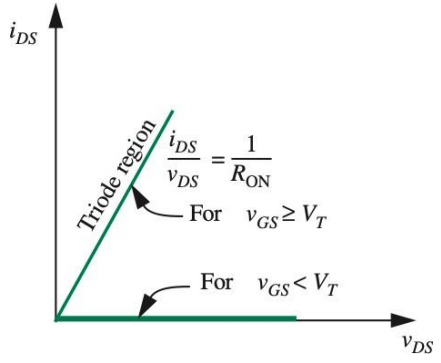




SR Model



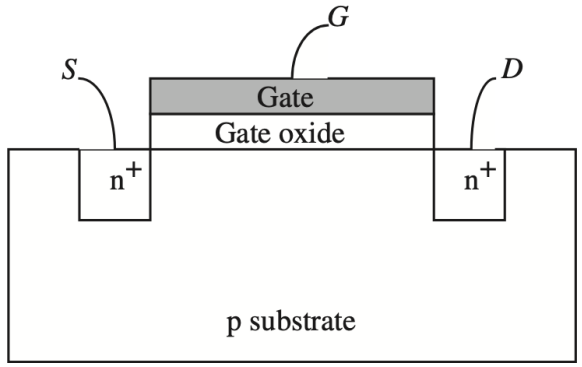


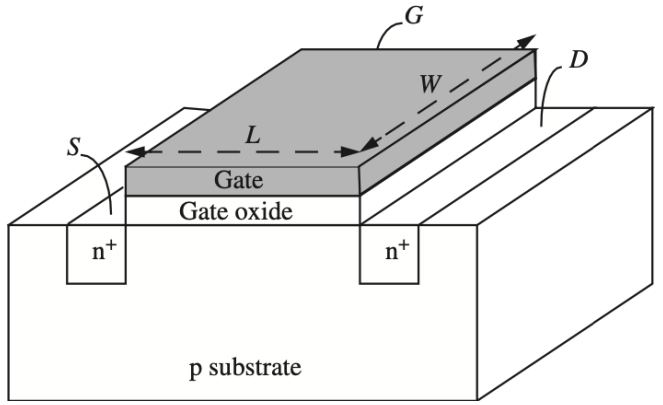


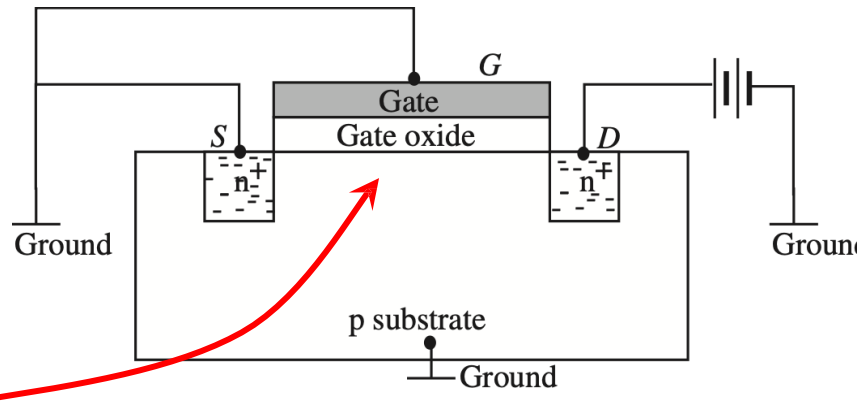
$$R_{ON} = \frac{1}{k_n' \frac{W}{L}(v_{GS} - V_T - \frac{1}{2}v_{DS})}$$

Construction of Real MOSFET

Simplified cross section and 3D view

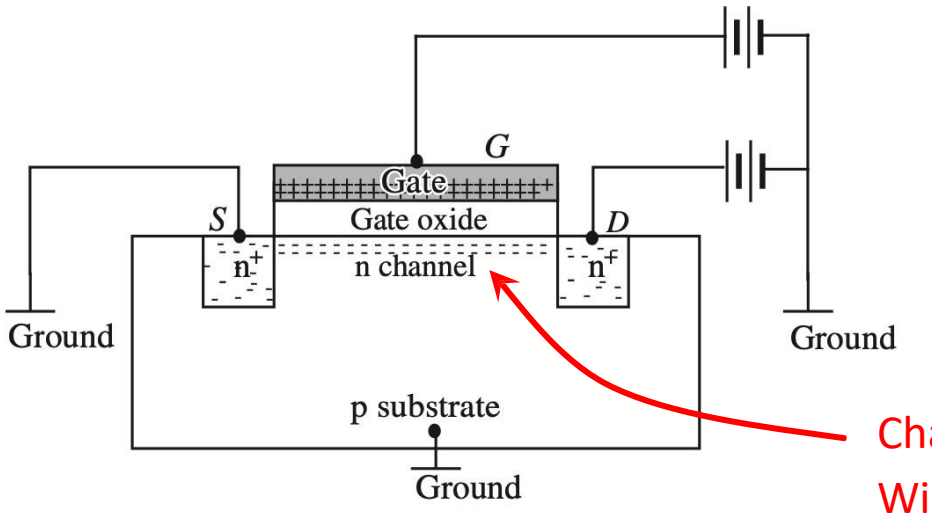






No channel, open ckt

$V_{12} = 0V$



$V_{12} > V_{\$}$

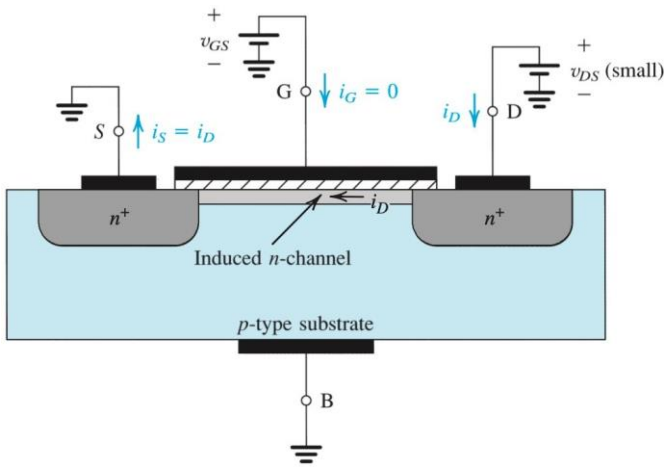
Channel created

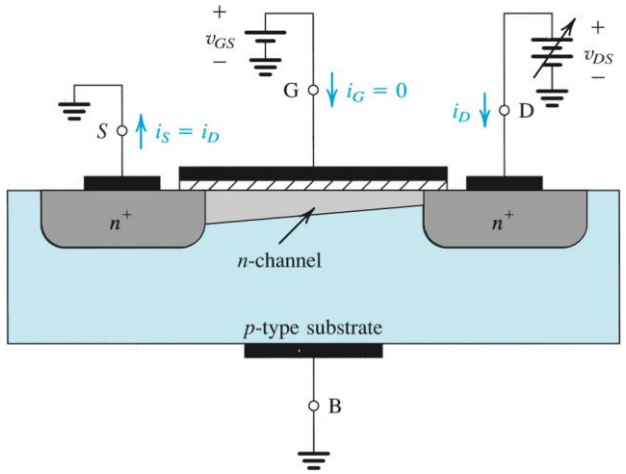
Will have some R

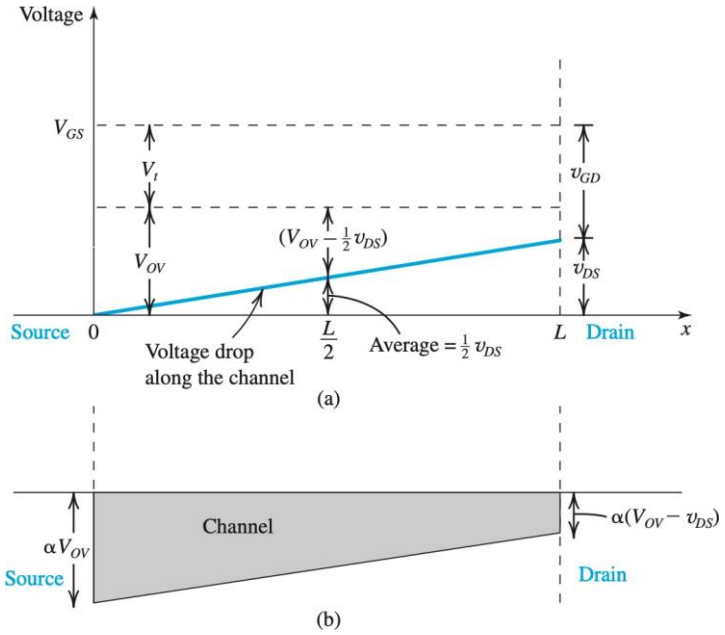
-> SR model

Real MOSFET

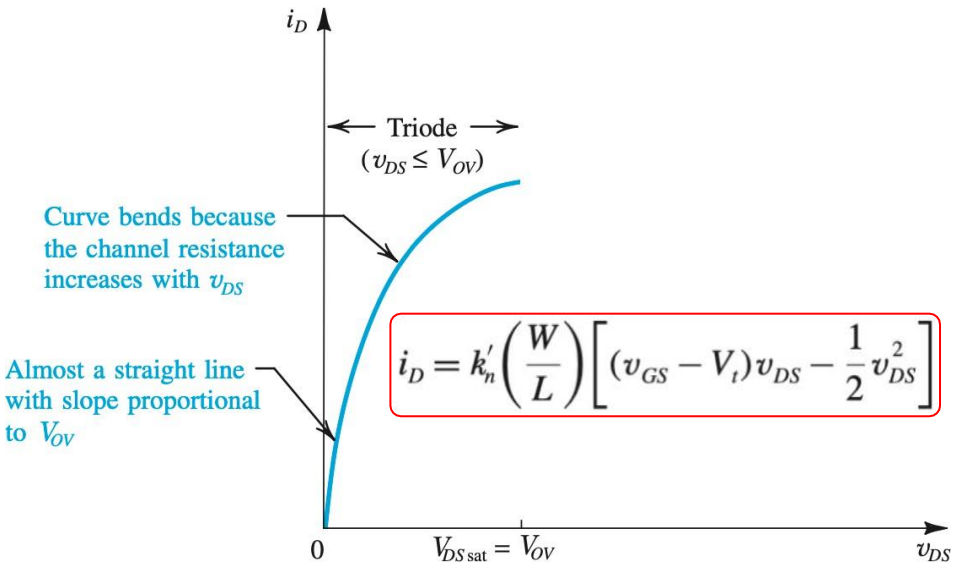
- For small V_{DS}, uniform channel, hence fixed R_{ON} therefore SR model valid.
- As V_{DS} is increased, channel becomes tapered cause $V_{GD}\downarrow$. Resistance ↑, slope ↓.
- This mode is called the **triode mode**. Condition: $V_{DS} < V_{OV}$

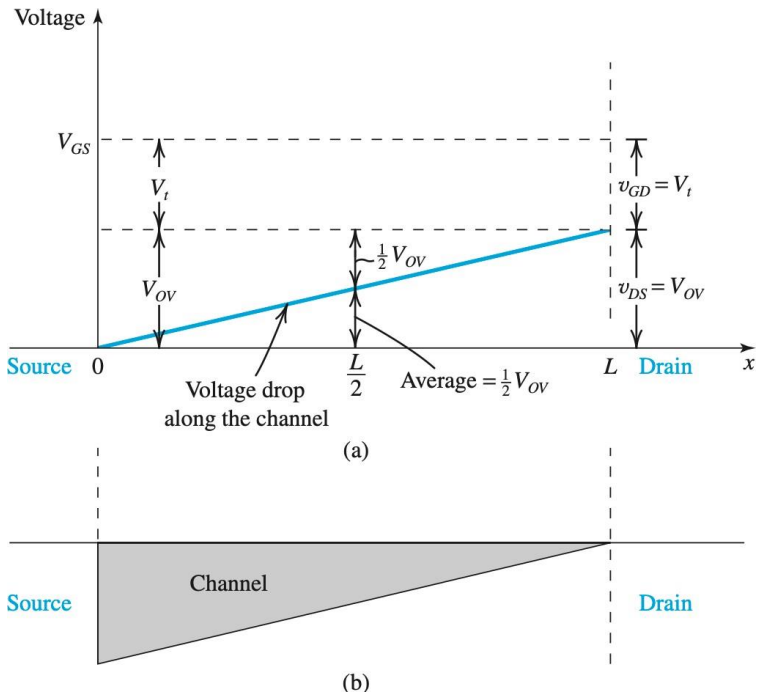


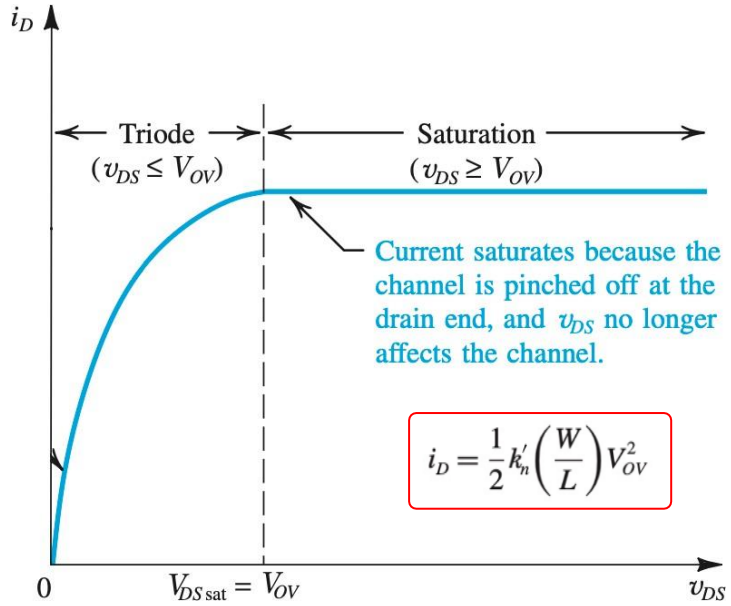




Real MOSFET

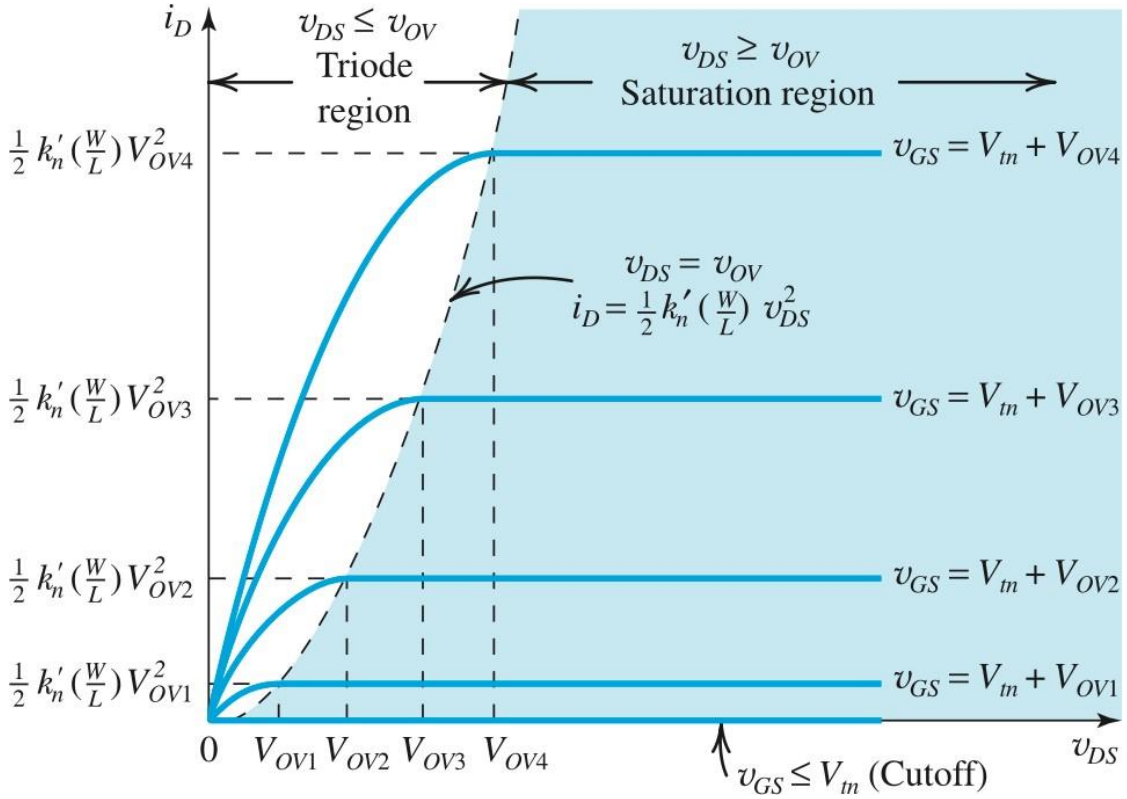






- When $V_{DS} = V_{OV}$, channel pinches off.
- Increasing V_{DS} further have no effect on channel shape. Hence, current saturates
- This mode is called the **saturation mode**. Condition: $V_{DS} \geq V_{OV}$
- Behaves like a **current source** (constant current) that depends on V_{OV}'

IV Characteristics of Real MOSFET



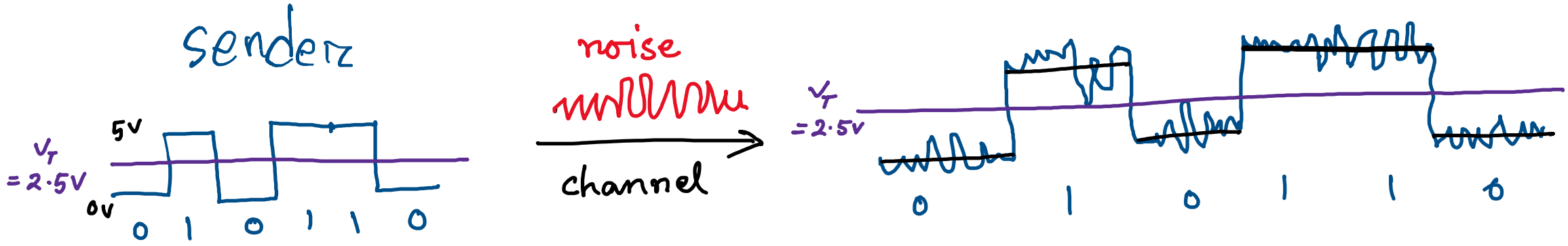
Mode	Condition	Equation
Cutoff	$V_{GS} < V_T$	$I_D = 0$
Triode	$V_{GS} \ge V_T$ $V_{DS} < V_{OV}$	$I_D = k[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2]$
Saturation	$V_{GS} \ge V_T$ $V_{DS} \ge V_{OV}$	$I_D = \frac{k}{2}V_{OV}^2$

$$V_{GS} - V_T = V_{OV}$$

$$k_n = \frac{k_n' W}{L}$$

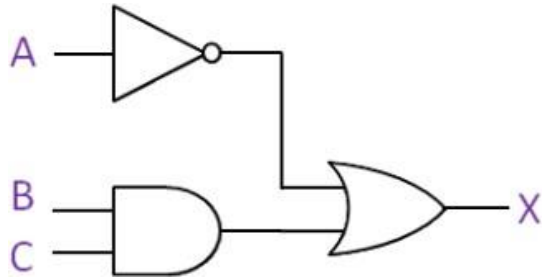
Digital Representation

Suppose you want to send 010110



- Single value based representaion fails in the presence of noise
- Better approach – threshold-based system
- Simplest: Logical 0 = $V < V_T$ Logical 1 = $V > V_T$

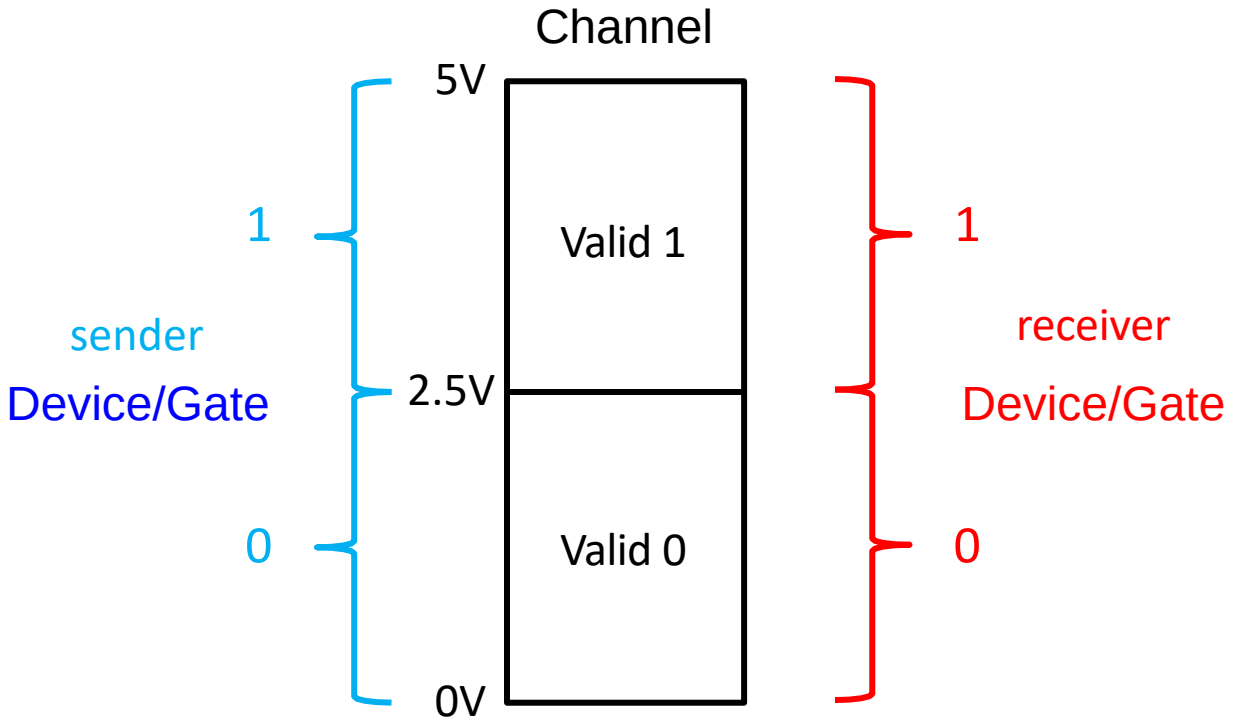
Static Discipline



- Specification for “all” digital devices
- Requires devices to adhere to common representation to ensure that **valid input produces valid output**
- This means, if
  - Sender sends “0” → (noise) Channel → Receiver interprets as “0”
  - Sender sends ”1” → (noise) Channel → Receiver interprets as “1”

Static Discipline

Naïve approach: Single threshold-based system



$V_T = 2.5\ V$

sender

Logical 0: $V_o < V_T$
Logical 1: $V_o > V_T$

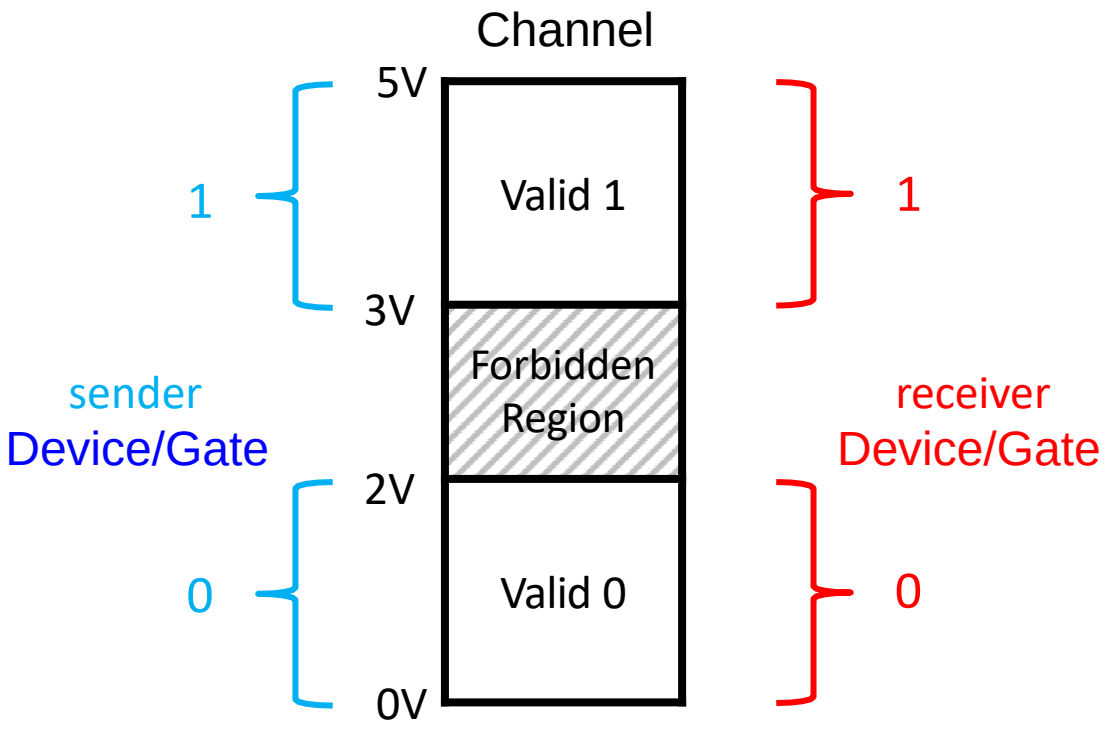
receiver

Logical 0: $V_i < V_T$
Logical 1: $V_i > V_T$

What if $V_i = 2.5$ V? It is **undefined**!

Static Discipline

Double threshold based system



V_H= High voltage threshold = $3V$

V_L= High voltage threshold = $2\ V$

sender

Logical 0: $V_o < V_L$

Logical 1: $V_o > V_H$

receiver

Logical 0: $V_i < V_L$

Logical 1: $V_i > V_H$

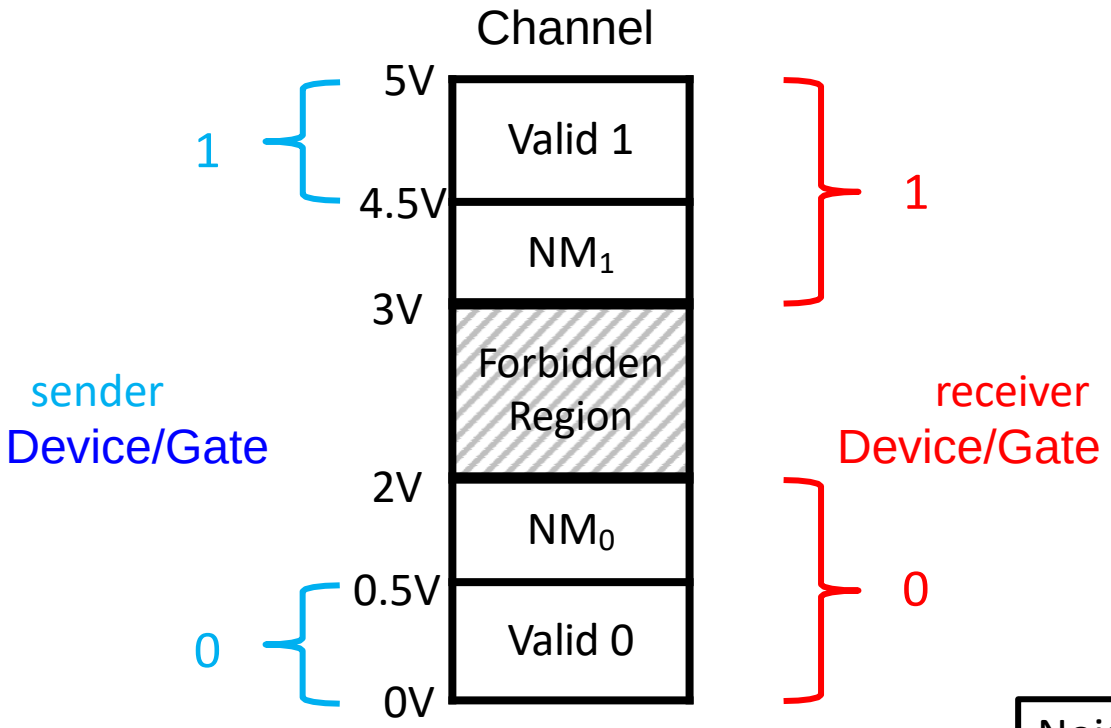
What if $V_o = 1.9V$ and channel noise is $0.5V$?

$V_i = 1.9V + 0.5V = 2.4V$ = invalid

➔ valid output producing invalid input, i.e., no margin for noise

Static Discipline

Four threshold-based system → Tighter restriction on sender (**output**)



V_{OH}= Output high voltage threshold = $4.5V$
V_{OL} =Output low voltage threshold = $0.5V$
V_{IH} =Input high voltage threshold = $3V$
V_{IL} =Input low voltage threshold = $2V$

sender

Logical 0: $V_o < V_{OL}$
Logical 1: $V_o > V_{OH}$

receiver

Logical 0: $V_i < V_{IL}$
Logical 1: $V_i > V_{IH}$

For static discipline, $V_{OL} < V_{IL} < V_{IH} < V_{OH}$

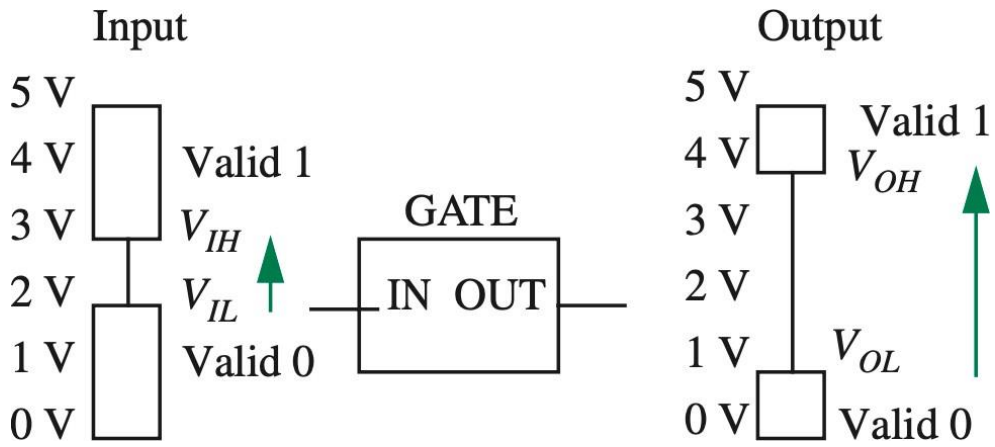
Noise margins (NM):

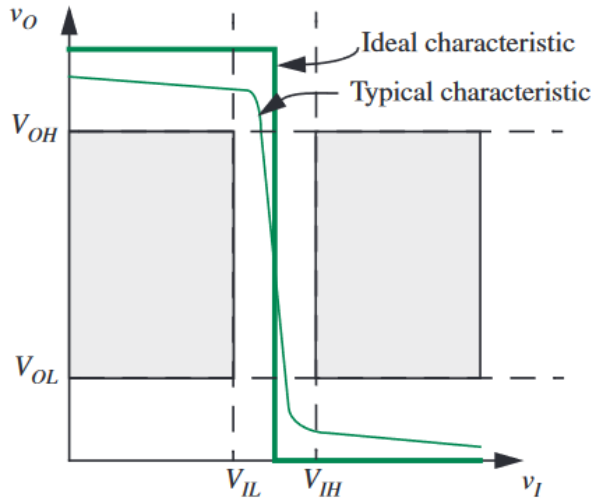
- $NM_1 = V_{OH} - V_{IH} = 4.5 - 3 = 1.5$ V (significance?)
- $NM_0 = V_{IL} - V_{OL} = 2 - 0.5 = 1.5$ V (significance?)

Static Discipline

Four threshold-based system → Tighter restriction on sender (**output**)

V_{OH}: The lowest output voltage value that a digital device **can produce** when it outputs a logical **1**.
V_{OL}: The highest output voltage value that a digital device **can produce** when it outputs a logical **0**.

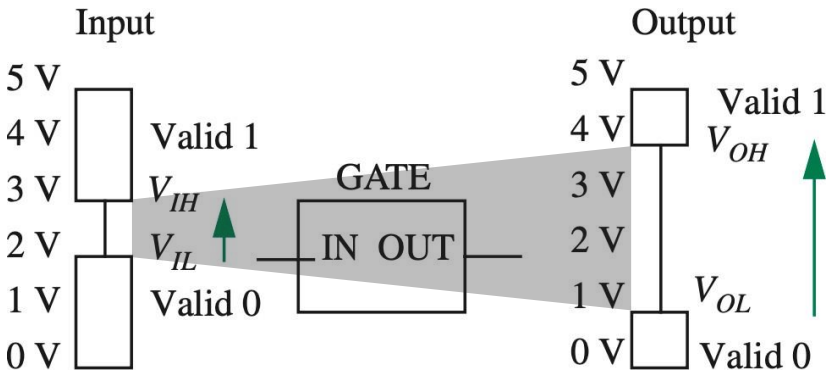




V_{IH}: The *lowest input voltage* value that a digital device **must recognize** as a logical **1**.
V_{IL}: The *highest input voltage* value that a digital device **must recognize** as a logical **0**.

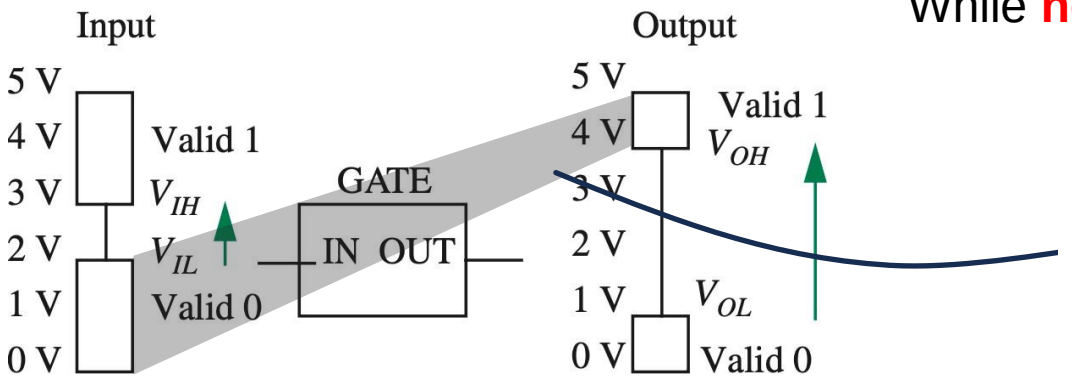
Static Discipline and VTC graph

Four threshold-based system → Tighter restriction on sender (**output**)



During high to low or low to high **transition**:

Higher Slope in VTC graph



While **not** in **transition**; at logical **HIGH** or **LOW** voltage level:

Smaller Slope in VTC graph

Static Discipline and VTC graph

During high to low or low to high **transition**:

Slope > 1

While **not** in **transition**; at logical **HIGH** or **LOW** voltage level:

Slope < 1

Slope < 1