CSE251: Electronic Devices and Circuits

Lecture: 14 - 16 – MOSFET

Prepared By:

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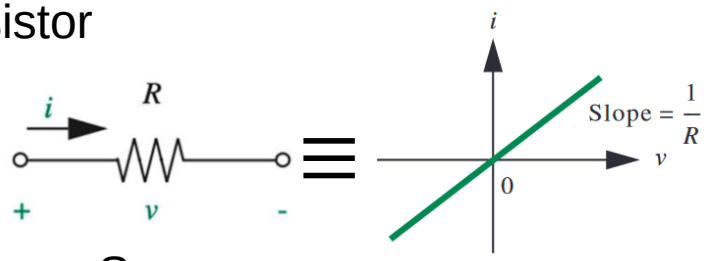
Outline

- Introduction to Electronic Switches
- Logic Functions using Switches
- Introduction to a voltage-controlled switch - MOSFET
- Designing Logic gates with MOSFETs
- VTC – Voltage Transfer Characteristics

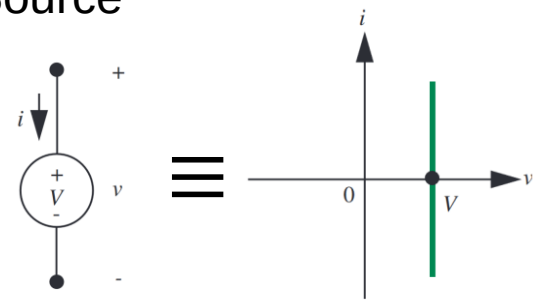
Two terminal Devices

Linear Devices

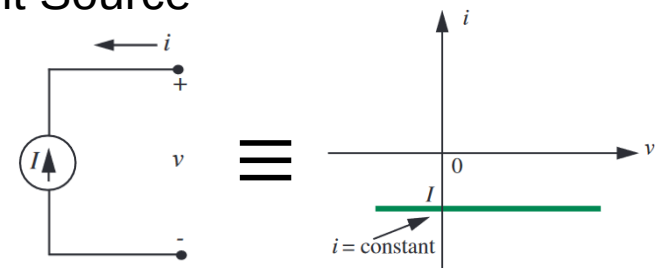
Resistor



Voltage Source



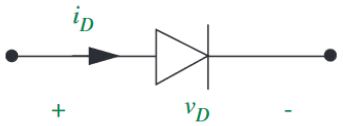
Current Source



IV characteristics of two terminal devices are fixed.

Non-linear Devices

Diode



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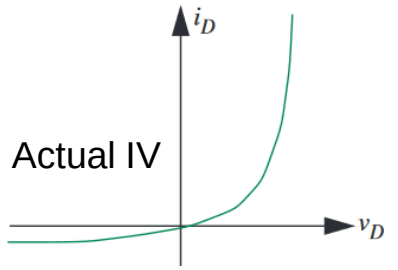
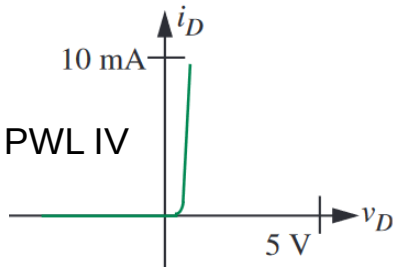


PWL: Piecewise Linear



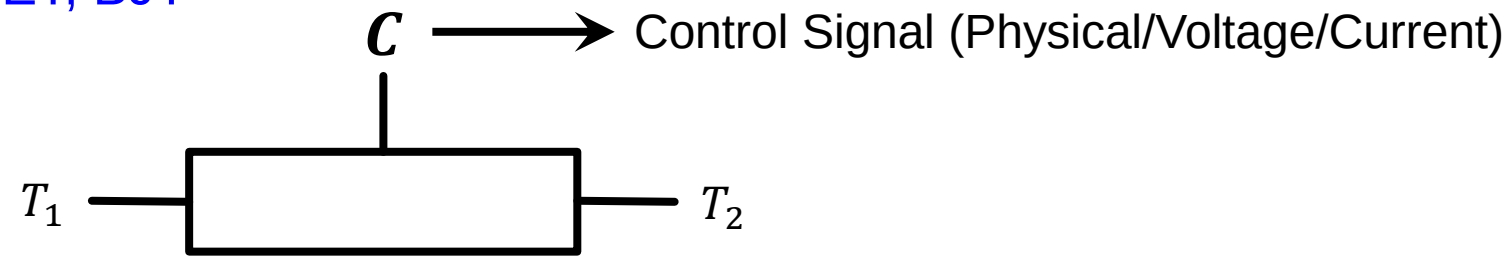
IV characteristics of **three terminal devices** can be changed

Three terminal Devices

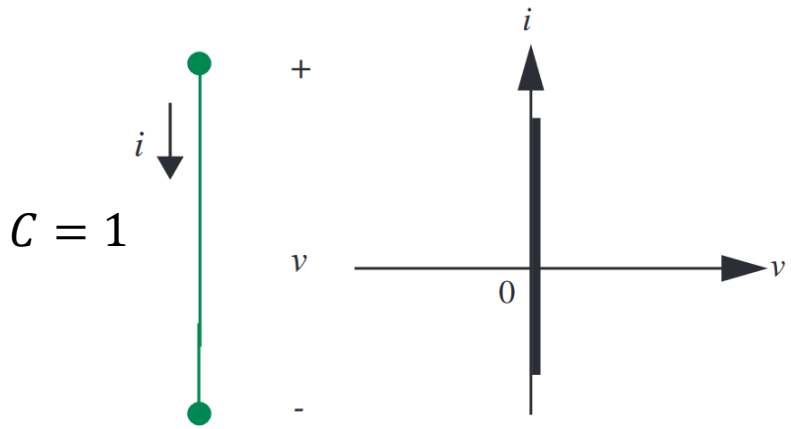
IV of two terminal can be controlled using a third terminal.

Example: Switch, MOSFET, BJT

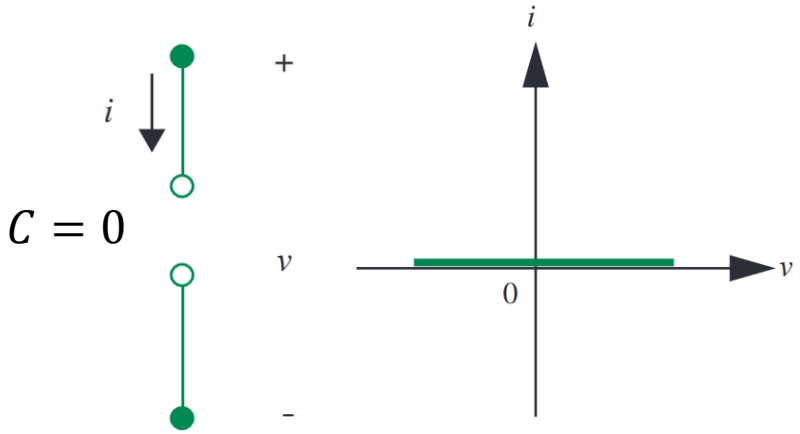
Switch



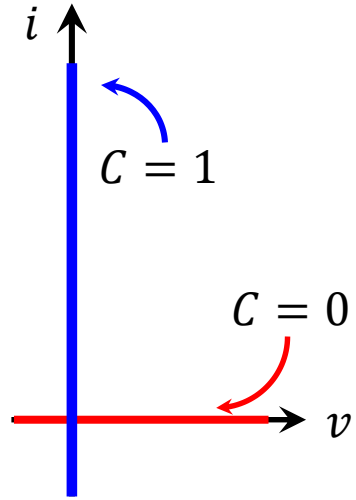
IV characteristics between T_1 and T_2 can be controlled by C



Switch **ON**

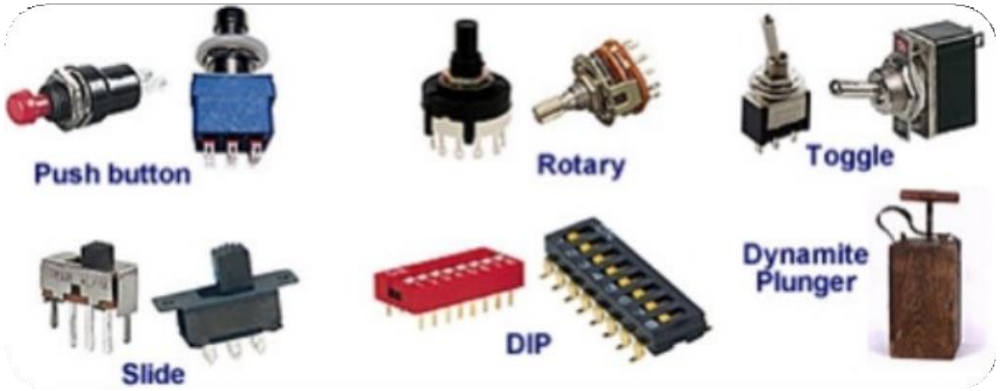


Switch **OFF**

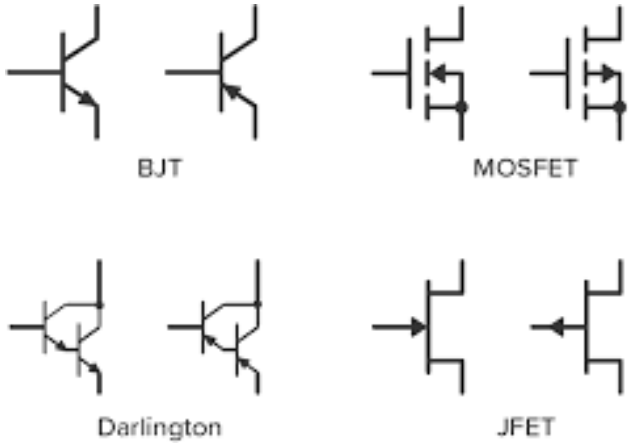


Switch – Types

- Depending on the control, the switch can be
  - **Analog**: Controlled using physical toggle/button
  - **Digital**: Controlled using voltage or current. Example – MOSFET (voltage controlled), BJT (current controlled)



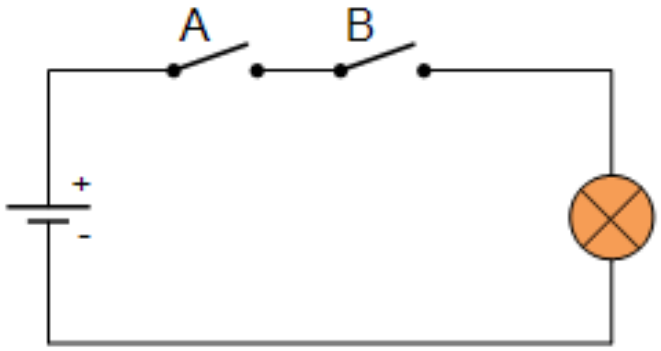
Analog switches



Digital switches (Transistors)

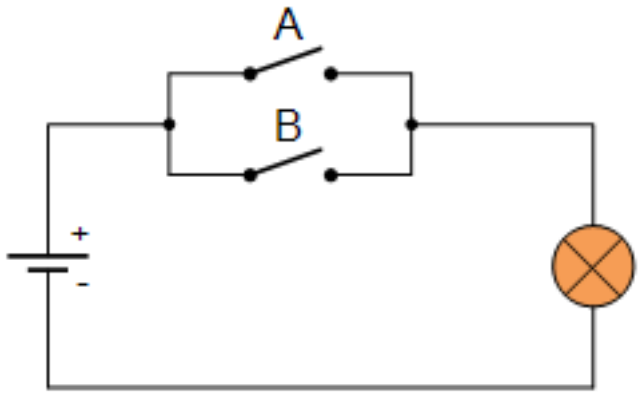
Switch Application – Logic Gates

- We can use switches to build logic gates



A	B	Bulb
0	0	OFF
0	1	OFF
1	0	OFF
1	1	ON

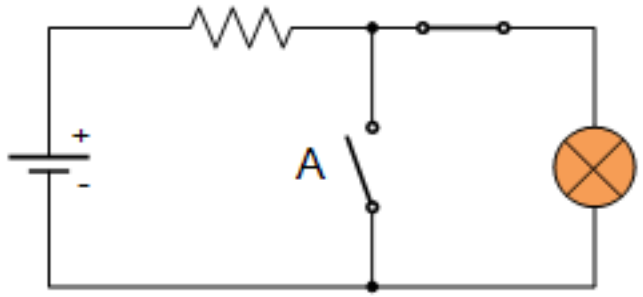
AND operation



A	B	Bulb
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

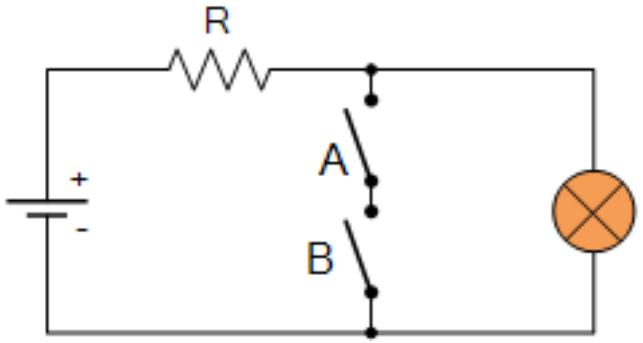
OR operation

Switch Application – Logic Gates



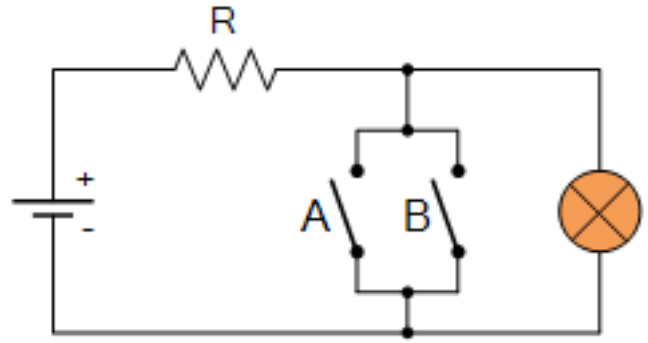
A	Bulb
0	ON
1	OFF

NOT operation



A	B	Bulb
0	0	ON
0	1	ON
1	0	ON
1	1	OFF

NAND operation



A	B	Bulb
0	0	ON
0	1	OFF
1	0	OFF
1	1	OFF

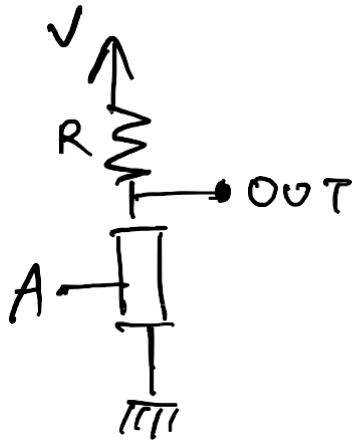
NOR operation

These circuits are “preferred” – because they can be cascaded to build combinational logic circuits

-> if we remove the bulb and use the voltage across instead to cascade and drive the next gate

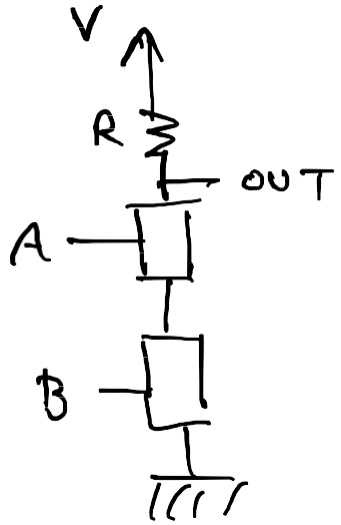
Switch Application – Logic Gates

Alternative representations:



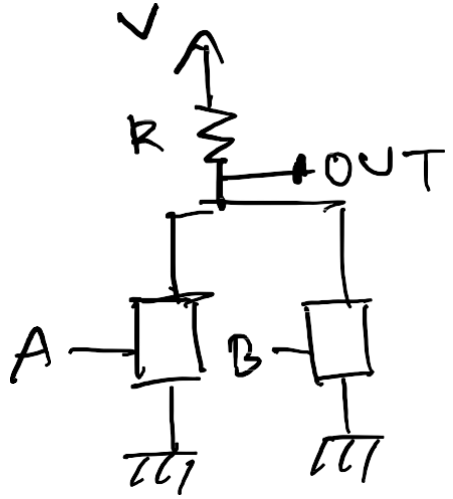
$OUT = \overline{A}$

(NOT)



$OUT = \overline{AB}$

(NAND)

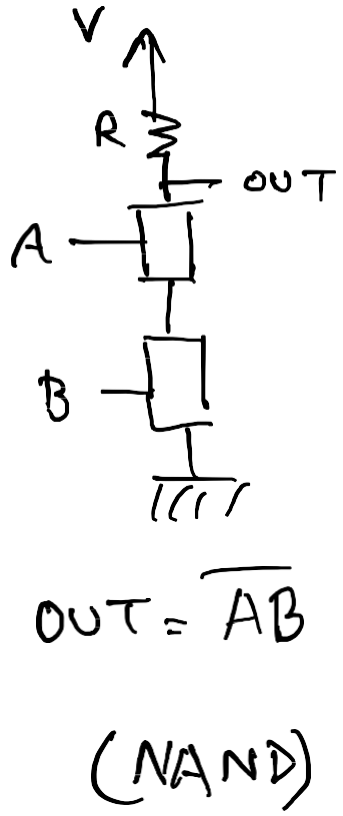


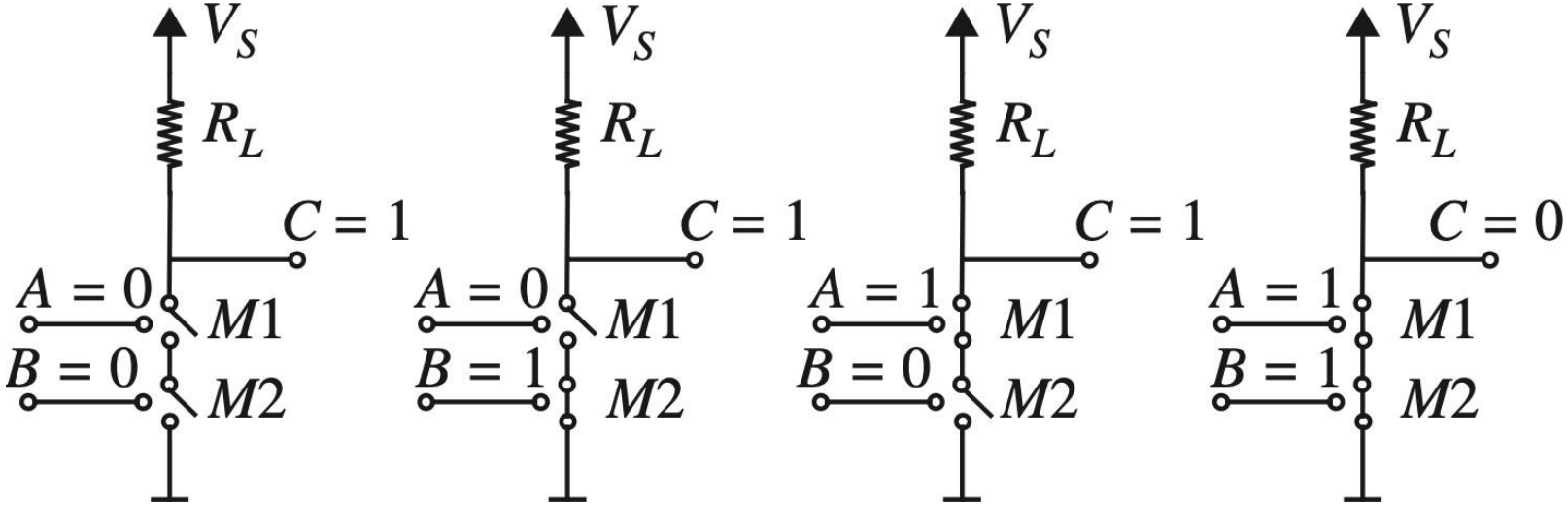
$OUT = \overline{A+B}$

(NOR)

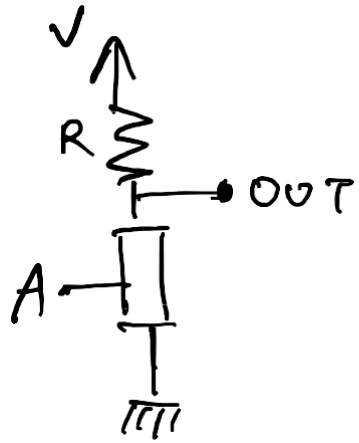
Switch Application – Logic Gates

Alternative representations:



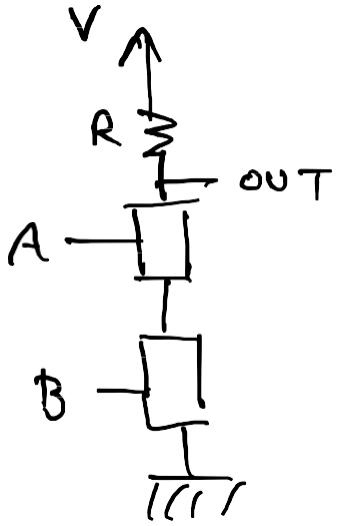


Switch Application – Logic Gates



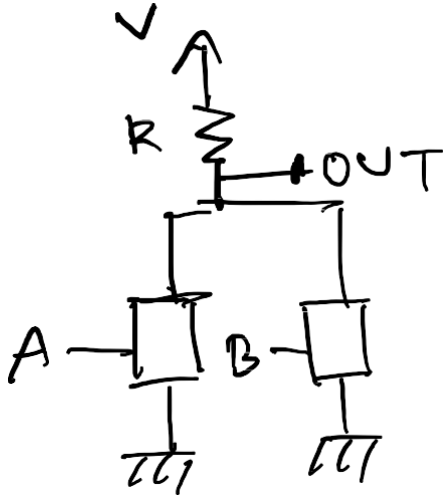
$OUT = \overline{A}$

A	V_{OUT}
0	5V
1	0V



$OUT = \overline{AB}$

A	B	V_{OUT}
0	0	5V
0	1	5V
1	0	5V
1	1	0V

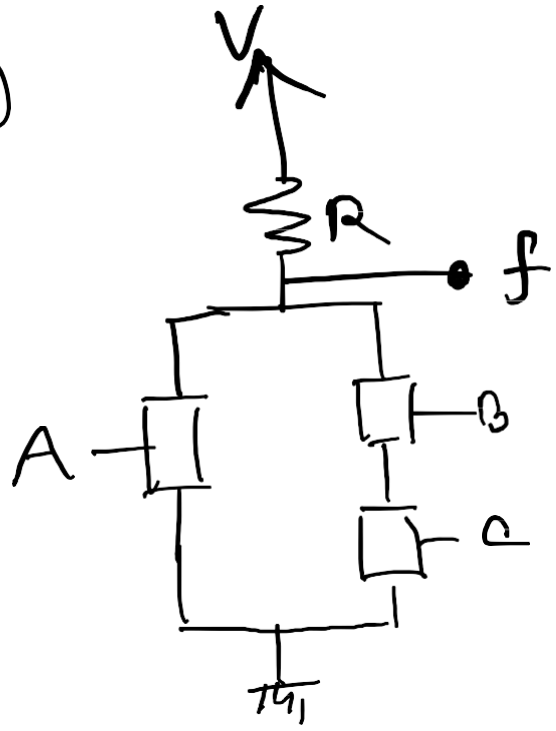


$OUT = \overline{A+B}$

A	B	V_{OUT}
0	0	5V
0	1	0V
1	0	0V
1	1	0V

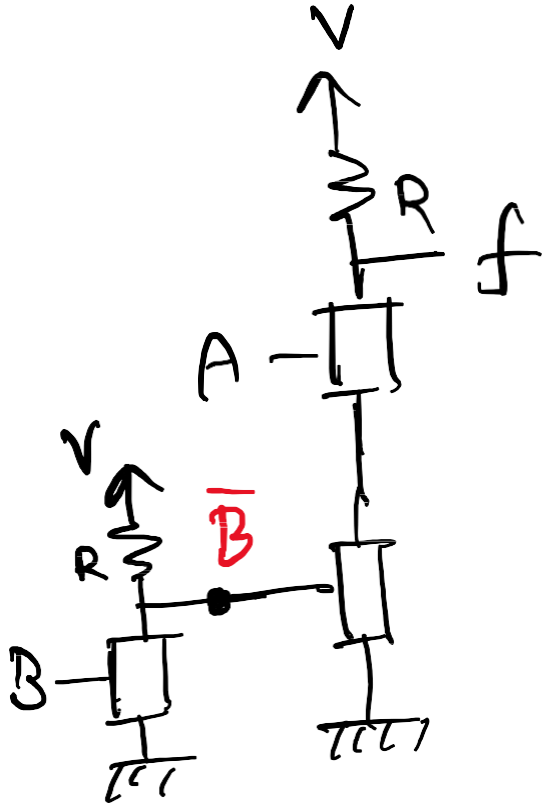
Examples

1



$$f = \overline{A + B.C}$$

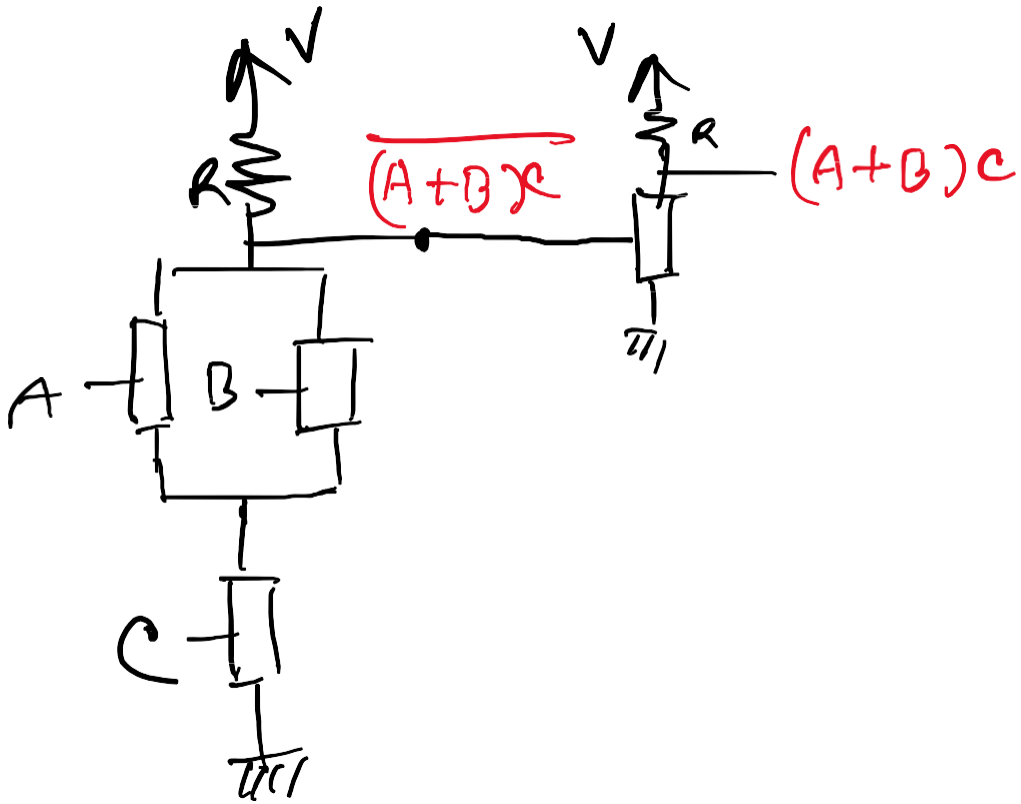
2



$$f = \overline{A\overline{B}}$$

Example

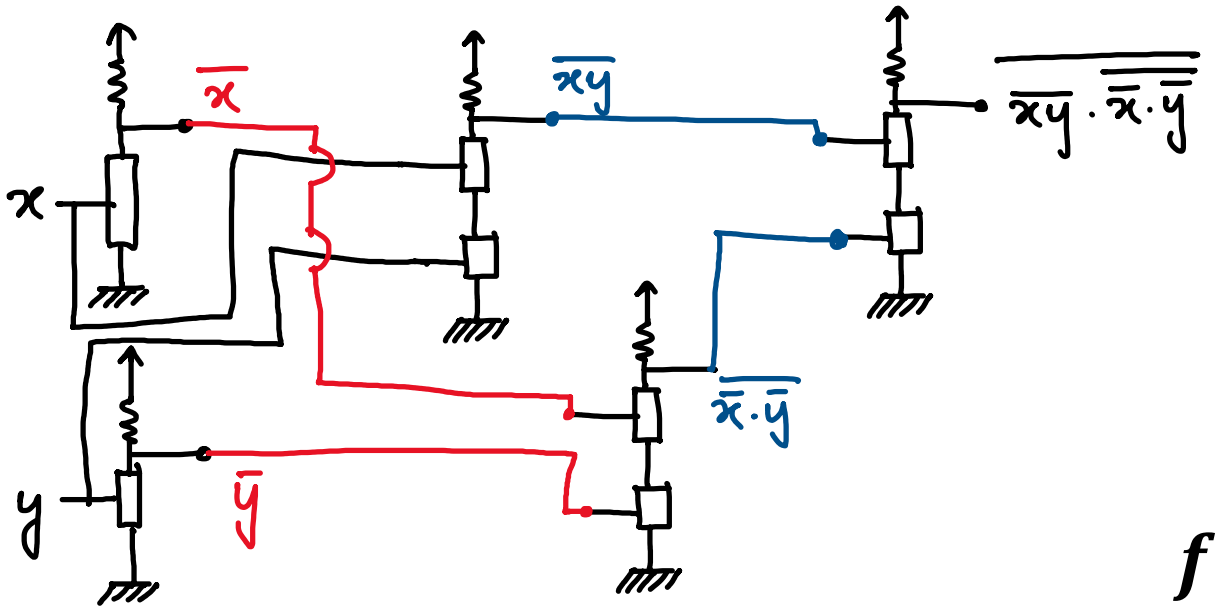
Implement using switches: $f = (A + B)C$



Practice Problem 1

In digital systems, binary data may be subjected to noise that can alter a 0 to a 1 or a 1 to a 0.

A simple way to check if any error has occurred is to use an **even parity checker**. If there are two input bits x and y, the output of the even parity checker (denoted as f) will be **HIGH** if there are even number of 1s, i.e., if both x and y are 0 or if both of them are 1.



x	y	f
0	0	
0	1	
1	0	
1	1	

$$f = x \cdot y + \overline{x} \cdot \overline{y} = \overline{\overline{x \cdot y + \overline{x} \cdot \overline{y}}}$$
$$= \overline{\overline{x.y} \cdot \overline{\overline{x} \cdot \overline{y}}}$$

Digital Representation

- Binary → Two states (0/False, 1/True)
- Binary variables in circuit, need to use two states of device/parameters

Voltage

5V → 1
0V → 0

0V → 1
3.3V → 0

Current

2mA → 1
3mA → 0

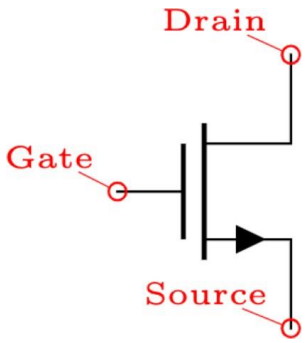
State

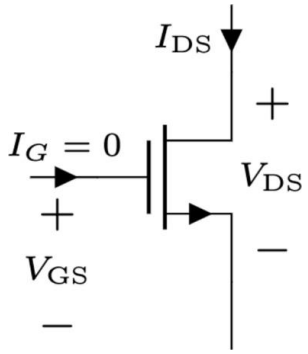
Diode
ON → 1
OFF → 0

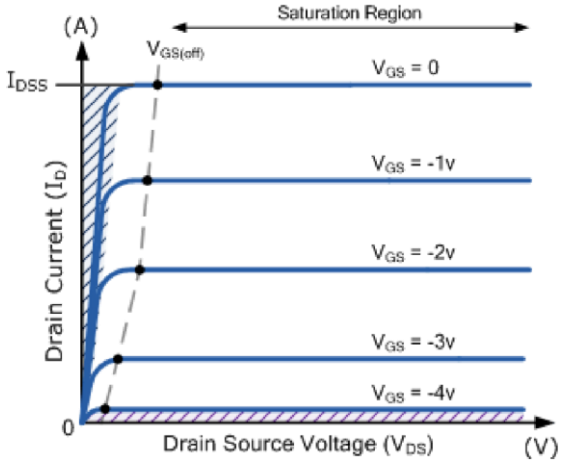
Memristor
Low resistance
High resistance

Transistors as Digital Switch

- Transistors are 3 terminal non-linear devices, can be used as switch
- 2 types – **Voltage Controlled**, **Current Controlled**
- **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor (**MOSFET**) are voltage controlled
- Control, $C = V_{GS}$. The IV characteristics (I_{DS} vs V_{DS}) depends on V_{GS}
- Actual dependency is complex.
- Will start with a simple (but approximate) one – **S-Model** (Switch Model)

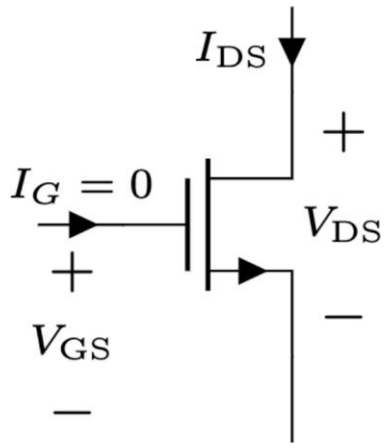


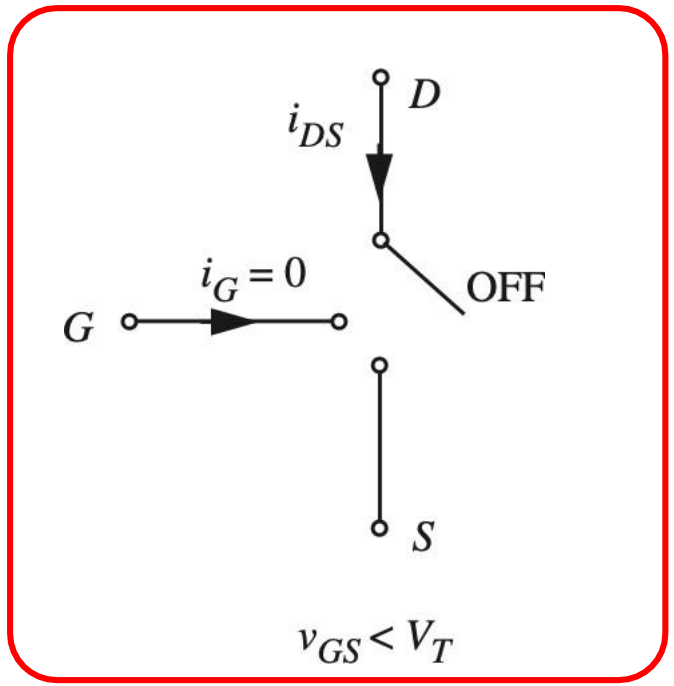


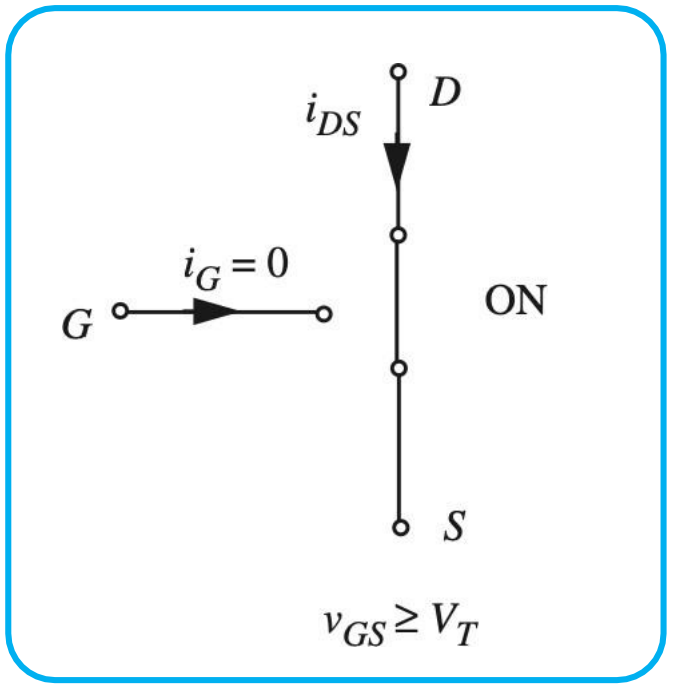


MOSFET S-Model

- The MOSFET (approximately) behaves like a switch
- C = V_{GS}. Here, $C = \text{“0”} \Rightarrow \boldsymbol{V_{GS} < V_T}$, and $C = \text{“1”} \Rightarrow \boldsymbol{V_{GS} < V_T}$







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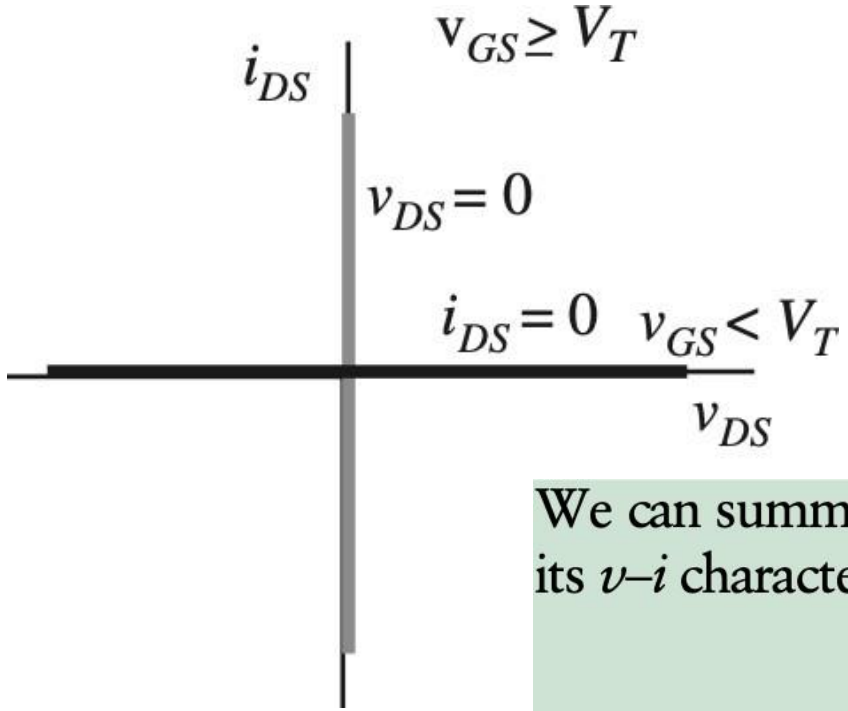


We can summarize the S model for the MOSFET in algebraic form by stating its v–i characteristics as follows:

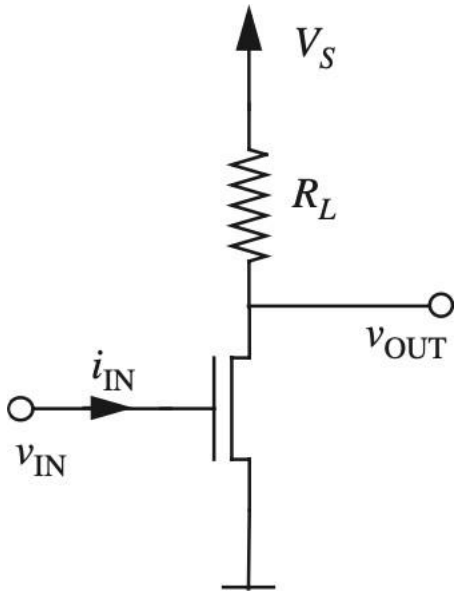
$$\text{for } v_{GS} < V_T, \quad i_{DS} = 0$$

and

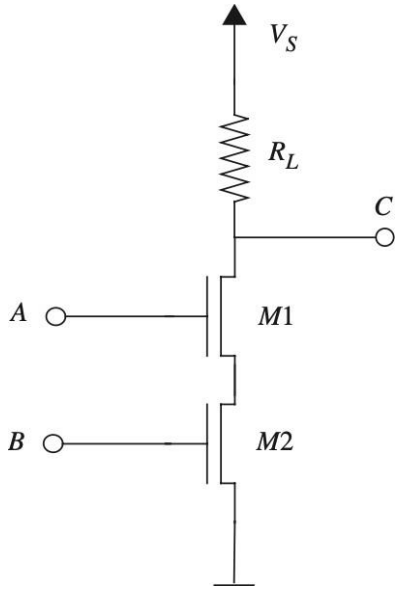
$$\text{for } v_{GS} \geq V_T, \quad v_{DS} = 0 \tag{6.2}$$

Logic Gates using MOSFET

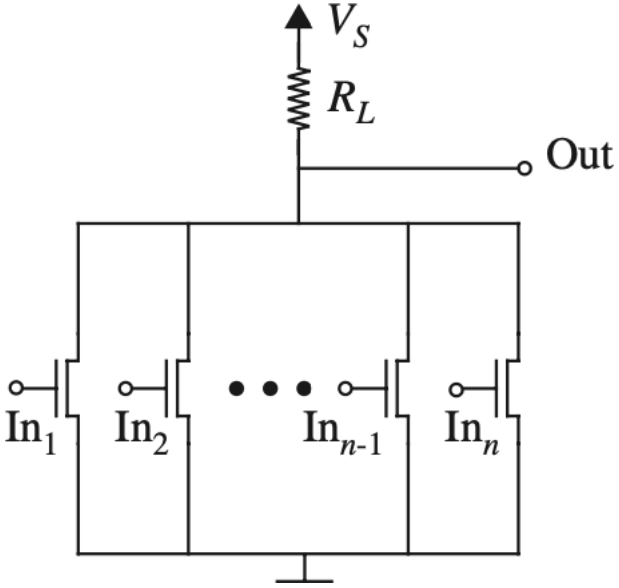
Just replace the switches with MOSFETs!



NOT Gate (Inverter)

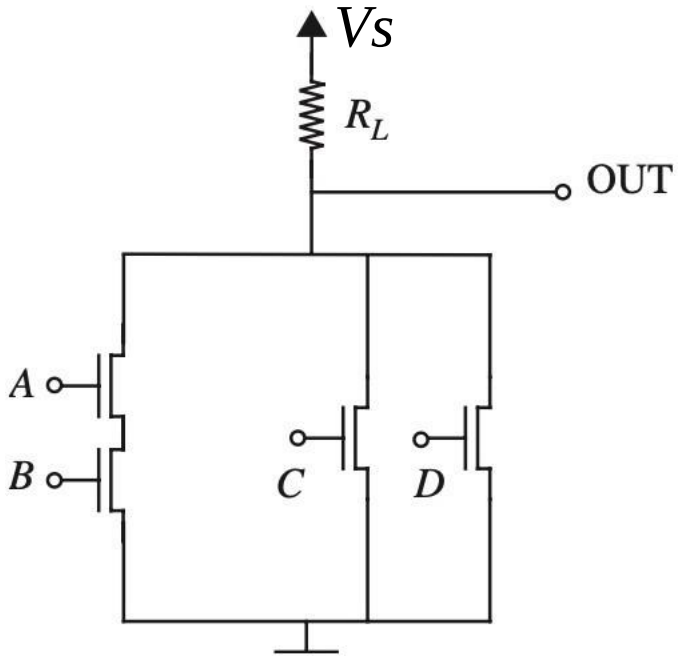


NAND Gate (Inverter)

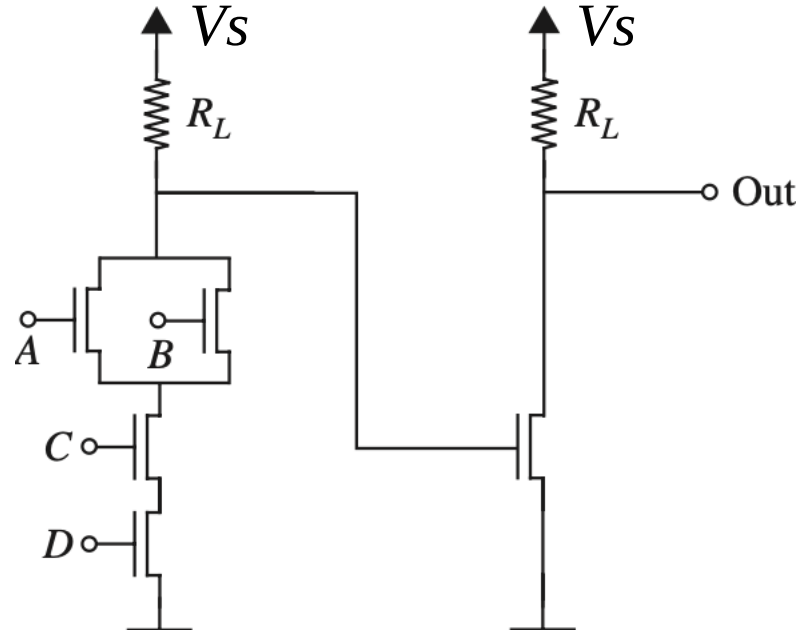


NOR Gate (Inverter)

MOSFET Logic Gates – More Examples



$$OUT = \overline{AB + C + D}$$



$$Out = \overline{\overline{(A + B)CD}} = (A + B)CD$$

Practice Problem 2

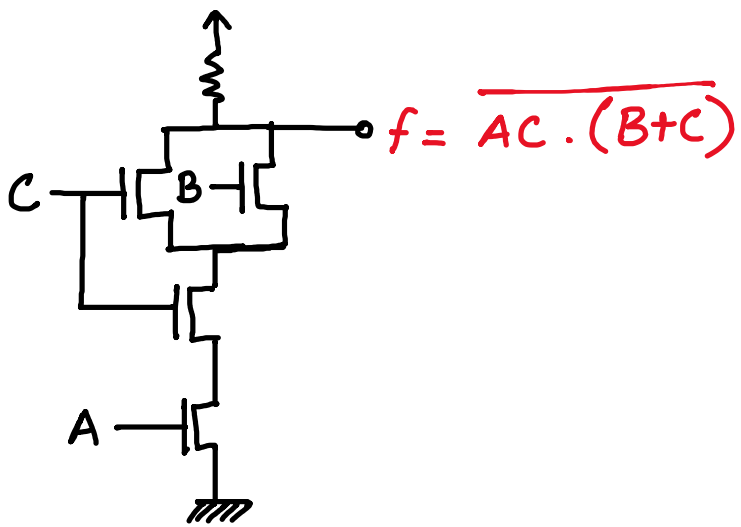
- **Design** a circuit using ideal MOSFETs (S-model) to implement the logic function

$$f = \overline{AC} + \overline{(B+C)}$$

$$= \overline{\overline{\overline{AC} + \overline{(B+C)}}}$$

$$= \overline{\overline{\overline{AC}} \cdot \overline{\overline{(B+C)}}} \quad \text{[De Morgan's Theorem]}$$

$$= \overline{AC \cdot (B+C)}$$



Practice Problem 1

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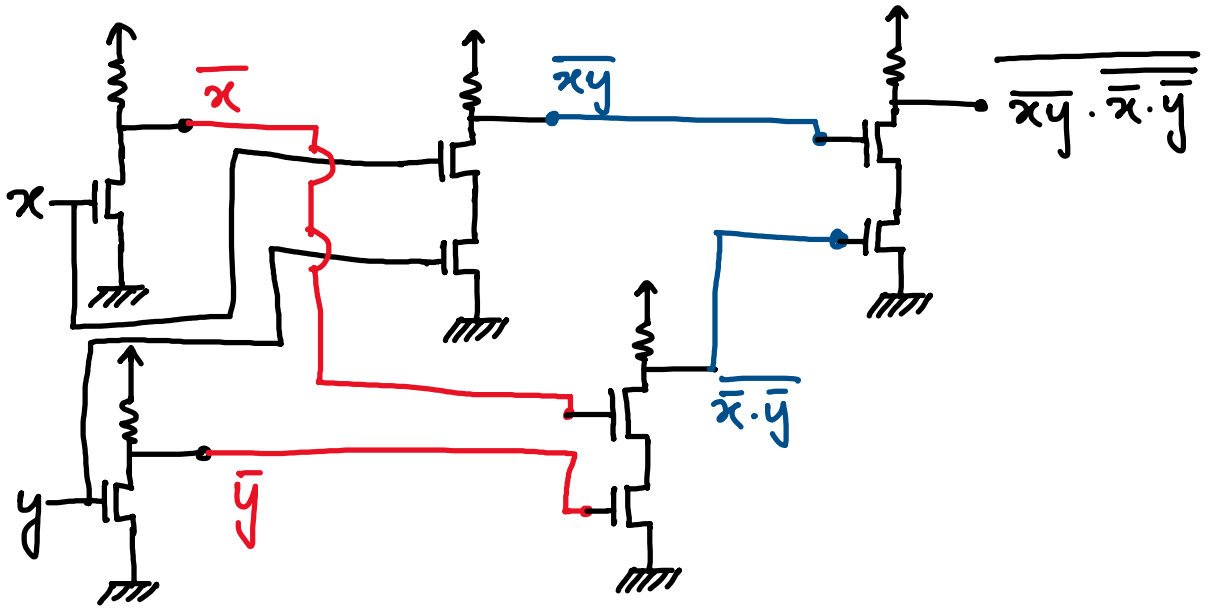


x	y	f
0	0	
0	1	
1	0	
1	1	

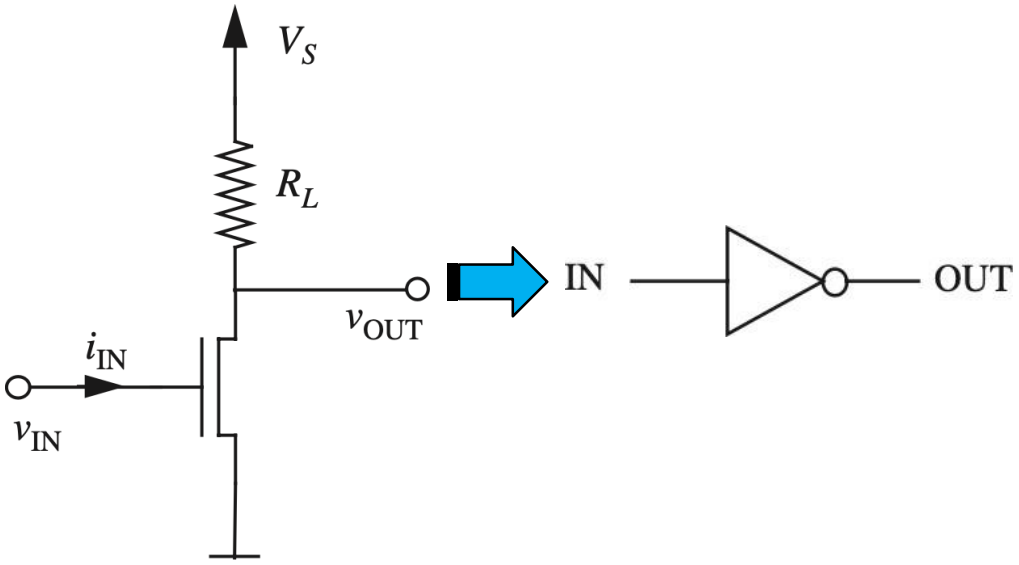
$$f = x \cdot y + \overline{x} \cdot \overline{y} = \overline{\overline{x \cdot y + \overline{x} \cdot \overline{y}}}$$
$$= \overline{\overline{x.y} \cdot \overline{\overline{x} \cdot \overline{y}}}$$

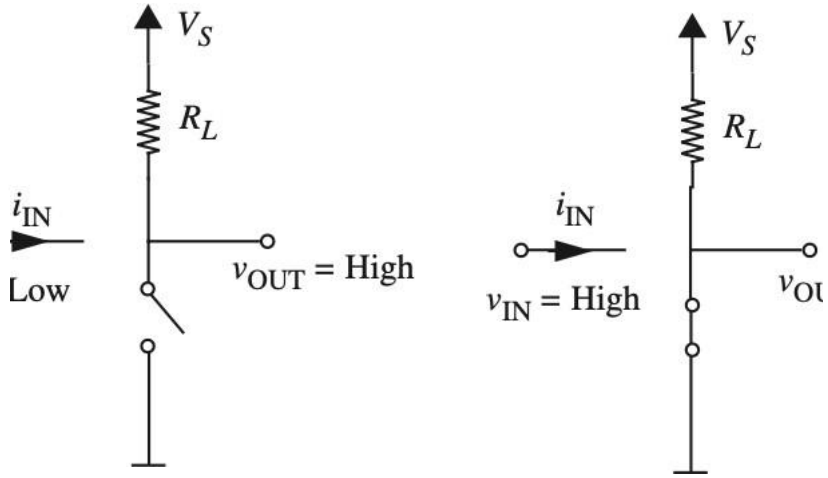
Voltage Transfer Characteristics (VTC)

- **Reminder:** VTC is a graph where x –axis = input voltage, y-axis = output voltage
- **Why?** Design logic gates to follow a given static discipline

When $v_{IN} < V_T$ (Logical 0) $v_{OUT} = V_S = 5$ V (Logical 1)

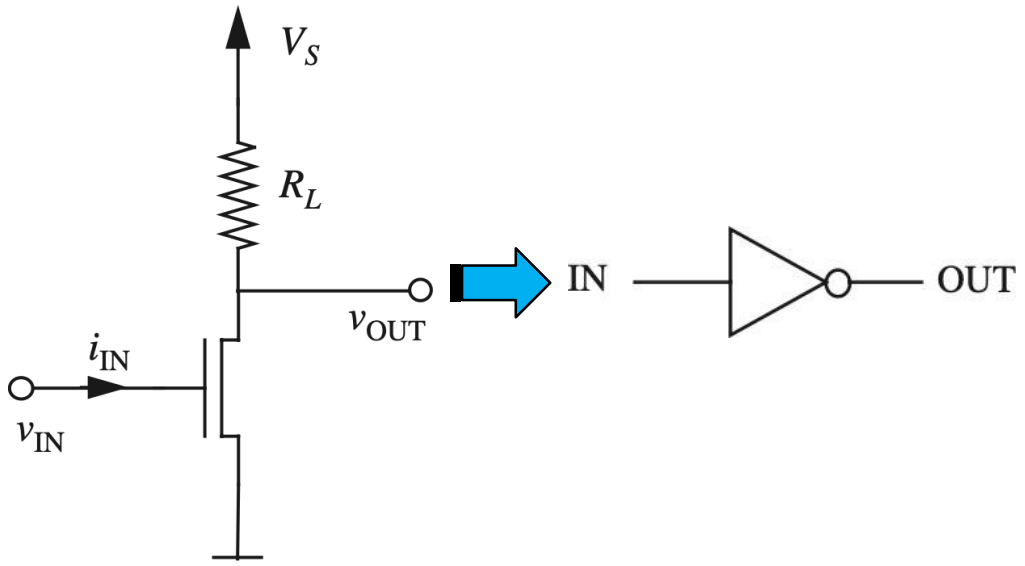
When $v_{IN} \geq V_T$ (Logical 1) $v_{OUT} = 0$ V (Logical 0)





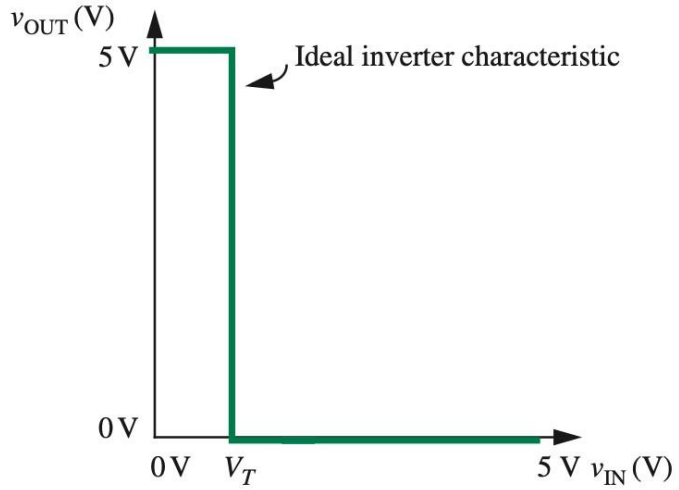
Voltage Transfer Characteristics (VTC)

- **Reminder:** VTC is a graph where x –axis = input voltage, y-axis = output voltage
- **Why?** Design logic gates to follow a given static discipline



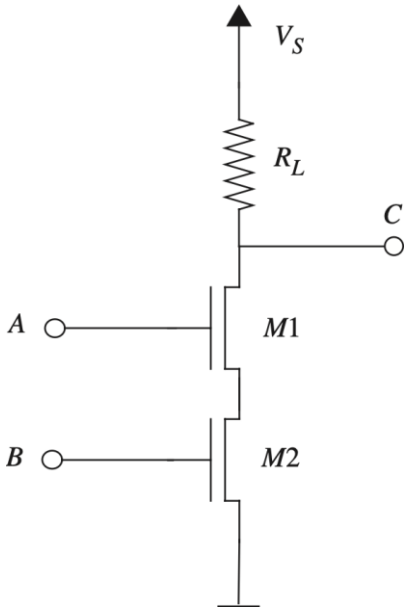
When $v_{IN} < V_T$ (Logical 0) $v_{OUT} = V_S = 5$ V (Logical 1)

When $v_{IN} \geq V_T$ (Logical 1) $v_{OUT} = 0$ V (Logical 0)

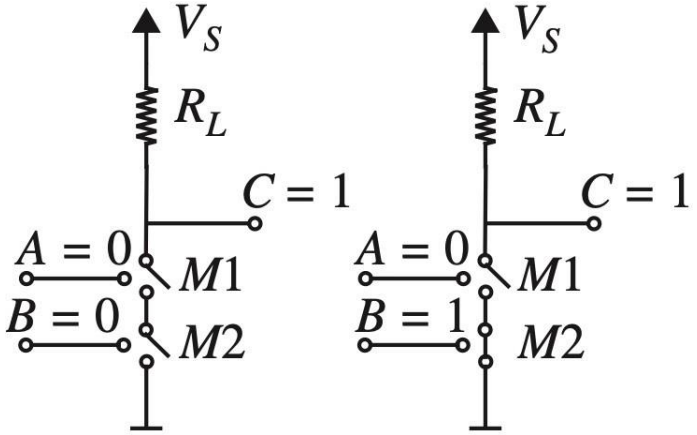


VTC of NAND gate

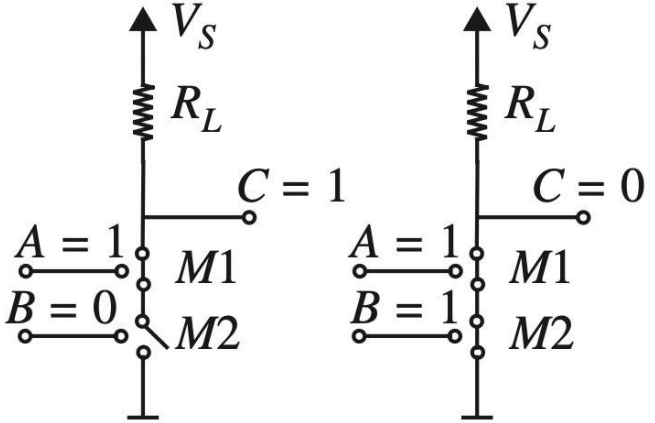
- We only have one $\boldsymbol{x}$ –axis, but two inputs
- **Solution:** Draw two VTC, one considering $V_A = 0$ one considering $V_A = 1$



When $V_A = 0$

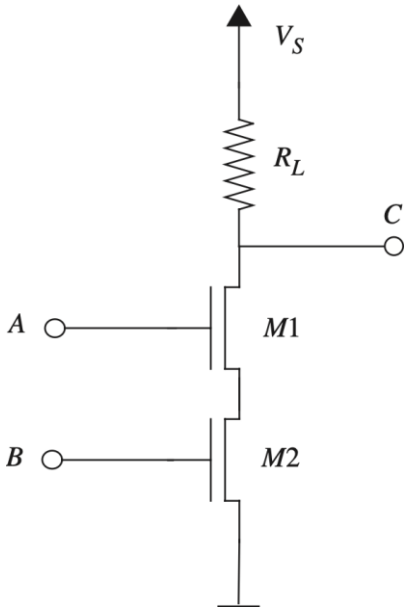


When $V_A = 1$

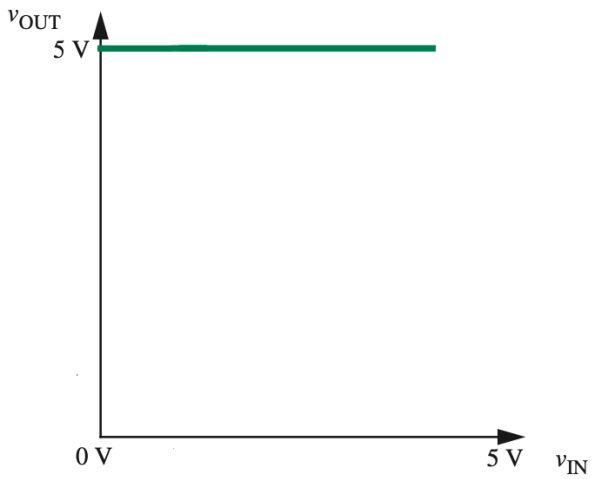


VTC of NAND gate

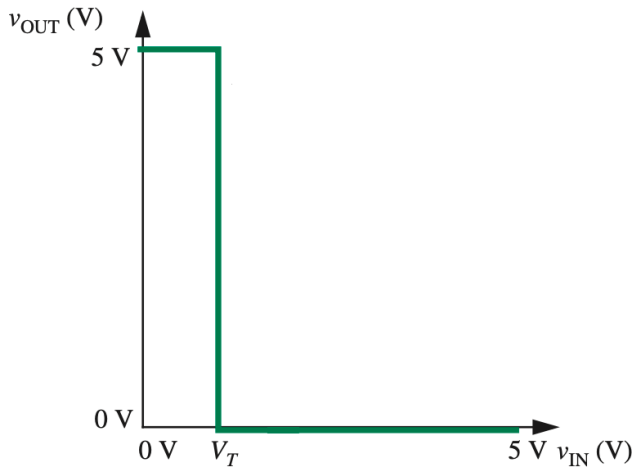
- We only have one $\boldsymbol{x}$ –axis, but two inputs
- **Solution:** Draw two VTC, one considering $V_A = 0$ one considering $V_A = 1$



When $V_A = 0$



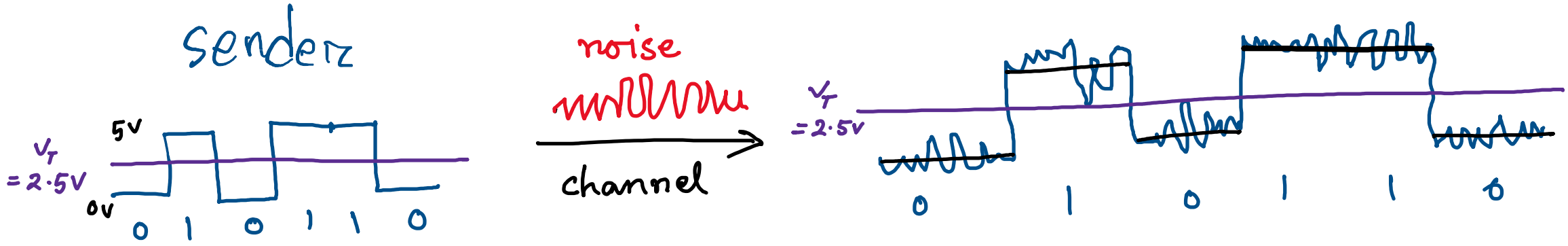
When $V_A = 1$



Homework: Find VTC for NOR gate

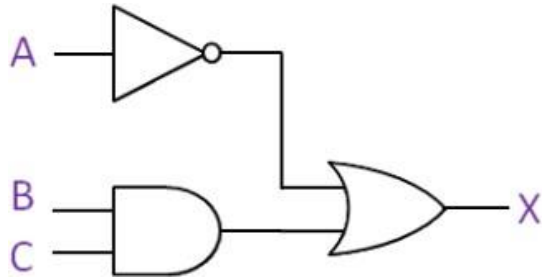
Digital Representation

Suppose you want to send 010110



- Single value based representaion fails in the presence of noise
- Better approach – threshold-based system
- Simplest: Logical 0 = $V < V_T$ Logical 1 = $V > V_T$

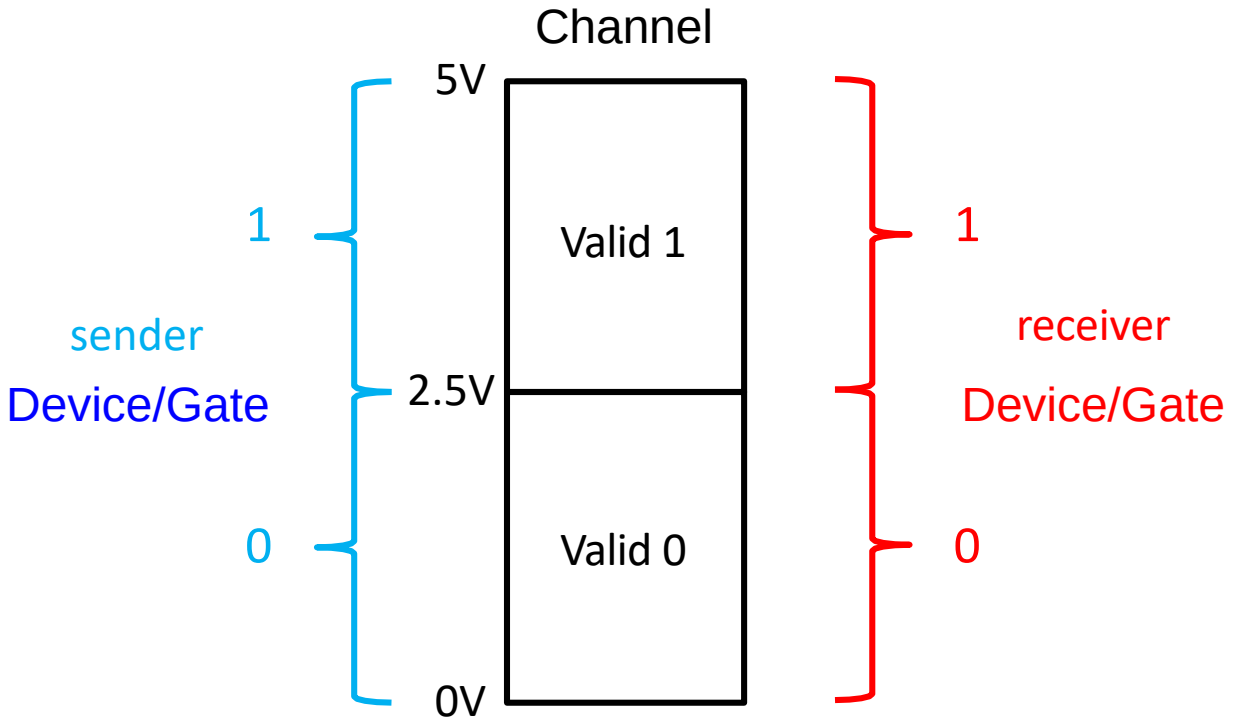
Static Discipline



- Specification for “all” digital devices
- Requires devices to adhere to common representation to ensure that **valid input produces valid output**
- This means, if
  - Sender sends “0” → (noise, Channel) → Receiver interprets as “0”
  - Sender sends ”1” → (noise, Channel) → Receiver interprets as “1”

Static Discipline

Naïve approach: Single threshold-based system



$V_T = 2.5\ V$

sender

Logical 0: $V_o < V_T$
Logical 1: $V_o > V_T$

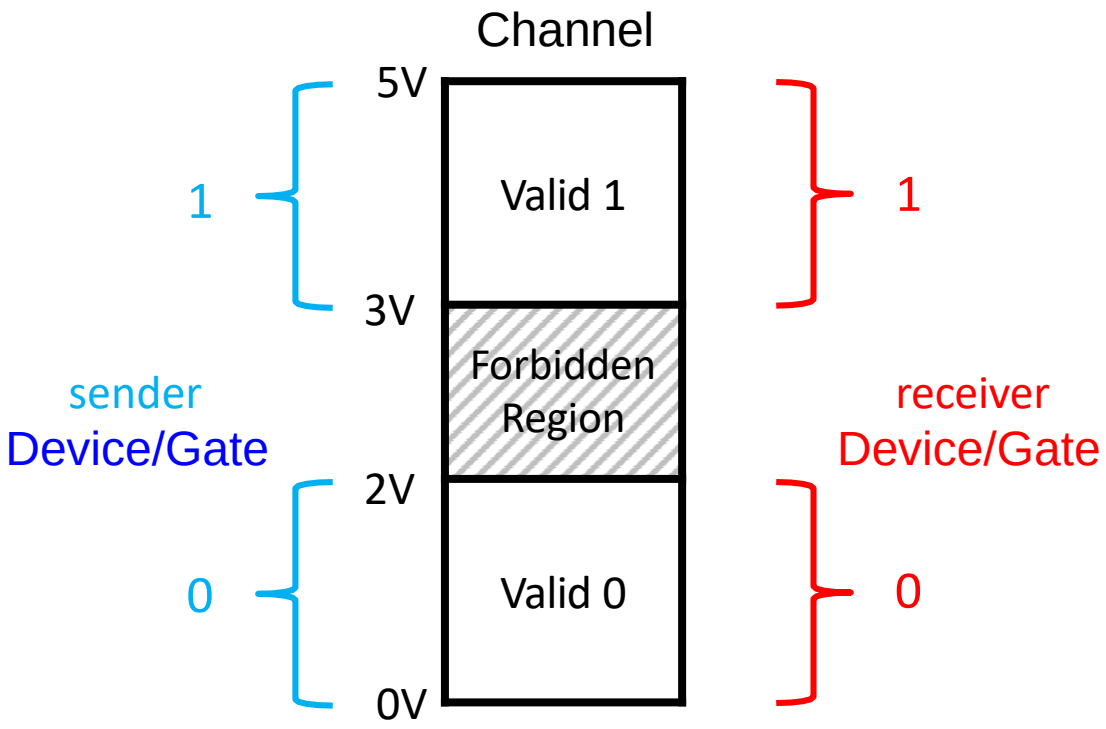
receiver

Logical 0: $V_i < V_T$
Logical 1: $V_i > V_T$

What if $V_i = 2.5$ V? It is **undefined**!

Static Discipline

Double threshold based system



V_H= High voltage threshold = $3V$

V_L= High voltage threshold = $2\ V$

sender	receiver
Logical 0: $V_o < V_L$	Logical 0: $V_i < V_L$
Logical 1: $V_o > V_H$	Logical 1: $V_i > V_H$

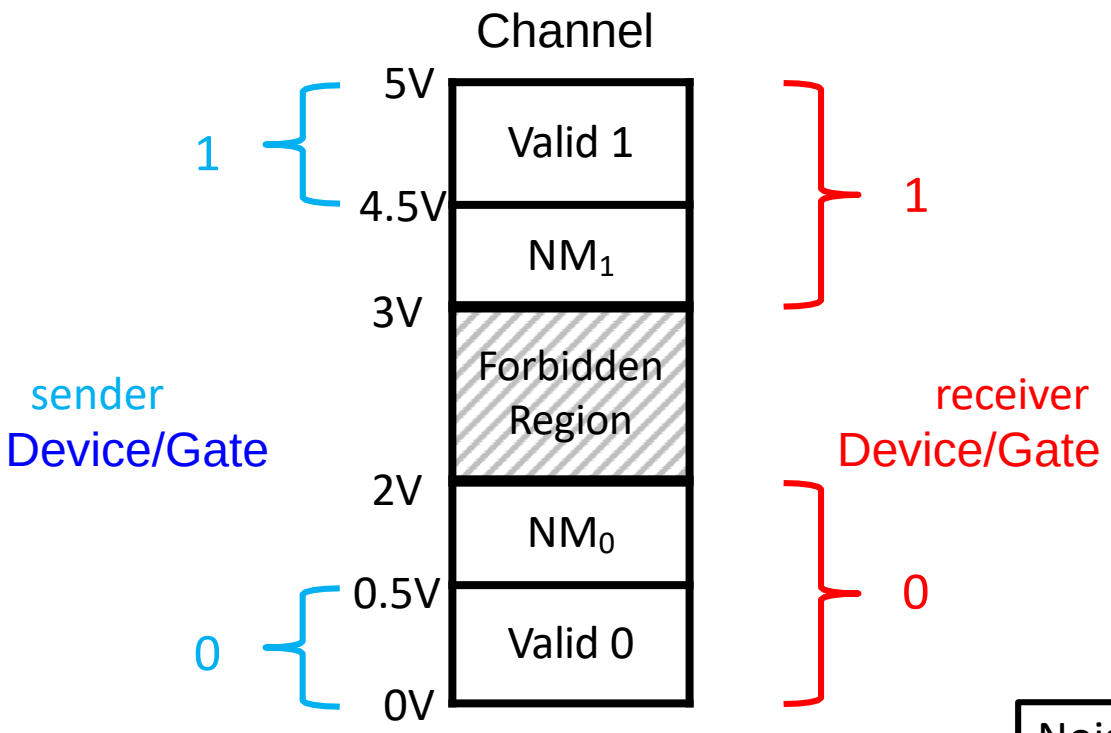
What if V_o =$1.9V$ and channel noise is $0.5V$?

V_i= $1.9V + 0.5V = 2.4V$ = invalid

➔ valid output producing invalid input, i.e., no margin for noise

Static Discipline

Four threshold-based system → Tighter restriction on sender (**output**)



V_{OH}= Output high voltage threshold = $4.5V$
V_{OL} =Output low voltage threshold = $0.5V$
V_{IH} =Input high voltage threshold = $3V$
V_{IL} =Input low voltage threshold = $2V$

sender

Logical 0: $V_o < V_{OL}$
Logical 1: $V_o > V_{OH}$

receiver

Logical 0: $V_i < V_{IL}$
Logical 1: $V_i > V_{IH}$

For static discipline, $V_{OL} < V_{IL} < V_{IH} < V_{OH}$

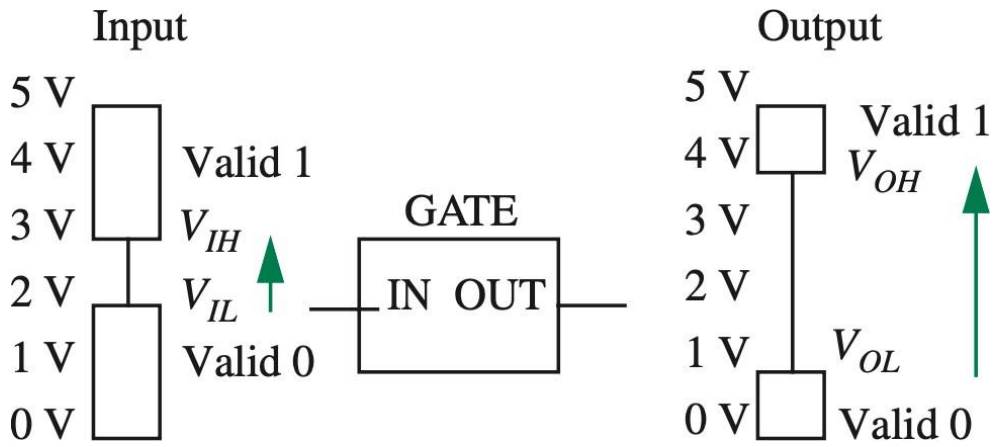
Noise margins (NM):

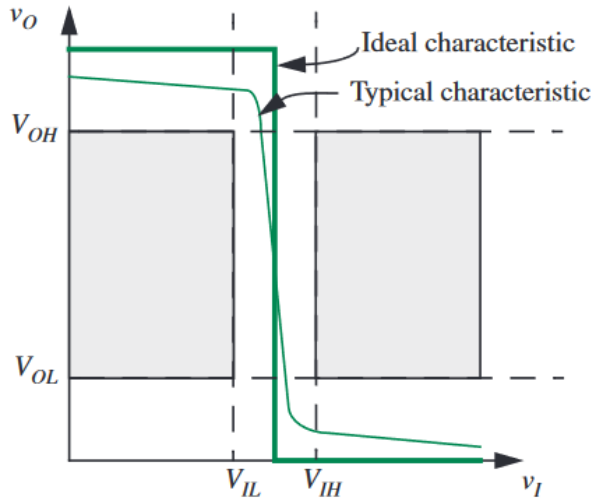
- $NM_1 = V_{OH} - V_{IH} = 4.5 - 3 = 1.5$ V (significance?)
- $NM_0 = V_{IL} - V_{OL} = 2 - 0.5 = 1.5$ V (significance?)

Static Discipline

Four threshold-based system → Tighter restriction on sender (**output**)

V_{OH}: The lowest output voltage value that a digital device **can produce** when it outputs a logical **1**.
V_{OL}: The highest output voltage value that a digital device **can produce** when it outputs a logical **0**.

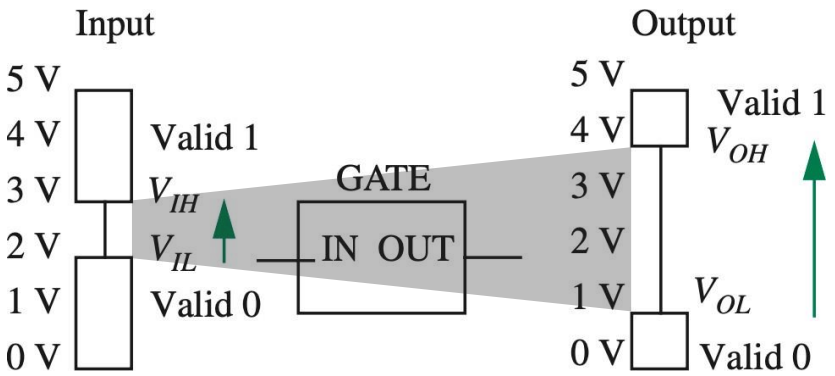




V_{IH}: The *lowest input voltage* value that a digital device **must recognize** as a logical **1**.
V_{IL}: The *highest input voltage* value that a digital device **must recognize** as a logical **0**.

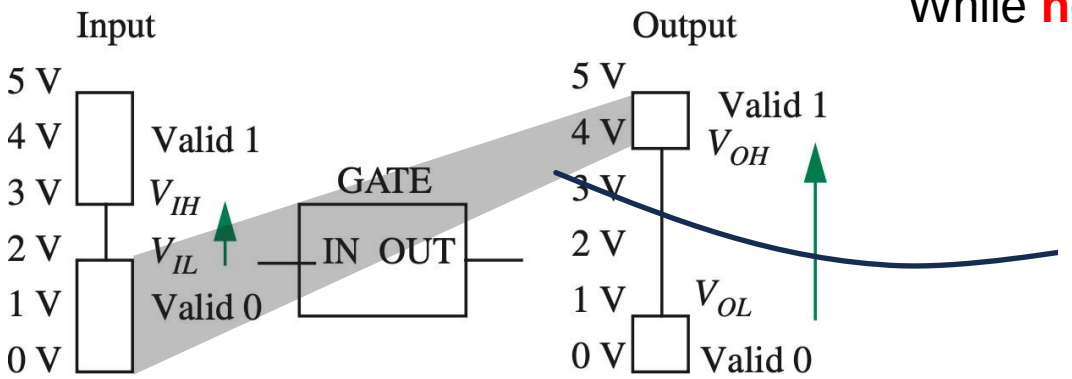
Static Discipline and VTC graph

Four threshold-based system → Tighter restriction on sender (**output**)



During high to low or low to high **transition**:

Higher Slope in VTC graph



While **not** in **transition**; at logical **HIGH** or **LOW** voltage level:

Smaller Slope in VTC graph

Static Discipline and VTC graph

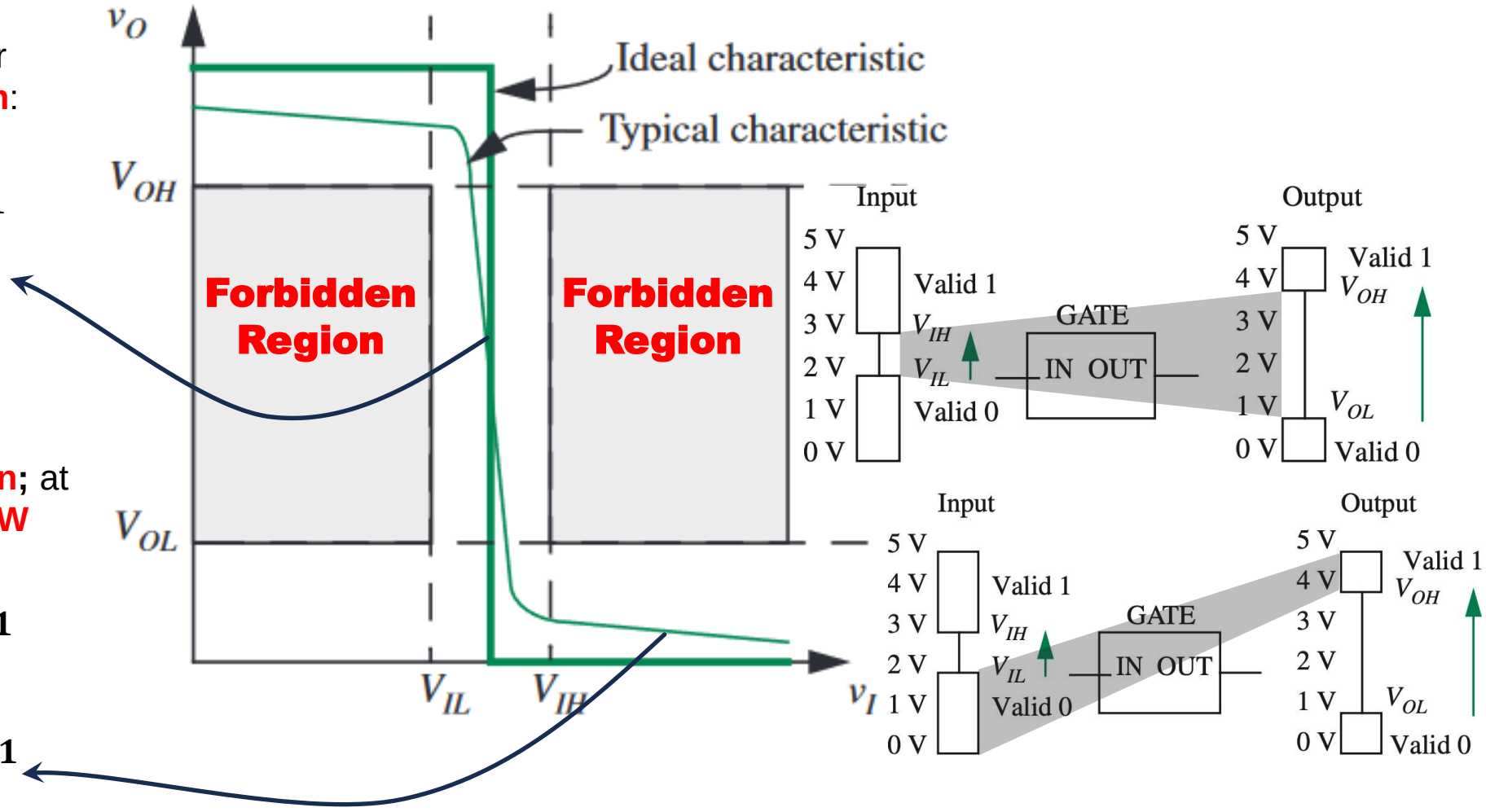
During high to low or low to high **transition**:

Slope > 1

While **not** in **transition**; at logical **HIGH** or **LOW** voltage level:

Slope < 1

Slope < 1



Next Class

- Constructing a *real* MOSFET – n/p-channel
- Operation of an Ideal FET- Cut-Off, Saturation and Triode Mode
- Output Characteristics
- PWL Model and Non-ideal Analysis: SR model
- Real MOSFET equations
- Introduction to Static analysis