CSE251: Electronic Devices and Circuits

Lecture: MOSFET 2

Prepared By:

Shadman Shahid (SHD)

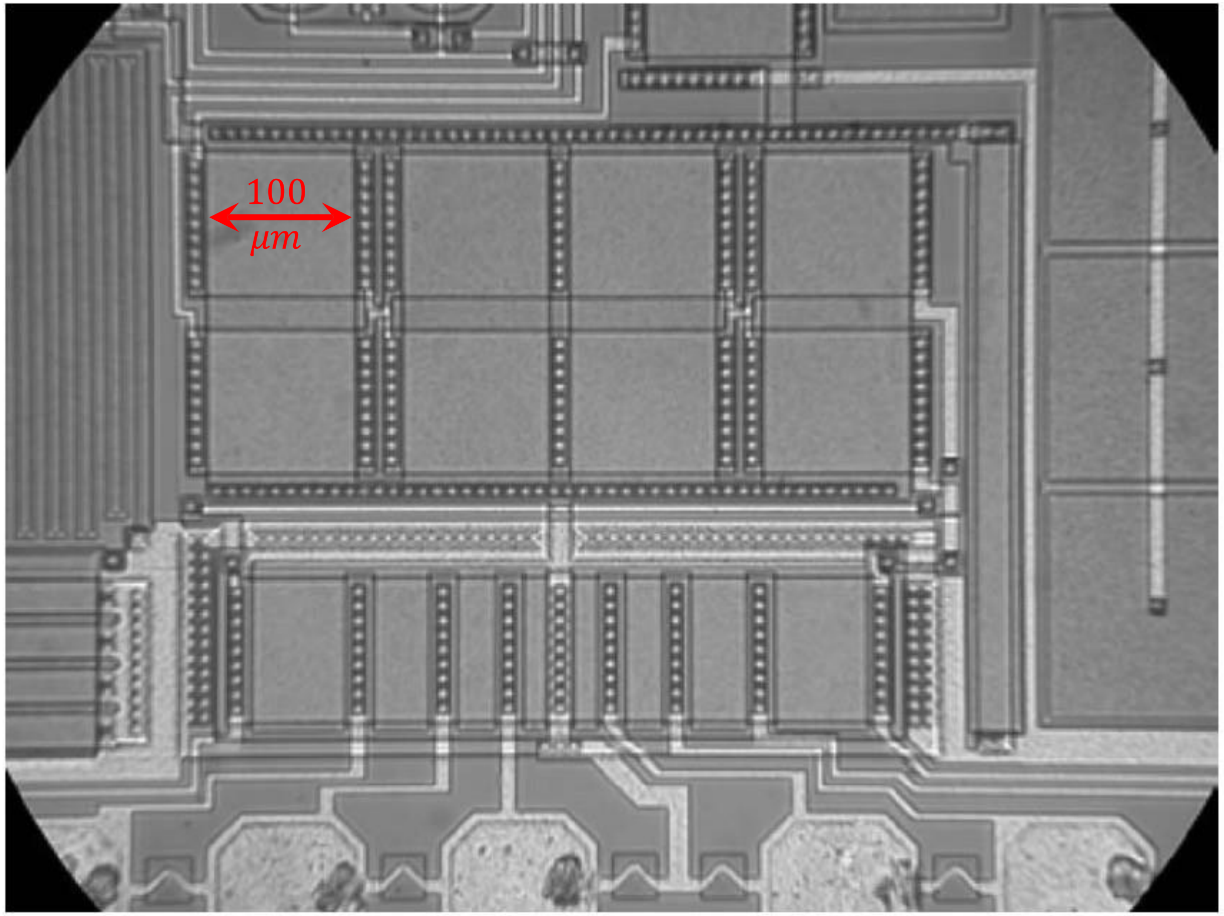
Lecturer, Department of Computer Science and Engineering, School of Data and Sciences, BRAC University

Email: ext.shadman.shahid@bracu.ac.bd

Outline

- Constructing a *real* MOSFET – n/p-channel
- **Operation of an MOSFET-**
    1. Cut-Off
    2. Saturation
    3. Triode Mode
- Output Characteristics
- PWL Model and Non-ideal Analysis: **SR model**
- Real MOSFET equations
- Introduction to Static analysis

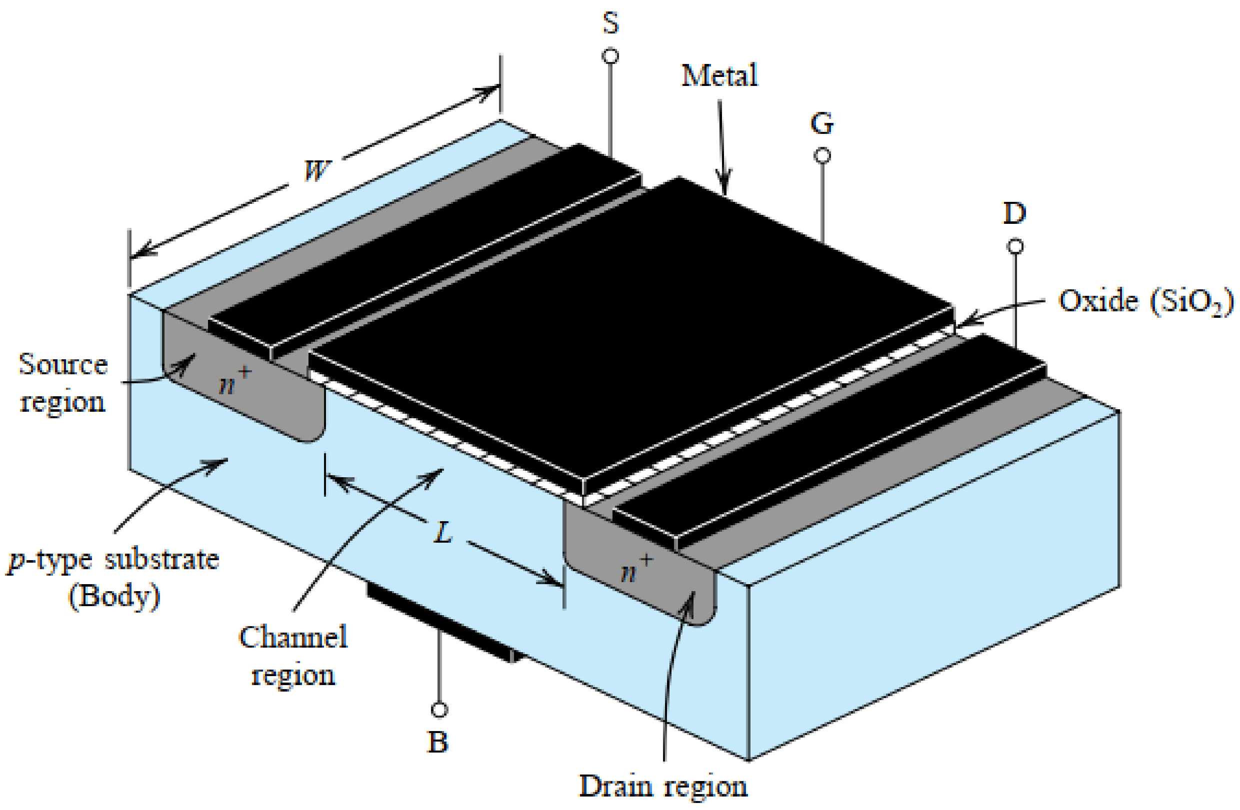
Construction of Real MOSFET

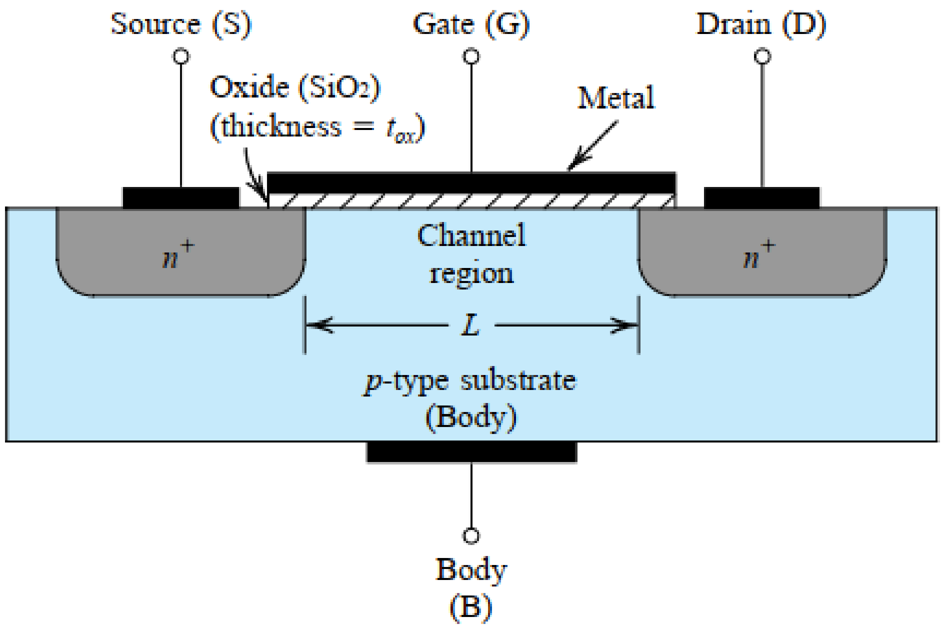


Top view of several n-channel MOSFETs fabricated on a chip. The square MOSFETs in the center of the photograph have a width and length of 100 µm. (Photograph Courtesy of Maxim Integrated Products.)

Real MOSFET – Enhancement Type

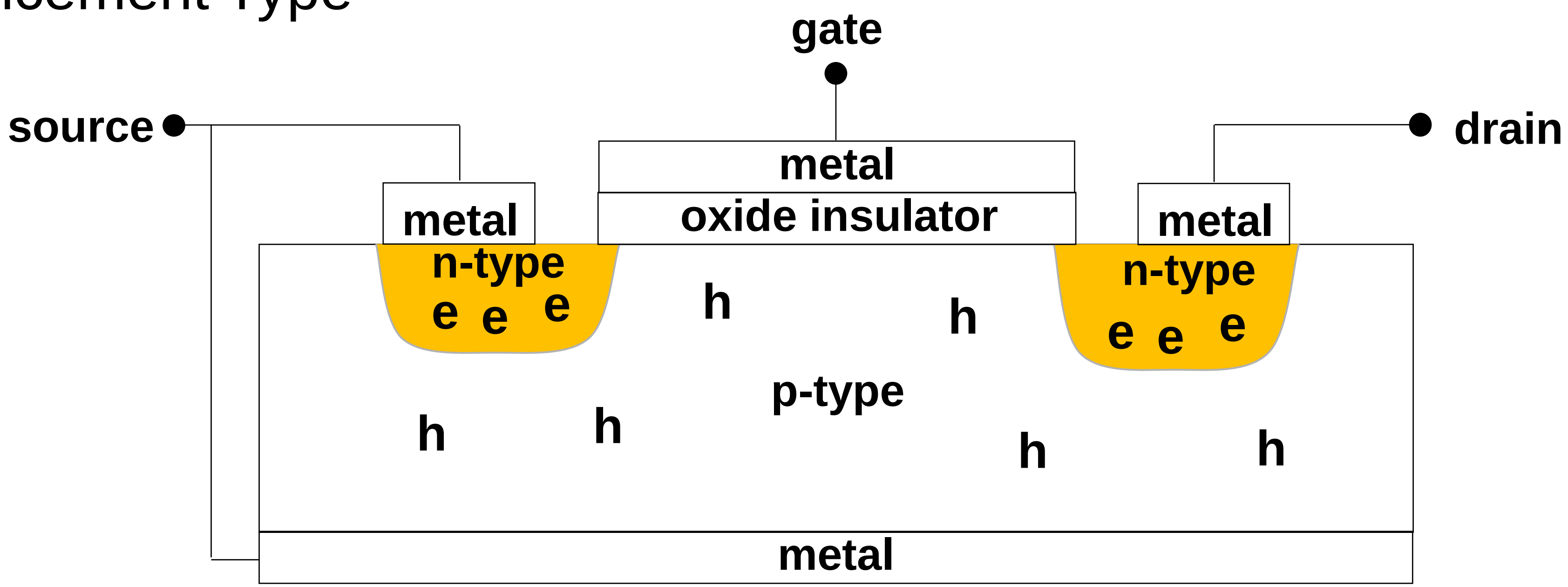
Device Structure (*n*-channel **MOS**FET**)**



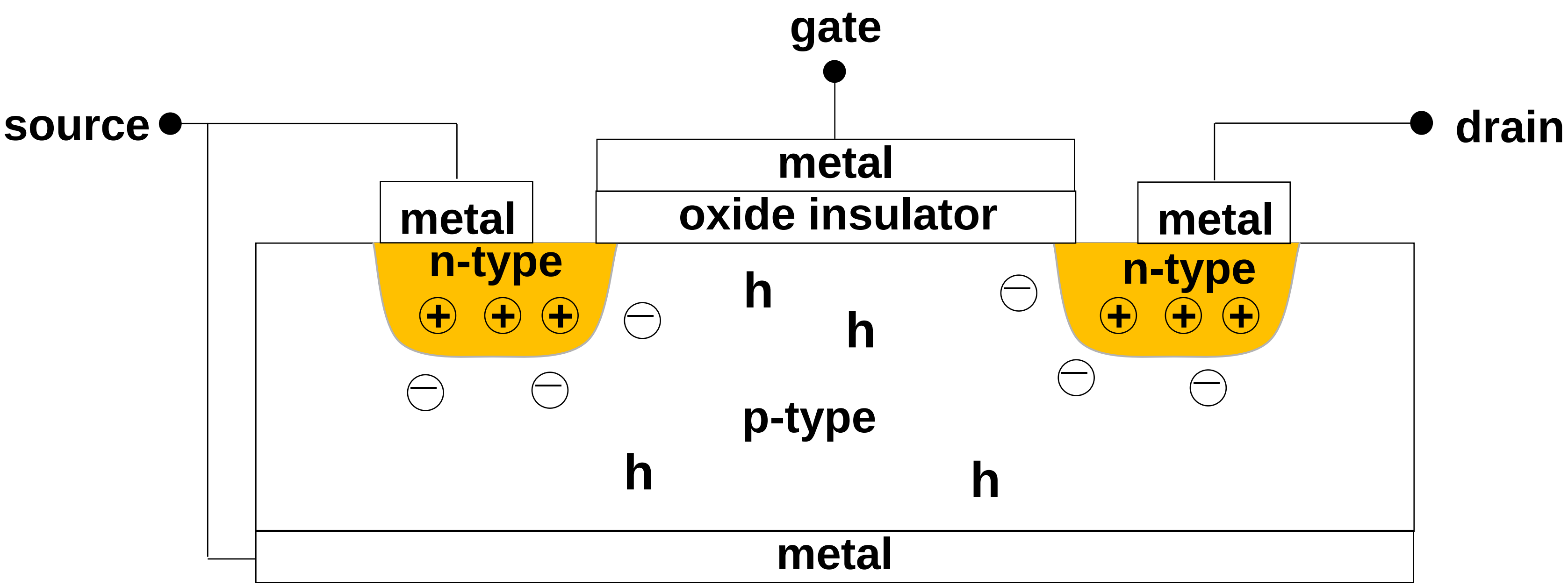


***n*-cha**nnel **MOS**FET (NMOS) Physical Structure

Enhancement Type



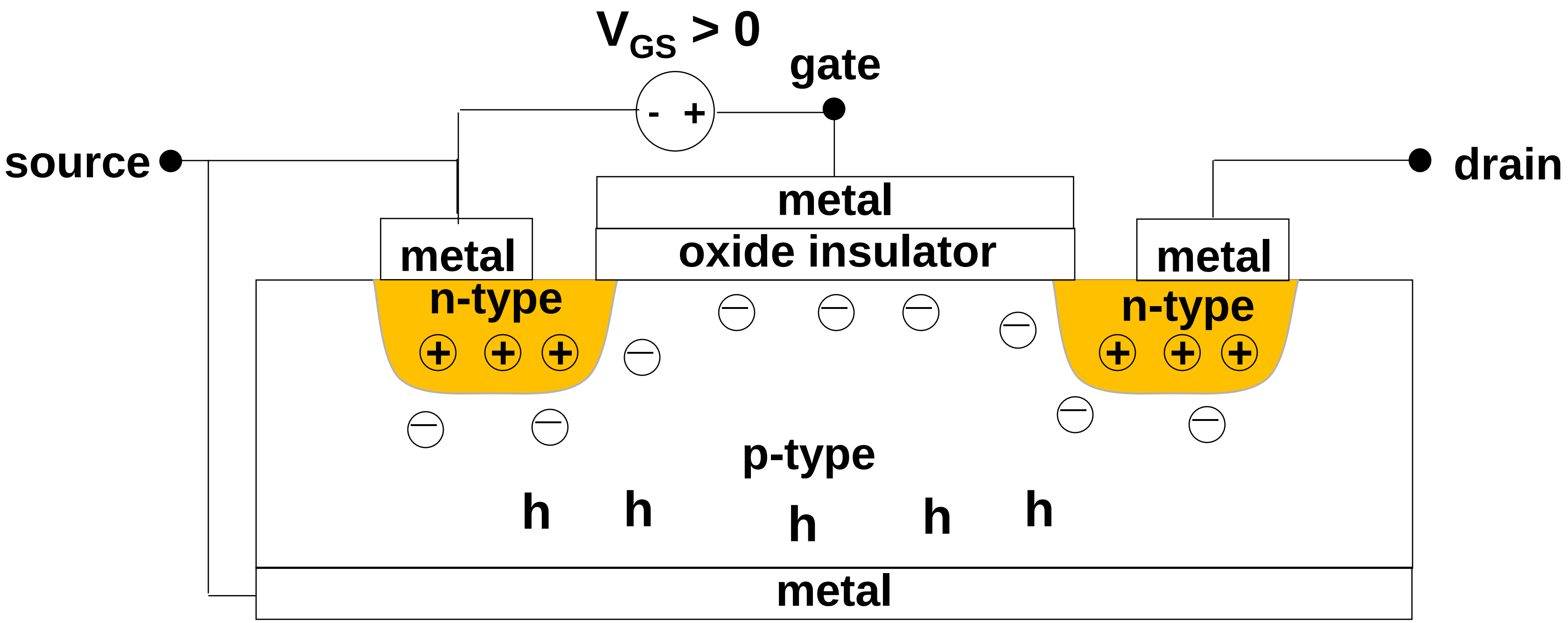
NMOS in Equilibrium



When the transistor is left alone, some electrons from the n-type wells diffuse into the p-type material to fill holes.

This creates negative ions in the p-type material and positive ions are left behind in the n-type material.

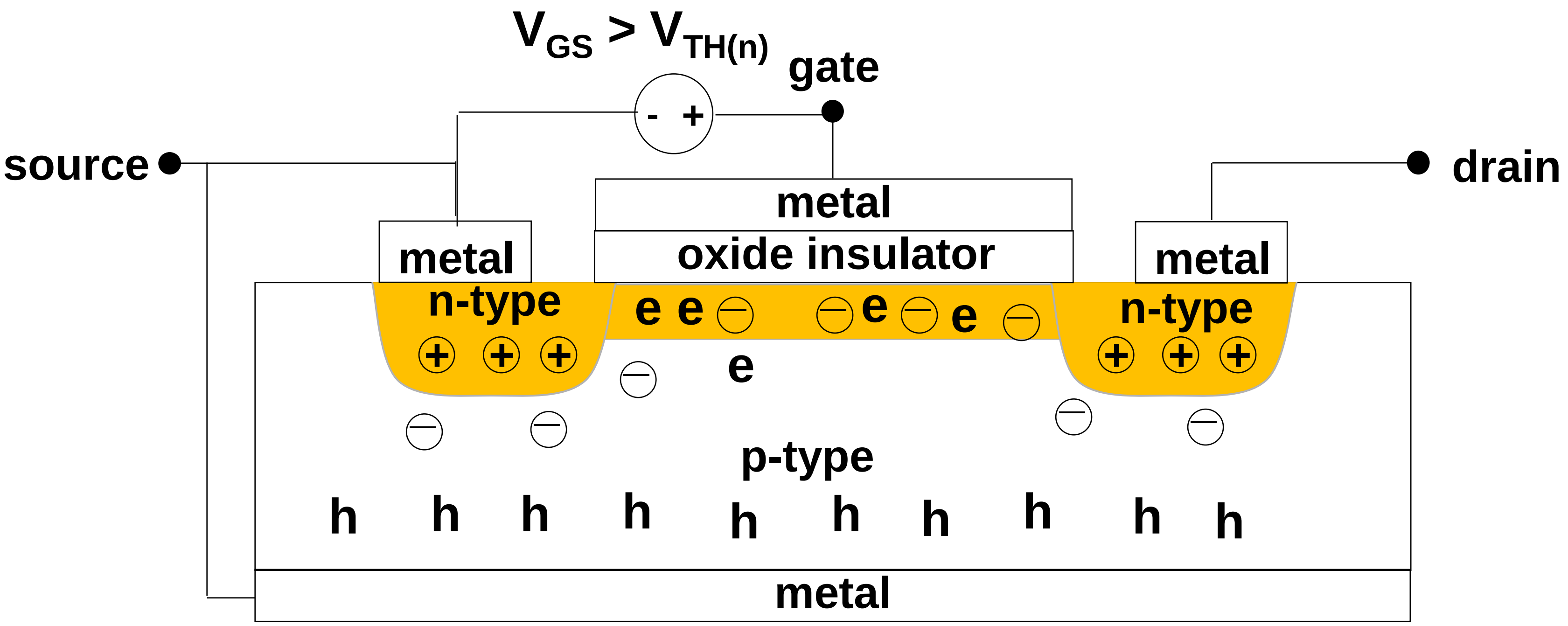
NMOS in Cutoff



When a small, positive V_{GS} is applied, holes “move away” from the gate.

Electrons from complete atoms elsewhere in the p-type material move to fill holes near the gate instead.

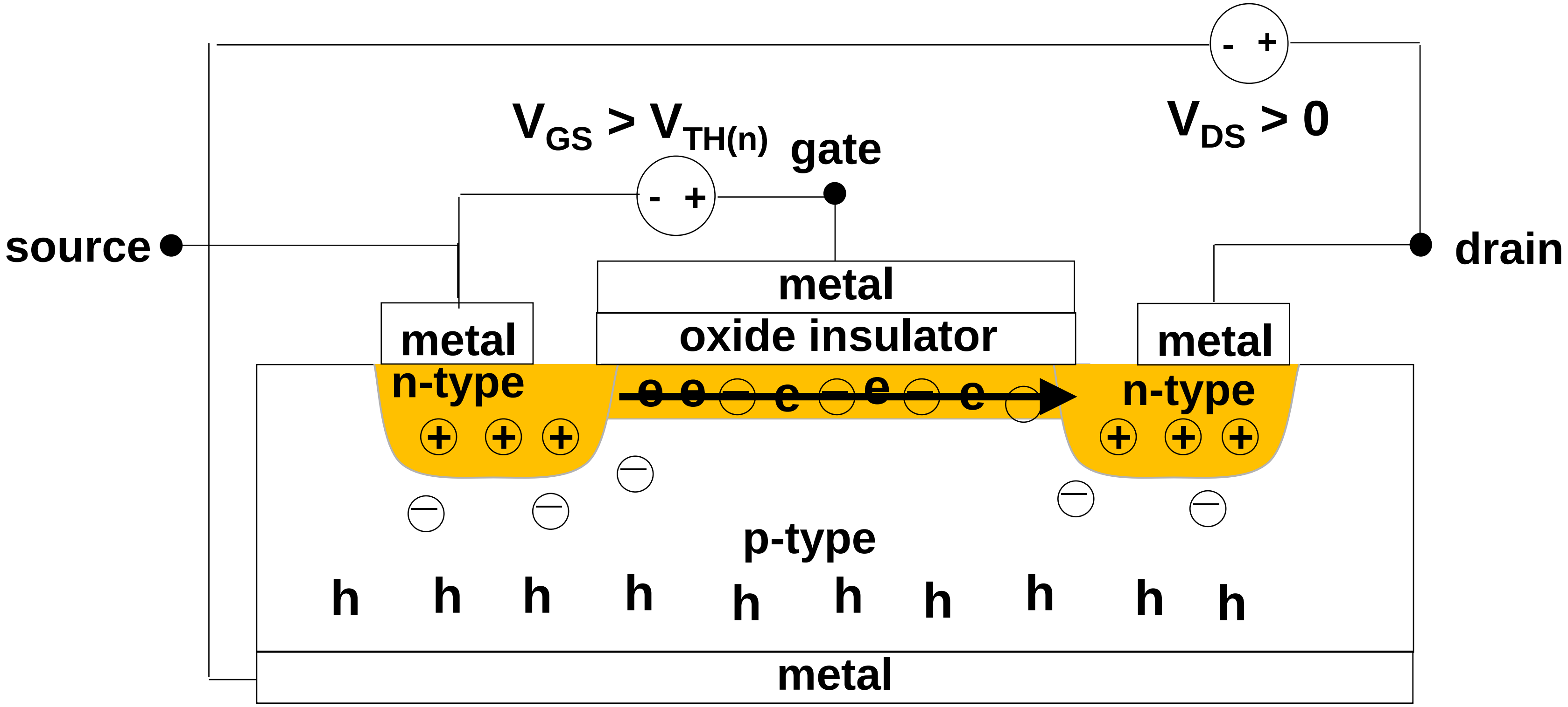
NMOS Transistor channel



When V_{GS} is larger than a **threshold** voltage $V_{TH(n)}$, the attraction to the gate is so great that free electrons collect there.

The applied V_{GS} creates an **induced n-type channel** under the gate (an area with free electrons).

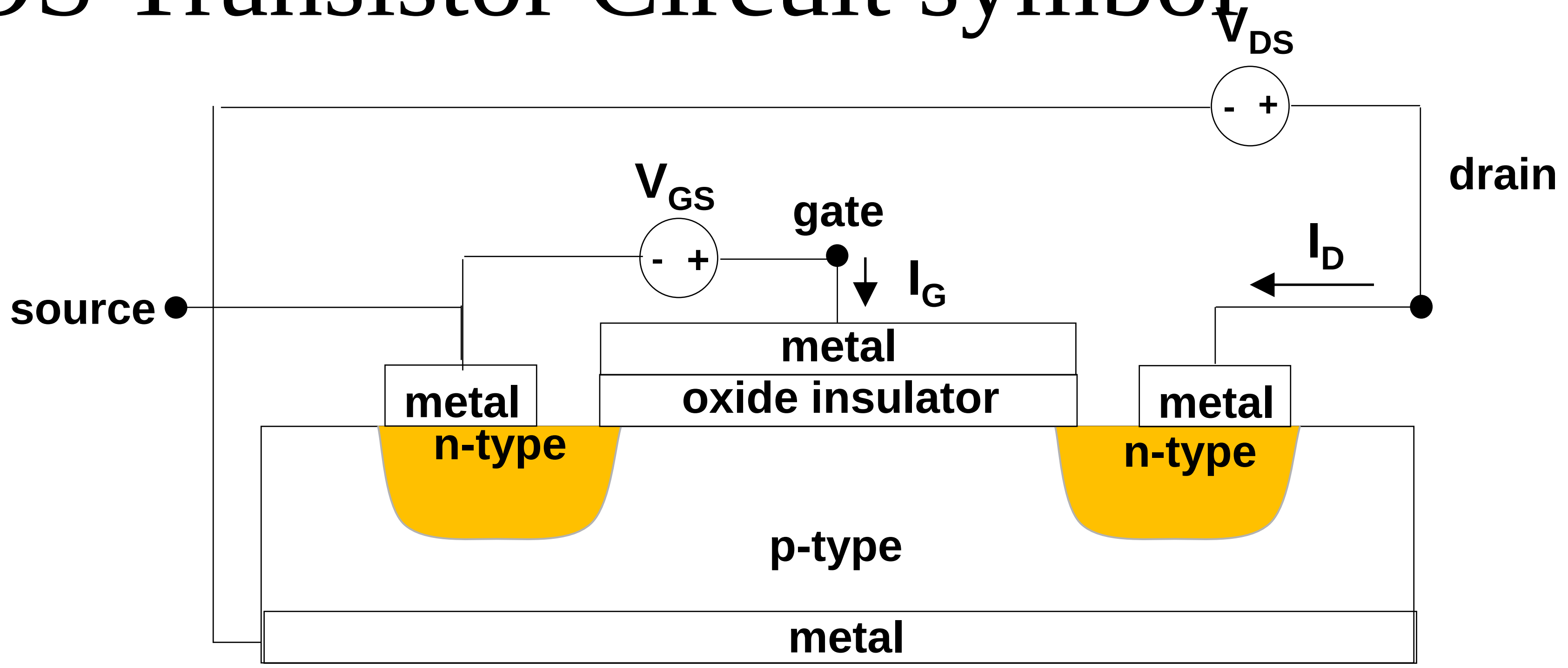
NMOS Trasistor Drain Current

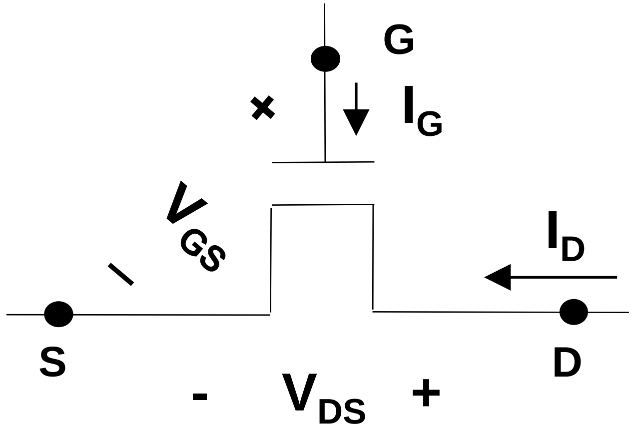


When a positive V_{DS} is applied, the free electrons flow from the source to the drain. (Positive current flows from drain to source).

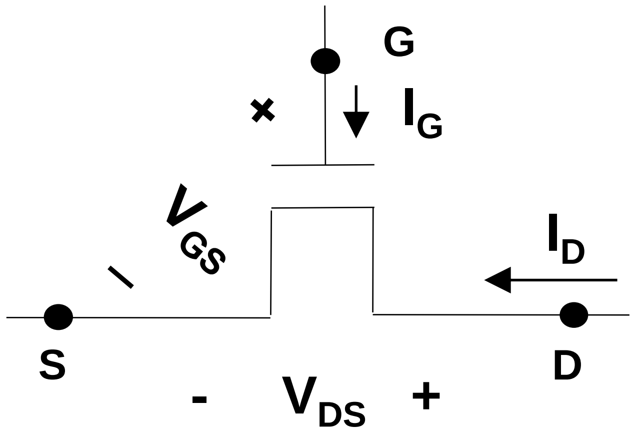
The amount of current depends on V_{DS}, as well as the number of electrons in the channel, channel dimensions, and material.

NMOS Transistor Circuit symbol





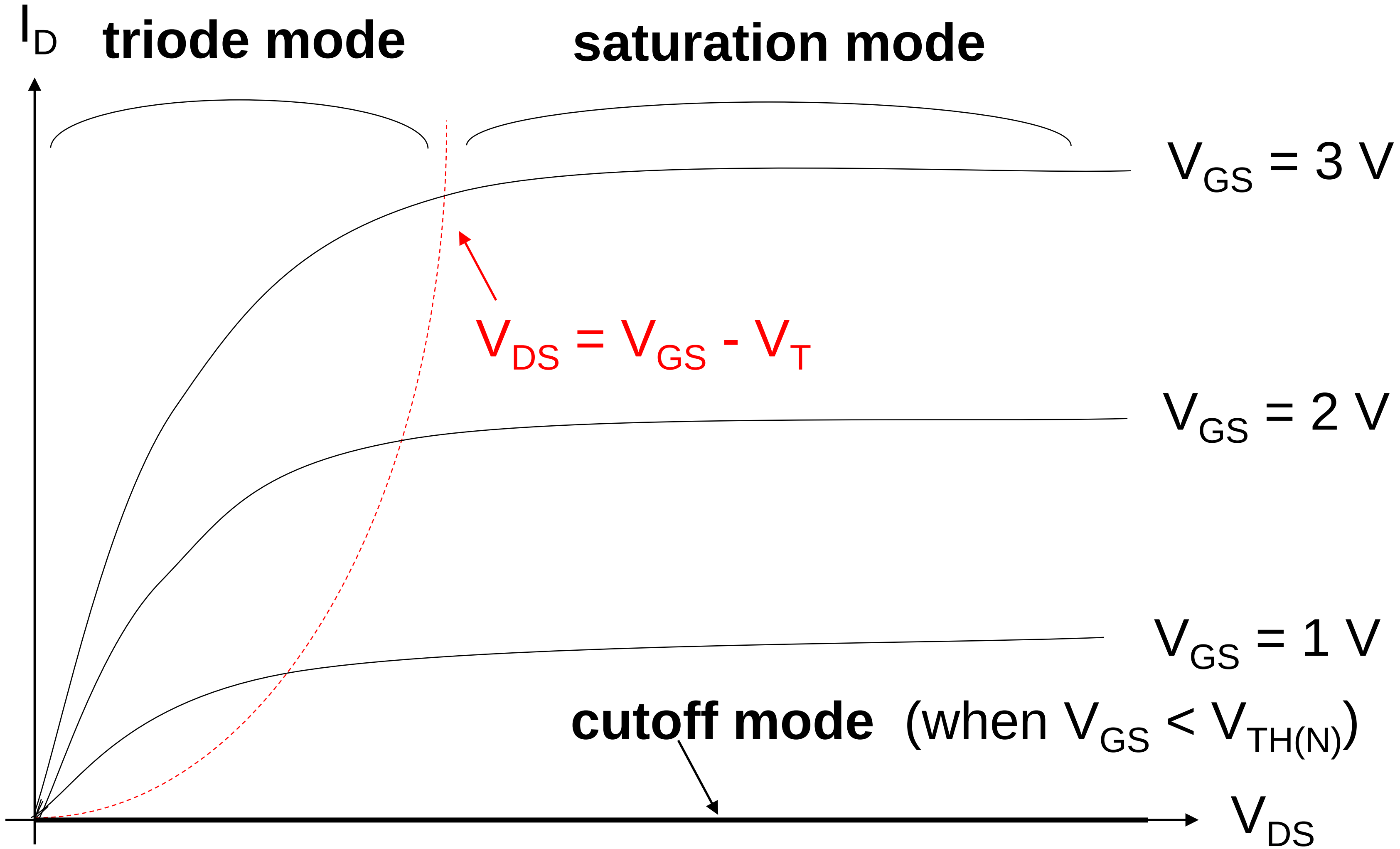
NMOS I-V Characteristic



- Since the transistor is a 3-terminal device, there is no single I-V characteristic.
- Note that because of the insulator, $I_G = 0$ A.
- We typically define the MOS I-V characteristic as

  I_D vs. V_{DS} for a fixed V_{GS}.
- The I-V characteristic changes as V_{GS} changes.

NMOS I-V Characteristic



Modes of Operation

- For small values of V_{GS}, $V_{GS} \le V_{TH(n)}$, the n-type channel is not formed. No current flows. This is **cutoff mode**.
- When $V_{GS} > V_{TH(n)}$, current I_D may flow from drain to source, and the following modes of current flow are possible.
  - The mode of current flow depends on the propelling voltage, V_{DS}, and the channel-inducing voltage,

    $V_{GS} – V_{TH(n)}$.
  - When $V_{DS} < V_{GS} – V_{TH(n)}$, current is starting to flow. I_D increases rapidly with increased V_{DS}. This is **triode mode**.
  - When $V_{DS} \ge V_{GS} – V_{TH(n)}$, current is reaching its maximum value. I_D does not increase much with increased V_{DS}. This is called **saturation mode**.

Water Tap Analogy

Imagine the water tap on your kitchen sink.

- To make water flow, the water supply has to be connected to the water tap. This establishes a path for water to flow.
- Setting V_{GS} above the threshold voltage is like connecting the water supply.
- **Cutoff = water supply disconnected (no path for current flow)**
- Setting V_{GS} to a larger value is like connecting a high-pressure water supply—more flow can potentially occur.

Water Tap Analogy

- The water tap itself is used to adjust water flow. You can turn the flow up and down.
- V_{DS} is like the water tap. It controls the amount of flow.
- There is, of course, a saturation point. If you keep turning the water tap control, eventually you won’t get any more flow.
- **Triode = water tap in “normal range”, controls flow**
- **Saturation = water tap turned up to (or past) point for maximum flow**

NMOS Equations

Cutoff Mode

Occurs when $\boldsymbol{v_{GS} < V_T}$

$$\boldsymbol{I_D = 0}$$

Triode Mode

Occurs when $\boldsymbol{v_{GS} \geq V_T}$ and $\boldsymbol{v_{DS} < v_{GS} - V_T}$

$$\boldsymbol{I_{DS} = k_n' \frac{W}{L}\left(v_{GS} - V_T - \frac{1}{2} v_{DS}\right) v_{DS}}$$

Saturation Mode

Occurs when $\boldsymbol{v_{GS} > V_T}$ and $\boldsymbol{v_{DS} \geq v_{GS} - V_T}$

$$\boldsymbol{I_{DS} = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_T)^2}$$

$v_{GS} - V_T = V_{OV}$: Overdrive Voltage

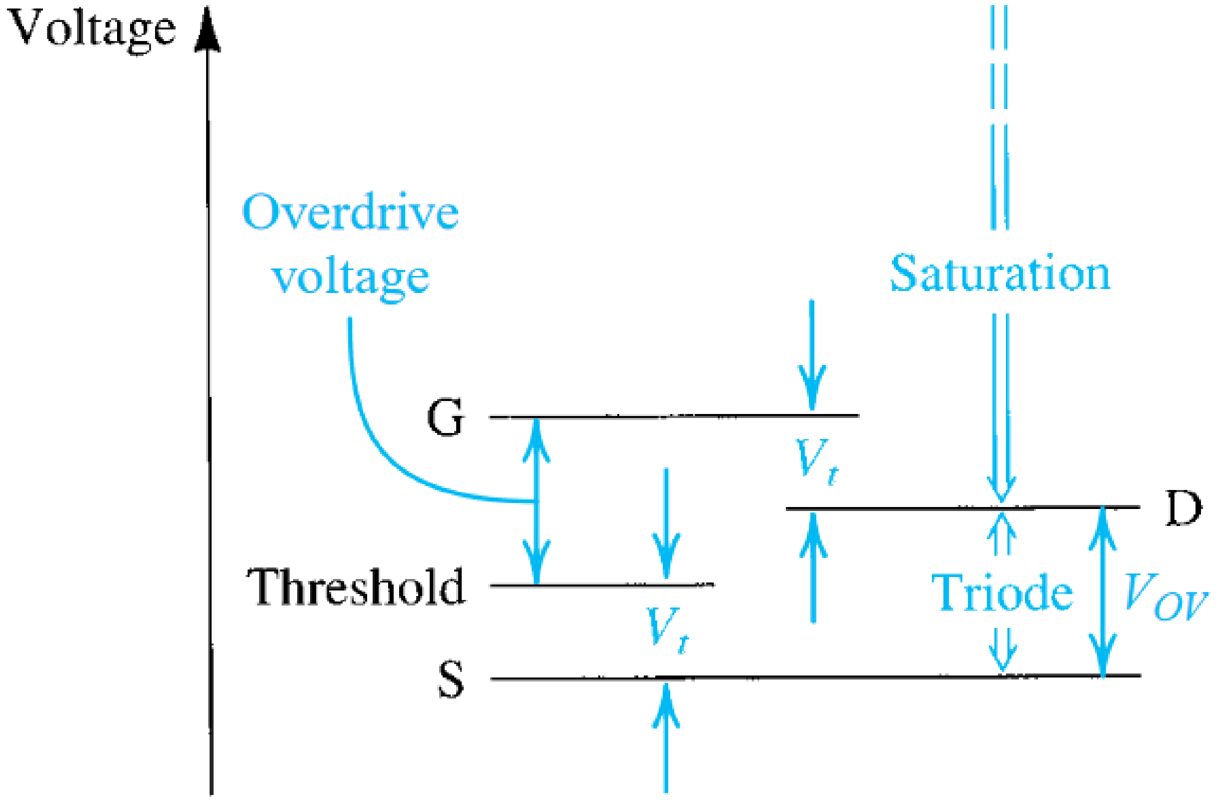
$\boldsymbol{V_{OV}}$

Indicates the available excess voltage at **gate** after forming the n-channel.

$\boldsymbol{V_T}$

The minimum voltage necessary at the **gate** terminal to form a channel.

Real MOSFET



$k_n = k_n' \frac{W}{L}$ MOSFET transconductance

v_{GS}: Gate Voltage

v_{DS}: Drain to Source Voltage

V_T: Threshold Voltage

$V_{OV} = v_{GS} - V_T$: Overdrive voltage

NMOS Triode Mode

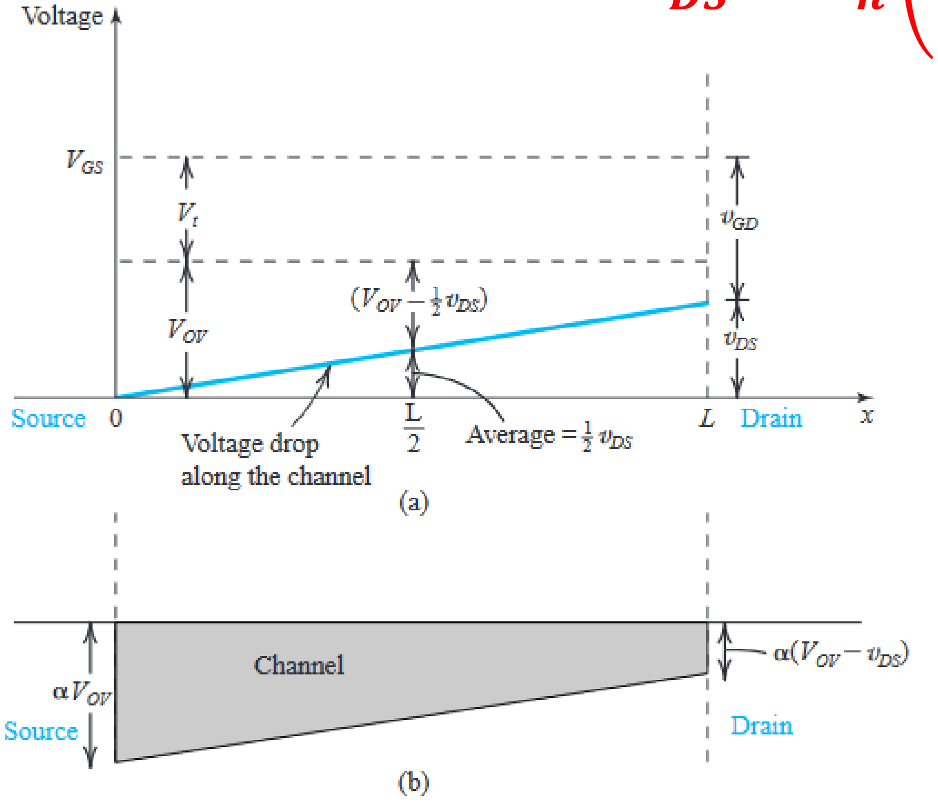
Occurs when $v_{GS} \geq V_T$ and $v_{DS} < v_{GS} - V_T$

$$I_{DS} = k_n\left(v_{GS} - V_T - \frac{1}{2}v_{DS}\right)v_{DS}$$

$$I_{DS} \propto k_n'$$

$$I_{DS} \propto \frac{W}{L}$$

$$I_{DS} \propto (V_{OV} - \frac{1}{2}v_{DS})$$



Overdrive Voltage is defined as:

$$V_{OV} = v_{GS} - V_T$$

In triode mode, average voltage across channel is actually:

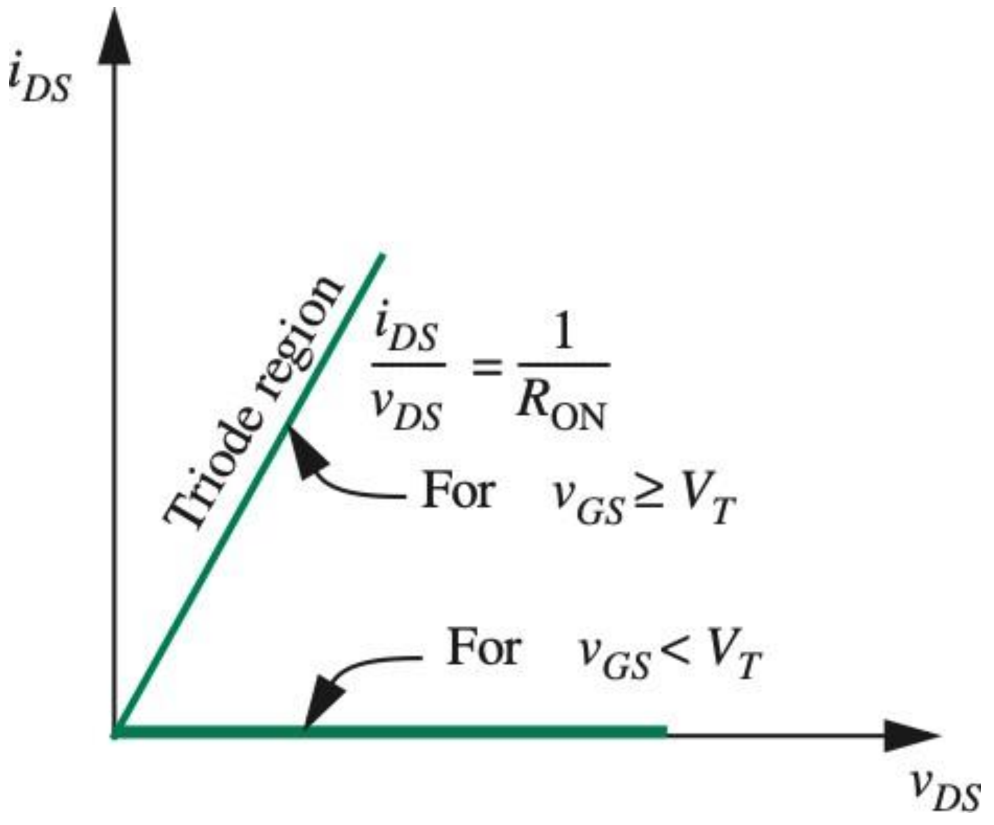
$$(V_{OV} - \frac{1}{2}v_{DS})$$

NMOS Triode Mode

$$I_{DS} = k_n' \frac{W}{L}\left(v_{GS} - V_T - \frac{1}{2} v_{DS}\right) v_{DS}$$

$$I_{DS} = \frac{1}{R_{ON}} v_{DS}$$

$$\boxed{\begin{aligned} R_{ON} &= \frac{1}{k_n' \frac{W}{L}\left(v_{GS} - V_T - \frac{1}{2} v_{DS}\right)} \\ &= \frac{1}{k_n\left(V_{OV} - \frac{1}{2} v_{DS}\right)} \end{aligned}}$$



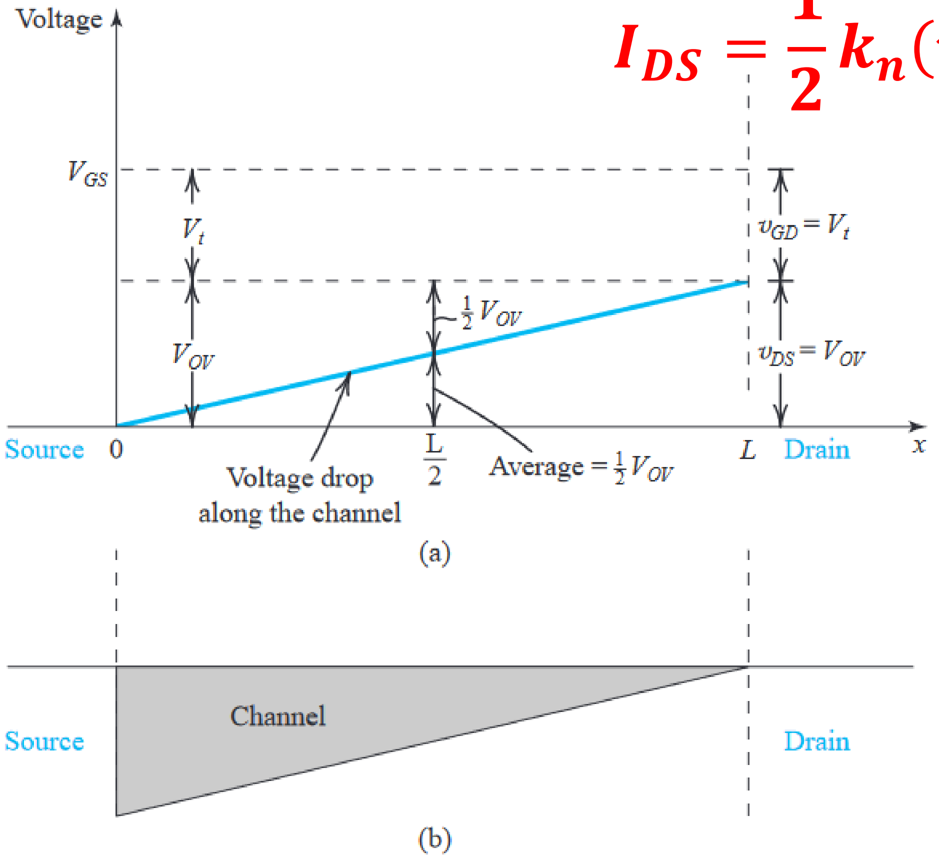
NMOS Saturation mode

Occurs when $\boldsymbol{v_{GS} > V_T}$ and $\boldsymbol{v_{DS} \geq v_{GS} - V_T}$

$$\boldsymbol{I_{DS} = \frac{1}{2} k_n (v_{GS} - V_T)^2 = \frac{1}{2} k_n V_{OV}^2}$$

$$\boldsymbol{I_{DS} \propto k_n'}$$

$$\boldsymbol{I_{DS} \propto \frac{W}{L}}$$



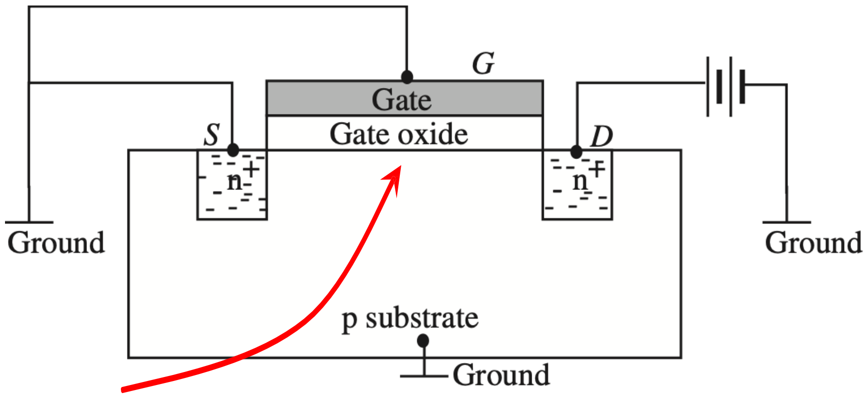
Overdrive Voltage is defined as:

$$V_{OV} = v_{GS} - V_T$$

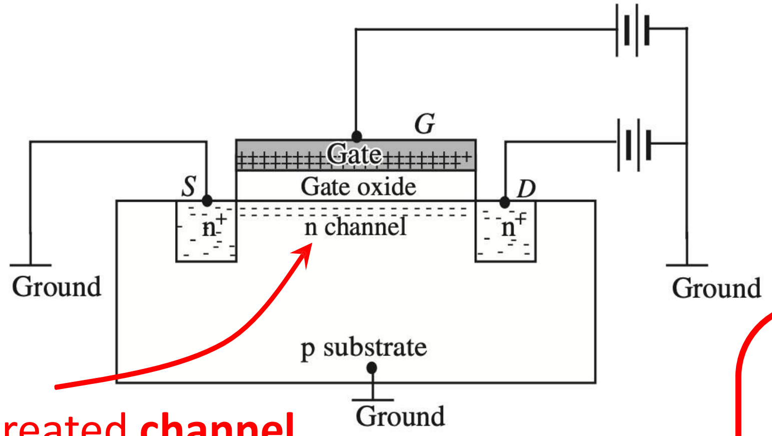
In **Saturation** mode, average voltage across channel fixed at:

$$\frac{1}{2} V_{OV}$$

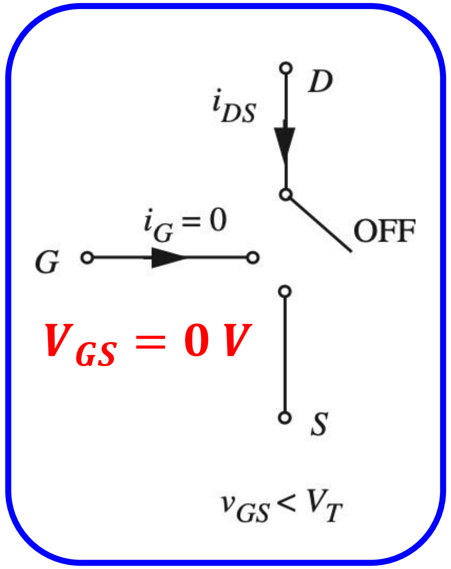
n-channel MOSFET - Summary



No channel, open ckt



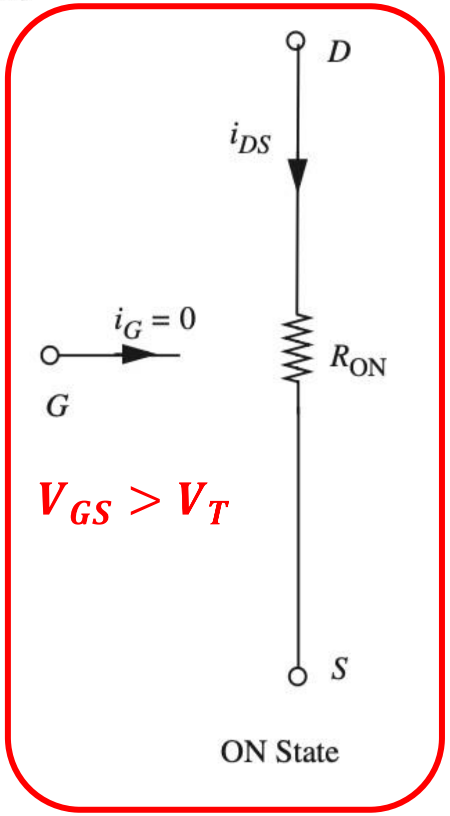
The created **channel**
will have some R
-> SR model



Cut off mode

G – Gate: Trigger terminal
S – Source: Charge carrier reservoir
D – Drain: Charge carrier sink

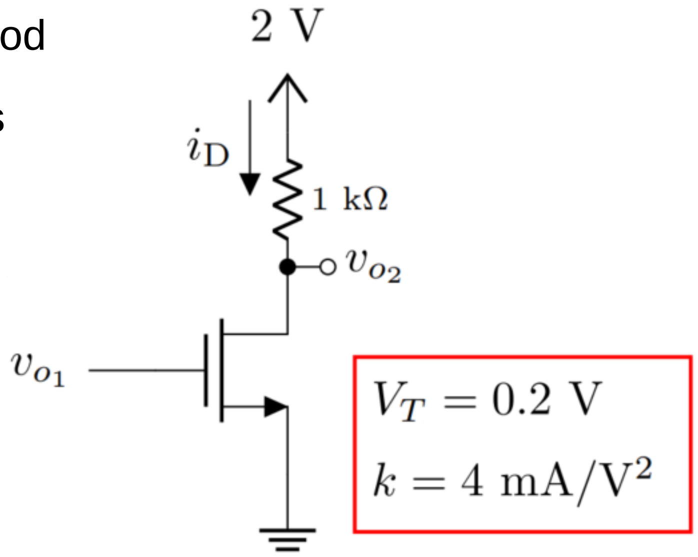
Small v_{DS}: Triode Mode
Large v_{DS}: Saturation Mode



Solving Circuits with MOSFET

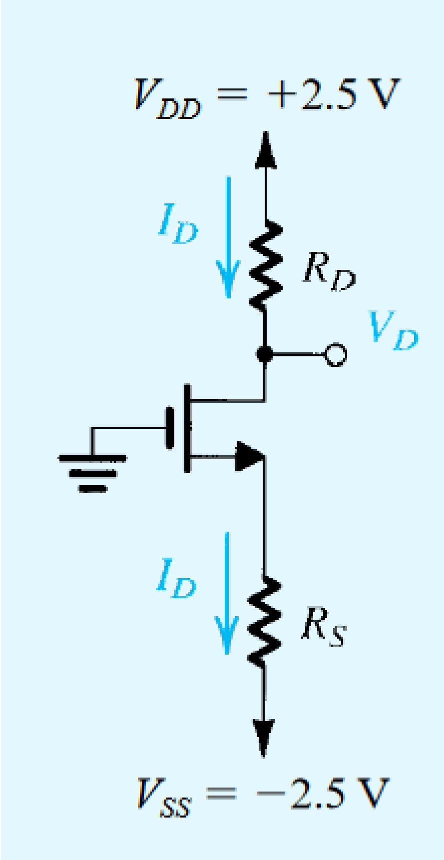
- Use **Method of Assumed State**!
- Three steps:
  - **Assume**: One of the modes (Cutoff, Triode, Saturation)
  - **Solve**: Use corresponding equation and KCL+KVL
  - **Verify**: Check if the conditions of V_{GS} and V_{DS} are satisfied. If not, repeat.
- Might need to solve quadratic equation ($ax^2 + bx + c = 0$).
- If we get two roots, choose the one that's ***favorable*** to your assumption

Analyze the circuit to find $\boldsymbol{i_D}$ and $\boldsymbol{v_{O2}}$ using the Method of Assumed State. Here, the input of the MOSFET is $\boldsymbol{v_{o1} = 1\ V}$. You must validate your assumptions.

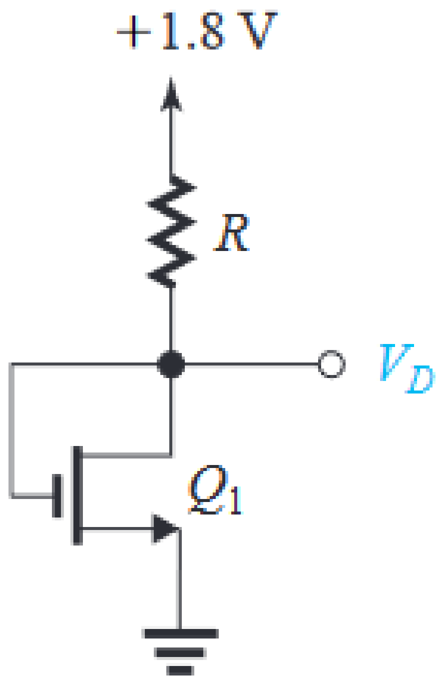


- Design the circuit, that is, determine the values of R_D and R, so that the transistor operates at $\boldsymbol{I_D} = 0.4\ \mathrm{mA}$ and $\boldsymbol{V_D} = +0.5\ \mathrm{V}$. The NMOS transistor has $\boldsymbol{V_T} = 0.7\ \mathrm{V}$, $\boldsymbol{k} = 3.2\ \mathrm{mA/V^2}$.

What is the mode of this transistor?

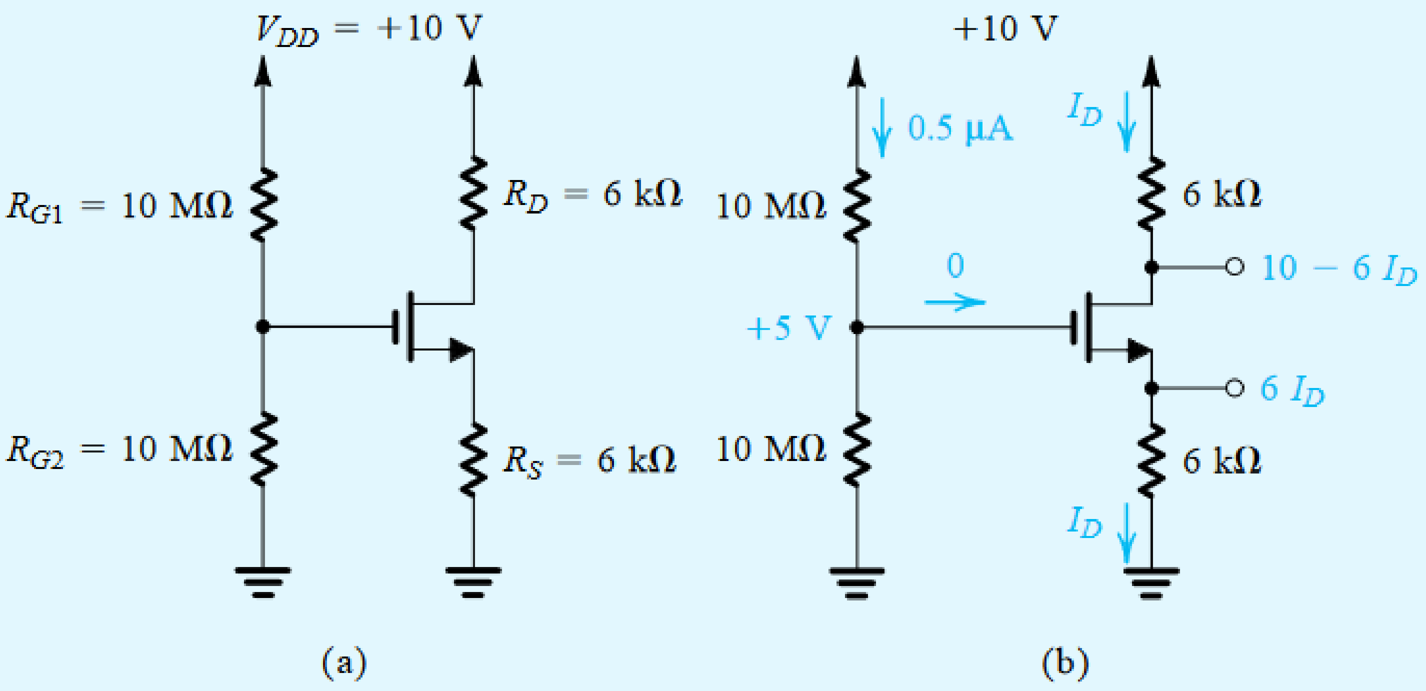


- For the circuit, find the value of R that results in $V_D = 0.8$ V. The MOSFET has $V_T = 0.5$ V, $k_n' = \mu_n C_{OX} = 0.4$ mA/V^2, $\frac{W}{L} = \frac{0.72\ \mu\text{m}}{0.18\ \mu\text{m}}$



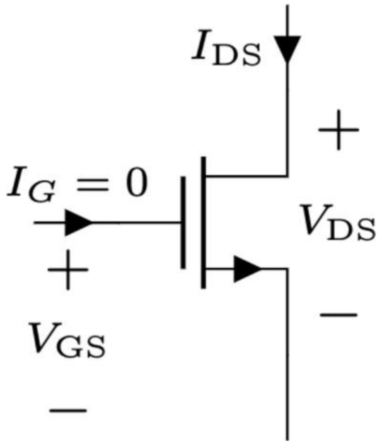
$$k_n = k_n' \frac{W}{L} = 1.6\ \text{mA/V}^2$$

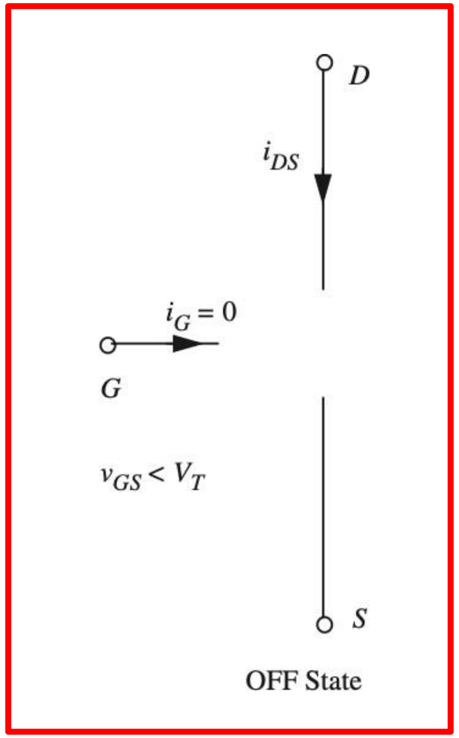
Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

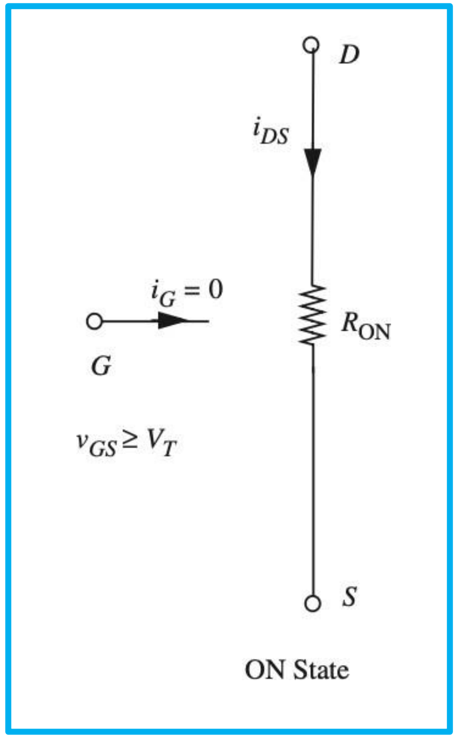


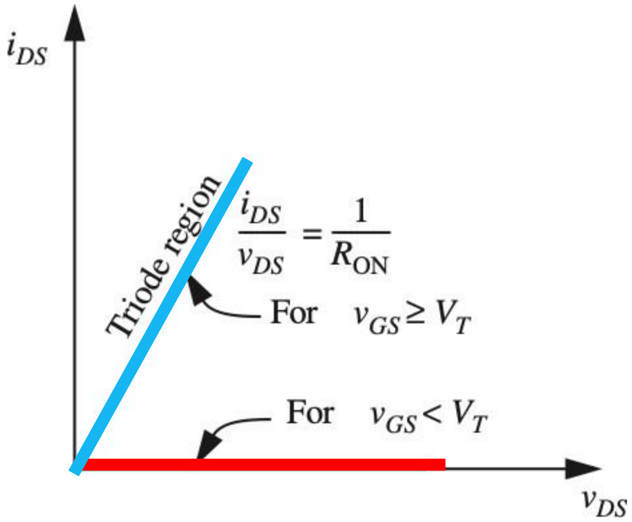
n-channel MOSFET - Summary

SR Model:









$$R_{ON} = \frac{1}{k_n(V_{OV} - \frac{1}{2}v_{DS})}$$

V_{OV}

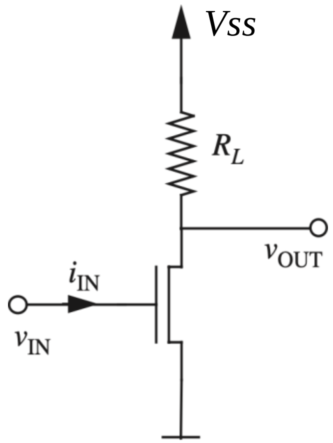
Indicates the available excess voltage at **gate** after forming the n-channel.

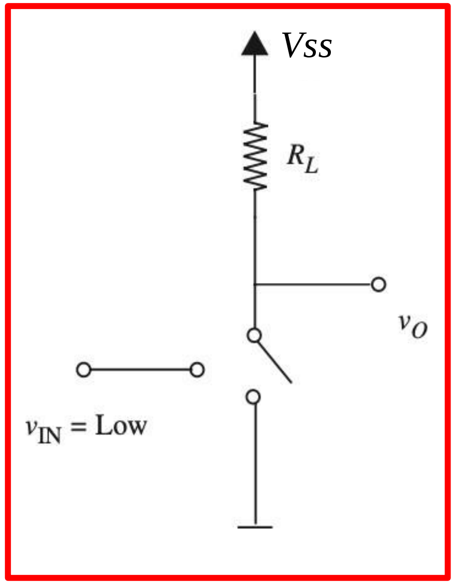
- SR model is a better approximation than S model.
- **Triode Mode exists until:** v_{DS} **<=** $(v_{GS} - V_T)$

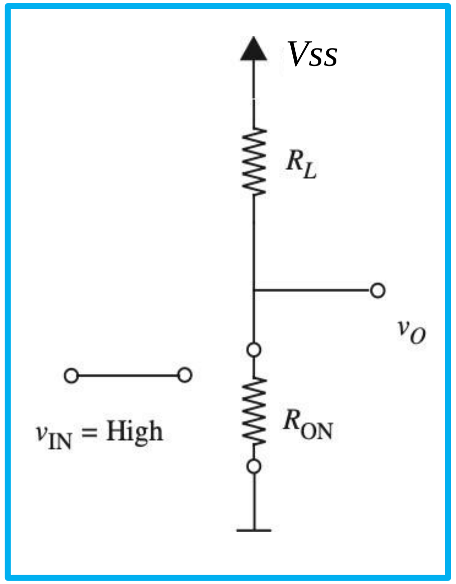
SR Model - Inverter

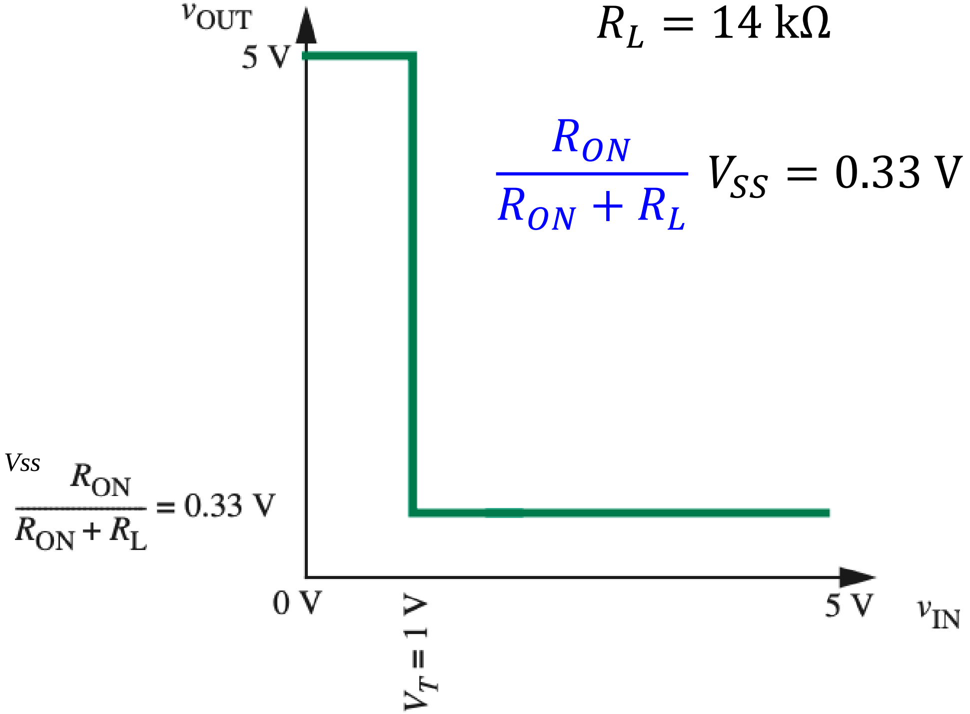
For example, If

$$V_{SS} = 5\ \text{V},$$
$$R_{ON} = 1\ \text{k}\Omega,$$
$$R_L = 14\ \text{k}\Omega$$







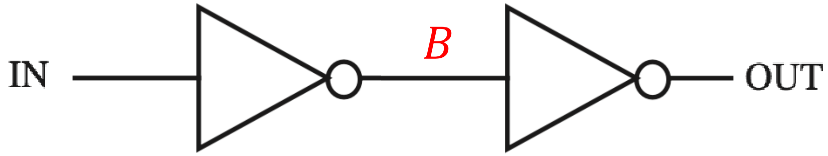


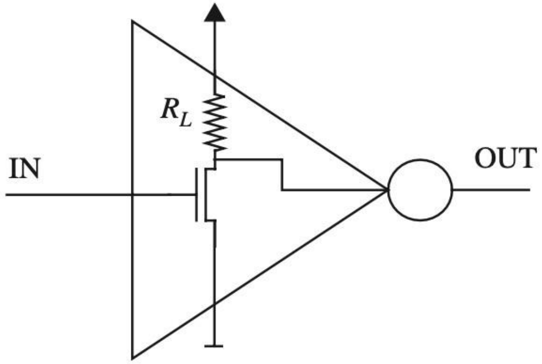
$$\frac{R_{ON}}{R_{ON} + R_L} V_{SS} = 0.33\ \text{V}$$

$$\boldsymbol{v_{o,\,HI}} = V_{SS}$$

$$\boldsymbol{v_{o,LO}} = \frac{R_{ON}}{R_{ON} + R_L} V_{SS}$$

Design of logic gates





Expected $\boldsymbol{V_T} = 0.4$ V

IN	B	OUT
Low ($V_{IN} < V_T$)	High ($5V$)	Low ($V_{OUT} = V_{OUT,Low}$)
High ($V_{IN} > V_T$)	Low ($V_{OUT,Low}$)	High (5V)

Actual

IN	B	OUT
Low ($V_{IN} < V_T$)	High ($5V$)	Low ()
High ($V_{IN} > V_T$)	Low ()	Low ()

Therefore, need to design logic gates properly such that

$$\frac{R_{ON}}{R_{ON} + R_L} V_{SS} < V_T$$

$V_T = 0.4$ V, $V_S = 5$ V, $R_{ON} = 1$ kΩ, $R_L = 9$kΩ

$$\boldsymbol{V_{OUT,HI}} = V_{SS}$$

$$\boldsymbol{V_{OUT,LOW}} = \frac{R_{ON}}{R_{ON} + R_L} V_{SS} = 5 \cdot \frac{1}{1+9} = 0.5 \text{ V}$$

Design of logic gates - Example

Assume the following values for the inverter circuit parameters: $V_S = 5\text{ V}, V_T = 1\text{ V}$, and $R_L = 10\text{ k}\Omega$. Assume, further, that $\frac{\mathbf{1}}{\boldsymbol{k_n V_{OV}}} = \mathbf{5}$ for the MOSFET. Determine a $(\frac{W}{L})$ sizing for the MOSFET so that the inverter gate output for a logical 0 is able to switch OFF the MOSFET of another inverter.

Solution:

$$V_S \cdot \frac{R_{ON}}{R_{ON} + R_L} < V_T$$

$$\Rightarrow 5\frac{R_{ON}}{R_{ON} + R_L} < 1$$

$$\Rightarrow 5R_{ON} < R_{ON} + 10$$

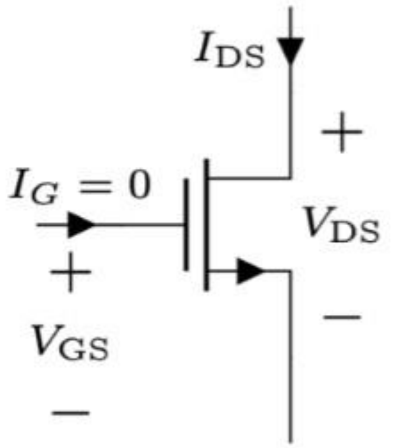
$$\Rightarrow R_{ON} < \frac{10}{4}\text{ k}\Omega = 2.5\text{ k}\Omega$$

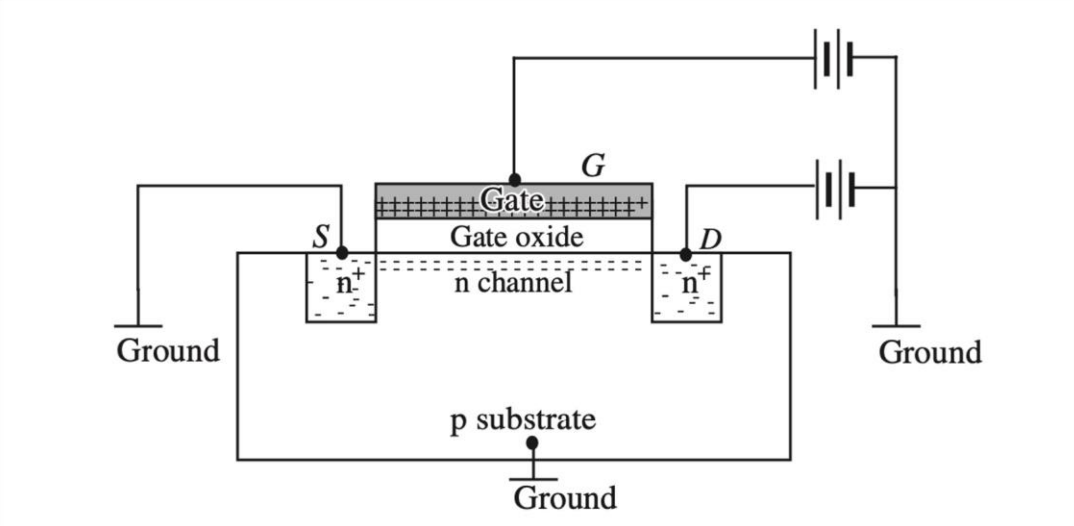
Now, $$R_{ON} = \frac{1}{k_n V_{OV}} = \frac{1}{k_n' \frac{W}{L} V_{OV}} = \frac{1}{5} \times \frac{1}{W/L}$$

Hence $$\frac{5}{W/L} < 2.5$$

$$\Rightarrow \frac{W}{L} > \frac{5}{2.5} = 2$$

Review – MOSFET





Control = $V_{GS} = V_G - V_S$ controls the IV between drain-source (I_{DS} vs V_{DS})

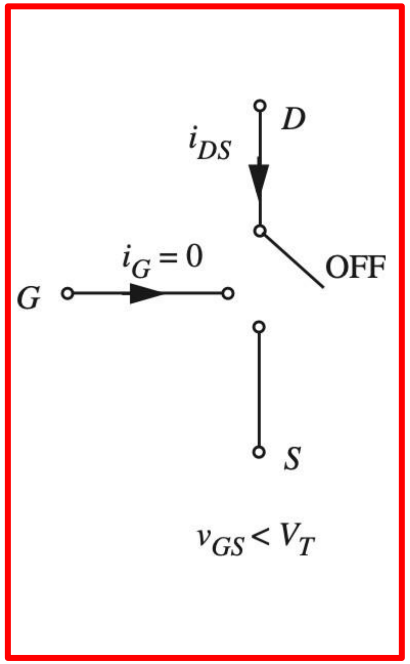
Threshold voltage = V_{T}, minimum voltage required to create the channel

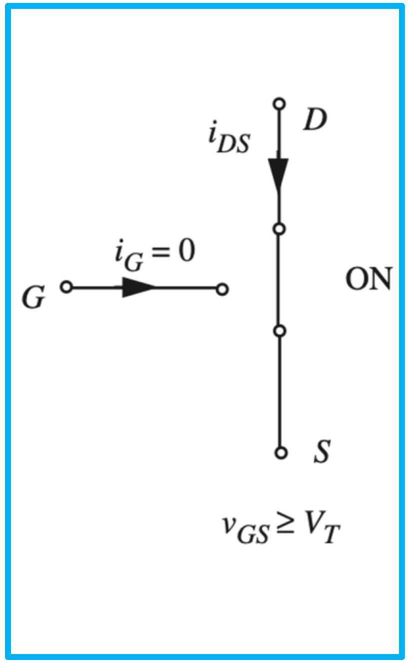
Models

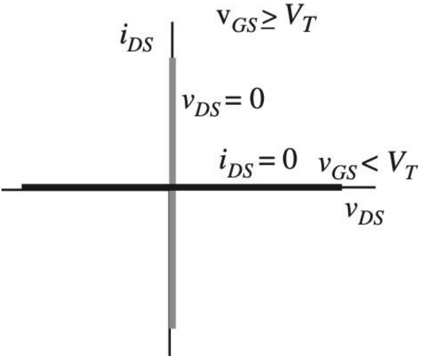
1. **S Mode**: Assumes an ideal channel with zero resistance
2. **SR Model**: Assumes finite channel resistance, R_{ON}, depends on $V_{GS} - V_T = V_{OV}$

MOSFET Linear Models

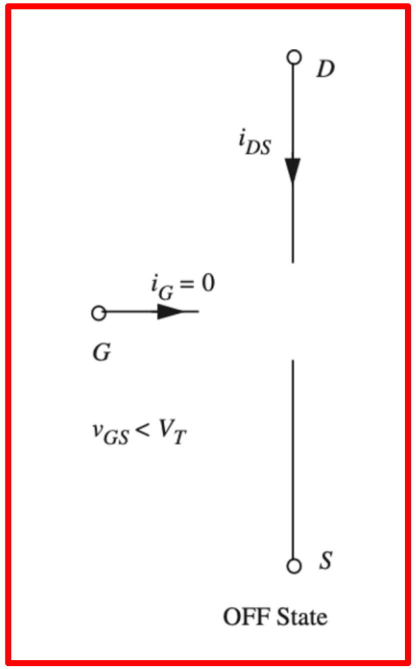
S Model

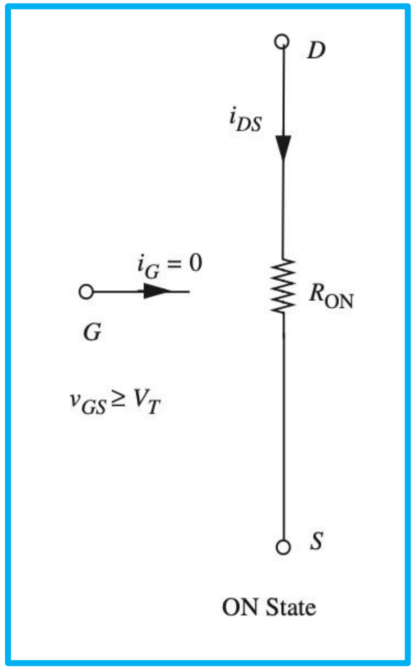


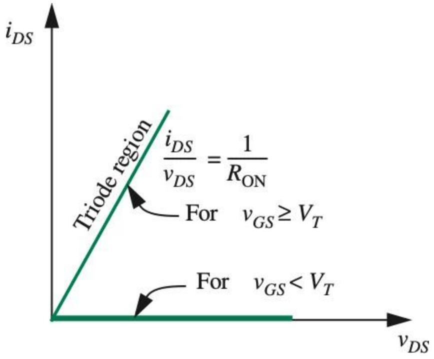




SR Model



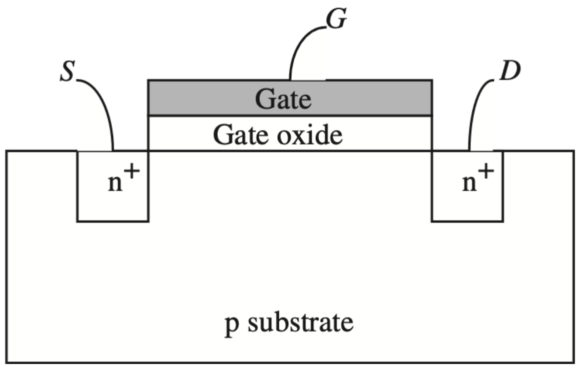


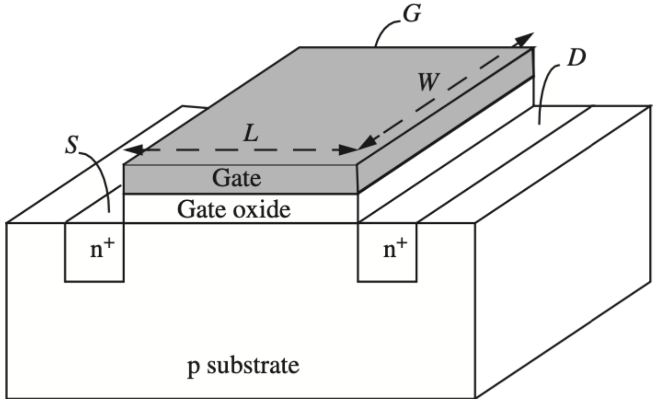


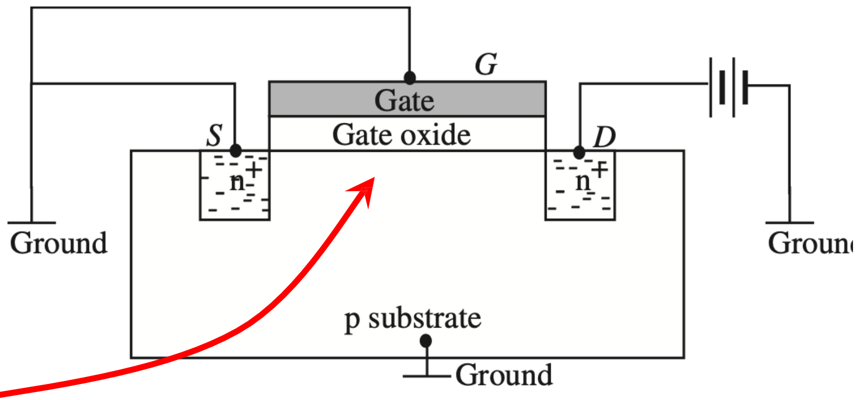
$$R_{ON} = \frac{1}{k_n' \frac{W}{L}\left(v_{GS} - V_T - \frac{1}{2} v_{DS}\right)}$$

Construction of Real MOSFET

Simplified cross section and 3D view

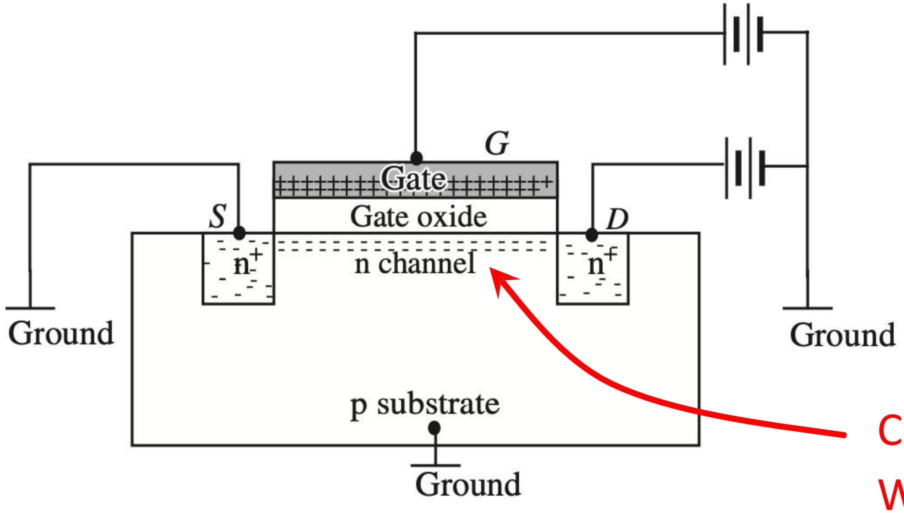






No channel, open ckt

$V_{12} = 0V$



$V_{12} > V_{\$}$

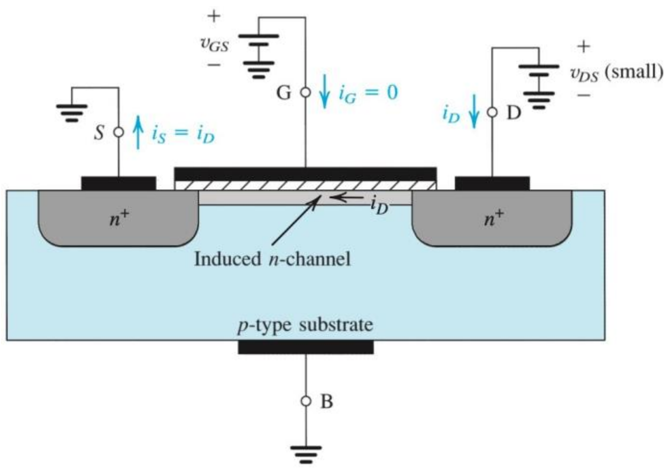
Channel created

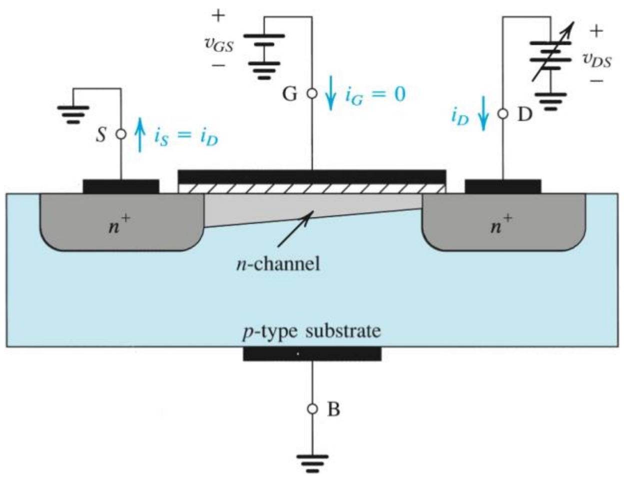
Will have some R

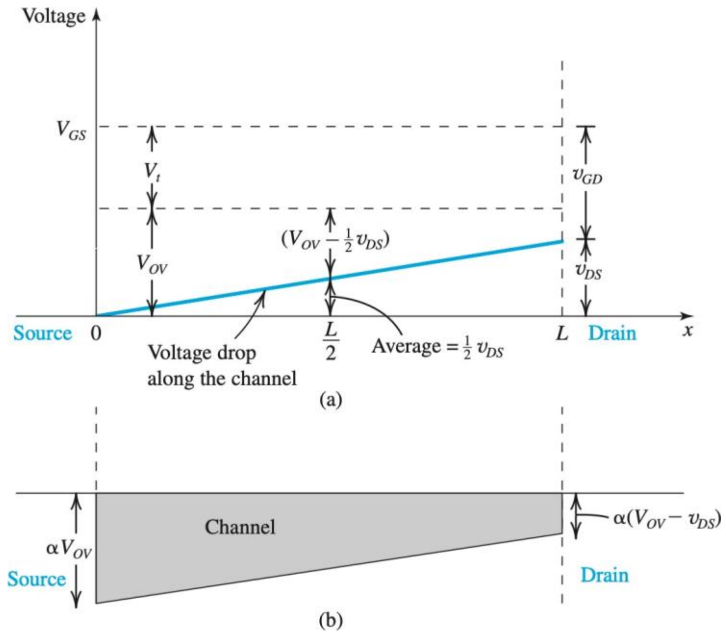
-> SR model

Real MOSFET

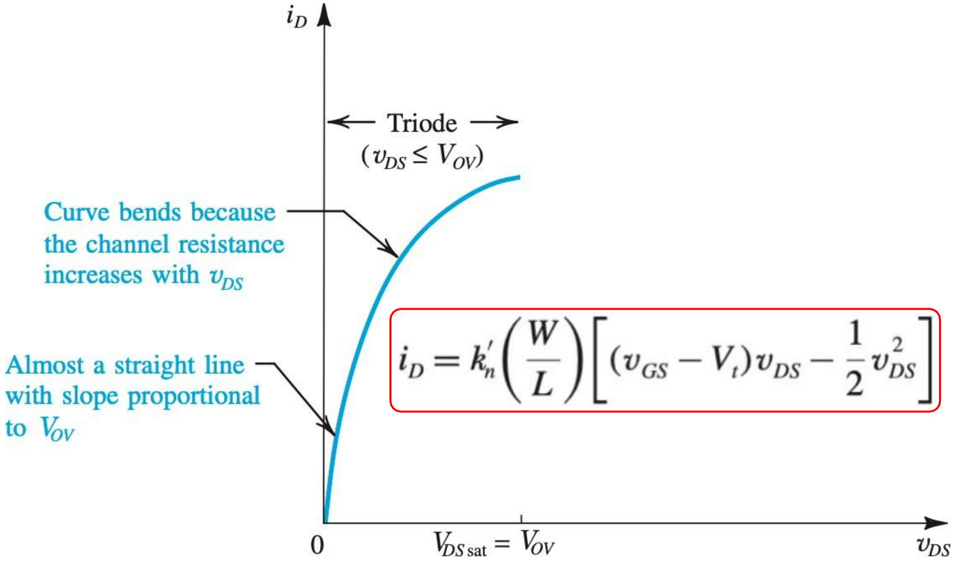
- For small V_{DS}, uniform channel, hence fixed R_{ON} therefore SR model valid.
- As V_{DS} is increased, channel becomes tapered cause $V_{GD}\downarrow$. Resistance $\uparrow$, slope $\downarrow$.
- This mode is called the **triode mode**. Condition: $V_{DS} < V_{OV}$

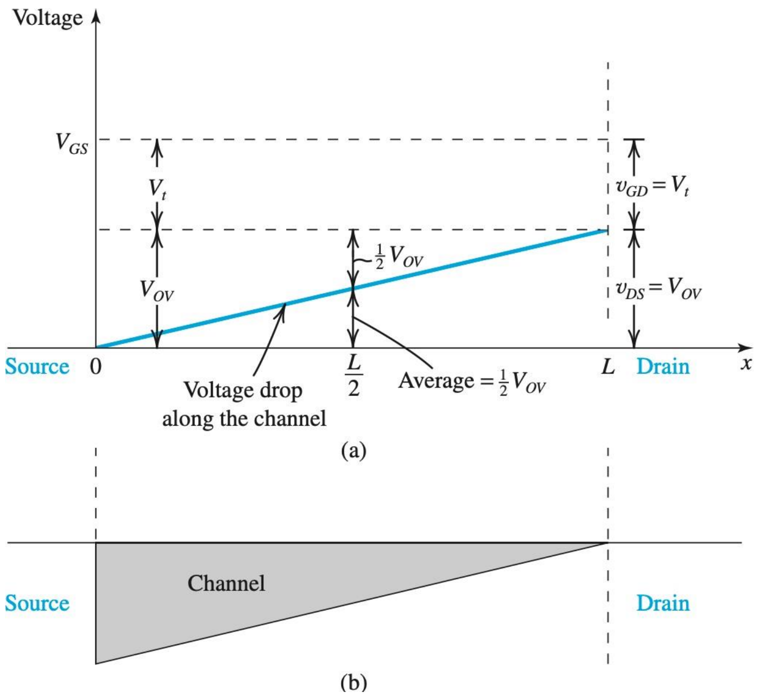


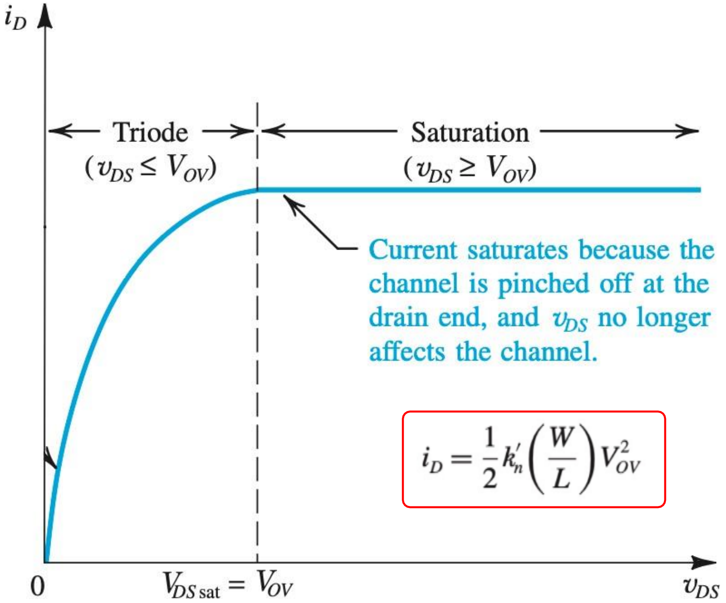




Real MOSFET

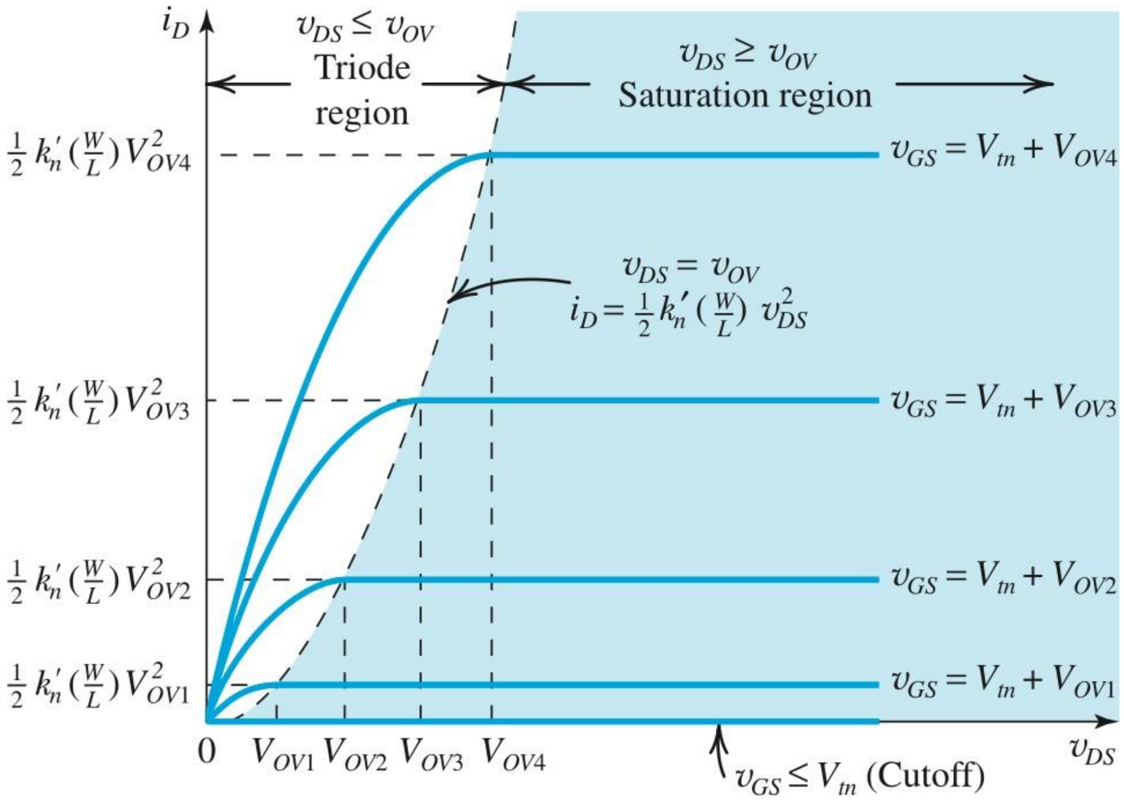






- When $V_{DS} = V_{OV}$, channel pinches off.
- Increasing V_{DS} further have no effect on channel shape. Hence, current <u>saturates</u>
- This mode is called the **saturation mode**. Condition: $V_{DS} \ge V_{OV}$
- Behaves like a **<u>current source</u>** (constant current) that depends on V_{OV}'

IV Characteristics of Real MOSFET



Mode	Condition	Equation
Cutoff	$V_{GS} < V_T$	$I_D = 0$
Triode	$V_{GS} \ge V_T$ $V_{DS} < V_{OV}$	$I_D = k[V_{OV}V_{DS} - \frac{1}{2}V_{DS}^2]$
Saturation	$V_{GS} \ge V_T$ $V_{DS} \ge V_{OV}$	$I_D = \frac{k}{2}V_{OV}^2$

$$V_{GS} - V_T = V_{OV}$$

$$k_n = \frac{k_n' W}{L}$$