Name of the experiment:

Design and Implementation of 4-bit Parallel Binary Adder.

Objective:

- For designing half and full adder
- For designing and implementing 4-bit parallel binary adder using IC-74283.

Required Components and equipments:

(i) IC – 7408 (AND)

(ii) IC – 7432 (OR)

(iii) IC – 7486 (XOR)

(iv) IC – 74283 (4-bit Binary adder)

(v) AT – 700 (Portable Analog/Digital Laboratory)

Experimental Setup:

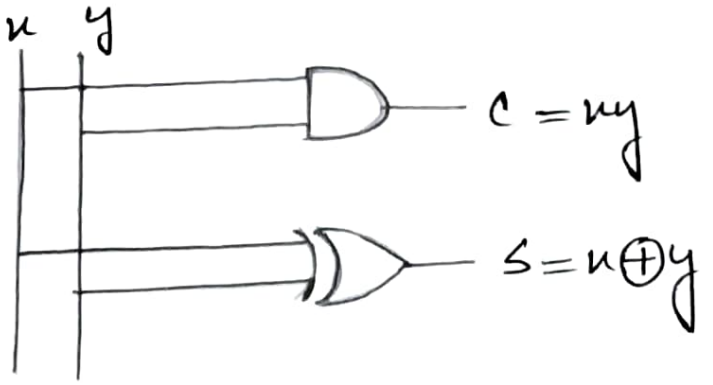

Fig: Half adder circuit

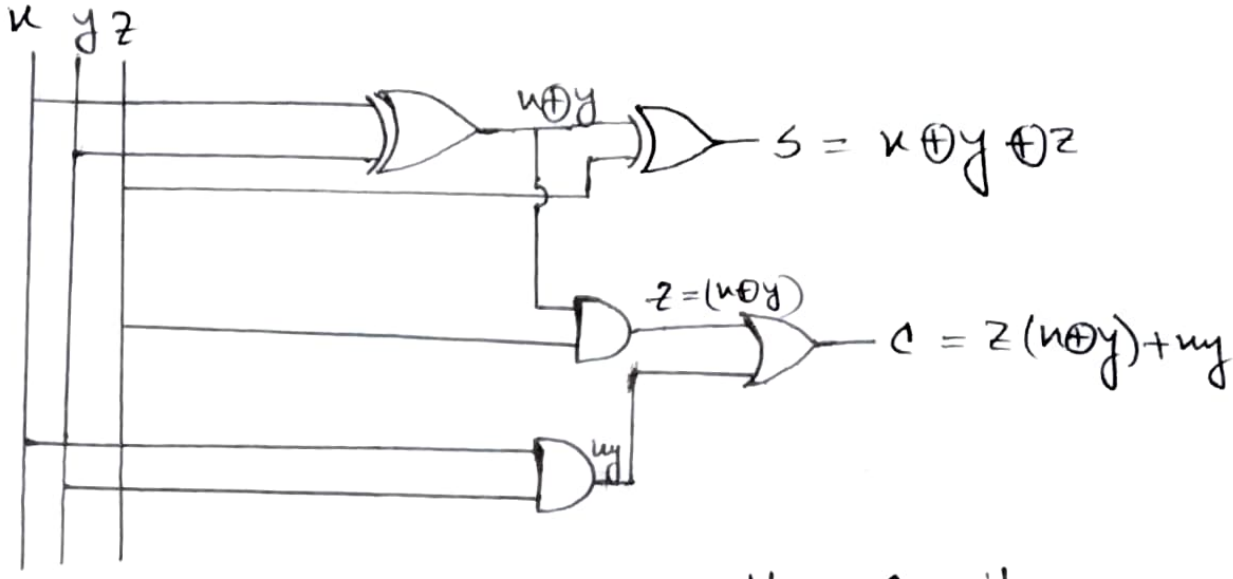

figure: Full adder circuit.

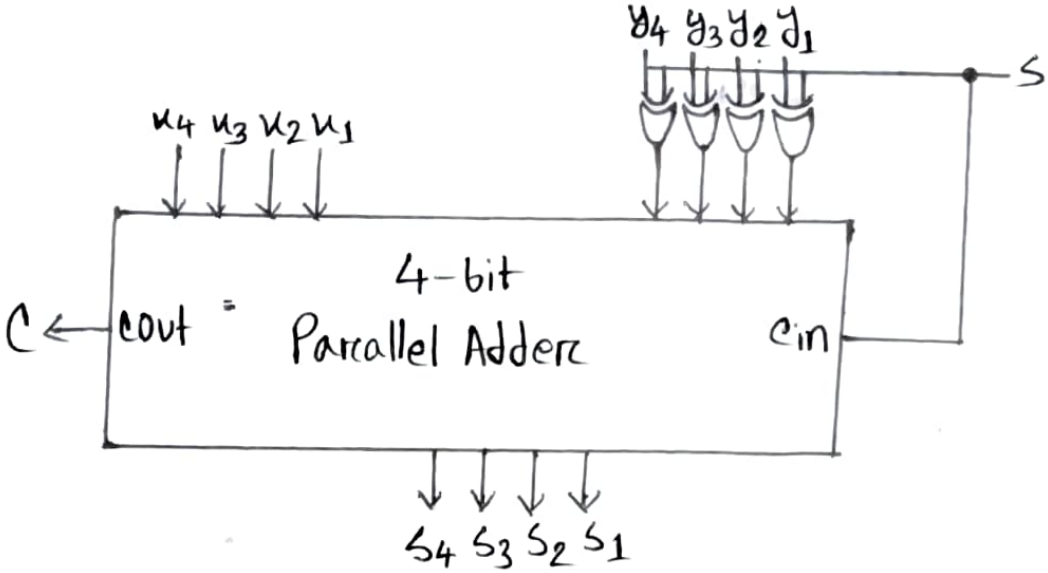

figure: 4bit Parallel Adder.

Results (Truth Table) and Discussions:

* Half adder:

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Equation: $S = x \oplus y$

$C = xy$

The half adder is able to add two single binary digits and provide an output and a carry value. One AND gate and One XOR gate is needed to create the circuit of half adder.

* Full Adder:

x	y	z	c	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Equation:

$S = x \oplus y \oplus z$

$C = z(x \oplus y) + xy$

A full adder is a combinational circuit that forms the arithmatic sum of three input bits It consists of three inputs and two outputs Two of the input variables are denoted by x & y represent the two significant bits to be added. The third input z represents the carrry of the previous lower significant position. The two outputs are designed by the symbols S and C. The binary S gives the value of the least significant bit of the sum. The binary variable C gives the output carrry.

4-bit parallel adder

A	B	Cin	Sum	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Equation:

$S_i = x_i \oplus y_i \oplus C_i$

$C_{i+1} = x_i y_i + (x_i \oplus y_i) C_i$

A binary parallel adder is a digital function that produces the arithmatic sum of two binary numbers in parallel. It consists of full adder connected in cascade, with the output carry from one full adder connected to the input of next full adder.