module four\_bits\_bcd\_adder(a,b,c\_in,s,carry);

input [3:0] a,b;

input c\_in;

output [3:0] s;

output carry;

reg [4:0] s1;

reg [3:0] s;

reg carry;

always @(a,b,c\_in)

begin

s1 = a+b+c\_in;

if(s1 > 9)

begin

s1 = s1+6;

carry = 1;

s = s1[3:0];

end

else

begin

carry = 0;

s = s1[3:0];

end

end

endmodule