VGA Controller Project

1. Introduction

This project aims to create a VGA display controller that supports three different resolutions: 640x480, 1024x768, and 1280x1024. Implemented in VHDL, the controller allows the user to toggle between resolutions using hardware buttons. Each resolution has its own pixel clock frequency and synchronization parameters to meet VGA standards, which are managed by a custom Clock Divider IP core. The final design produces stable video output with accurate RGB, `hsync`, and `vsync` signals across all three resolutions.

2. Resolution 1: 640x480

The 640x480 resolution is a standard VGA display mode with a 25.175 MHz pixel clock, generating a 60 Hz refresh rate. This resolution is often used as a default setting due to its lower resource demands.

VGA Timing Parameters

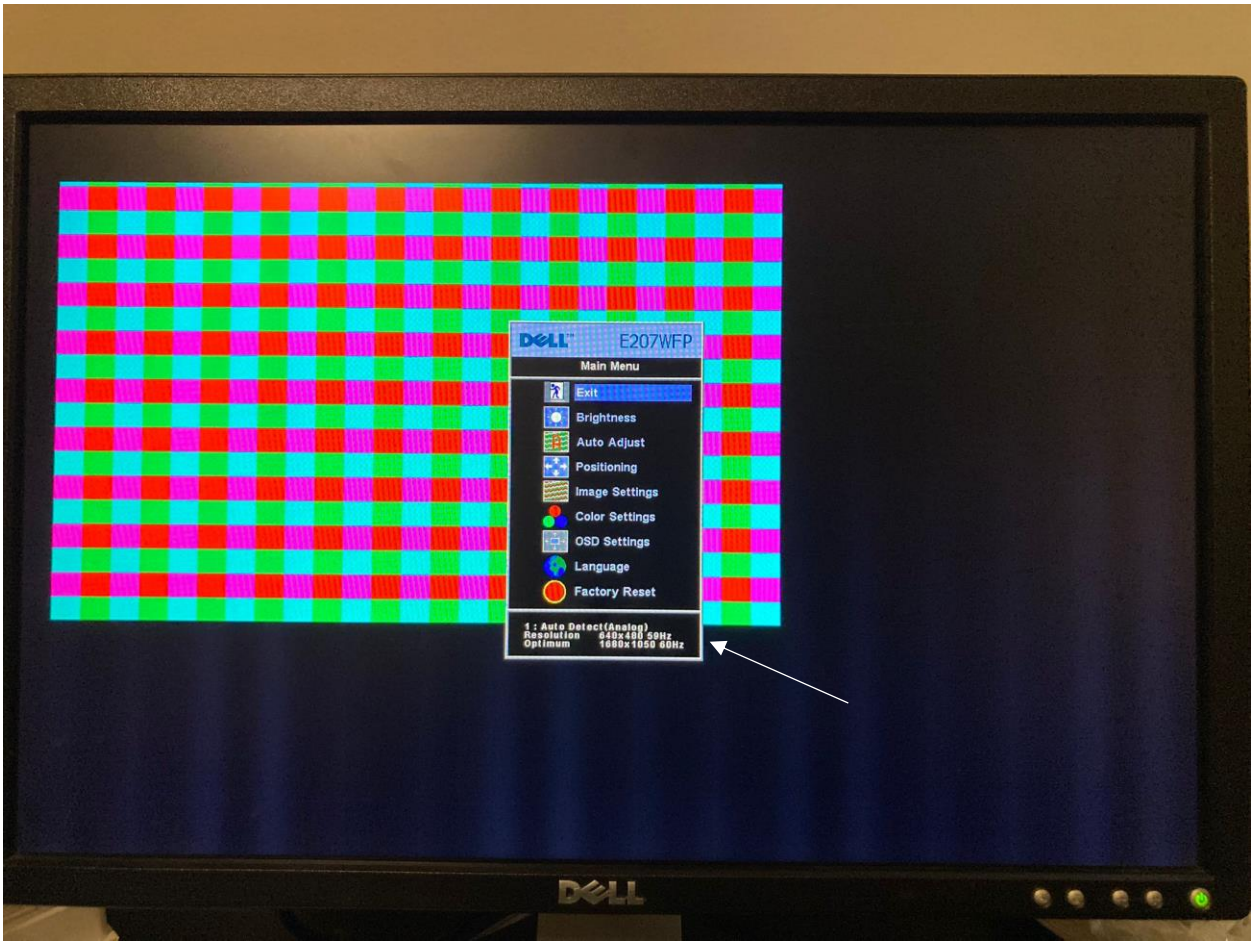
Horizontal Pixels: 800 (640 active display, 160 sync/back porch)

Vertical Lines: 525 (480 active display, 45 sync/back porch)

Pixel Clock: 25.175 MHz

The horizontal and vertical synchronization signals (`hsync` and `vsync`) are managed by counters. The active display region is determined by comparing these counters to the timing parameters, generating a `vidon` signal for active pixels.

The 640x480 module uses two counters: one for horizontal timing (counts each pixel across a line) and one for vertical timing (counts each line in a frame). When the counters reach preset values for synchronization, they reset, and a new frame starts. This timing generates stable `hsync`, `vsync`, and RGB output signals.



3. Resolution 2: 1024x768

1024x768 is a higher resolution than 640x480, with a 65 MHz pixel clock. This resolution requires increased horizontal and vertical timing counts to accommodate the higher pixel density and refresh rate.

VGA Timing Parameters

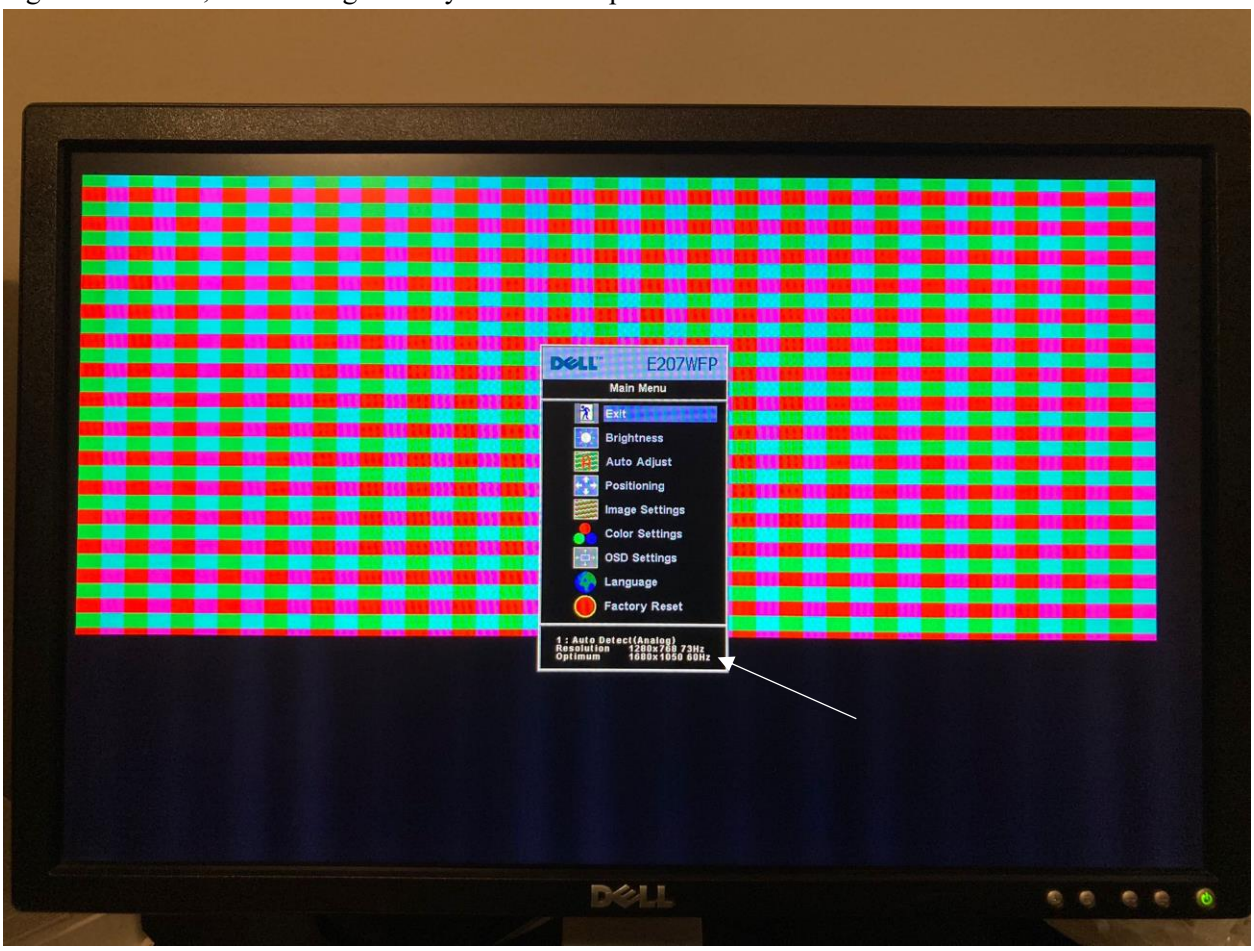
Horizontal Pixels: 1344 (1024 active display, 320 sync/back porch)

Vertical Lines: 806 (768 active display, 38 sync/back porch)

Pixel Clock: 65 MHz

Similar to 640x480, the horizontal and vertical counters manage synchronization signals based on timing parameters specific to 1024x768 resolution. This setup allows the VGA module to display a stable image with `hsync`, `vsync`, and `vidon` signals for active display regions.

The 1024x768 module adjusts the counter parameters for both horizontal and vertical counts to reflect the increased pixel and line counts. This configuration ensures the output aligns with VGA standards for the higher resolution, maintaining stability across multiple frames.



4. Resolution 3: 1280x1024

1280x1024 resolution provides the highest pixel density in this design, requiring a pixel clock frequency of 108 MHz. This resolution is typical for applications needing greater detail and fidelity.

VGA Timing Parameters

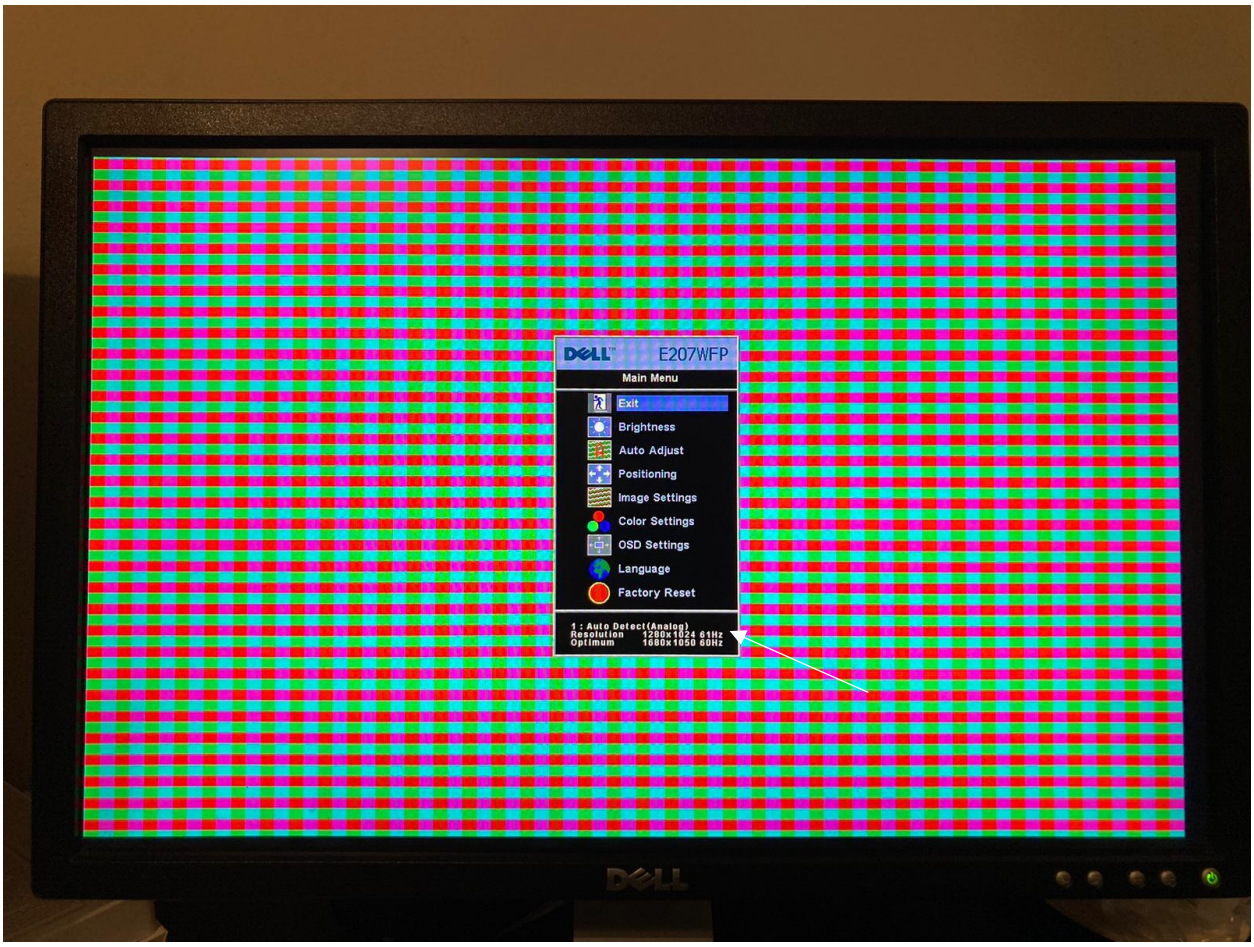
Horizontal Pixels: 1688 (1280 active display, 408 sync/back porch)

Vertical Lines: 1066 (1024 active display, 42 sync/back porch)

Pixel Clock: 108 MHz

The module uses horizontal and vertical counters with timing values specific to 1280x1024 resolution. This setup produces correct `hsync`, `vsync`, and `vidon` signals for a stable image, even with the higher pixel clock requirements.

In the 1280x1024 module, the horizontal and vertical counters operate with larger timing constants to accommodate the increased pixel density and higher pixel clock frequency. This ensures that the `hsync` and `vsync` signals are aligned for smooth, flicker-free output.



5. Button Handling

The VGA controller includes button inputs for adjusting resolution. Three buttons control resolution selection: one to increase resolution, one to decrease it, and a reset button to return to 640x480.

Each button input is debounced using a counter-based logic to filter out mechanical noise. Only stable button presses trigger a resolution change, preventing unintentional toggling.

Each button is assigned a unique function:

Button 0: Increases resolution.

Button 1: Decreases resolution.

Button 3: Resets resolution to 640x480.

The button state machine tracks which resolution is active and updates the `res_sel` signal, which selects the appropriate VGA timing module and pixel clock frequency.

6. Clock Divider IP

To support different VGA resolutions, the design requires three pixel clock frequencies (25.175 MHz, 65 MHz, and 108 MHz). The Clock Divider IP generates these frequencies from a 100 MHz system clock.

Clock Frequencies

25.175 MHz: Required for 640x480 resolution.

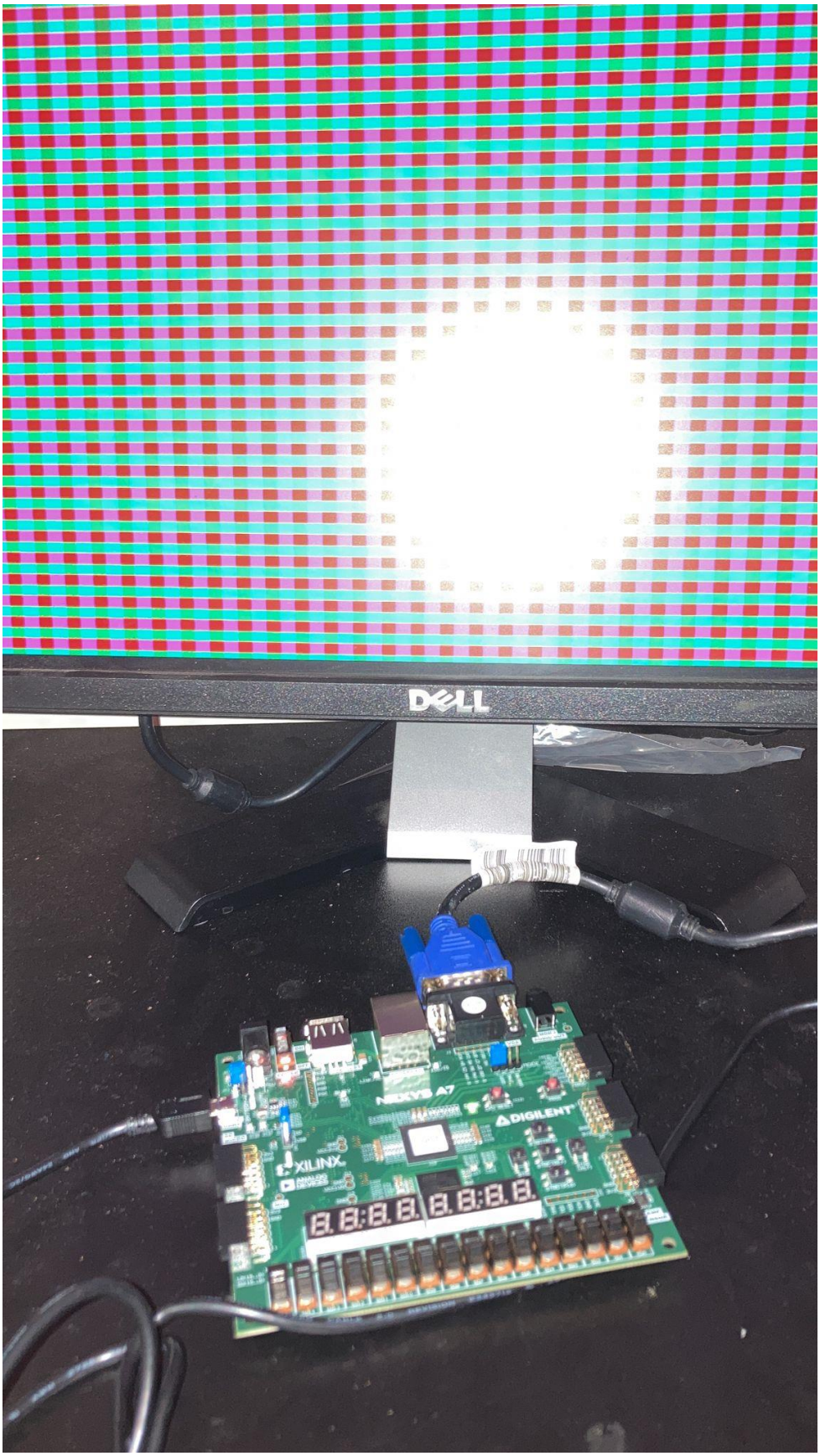
65 MHz: Required for 1024x768 resolution.

108 MHz: Required for 1280x1024 resolution.

The Clock Divider IP, implemented using `clk_wiz`, outputs all three frequencies. A multiplexer controlled by the `res_sel` signal dynamically selects the pixel clock. This configuration allows smooth switching between resolutions without interrupting the VGA sync signals.

7. Hardware Implementation

Implementing the VGA display controller on the Nexys A7 FPGA board involved configuring the hardware to interface correctly with VGA output and control inputs. The design was synthesized and deployed onto the Nexys A7, requiring the assignment of specific pins for VGA signals and user button controls in the XDC file. VGA pins for horizontal and vertical synchronization, as well as red, green, and blue color channels, were mapped according to the Nexys A7's pinout, ensuring the display generated consistent resolutions across 640x480, 800x600, and 1024x768 modes. Button handling, used for toggling resolutions, required carefully mapping the on-board push buttons in the XDC file to allow responsive, real-time control during operation.


DELL
NEXYS A7
DIGILENT
XILINX

8. Challenges

Ensuring glitch-free switching was critical, so the clock switching logic includes synchronization to prevent glitches or flickering on the screen during resolution changes.

9. Conclusion

This VGA controller project demonstrates a modular and scalable approach to supporting multiple resolutions on FPGA. The design achieves stable video output with accurate synchronization signals for each resolution. Button handling with debouncing allows for reliable resolution toggling, and the Clock Divider IP efficiently provides the required pixel clock frequencies for each resolution.

The modular design allows for further expansion, such as adding additional resolutions or integrating additional display features. Overall, the project meets VGA standards across resolutions and provides a versatile platform for video output in FPGA applications.