**Sri Sivasubramaniya Nadar College of Engineering**

 **(An Autonomous Institution, Affiliated to Anna University, Chennai)**

Department of Computer Science and Engineering

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| **Degree & Branch** | Five Year Integrated M.Tech (CSE) | | | **Semester** | II |
| **Subject Code & Name** | |  | | --- | | **ICS1201 - Fundamentals of Computer Organization and Architecture** | | | | | |
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## **Problem Statement**

A processor has 19-bit address lines and needs to interface with:

* Two **64K x 8 ROM** chips
* Four **32K x 8 RAM** chips

You are required to:

1. List the **MSI devices** used for memory interfacing.
2. Construct the **memory interface diagram**, specify address lines used by each chip, and identify the **address ranges** in hexadecimal.
3. Check for **mirror addressing** and clearly explain if any mirror address ranges exist.

## **Q1: MSI Devices Required for Designing the Circuit (5 Marks)**

### ****Explanation****

Medium Scale Integration (MSI) devices help in decoding address lines and selecting the right memory chip. The following devices are used:

### ****List of MSI Devices****

1. **3-to-8 Line Decoder (e.g., 74LS138)**
   * **Purpose**: Selects one of eight memory blocks.
   * **Inputs**: A16, A17, A18
   * **Used to select**: ROM1, ROM2, and the RAM block
2. **2-to-4 Line Decoder (e.g., 74LS139)**
   * **Purpose**: Selects one of the four RAM chips
   * **Inputs**: A15, A16
   * **Enable input**: Connected to output Y2 of the 3-to-8 decoder
3. **AND Gates (Optional)**
   * **Purpose**: Combine decoder outputs with control signals (RD, WR) to ensure correct chip selection
4. **Buffers (Optional, e.g., 74LS245)**
   * **Purpose**: Manage bidirectional flow of data on data bus D0–D7

## **Q2: Memory Interface Diagram and Address Range (30 Marks)**

### ****Step 1: Understanding the Address Lines****

* Processor has **19 address lines** → can address up to **219 = 524,288 bytes = 512 KB**
* **ROM chips (64K x 8)** require **A0–A15** = 64 KB each
* **RAM chips (32K x 8)** require **A0–A14** = 32 KB each

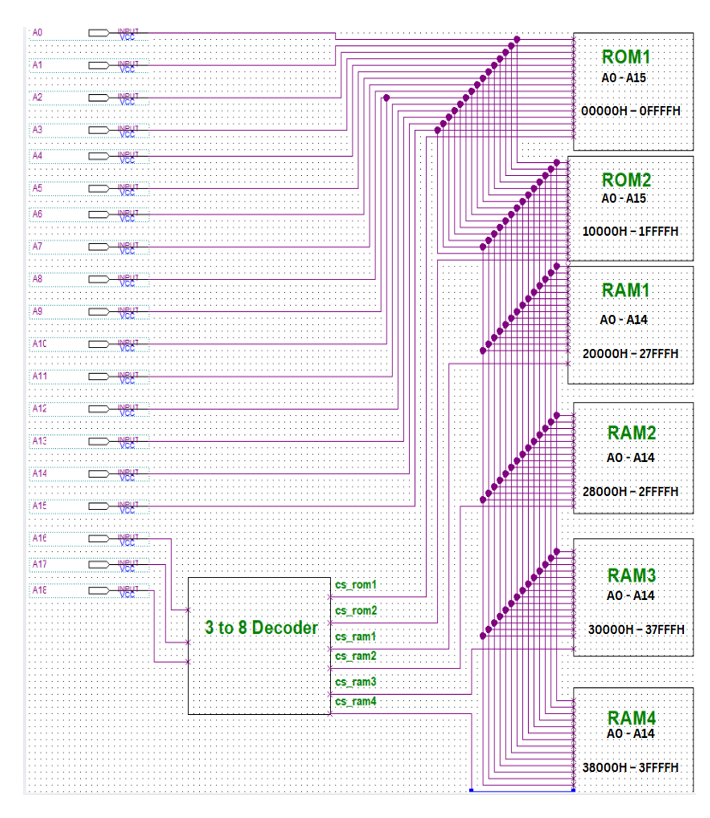
### ****Step 2: Chip Selection Strategy****

* Use **A16, A17, A18** with a **3-to-8 decoder** to generate 8 output lines
* Assign:
  + **Y0 → ROM1**
  + **Y1 → ROM2**
  + **Y2 → RAM Block** (Enabled to further decode 4 RAMs)
* Use **A15 and A16** with a **2-to-4 decoder** to select each RAM chip inside the RAM block (Only when Y2 = 1)

### ****Step 3: Address Range Calculation****

| **Chip** | **Size** | **Address Lines Used** | **Select Signal (Binary A18–A16)** | **Address Range (Hex)** |
| --- | --- | --- | --- | --- |
| ROM1 | 64K x 8 | A0–A15 | 000 | 00000H – 0FFFFH |
| ROM2 | 64K x 8 | A0–A15 | 001 | 10000H – 1FFFFH |
| RAM1 | 32K x 8 | A0–A14 | 0100 | 20000H – 27FFFH |
| RAM2 | 32K x 8 | A0–A14 | 0101 | 28000H – 2FFFFH |
| RAM3 | 32K x 8 | A0–A14 | 0110 | 30000H – 37FFFH |
| RAM4 | 32K x 8 | A0–A14 | 0111 | 38000H – 3FFFFH |

### ****Step 4: Memory Interface Diagram****



**Textual Description of the Block Diagram:**

[Processor]

| Address Bus: A0–A18

| Data Bus: D0–D7

| Control Signals: RD, WR

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|---> [3-to-8 Decoder (74LS138)]

| Inputs: A16, A17, A18

| Outputs:

| Y0 → CS\_ROM1

| Y1 → CS\_ROM2

| Y2 → Enable for RAM block

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|---> [2-to-4 Decoder (74LS139)]

Inputs: A15, A16

Enable: Y2 from 3-to-8 Decoder

Outputs:

Y0 → CS\_RAM1

Y1 → CS\_RAM2

Y2 → CS\_RAM3

Y3 → CS\_RAM4

Each chip connects:

- Address Lines: A0–A15 for ROM, A0–A14 for RAM

- Data Bus: D0–D7

- Control: RD for ROM, RD/WR for RAM

## **Q3: Analysis of Mirror Address Ranges (5 Marks)**

### ****What is Mirror Addressing?****

Mirror address ranges occur when higher address lines are **not fully decoded**, causing **repetition** of address blocks. This can cause **unintended access** to memory.

### ****Check for Mirror Addressing****

* Total Address Lines: A0 to A18 (19 lines)
* **ROM** uses A0–A15 internally, with A16–A18 for chip selection → **Fully decoded**
* **RAM** uses A0–A14 internally, with A15–A18 for chip selection → **Fully decoded**
* Since **all 19 address lines are decoded**, there are **no mirror address ranges**.

### ****Mirror Address Table****

| **Chip** | **Main Address Range** | **Mirror Address Range** |
| --- | --- | --- |
| ROM1 | 00000H – 0FFFFH | None |
| ROM2 | 10000H – 1FFFFH | None |
| RAM1 | 20000H – 27FFFH | None |
| RAM2 | 28000H – 2FFFFH | None |
| RAM3 | 30000H – 37FFFH | None |
| RAM4 | 38000H – 3FFFFH | None |

### ****Conclusion****

* All 19 address lines are utilized in decoding.
* Each memory block is uniquely addressed.
* **No mirror addressing exists.**

## **Final Conclusion**

This memory interfacing design for a processor with 19 address lines successfully connects:

* **Two 64K x 8 ROM chips**
* **Four 32K x 8 RAM chips**

By using **MSI devices** such as a **3-to-8 decoder (74LS138)** and a **2-to-4 decoder (74LS139)**, the design ensures:

* **Unique address ranges** for all memory chips
* **No overlap** or mirror addressing
* **Efficient and organized decoding**

Thus, the system is fully functional, reliable, and logically designed for error-free operation.

**Learning Outcome**

* Understood how to interface ROM and RAM with a processor using address decoding.
* Learned to use 3-to-8 and 2-to-4 decoders for memory chip selection.
* Calculated address ranges and assigned them without overlaps.
* Identified and avoided mirror addressing by full address line decoding.
* Gained clarity on memory mapping and chip select logic in hardware design.