**COURSE CODE COURSE TITLE L T P E C**

**ICS1201**

**FUNDAMENTALS OF COMPUTER**

**ORGANIZATION AND ARCHITECTURE**

**3 0 0 0 3**

**OBJECTIVES**

To learn the basic structure and operations of a computer

To understand and develop proficiency in the design and implementation of Arithmetic and

Logic Unit (ALU), fixed-point and floating-point arithmetic units

To design and implement a MIPS processor with a pipelined datapath and control

implementation

To gain a comprehensive understanding of memory hierarchies, cache systems, virtual

memories, and effective communication with input/output (I/O) devices in computer systems.

To understand parallelism and multi-core processors.

**UNIT I COMPUTER ARCHITECTURE: HISTORY, TRENDS, PERFORMANCE 9**

Introduction; Historical Perspective of Computers; Defining Computer Architecture; Trends in Technology;

Trends in Power and Energy in Integrated Circuits; Dependability; Functional Units – Basic Operational

Concepts – Performance; MIPS Instructions: Operations, Operands –Instruction representation – Logical

operations – Decision making; Addressing modes; Parallelism and Instructions: Synchronization

**UNIT II COMPUTER ARITHMETIC 9**

Addition and subtraction; Multiplication; Division; Floating Point Representation: Floating point Operations,

Parallelism and Computer Arithmetic: Subword Parallelism

**UNIT III PIPELINING AND CONTROL UNIT 9**

Processor: MIPS implementation - Building a datapath; Control implementation scheme; Pipelining:

Pipelined datapath and control – Handling data hazards & Control hazards – Static Branch Prediction, Dynamic

Branch Prediction,– Exceptions; Instruction-Level Parallelism: Concepts and Challenges; Reducing Branch

Costs with Advanced Branch Prediction

**UNIT IV MEMORY & I/O SYSTEMS 9**

Memory Hierarchy; Memory technologies; Cache Memory: Basics and cache mapping techniques; Measuring

and improving cache performance; Virtual Memory: TLBs; Parallelism and Memory Hierarchy: Redundant

Arrays of Inexpensive Disks; Accessing I/O devices – Interrupts; Direct memory access; Bus structure – Bus

operation – Arbitration; Interface circuits; USB.

**UNIT V PARALLEL ARCHITECTURES 9**

Parallel processing challenges; Flynn’s classification: SISD – MIMD – SIMD – SPMD and Vector

Architectures; Hardware multithreading; Multi-core processors and other shared memory;

Multiprocessors, Clusters, Warehouse Scale Computers, and Other Message-Passing Multiprocessors,

Introduction to Graphics Processing Units

**TOTAL PERIODS: 45**

**COURSE OUTCOMES**

**On successful completion of this course, the student will be able to:**

CO1 Explain the basics structure of computers, operations and instructions and measure their

performance with suitable metrics.(K3)

CO2 Construct arithmetic and logic unit.(K3)

CO3 Analyse and compare pipelined vs. unpipelined execution unit performance.(K4)

CO4 Analyse various memory systems and understand I/O communication(K4)

CO5 Explain parallel processing architectures.(K2)

**TEXTBOOKS**

**1** David A Patterson, John L Hennessy, “Computer Organization and Design: The

Hardware/Software Interface”, 5th Edition, Morgan Kaufmann / Elsevier, 2014.

**2** Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Naraig Manjikian, “Computer Organization

and Embedded Systems”, 6th Edition, Tata McGraw Hill, 2022.

**REFERENCE BOOKS**

**1** John L Hennessey, David A Patterson, “Architecture – A Quantitative Approach”, 5th edition,

Morgan Kaufmann, Elsevier, 2012 (Units I, III)

**2** John P Hayes, “Computer Architecture and Organization”, 3rd Edition, Tata McGraw Hill,

2012

**3** Morris Mano M, “Computer System Architecture”, Revised 3rd Edition, Pearson Publication,

2017

**4** Chakraborty P, “Computer Architecture and Organization”, JAICO Publishing House, 2010