INDIAN INSTITUTE OF INFORMATION TECHNOLOGY,NAGPUR

TOPIC : Adiabatic JK Flipflop

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ADIABATIC JK FLIPFLOP

----------*****CONTENTS*****----------

1.OBJECTIVE:

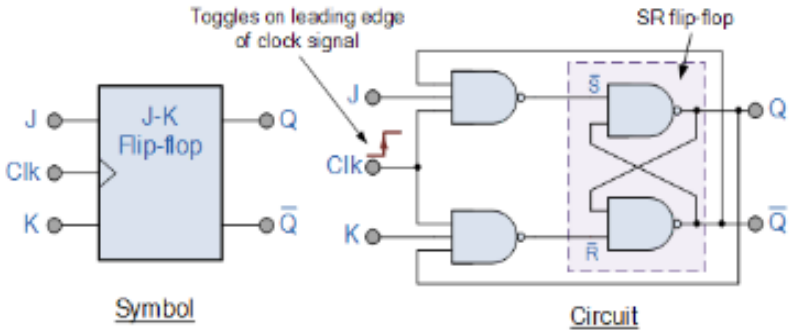
The objective of the project was to design the CMOS layout for the adiabatic JK flipflop .Also write the netlist for the circuit and verifying it using ngspice.

2.INTRODUCTION:

In the realm of digital circuits, energy efficiency has become a paramount concern, especially with the proliferation of battery-powered and energy-constrained devices. Adiabatic logic represents a promising approach to address this challenge, offering the potential for significant reductions in power consumption without sacrificing performance. At the heart of adiabatic logic lies the adiabatic JK flip-flop, a key building block that exemplifies the principles of energy-efficient design.

2.1. JK FLIPFLOP:

Flip-flops are bistable multivibrators capable of maintaining one of two stable states (commonly referred to as "0" or "1") until triggered to switch by an external signal, typically a clock pulse. These devices are crucial for sequential logic circuits, where the output depends not only on the current inputs but also on the previous states of the system.



Circuit and symbol representation of JK Flipflop

TRUTH TABLE OF JK FLIPFLOP:

CLK	J	K	Q_{next}	Comment
Rising edge	0	0	Q	Hold state
Rising edge	0	1	0	Reset
Rising edge	1	0	1	Set
Rising edge	1	1	$\overline{Q}$	Toggle
Non-rising	X	X	Q	No change

2.2 .ADIABATIC LOGIC:

. Low-power design can be applied on various different levels, such as the architectural level, the gate level, and the technology level. Apart from that, also a number of alternative logic-design styles are presented to report on their characteristics regarding power consumption.

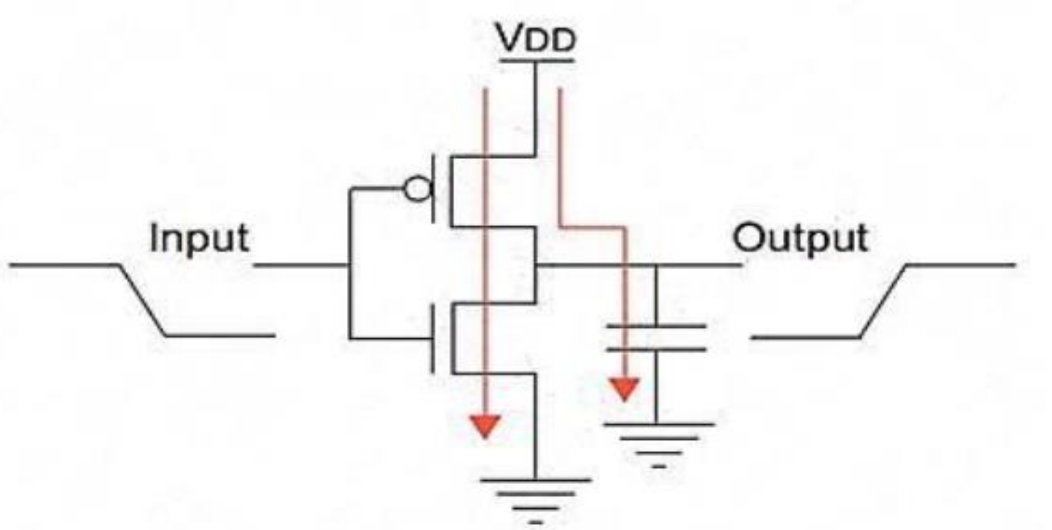
Passive losses due to leakage currents are in focus with on-going shrinking of microelectronic circuits. Power-gating does not supply power to the inactive circuits from the power supply. Uncritical paths within a complex system can be equipped with higher devices, allowing for a trade-off of speed for passive losses. Apart from these circuit level methods to reduce leakage losses also new transistor models are presented to minimize leakage losses in circuits.

Adiabatic Logic technique is one of the best circuit design methods to reduce energy consumption in different operations. Analysis on the gate level suggests a major cutdown of losses in adiabatic logic as compared to static CMOS. Out of a large numbers of adiabatic topologies only a few satisfy our requirements , as those are compatible to a static CMOS design flow and robust with respect to P-V-T variation and apply a manageable number of clocked power supplies that can be generated in an energy efficient manner.

2.3 CHARGING PROCESS IN ADIABATIC PROCESS:

Energy dissipation in a simple CMOS inverter is influenced by the input signal's transition from 1 to 0. When this occurs, energy is transferred from the source to charge the output capacitor to the supply voltage. This charge, denoted by Q = C, is removed from the voltage source, constituting an energy quantum, E(t) = Q. The energy stored on the capacitor at voltage V is given by 1/2CV^2.

$$EC=1/2CV^2$$



The energy dissipated in the circuit equals the difference between the energy transferred from the sources and the energy stored in the circuit. When the input level changes from 0 to 1, the NMOS channel becomes ON while the PMOS is OFF in steady-state condition. The charge stored on the output capacitance is then dissipated to the ground via the NMOS. The energy dissipation due to the switching of input level is given as 1/2 αC, where α represents the switching probability of the circuit. Various methods are employed to reduce energy dissipation in static CMOS, including reducing the number of transistors used, minimizing capacitive load (C), and optimizing voltage supply. These strategies are crucial for enhancing energy efficiency and minimizing power consumption in CMOS circuits.

$$EC=1/2\alpha CV^2$$

In contrast to the above method Adiabatic Logic doesn't suddenly switches from 0 to1 (and vice versa), but a voltage ramp is used to charge and recover the energy from the output of the circuit. The principle of operation of an adiabatic gate is presented for a buffer gate in the Efficient Charge Recovery Logic (ECRL) . The gate consists of two cross coupled PMOS devices that are used to store the information. Two NMOS devices are used to construct the logic function. Four-phase power clock signals drives the cascade gates. Input signal for the ECRL gate are shifted by 90 degree with respect to the applied power clock signal.

Two adiabatic logic families are present, one is

1.Positive Feedback Adiabatic Logic (PFAL)

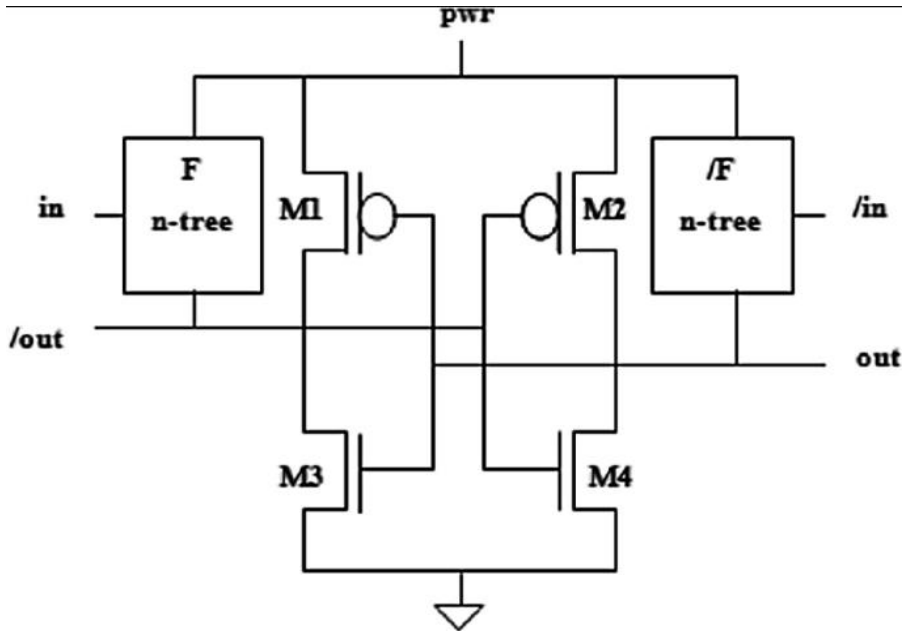
2. Efficient Charge Recovery Logic(ECRL).

Both operate in the same four-phase power-clock supply. PFAL is designed by the cross coupling of two inverters, which is the latch element. They store the output state when the input signal gradually decreases. A cross coupled PMOS pair is used in case of ECRL based on Cathode Voltage Switch Logic (CVSL). PFAL and ECRL use logic block constructed from NMOS. Logic blocks are connected from the power clock Φ to the output nodes for PFAL and from the output to Ground for ECRL.

In this ,the adiabatic JK flipflop is designed by using the Positive Feedback Adiabatic Logic (PFAL) .

2.4. POSITIVE FEEDBACK ADIABATIC LOGIC:

PFAL is a dual-rail logic family comprised of a pair of cross-coupled inverters. Unlike traditional CMOS logic, PFAL utilizes a power-clock to supply voltage instead of a static DC supply. NMOS devices are employed between the power-clock and the output, with complementary inputs provided to these transistors. This configuration results in low resistance between the power-clock and the asserted output, while the non-asserted path exhibits high impedance. Operation occurs only when there's a substantial voltage difference between these two points. Additionally, PFAL allows for output recovery through reverse-flowing data, minimizing power loss due to leakage. This innovative approach makes PFAL one of the most efficient MOSFET-only logic families available.



Positive Feedback Adiabatic Logic (PFAL)

2.5 JK FLIPFLOP CIRCUIT DESIGN:

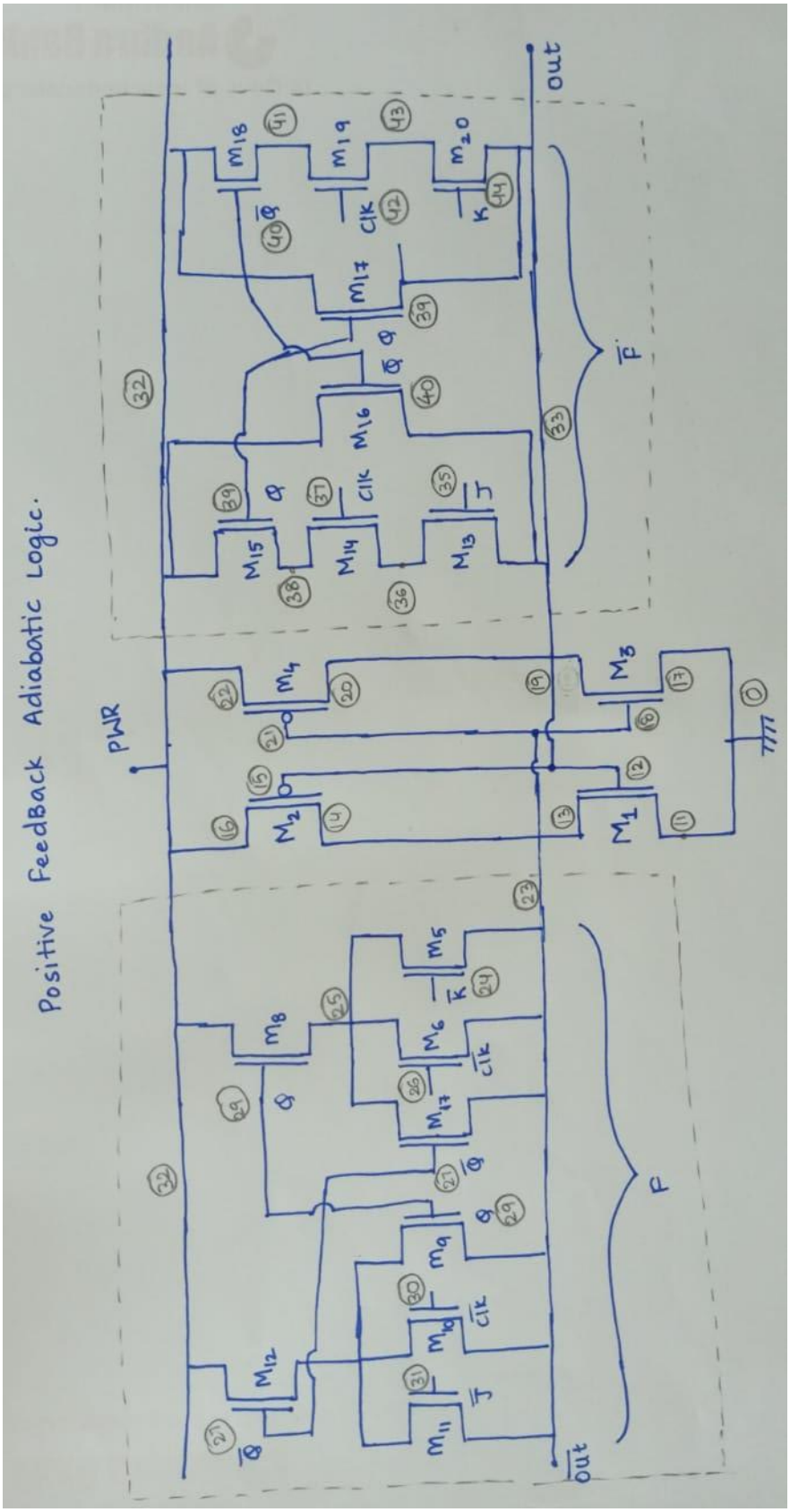
The JK flipflop was designed with the help of Positive Feedback Adiabatic Logic. The process of designing the JK flipflop is as follows

- The two inverters were cross coupled together. This cross coupling of the inverters helps to achieve the energy efficiency and noise immunity. Cross-coupling involves connecting the outputs of two inverters to each other's inputs. This configuration enables the inverters to operate in a complementary manner, enhancing the circuit's performance in several ways.
- The functionality circuit of the JK flipflop was made only with the NMOS logic and placed in parallel with power supply and output.
- The inverse of the JK flipflop was also placed on the opposite side with NMOS logic and placed in parallel with power supply and output.
- The outputs were checked at the respective gates.
- Make sure that the similar inputs at the different gates have exactly same wave form.

3.SOFTWARES USED :

NG spice and Microwind 3.0 version.

4.CIRCUIT DIAGRAM OF JK FLIPFLOP BY PFAL :

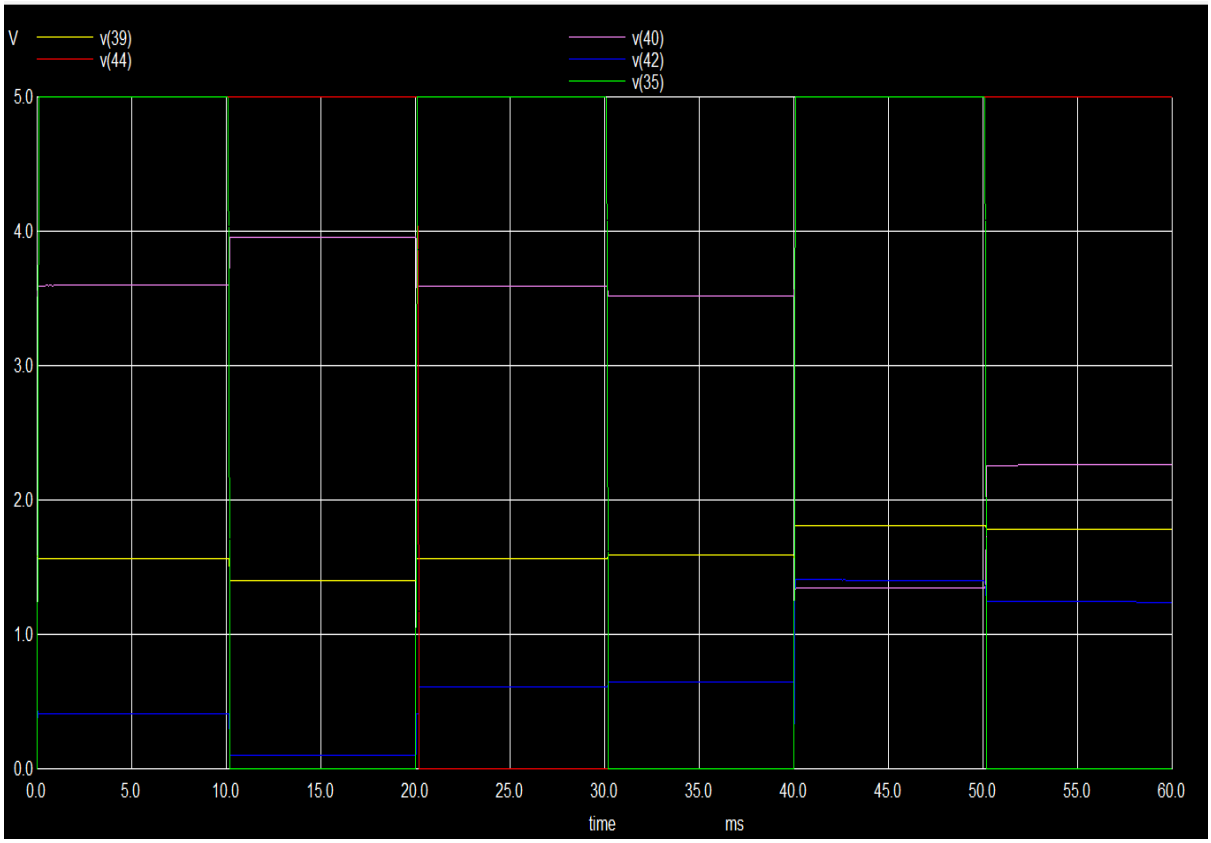


5.NETLIST FOR JK FLIPFLOP:

```
**adiabatic JK flipflop**
.subckt inverter 1 2 3
M1  3 1 0 0 nmod w=100u l=10u
M2  3 1 2 2 pmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
.ends
vdd 2 0 dc 5
vj 35 0 pulse(0 5 0 0 0 10m 20m)
vk 44 0 pulse(0 5 0 0 0 20m 40m)
vclk 37 2 pulse(0 5 0 0 0 10m 20m)
xj 35 2 31 inverter
xk 44 2 24 inverter
xclk 37 2 30 30 inverter
xq 29 2 27 inverter
xq1 39 2 40 inverter
x1 33 2 23 inverter
x2 23 2 33 inverter
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
M5 25 24 23 23 nmod w=100u l=10u
M6 25 26 23 23 nmod w=100u l=10u
M7 25 27 23 23 nmod w=100u l=10u
M8 32 29 25 25 nmod w=100u l=10u
M9 28 29 23 23 nmod w=100u l=10u
M10 28 30 23 23 nmod w=100u l=10u
M11 28 31 23 23 nmod w=100u l=10u
M12 32 27 28 28 nmod w=100u l=10u
M13 36 35 33 33 nmod w=100u l=10u
M14 38 37 36 36 nmod w=100u l=10u
```

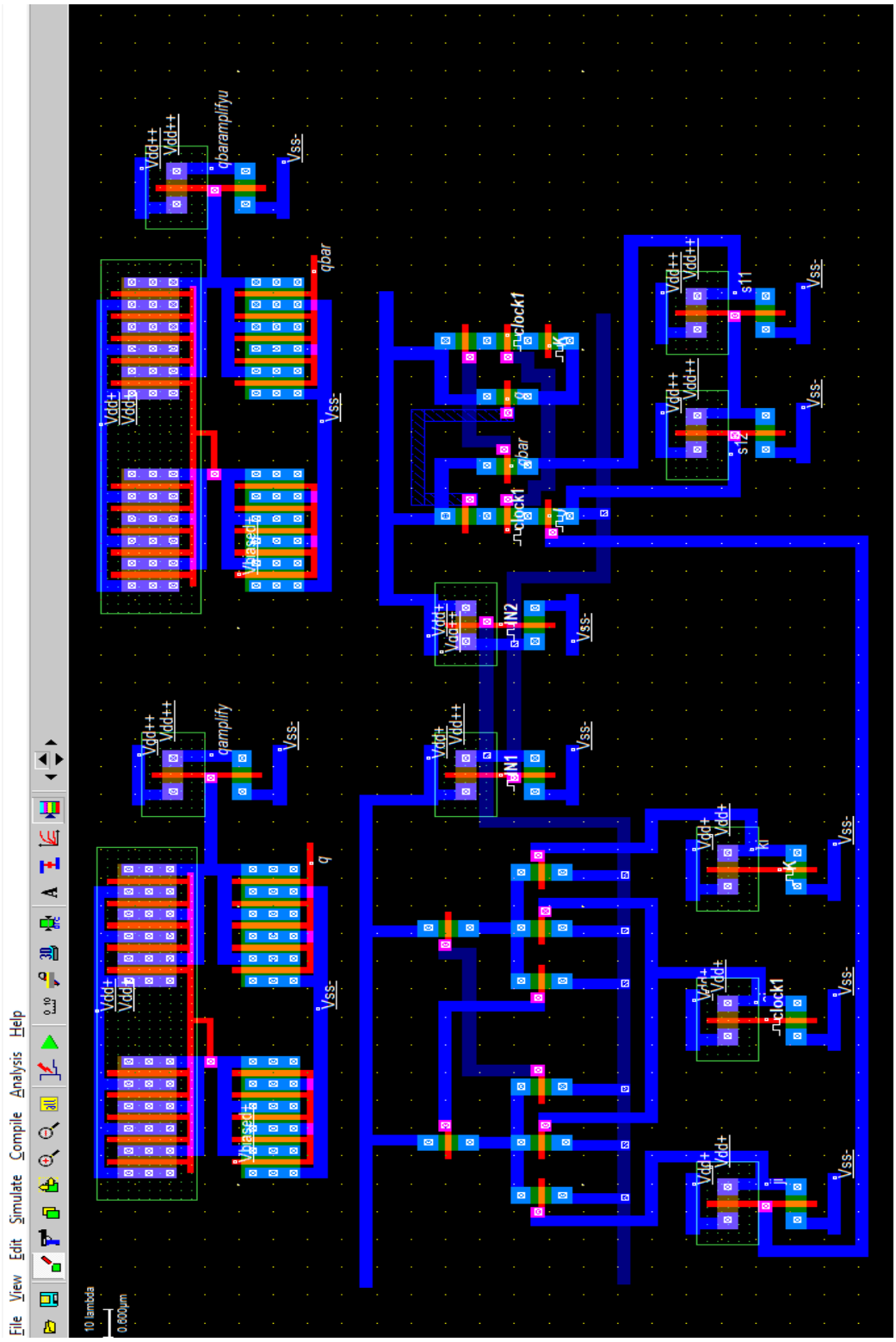
```
M15 32 39 38 38 nmod w=100u l=10u
M16 32 40 33 33 nmod w=100u l=10u
M17 32 39 33 33 nmod w=100u l=10u
M18 32 40 41 41 nmod w=100u l=10u
M19 41 42 43 43 nmod w=100u l=10u
M20 43 44 33 33 nmod w=100u l=10u
    .tran 0.1m 60m
    .control
    run
  plot v(35) v(44) v(42) v(39) v(40)
    .endc
    .end
```

OUTPUT FOR THE NETLIST:

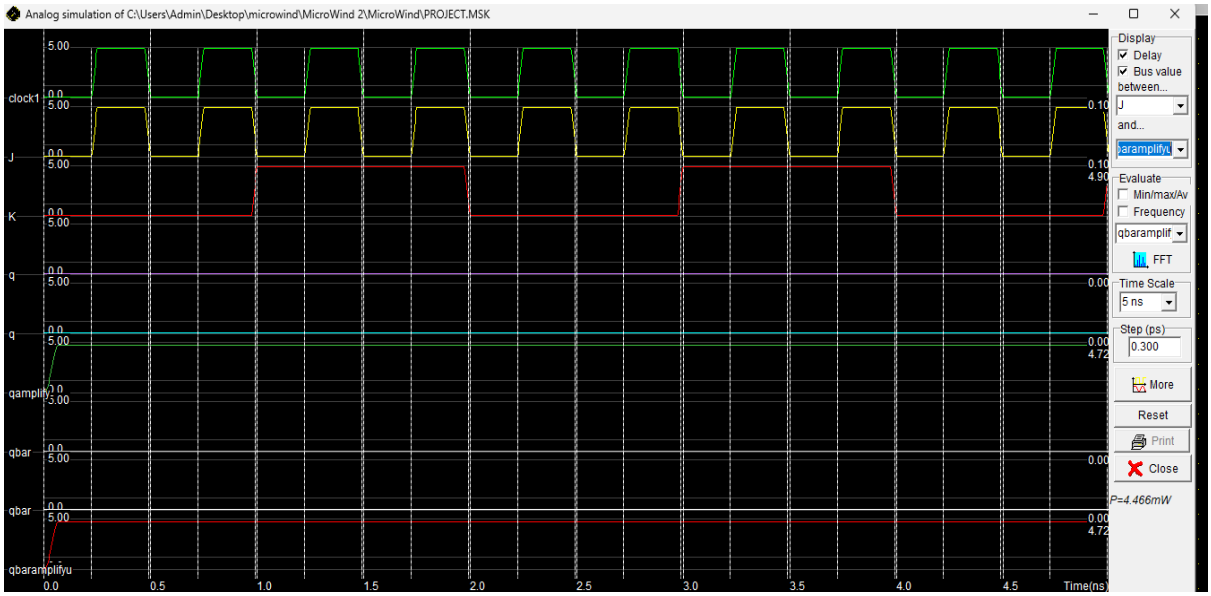


** Green(35)-J ;Red(44)-k; Yellow(39)-q; Purple(40)- qbar ;blue(42) -clk.

6.LAYOUT DESIGNING OF ADIABATIC JK FLIPFLOP USING MICROWIND:



OUTPUT:



Although the outputs in microwind (q amplify and qbar amplify) seems to be the same (straight line),there is a voltage difference for the level 1 and level 0. The difference between the level 1 and level 0 is around 0.09v.This is due the voltage decrement after every stage and as we can observe there are many stages in the layout design causing this effect. But the clear output was shown in the netlist output .

The voltages(approx) that were detected in the microwind were mentioned in table 1.1.

J	K	Q	Voltage (q)	Qbar	Voltage(Qbar)
0	0	Q_n	4.81v	Q_n'	4.90v
0	1	0	4.81v	1	4.90v
1	0	1	4.90v	0	4.81v
1	1	Q_n'	4.81v	Q_n	4.90v

Note :

These voltages are after amplifying the initial output voltages.

7.CONCLUSION:

Hence, the adiabatic JK flipflop was performed successfully in the ng spice and optimally performed in the microwind.

8.REFRENCES:

- Research paper :Adiabatic Logic Design for Low Power VLSI Applications by kiran kumar sahu

- https://www.researchgate.net/figure/Modified-Positive-Feedback-Adiabatic-Logic-PFAL_fig3_346582984
- https://www.youtube.com/watch?v=8gYlVsz2JWk
- P. Bhati and N. Z. Rizvi, "Adiabatic logic: An alternative approach to low power application circuits," 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, India, 2016, pp. 4255-4260, doi: 10.1109/ICEEOT.2016.7755521. keywords: {Adiabatic;Adders;Power dissipation;Switches;Clocks;MOSFET;Power supplies;PFAL;VLSI;CMOS Logic;Adiabatic logic;MUX;Adder},