

<b>i2c_address_translate Project Status</b>			
<b>Project File:</b>	i2c.xise	<b>Parser Errors:</b>	No Errors
<b>Module Name:</b>	i2c_address_translate	<b>Implementation State:</b>	Programming File Generated
<b>Target Device:</b>	xc3s100e-5vq100	<b>• Errors:</b>	No Errors
<b>Product Version:</b>	ISE 14.7	<b>• Warnings:</b>	2 Warnings (1 new)
<b>Design Goal:</b>	Balanced	<b>• Routing Results:</b>	All Signals Completely Routed
<b>Design Strategy:</b>	Xilinx Default (unlocked)	<b>• Timing Constraints:</b>	All Constraints Met
<b>Environment:</b>	System Settings	<b>• Final Timing Score:</b>	0 (Timing Report)

<b>Device Utilization Summary</b>				[ - ]
<b>Logic Utilization</b>	<b>Used</b>	<b>Available</b>	<b>Utilization</b>	<b>Note(s)</b>
Number of Slice Flip Flops	29	1,920	1%	
Number of 4 input LUTs	102	1,920	5%	
Number of occupied Slices	57	960	5%	
Number of Slices containing only related logic	57	57	100%	
Number of Slices containing unrelated logic	0	57	0%	
Total Number of 4 input LUTs	102	1,920	5%	
Number of bonded IOBs	20	66	30%	
IOB Flip Flops	1			
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.40			

<b>Performance Summary</b>	[ - ]
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<b>Final Timing Score:</b>	0 (Setup: 0, Hold: 0)	<b>Pinout Data:</b>	Pinout Report
<b>Routing Results:</b>	All Signals Completely Routed	<b>Clock Data:</b>	Clock Report
<b>Timing Constraints:</b>	All Constraints Met		

<b>Detailed Reports</b>					[ - ]
<b>Report Name</b>	<b>Status</b>	<b>Generated</b>	<b>Errors</b>	<b>Warnings</b>	<b>Infos</b>
Synthesis Report	Current	Thu Nov 20 15:22:04 2025	0	2 Warnings (1 new)	1 Info (0 new)
Translation Report	Current	Thu Nov 20 15:23:17 2025	0	0	0
Map Report	Current	Thu Nov 20 15:23:20 2025	0	0	2 Infos (0 new)
Place and Route Report	Current	Thu Nov 20 15:23:25 2025	0	0	2 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Thu Nov 20 15:23:26 2025	0	0	6 Infos (0 new)
Bitgen Report	Current	Thu Nov 20 15:23:32 2025	0	0	0

<b>Secondary Reports</b>			[ - ]
<b>Report Name</b>	<b>Status</b>	<b>Generated</b>	
ISIM Simulator Log	Current	Thu Nov 20 15:28:44 2025	
Post-Synthesis Simulation Model Report	Current	Thu Nov 20 15:30:19 2025	
WebTalk Log File	Current	Thu Nov 20 15:23:32 2025	

**Date Generated:** 11/20/2025 - 15:30:59