Synthesis Report

Thu Nov 20 15:34:22 2025

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Release 14.7 - xst P.20131013 (lin64)
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-->
Parameter TMPDIR set to xst/projnav.tmp


Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.02 secs

-->
Parameter xsthdpdir set to xst


Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.02 secs

-->
Reading design: i2c_address_translate.prj

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=========================================================================
*                      Synthesis Options Summary                        *
=========================================================================
---- Source Parameters
Input File Name                    : "i2c_address_translate.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "i2c_address_translate"
Output Format                      : NGC
Target Device                      : xc3s100e-5-vq100

---- Source Options
Top Module Name                    : i2c_address_translate
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
Safe Implementation                : No
FSM Style                          : LUT
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : Yes
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
ROM Style                          : Auto
Mux Extraction                     : Yes
Resource Sharing                   : YES
Asynchronous To Synchronous        : NO
Multiplier Style                   : Auto
Automatic Register Balancing       : No

---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 500
Add Generic Clock Buffer(BUFG)     : 24
Register Duplication               : YES
Slice Packing                      : YES
Optimize Instantiated Primitives   : NO
Use Clock Enable                   : Yes
Use Synchronous Set                : Yes
Use Synchronous Reset              : Yes
Pack IO Registers into IOBs        : Auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
Keep Hierarchy                     : No
Netlist Hierarchy                  : As_Optimized
RTL Output                         : Yes
Global Optimization                : AllClockNets
Read Cores                         : YES
Write Timing Constraints           : NO
Cross Clock Analysis               : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : Maintain
Slice Utilization Ratio            : 100
BRAM Utilization Ratio             : 100
Verilog 2001                       : YES
Auto BRAM Packing                  : NO
Slice Utilization Ratio Delta      : 5

=========================================================================


=========================================================================
*                          HDL Compilation                              *
=========================================================================
Compiling verilog file "i2c.v" in library work
Module  compiled
No errors in compilation
Analysis of file <"i2c_address_translate.prj"> succeeded.


=========================================================================
*                     Design Hierarchy Analysis                         *
=========================================================================
Analyzing hierarchy for module  in library .


=========================================================================
*                            HDL Analysis                               *
=========================================================================
Analyzing top module .
Module  is correct for synthesis.


=========================================================================
*                            HDL Synthesis                              *
=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit .
    Related source file is "i2c.v".
WARNING:Xst:646 - Signal  is assigned but never used. This unconnected signal will be trimmed during the optimization process.
WARNING:Xst:646 - Signal  is assigned but never used. This unconnected signal will be trimmed during the optimization process.
    Register  equivalent to  has been removed
    Found finite state machine  for signal .
    -----------------------------------------------------------------------
    | States             | 7                                              |
    | Transitions        | 23                                             |
```

```
    | Inputs            | 6                                          |
    | Outputs           | 8                                          |
    | Clock             | clk                       (rising_edge)    |
    | Reset             | rst                       (positive)       |
    | Reset type        | asynchronous                               |
    | Reset State       | 0000                                       |
    | Encoding          | automatic                                  |
    | Implementation    | LUT                                        |
    -----------------------------------------------------------------
    Found 1-bit register for signal .
    Found 4-bit register for signal .
    Found 4-bit adder for signal  created at line 67.
    Found 8-bit register for signal .
    Found 8-bit register for signal .
    Found 7-bit comparator equal for signal  created at line 94.
    Found 1-bit register for signal .
    Found 1-bit register for signal .
    Found 1-bit register for signal .
    Found 1-bit register for signal .
    Summary:
        inferred   1 Finite State Machine(s).
        inferred  25 D-type flip-flop(s).
        inferred   1 Adder/Subtractor(s).
        inferred   1 Comparator(s).
        inferred   1 Multiplexer(s).
Unit  synthesized.

INFO:Xst:1767 - HDL ADVISOR - Resource sharing has identified that some arithmetic operations in this design can share the same physical resources for reduced device utilization. For improved clock frequency you may try to disable resource sharing.

=========================================================================
HDL Synthesis Report

Macro Statistics
# Adders/Subtractors                                   : 1
 4-bit adder                                          : 1
# Registers                                            : 15
 1-bit register                                       : 13
 4-bit register                                       : 1
 8-bit register                                       : 1
# Comparators                                          : 1
 7-bit comparator equal                               : 1
# Multiplexers                                         : 1
 1-bit 8-to-1 multiplexer                             : 1

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================

Analyzing FSM  for best encoding.
Optimizing FSM  on signal  with gray encoding.
------------------
 State | Encoding
------------------
 0000  | 000
 0001  | 001
 0010  | 011
 0011  | 010
 0100  | 110
 0101  | 111
 0110  | 101
------------------

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# FSMs                                                 : 1
# Adders/Subtractors                                   : 1
 4-bit adder                                          : 1
# Registers                                            : 25
 Flip-Flops                                           : 25
# Comparators                                          : 1
 7-bit comparator equal                               : 1
# Multiplexers                                         : 1
 1-bit 8-to-1 multiplexer                             : 1

=========================================================================

=========================================================================
*                         Low Level Synthesis                           *
=========================================================================

Optimizing unit  ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block i2c_address_translate, actual ratio is 5.
FlipFlop step_now_FSM_FFd2 has been replicated 1 time(s)
FlipFlop prev_scl has been replicated 1 time(s) to handle iob=true attribute.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                            : 30
 Flip-Flops                                           : 30

=========================================================================

=========================================================================
*                           Partition Report                            *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.

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=========================================================================
*                            Final Report                               *
=========================================================================
Final Results
RTL Top Level Output File Name     : i2c_address_translate.ngr
Top Level Output File Name         : i2c_address_translate
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : No

Design Statistics
# IOs                              : 20

Cell Usage :
# BELS                             : 106
#      LUT2                        : 9
#      LUT2_L                      : 1
#      LUT3                        : 25
#      LUT3_D                      : 3
#      LUT3_L                      : 1
#      LUT4                        : 39
#      LUT4_D                      : 8
#      LUT4_L                      : 16
#      MUXF5                       : 3
#      MUXF6                       : 1
# FlipFlops/Latches                : 30
#      FDC                         : 9
#      FDCE                        : 17
#      FDP                         : 4
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 19
#      IBUF                        : 17
#      OBUF                        : 2
=========================================================================
```

```
Device utilization summary:
---------------------------

Selected Device : 3s100evq100-5

 Number of Slices:                       54  out of    960     5%
 Number of Slice Flip Flops:             29  out of   1920     1%
 Number of 4 input LUTs:                102  out of   1920     5%
 Number of IOs:                          20
 Number of bonded IOBs:                  20  out of     66    30%
    IOB Flip Flops:                       1
 Number of GCLKs:                        1  out of     24     4%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

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=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clk                                | BUFGP                  | 30    |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
-----------------------------------+------------------------+-------+
Control Signal                     | Buffer(FF name)        | Load  |
-----------------------------------+------------------------+-------+
rst                                | IBUF                   | 30    |
-----------------------------------+------------------------+-------+

Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 5.609ns (Maximum Frequency: 178.299MHz)
   Minimum input arrival time before clock: 6.512ns
   Maximum output required time after clock: 4.063ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clk'
  Clock period: 5.609ns (frequency: 178.299MHz)
  Total number of paths / destination ports: 562 / 43
-------------------------------------------------------------------------
Delay:               5.609ns (Levels of Logic = 4)
  Source:            step_now_FSM_FFd1 (FF)
  Destination:       bit_pos_1 (FF)
  Source Clock:      clk rising
  Destination Clock: clk rising

  Data Path: step_now_FSM_FFd1 to bit_pos_1
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q             18   0.514   0.977  step_now_FSM_FFd1 (step_now_FSM_FFd1)
     LUT4_D:I1->O          2   0.612   0.410  sda_out_mux000011 (N5)
     LUT4:I2->O            7   0.612   0.632  bit_pos_mux0000<0>2_SW0 (N211)
     LUT3:I2->O            1   0.612   0.360  bit_pos_mux0000<1>_SW0 (N23)
     LUT4:I3->O            1   0.612   0.000  bit_pos_mux0000<1> (bit_pos_mux0000<1>)
     FDC:D                     0.268          bit_pos_2
    ----------------------------------------
    Total                      5.609ns (3.230ns logic, 2.379ns route)
                                       (57.6% logic, 42.4% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 206 / 47
-------------------------------------------------------------------------
Offset:              6.512ns (Levels of Logic = 5)
  Source:            scl_in (PAD)
  Destination:       data_read_7 (FF)
  Destination Clock: clk rising

  Data Path: scl_in to data_read_7
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            22   1.106   1.141  scl_in_IBUF (scl_in_IBUF)
     LUT2:I0->O            2   0.612   0.410  data_read_0_mux00004_SW0 (N21)
     LUT3:I2->O            1   0.612   0.426  data_read_0_mux00006137_SW0 (N59)
     LUT4:I1->O            8   0.612   0.712  data_read_0_mux00006137 (N28)
     LUT4:I1->O            1   0.612   0.000  data_read_7_mux000042 (data_read_7_mux0000)
     FDCE:D                    0.268          data_read_7
    ----------------------------------------
    Total                      6.512ns (3.822ns logic, 2.690ns route)
                                       (58.7% logic, 41.3% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 2 / 2
-------------------------------------------------------------------------
Offset:              4.063ns (Levels of Logic = 1)
  Source:            sda_out (FF)
  Destination:       sda_out (PAD)
  Source Clock:      clk rising

  Data Path: sda_out to sda_out
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDP:C->Q              2   0.514   0.380  sda_out (sda_out_OBUF)
     OBUF:I->O                 3.169          sda_out_OBUF (sda_out)
    ----------------------------------------
    Total                      4.063ns (3.683ns logic, 0.380ns route)
                                       (90.6% logic, 9.4% route)

=========================================================================


Total REAL time to Xst completion: 4.00 secs
Total CPU time to Xst completion: 3.21 secs

-->


Total memory usage is 614300 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    2 (   0 filtered)
Number of infos    :    1 (   0 filtered)
```