

i2c_address_translate Project Status			
Project File:	i2c.xise	Parser Errors:	No Errors
Module Name:	i2c_address_translate	Implementation State:	Programming File Generated
Target Device:	xc3s100e-5vq100	• Errors:	No Errors
Product Version:	ISE 14.7	• Warnings:	2 Warnings (1 new)
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	All Constraints Met
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	29	1,920	1%	
Number of 4 input LUTs	102	1,920	5%	
Number of occupied Slices	57	960	5%	
Number of Slices containing only related logic	57	57	100%	
Number of Slices containing unrelated logic	0	57	0%	
Total Number of 4 input LUTs	102	1,920	5%	
Number of bonded IOBs	20	66	30%	
IOB Flip Flops	1			
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.40			

Performance Summary	[-]
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Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Report
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports						[-]
Report Name	Status	Generated	Errors	Warnings	Infos	
Synthesis Report	Current	Thu Nov 20 15:22:04 2025	0	2 Warnings (1 new)	1 Info (0 new)	
Translation Report	Current	Thu Nov 20 15:23:17 2025	0	0	0	
Map Report	Current	Thu Nov 20 15:23:20 2025	0	0	2 Infos (0 new)	
Place and Route Report	Current	Thu Nov 20 15:23:25 2025	0	0	2 Infos (0 new)	
Power Report						
Post-PAR Static Timing Report	Current	Thu Nov 20 15:23:26 2025	0	0	6 Infos (0 new)	
Bitgen Report	Current	Thu Nov 20 15:23:32 2025	0	0	0	

Secondary Reports			[-]
Report Name	Status	Generated	
ISIM Simulator Log	Current	Thu Nov 20 15:28:44 2025	
Post-Synthesis Simulation Model Report	Current	Thu Nov 20 15:30:19 2025	
WebTalk Log File	Current	Thu Nov 20 15:23:32 2025	

Date Generated: 11/20/2025 - 15:30:59