Team Details

Team Name: CodeCrafters@1234

SR. NO	ROLE	NAME	ACADEMIC YEAR
1	**Team Leader**	*Sharvari Balapurkar*	*Third*
2	Member 1	*Roshani Mahale*	*Third*
3	Member 2	*Pavan Patil*	*Third*
4	Member 3	*Jayesh Mali*	*Third*

A team can have up to 4 members including the team leader. Add rows if necessary.

COLLEGE NAME

SVKM' s Institute of Technology, Dhule

TEAM LEADER CONTACT NUMBER

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TEAM LEADER EMAIL ADDRESS

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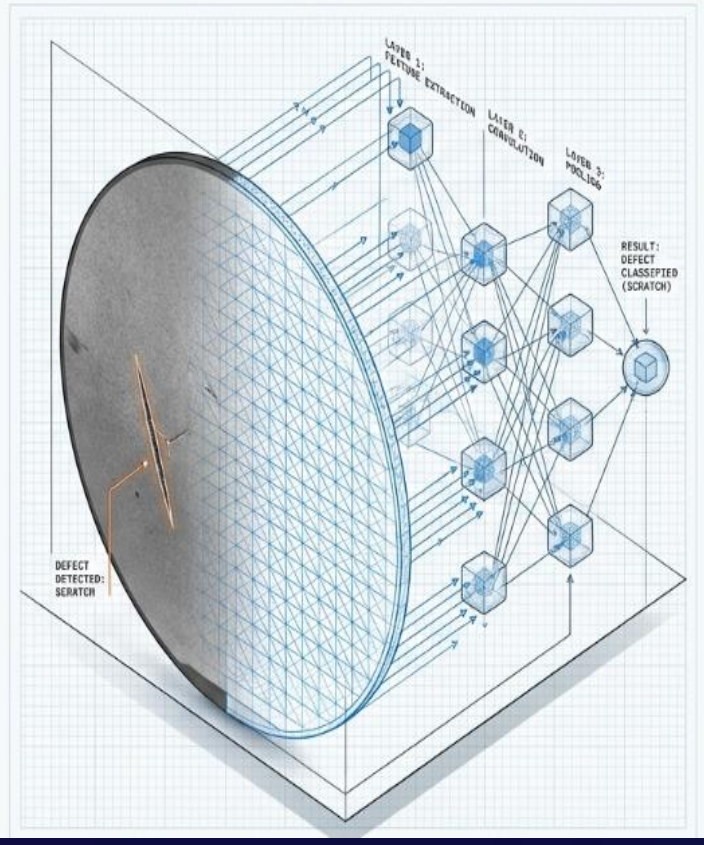
Problem Statement Addressed

Real-Time Wafer Defect Detection at at the Edge

Leveraging Lightweight CNNs and NXP Architecture for Latency-Free Quality Control.

TECHNICAL OVERVIEW: Migrating Automated Optical Inspection (AOI) from cloud infrastructure to embedded NXP i.MX RT systems for immediate defect classification.



Description :

- Semiconductor wafer defects cause significant yield loss and cost escalation.
- Manual inspection and rule-based systems are slow and error-prone.
- Cloud-based AI models suffer from latency, bandwidth, and privacy issues
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- There is a strong need for **real-time, edge-deployable AI solutions** for wafer inspection

Idea Description -

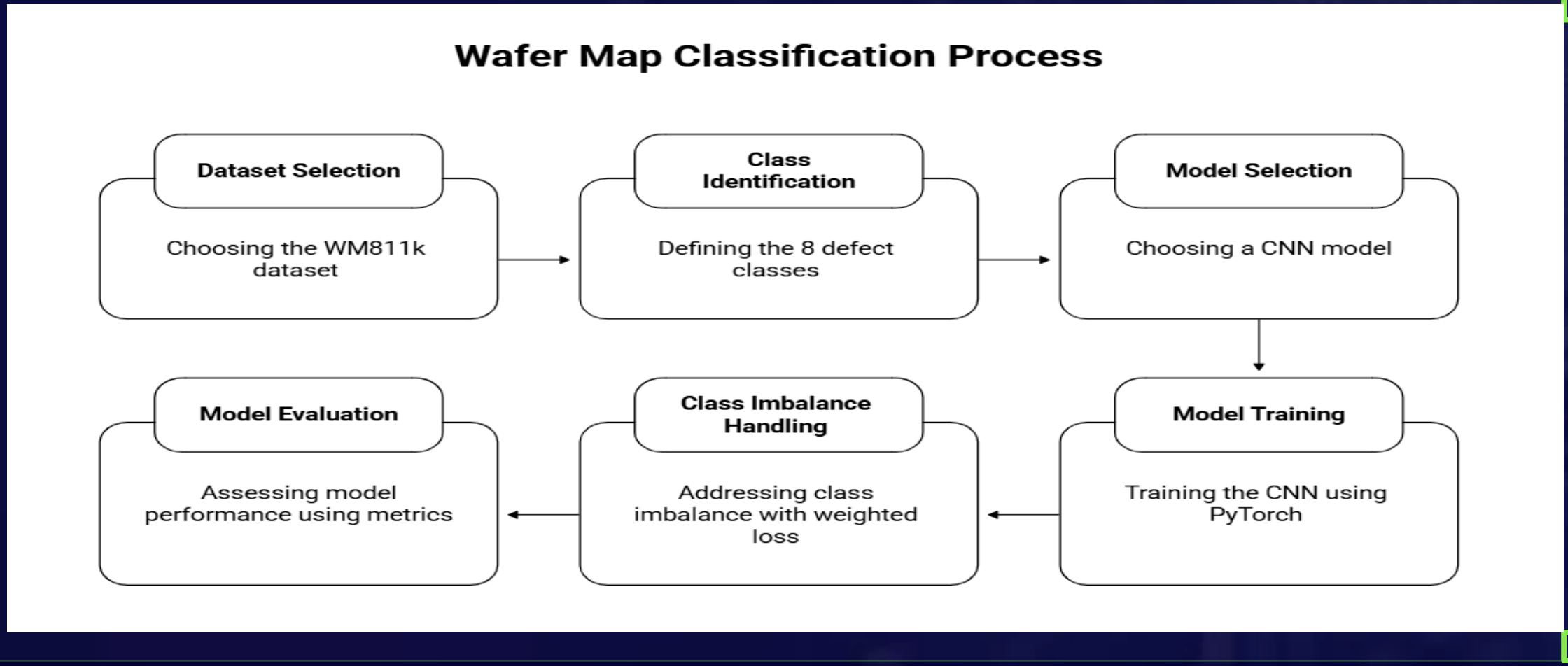
KEY CONCEPT & APPROACH :

- Use a **supervised AI/ML model (CNN)** to classify wafer defect images.
- Learn defect patterns directly from wafer map images.
- Design the model to be **lightweight and edge-friendly**.

SOLUTION OVERVIEW :

- Input: Grayscale wafer images
- Output: Classified defect category (Clean / Defect Type)
- Model runs locally on edge hardware (NXP-compatible)
- Reduces dependency on cloud-based inspection systems

Proposed Solution -



Innovation and Uniqueness

KEY INNOVATION

- Edge-first AI design instead of cloud-heavy models
- Focus on **deployability, stability, and real-time inference**
- Honest trade-off between accuracy and edge feasibility

COMPETITIVE ADVANTAGE

- Lightweight model suitable for constrained hardware
- ONNX-compatible for NXP eIQ toolchain
- Realistic industrial dataset (not synthetic or toy data)
- Transparent and explainable AI pipeline

Impact and Benefits

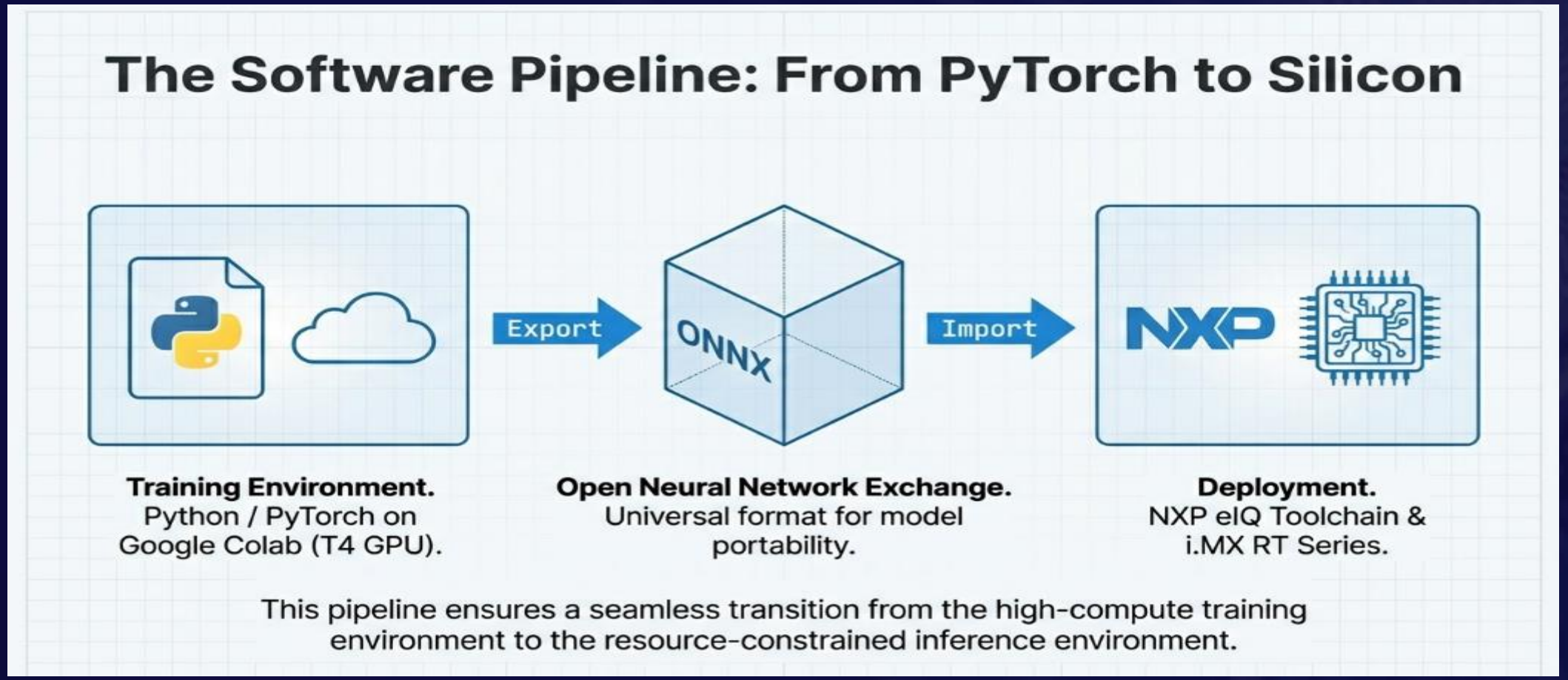
Primary Impact :

- Faster defect detection in semiconductor manufacturing
- Reduced inspection latency
- Improved yield monitoring at the production line

Quantifiable Outcomes :

- Real-time on-device inference
- Reduced cloud dependency
- Lower inspection cost
- Scalable across multiple fab locations

Technology & Feasibility/Methodology Used



GitHub Link

GitHub Repository

https://github.com/SharvariAB/Edge-AI-based-Wafer-Defect-Detection/tree/main