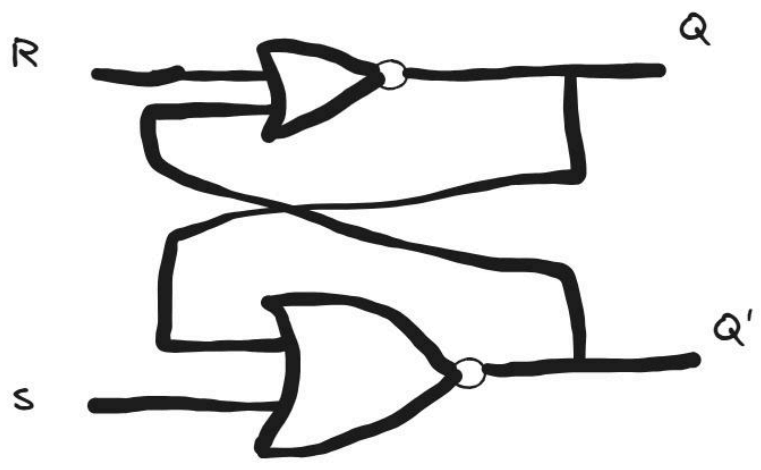
SR latch using NOR gate



Explanation of the Image: SR Latch using NOR Gate

This image represents an SR (Set-Reset) Latch built using NOR gates. The SR latch is a basic sequential logic circuit used for storing one bit of information. It has two inputs:

- S (Set): Used to set the output Q = 1 (high state).
- R (Reset): Used to reset the output Q = 0 (low state).

The circuit consists of two NOR gates, where:

- The output of each NOR gate is fed back into the other NOR gate as an input.
- The two outputs Q and Q' (Q complement) are always opposite to each other (Q' = NOT Q).

Working of SR Latch using NOR Gates

Case 1: S = 0, R = 0 (No Change / Memory State)

- If both S and R are 0, the latch remains in its previous state.
- The stored value does not change.
- Q and Q' remain in their previous states.

Case 2: S = 0, R = 1 (Reset State)

- The upper NOR gate has inputs R = 1 and Q', so it outputs Q = 0.
- The lower NOR gate now has inputs S = 0, Q = 0, so it outputs Q' = 1.
- The latch is in the reset state (Q = 0, Q' = 1).

Case 3: S = 1, R = 0 (Set State)

- The lower NOR gate has inputs S = 1 and Q, so it outputs Q' = 0.
- The upper NOR gate now has inputs R = 0, Q' = 0, so it outputs Q = 1.
- The latch is in the set state (Q = 1, Q' = 0).

Case 4: S = 1, R = 1 (Invalid / Undefined State)

- Both NOR gates output 0, causing an invalid state.
- This state is not allowed because it makes Q and Q' equal, violating the principle of an SR latch.

Truth Table of SR Latch using NOR Gate

S (Set)	R (Reset)	Q (Output)	Q' (Complement)	State
0	0	No Change	No Change	Memory
0	1	0	1	Reset
1	0	1	0	Set
1	1	Invalid	Invalid	Undefined

Conclusion

The SR Latch using NOR gates is a fundamental sequential circuit that stores one bit of data. It is used in memory units, flip-flops, and other digital logic applications. However, the S = 1, R = 1 state is invalid, so additional logic (like an SR latch with enable or a clocked SR flip-flop) is used in practical applications to avoid this issue.