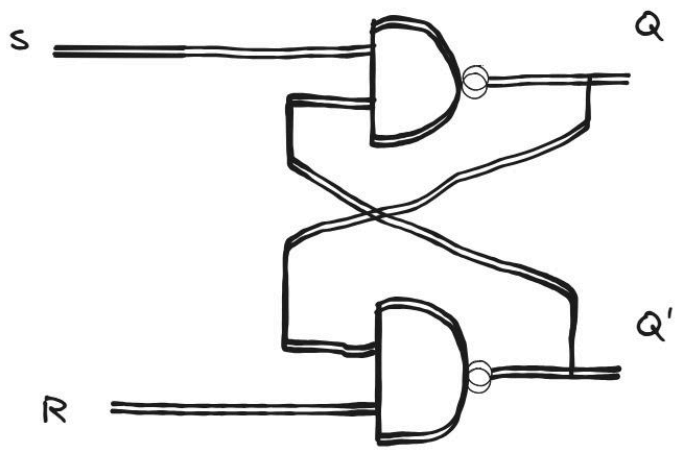
Explanation of the Image: SR Latch using NAND Gate



Explanation of the Image: SR Latch using NOR Gate

This image represents an SR (Set-Reset) Latch built using NAND gates. Like the NOR-based SR latch, this circuit is a sequential logic circuit that stores one bit of information. It has two inputs:

- S (Set): Used to set the output Q = 1.
- R (Reset): Used to reset the output Q = 0.

The circuit consists of two cross-coupled NAND gates, where:

- The output of each NAND gate is fed back into the other NAND gate as an input.
- The two outputs Q and Q' (Q complement) are always opposite to each other (Q' = NOT Q).

Working of SR Latch using NAND Gates

Case 1: S = 1, R = 1 (No Change / Memory State)

- If both S and R are 1, the latch remains in its previous state.
- The stored value does not change.
- Q and Q' remain in their previous states.

Case 2: S = 0, R = 1 (Set State)

- The upper NAND gate has inputs S = 0 and Q', so it outputs Q = 1.
- The lower NAND gate now has inputs R = 1, Q = 1, so it outputs Q' = 0.
- The latch is in the set state (Q = 1, Q' = 0).

Case 3: S = 1, R = 0 (Reset State)

- The lower NAND gate has inputs R = 0 and Q, so it outputs Q' = 1.
- The upper NAND gate now has inputs S = 1, Q' = 1, so it outputs Q = 0.
- The latch is in the reset state (Q = 0, Q' = 1).

Case 4: S = 0, R = 0 (Invalid / Undefined State)

- Both NAND gates output 1, causing an invalid state.
- This state is not allowed because it makes Q and Q' equal, violating the principle of an SR latch.

Truth Table of SR Latch using NAND Gate

S (Set)	R (Reset)	Q (Output)	Q' (Complement)	State
1	1	No Change	No Change	Memory
0	1	1	0	Set
1	0	0	1	Reset
0	0	Invalid	Invalid	Undefined

Conclusion

The SR Latch using NAND gates is another fundamental sequential circuit for storing one bit of data. It is commonly used in memory and digital circuits. However, the S = 0, R = 0 state is invalid, similar to the NOR-based SR latch, so additional logic (like a clocked SR latch) is used in practical applications to prevent this issue.