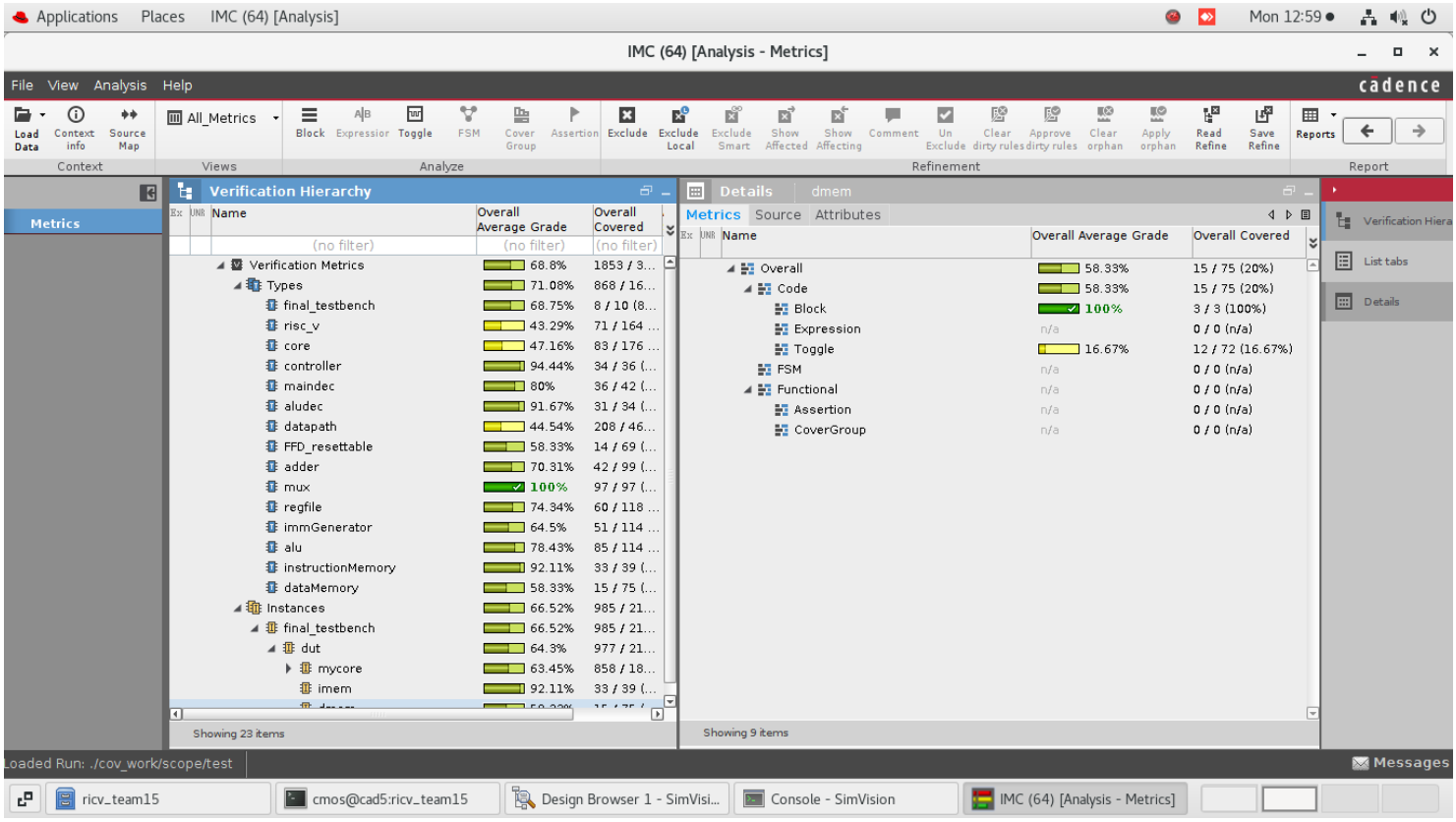
RISC-V
DSD Project

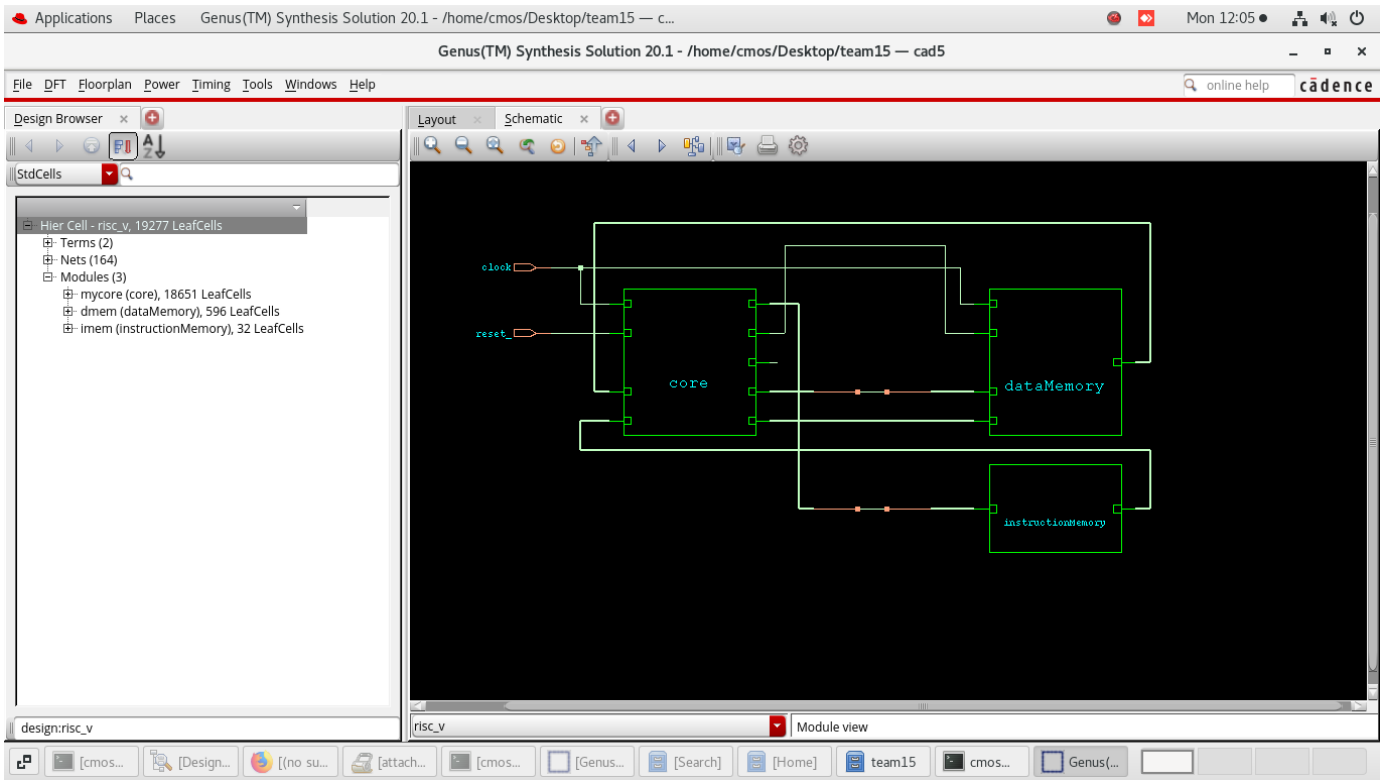
Team-15

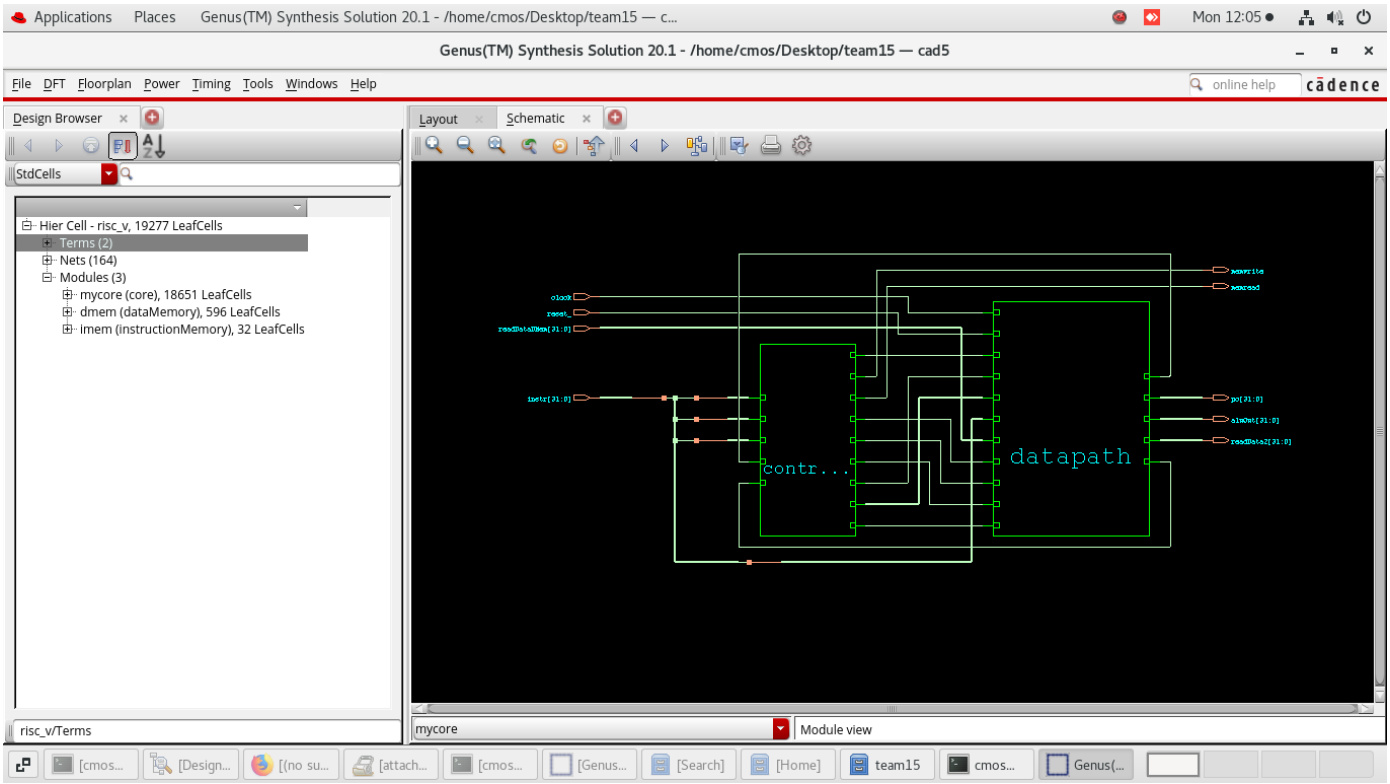
Sharath Vishwanath
Shashank D L
Sangmeshwari

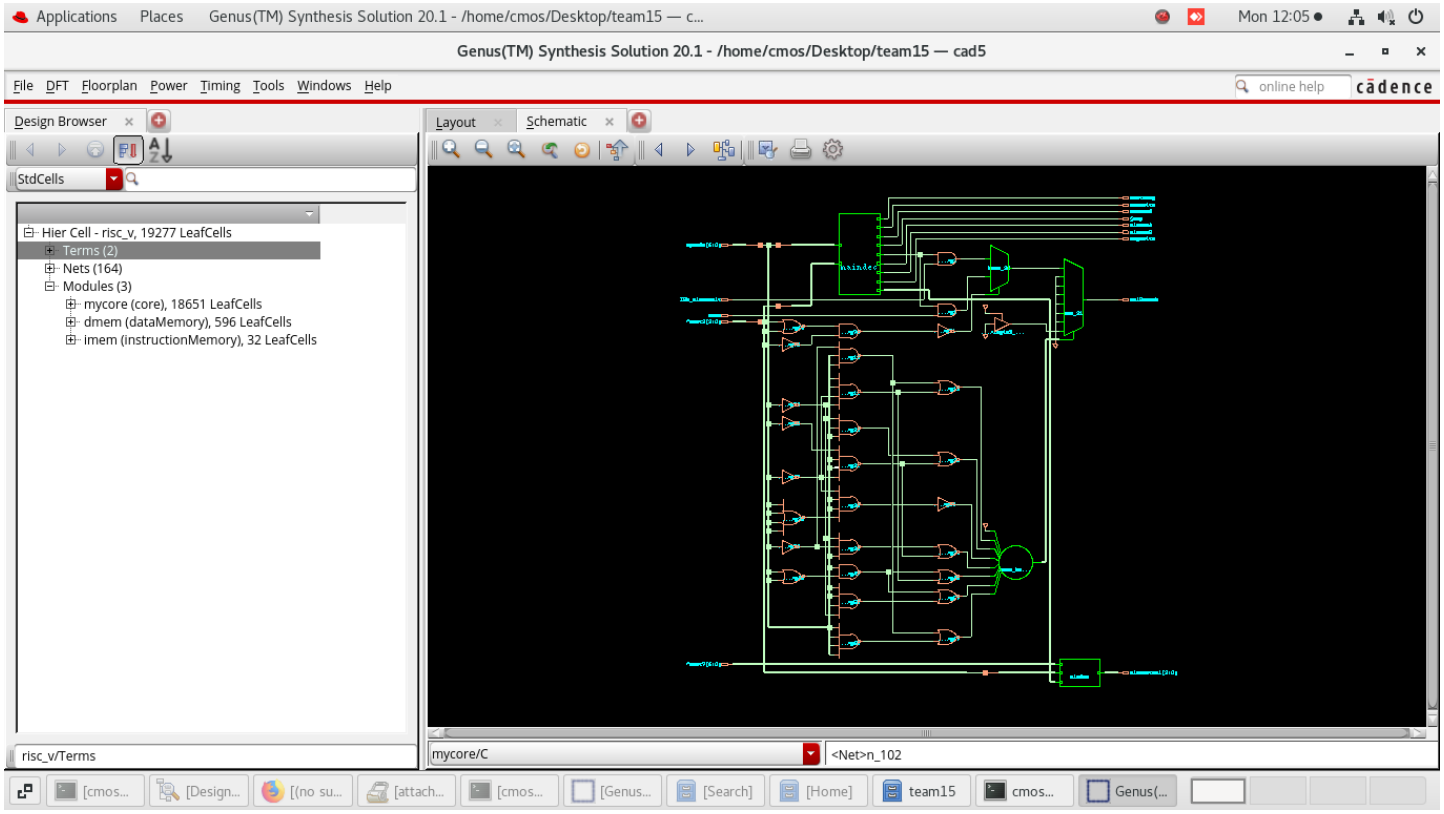
Coverage:

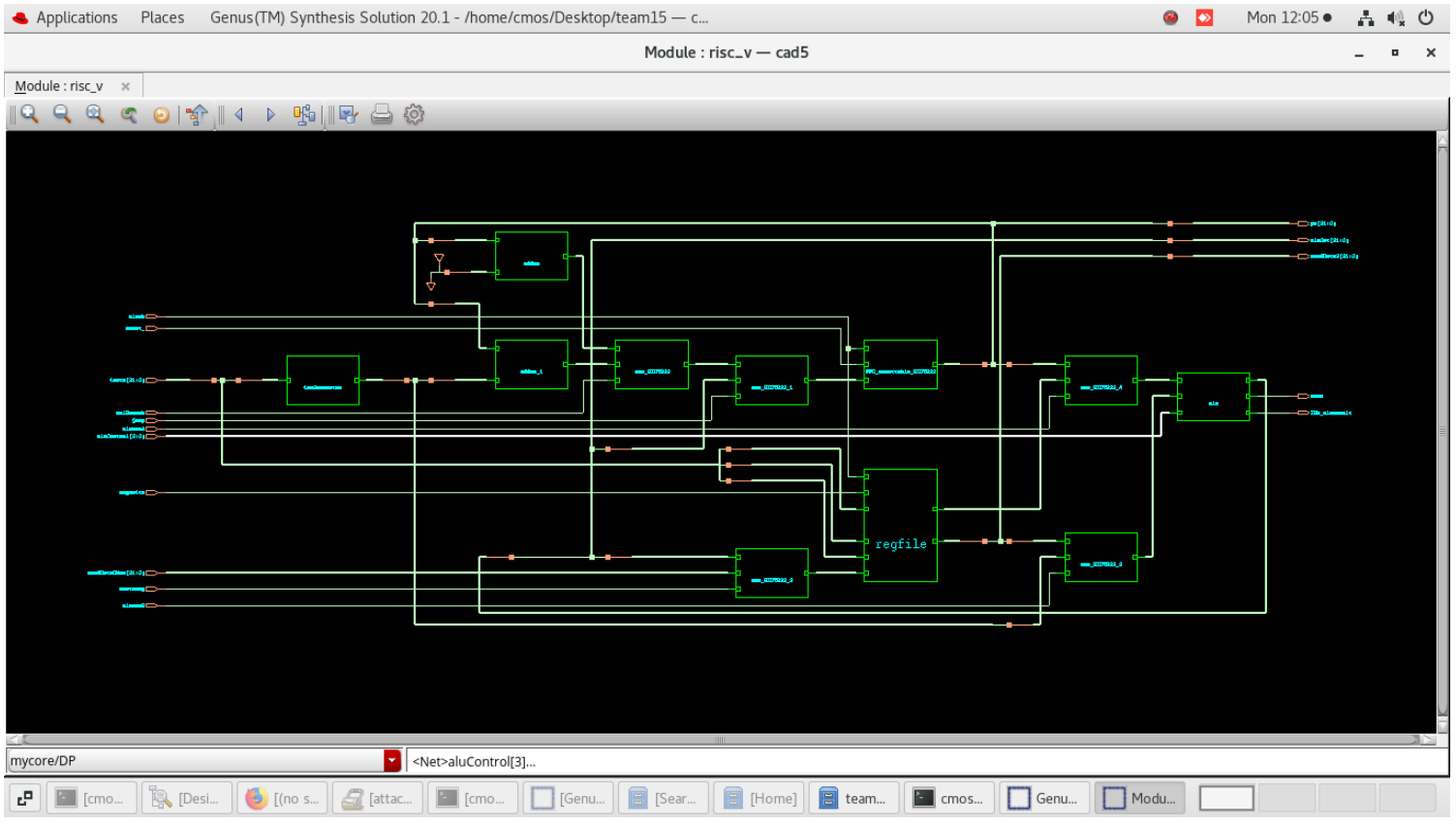


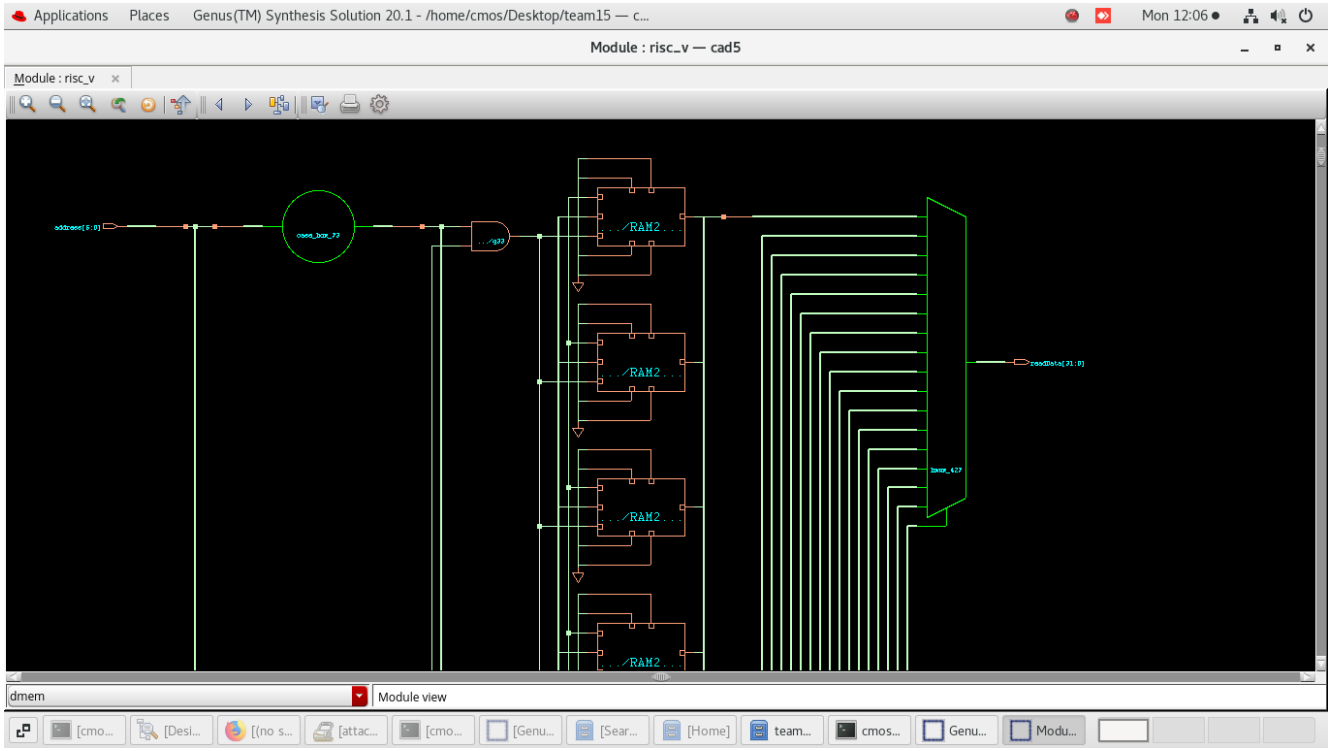
Synthesis:

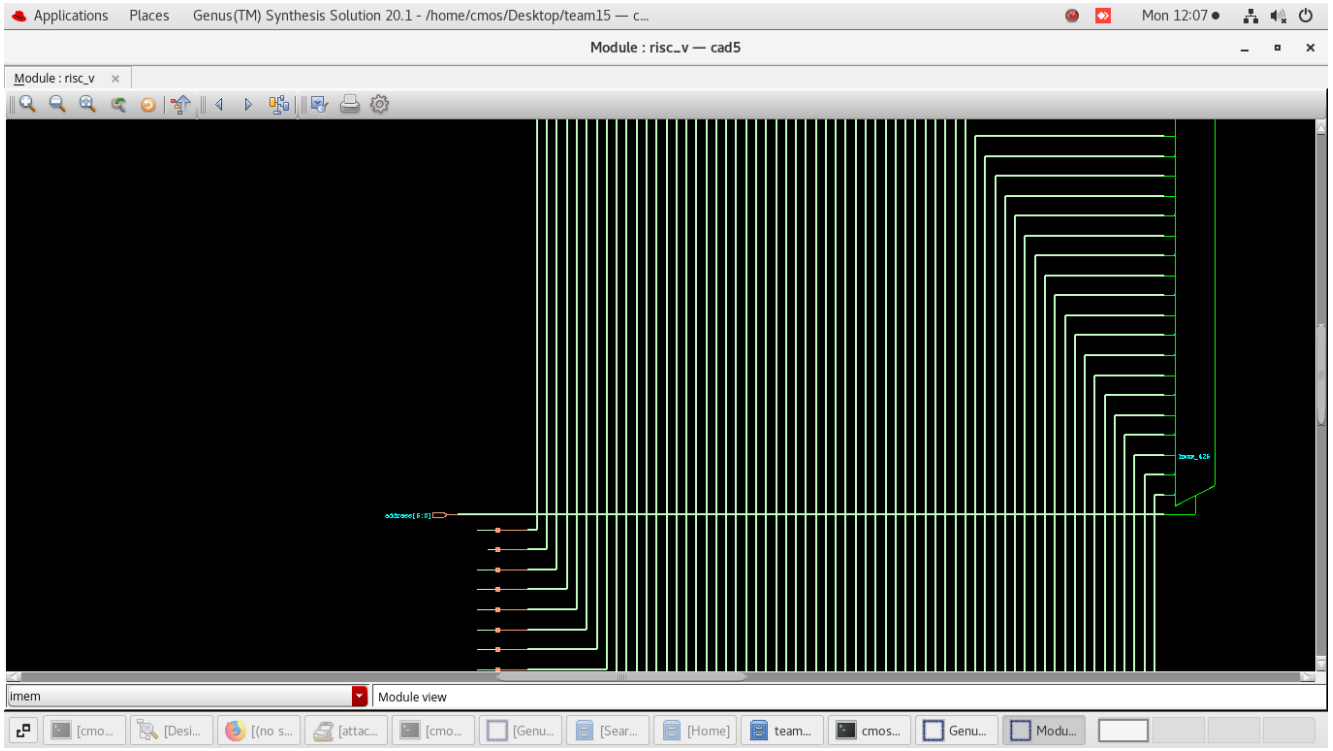

Applications
Places
Genus(TM) Synthesis Solution 20.1 - /home/cmos/Desktop/team15 — c...
Mon 12:05
Genus(TM) Synthesis Solution 20.1 - /home/cmos/Desktop/team15 — cad5
File DFT Floorplan Power Timing Tools Windows Help
online help
cadence
Design Browser
Layout
Schematic
StdCells
Hier Cell - risc_v, 19277 LeafCells
Terms (2)
Nets (164)
Modules (3)
mycore (core), 18651 LeafCells
dmem (dataMemory), 596 LeafCells
imem (instructionMemory), 32 LeafCells
clock
reset_
core
dataMemory
instructionMemory
design:risc_v
risc_v
Module view


Applications
Places
Genus(TM) Synthesis Solution 20.1 - /home/cmos/Desktop/team15 — c...
Mon 12:05
Genus(TM) Synthesis Solution 20.1 - /home/cmos/Desktop/team15 — cad5
File DFT Floorplan Power Timing Tools Windows Help
online help
cadence
Design Browser
Layout
Schematic
StdCells
Hier Cell - risc_v, 19277 LeafCells
Terms (2)
Nets (164)
Modules (3)
mycore (core), 18651 LeafCells
dmem (dataMemory), 596 LeafCells
imem (instructionMemory), 32 LeafCells
clock
reset_
contr...
datapath
risc_v/Terms
mycore
Module view

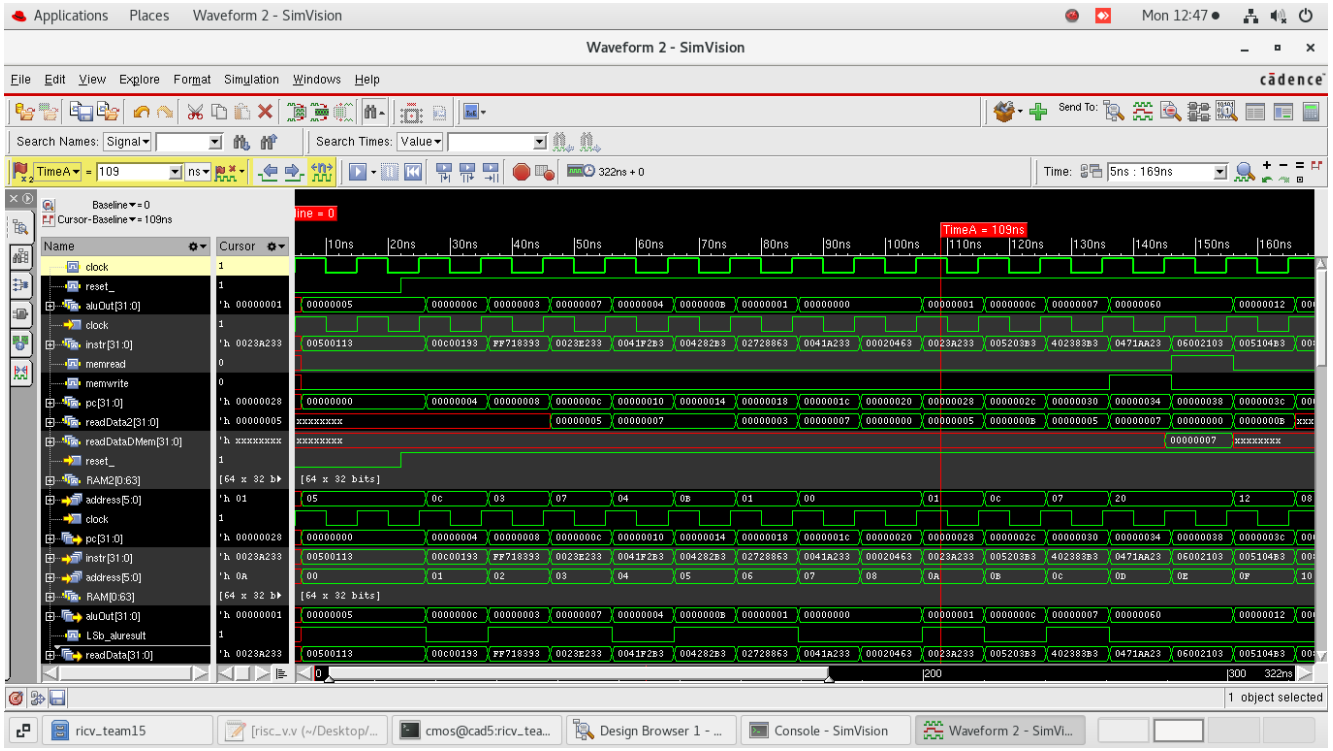

Applications Places Genus(TM) Synthesis Solution 20.1 - /home/cmos/Desktop/team15 — c...
Mon 12:05
Genus(TM) Synthesis Solution 20.1 - /home/cmos/Desktop/team15 — cad5
File DFT Floorplan Power Timing Tools Windows Help
online help
cadence
Design Browser
Layout
Schematic
StdCells
Hier Cell - risc_v, 19277 LeafCells
Terms (2)
Nets (164)
Modules (3)
mycore (core), 18651 LeafCells
dmem (dataMemory), 596 LeafCells
imem (instructionMemory), 32 LeafCells
risc_v/Terms
mycore/C
<Net>n_102
team15
Genus(...

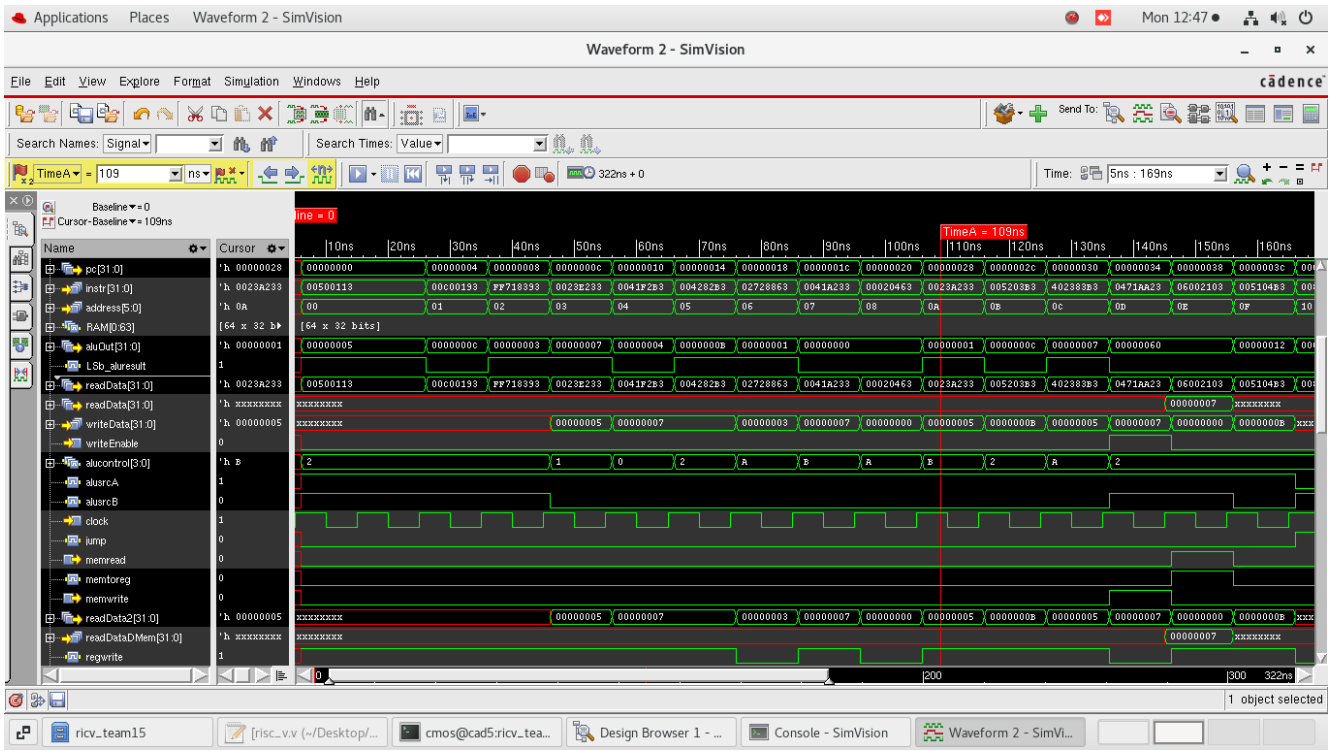

Applications Places Genus(TM) Synthesis Solution 20.1 - /home/cmos/Desktop/team15 — c...
Mon 12:05
Module : risc_v — cad5
Module : risc_v
regfile
mycore/DP
<Net>aluControl[3]...


Applications
Places
Genus(TM) Synthesis Solution 20.1 - /home/cmos/Desktop/team15 — c...
Mon 12:06
Module : risc_v — cad5
Module : risc_v
RAM2...
RAM2...
RAM2...
RAM2...
dmem
Module view

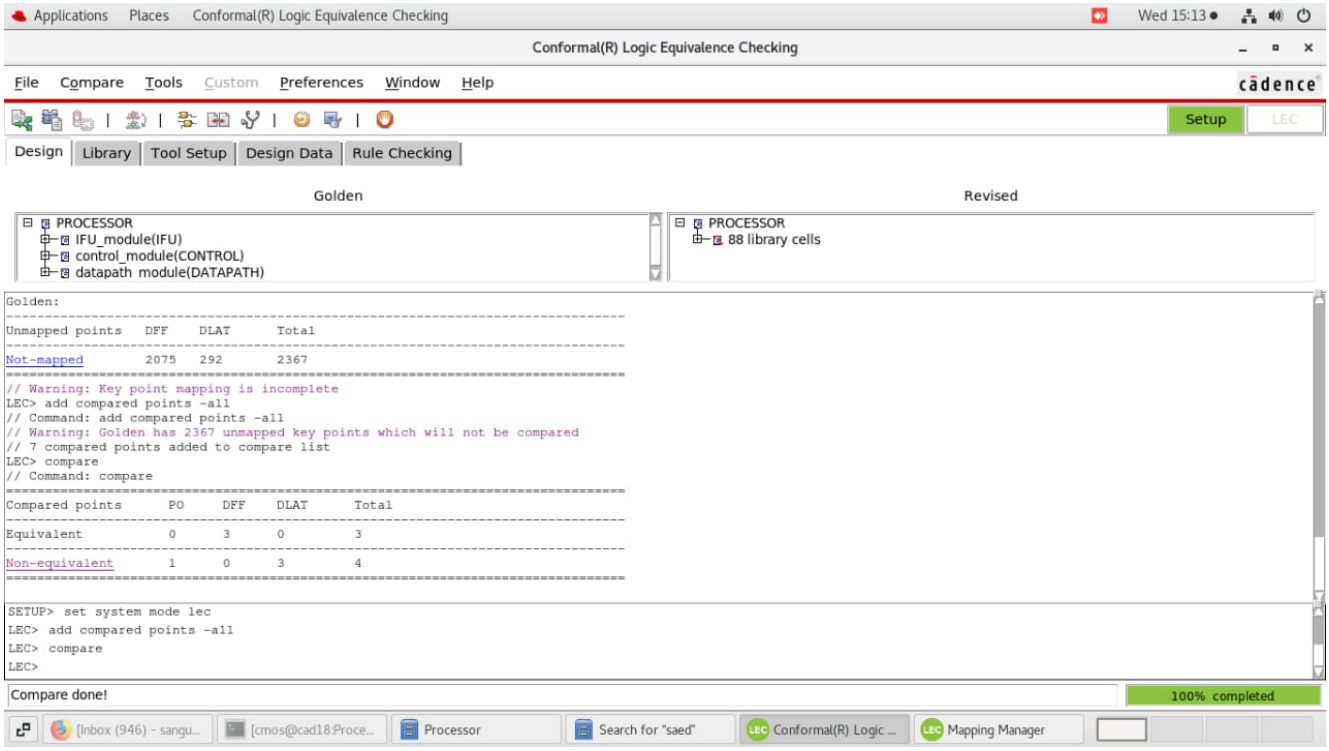

Applications
Places
Genus(TM) Synthesis Solution 20.1 - /home/cmos/Desktop/team15 — c...
Mon 12:07
Module : risc_v — cad5
Module : risc_v
imem
Module view

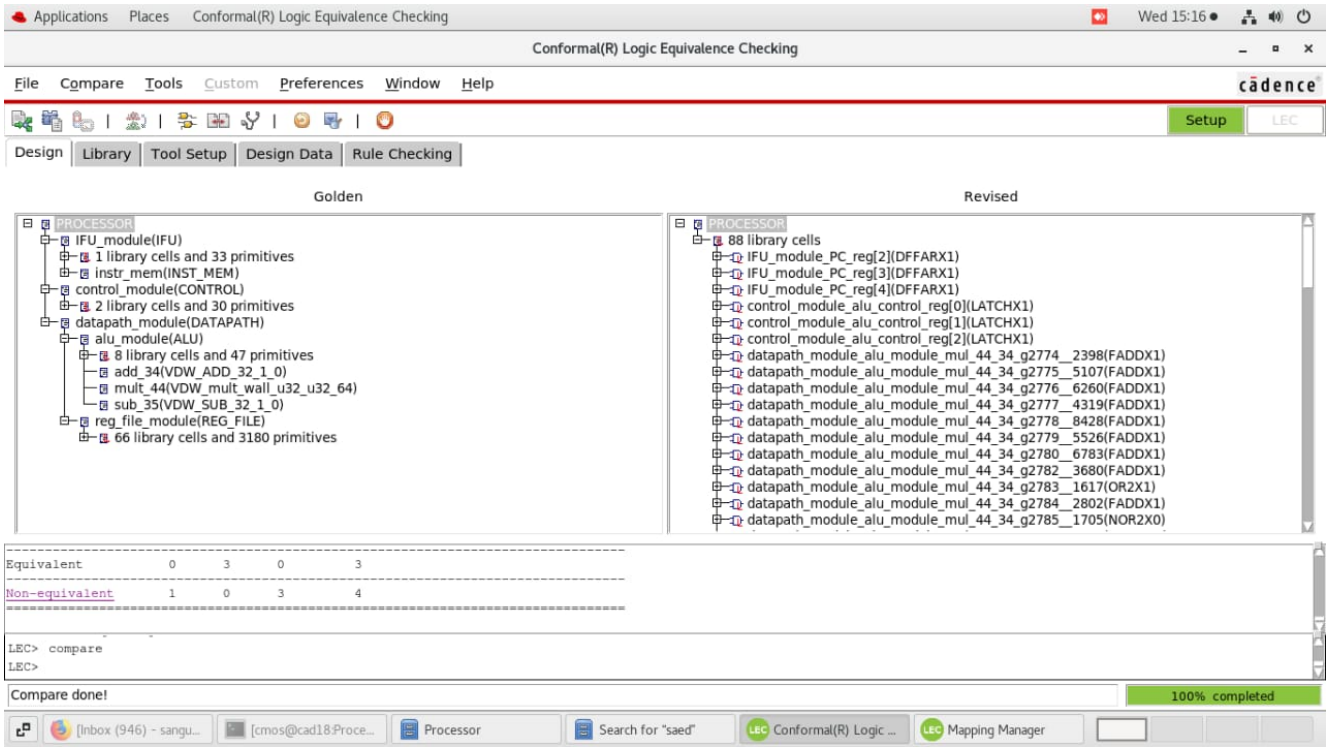
Simulation:

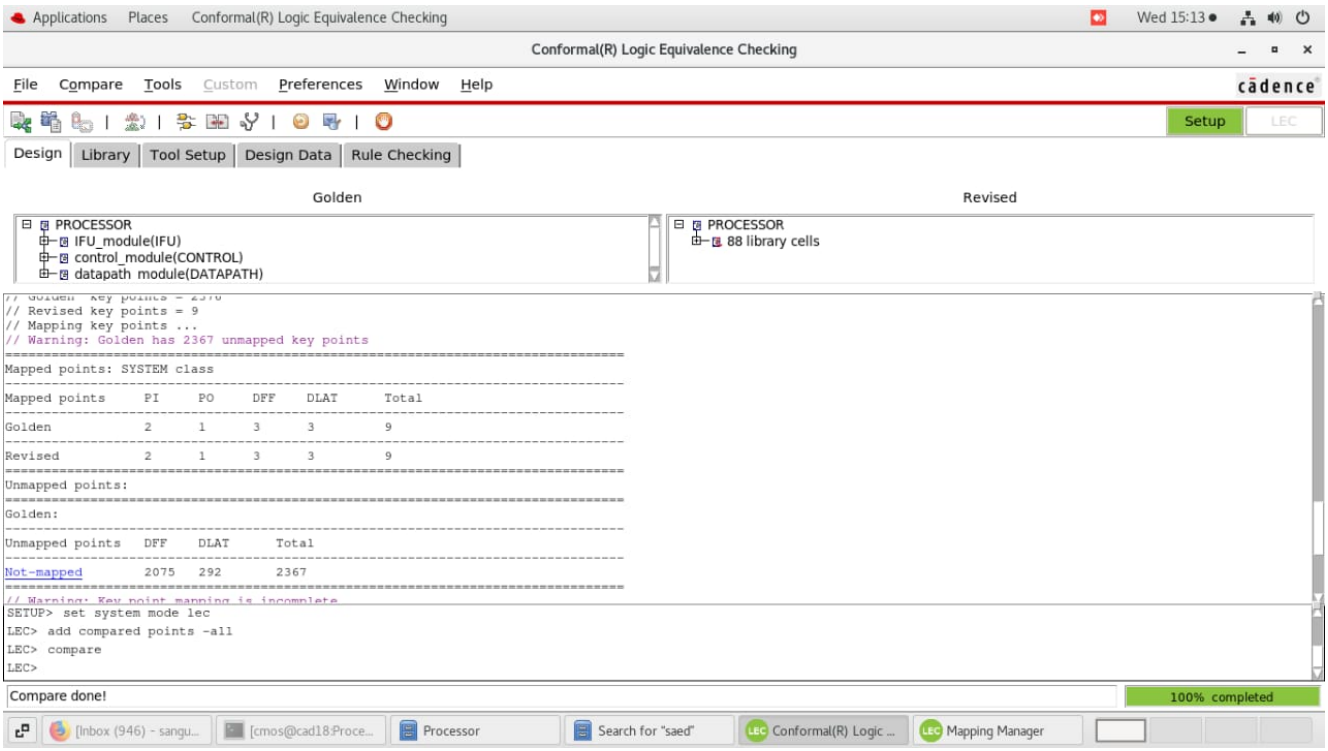

Applications Places Waveform 2 - SimVision
Mon 12:47
Waveform 2 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Search Names: Signal
Search Times: Value
TimeA = 109ns
Time: 5ns : 169ns
Name
Cursor
clock
reset_
aluOut[31:0]
instr[31:0]
memread
memwrite
pc[31:0]
readData2[31:0]
readDataDMem[31:0]
RAM2[0:63]
address[5:0]
RAM[0:63]
LSb_aluresult
readData[31:0]
1 object selected
ricv_team15
Design Browser 1 - ...
Console - SimVision
Waveform 2 - SimVi...

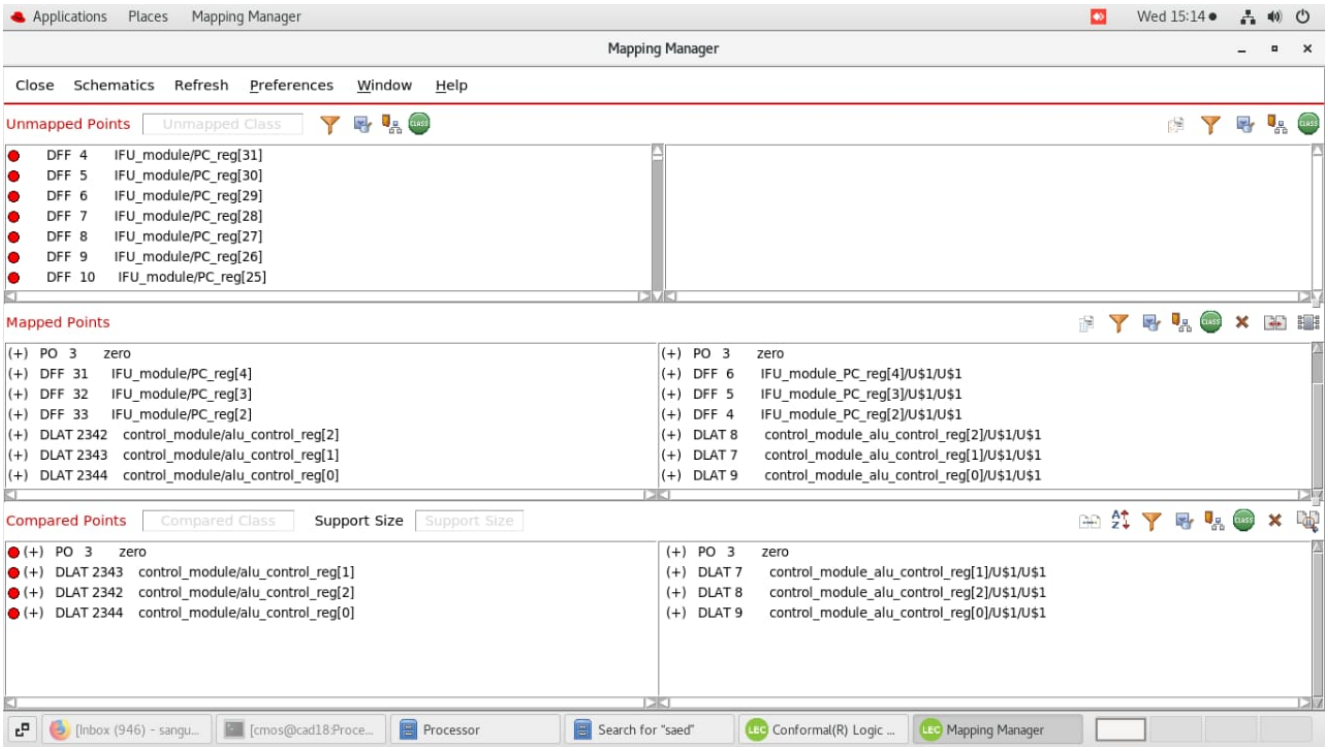

Applications Places Waveform 2 - SimVision
Mon 12:47
Waveform 2 - SimVision
File Edit View Explore Format Simulation Windows Help
cadence
Search Names: Signal
Search Times: Value
TimeA = 109ns
Time: 5ns : 169ns
Name
Cursor
pc[31:0]
instr[31:0]
address[5:0]
RAM[0:63]
aluOut[31:0]
LSb_aluresult
readData[31:0]
readData[31:0]
writeData[31:0]
writeEnable
alucontrol[3:0]
alusrcA
alusrcB
clock
jump
memread
memtoreg
memwrite
readData2[31:0]
readDataDMem[31:0]
regwrite
1 object selected
ricv_team15
Design Browser 1 - ...
Console - SimVision
Waveform 2 - SimVi...

Equivalence Checking:






Applications Places Conformal(R) Logic Equivalence Checking
Wed 15:13
Conformal(R) Logic Equivalence Checking
File Compare Tools Custom Preferences Window Help
cadence
Setup
LEC
Design Library Tool Setup Design Data Rule Checking
Golden
Revised
PROCESSOR
IFU_module(IFU)
control_module(CONTROL)
datapath module(DATAPATH)
PROCESSOR
88 library cells
// Revised key points = 9
// Mapping key points ...
// Warning: Golden has 2367 unmapped key points
Mapped points: SYSTEM class
Mapped points PI PO DFF DLAT Total
Golden 2 1 3 3 9
Revised 2 1 3 3 9
Unmapped points:
Golden:
Unmapped points DFF DLAT Total
Not-mapped 2075 292 2367
SETUP> set system mode lec
LEC> add compared points -all
LEC> compare
LEC>
Compare done!
100% completed
[Inbox (946) - sangu...
[cmos@cad18:Proce...
Processor
Search for "saed"
Conformal(R) Logic ...
Mapping Manager


Applications Places Mapping Manager
Wed 15:14
Mapping Manager
Close Schematics Refresh Preferences Window Help
Unmapped Points
Unmapped Class
DFF 4 IFU_module/PC_reg[31]
DFF 5 IFU_module/PC_reg[30]
DFF 6 IFU_module/PC_reg[29]
DFF 7 IFU_module/PC_reg[28]
DFF 8 IFU_module/PC_reg[27]
DFF 9 IFU_module/PC_reg[26]
DFF 10 IFU_module/PC_reg[25]
Mapped Points
(+) PO 3 zero
(+) DFF 31 IFU_module/PC_reg[4]
(+) DFF 32 IFU_module/PC_reg[3]
(+) DFF 33 IFU_module/PC_reg[2]
(+) DLAT 2342 control_module/alu_control_reg[2]
(+) DLAT 2343 control_module/alu_control_reg[1]
(+) DLAT 2344 control_module/alu_control_reg[0]
(+) PO 3 zero
(+) DFF 6 IFU_module_PC_reg[4]/U$1/U$1
(+) DFF 5 IFU_module_PC_reg[3]/U$1/U$1
(+) DFF 4 IFU_module_PC_reg[2]/U$1/U$1
(+) DLAT 8 control_module_alu_control_reg[2]/U$1/U$1
(+) DLAT 7 control_module_alu_control_reg[1]/U$1/U$1
(+) DLAT 9 control_module_alu_control_reg[0]/U$1/U$1
Compared Points
Compared Class
Support Size
Support Size
(+) PO 3 zero
(+) DLAT 2343 control_module/alu_control_reg[1]
(+) DLAT 2342 control_module/alu_control_reg[2]
(+) DLAT 2344 control_module/alu_control_reg[0]
(+) PO 3 zero
(+) DLAT 7 control_module_alu_control_reg[1]/U$1/U$1
(+) DLAT 8 control_module_alu_control_reg[2]/U$1/U$1
(+) DLAT 9 control_module_alu_control_reg[0]/U$1/U$1
[Inbox (946) - sangu...
[cmos@cad18:Proce...
Processor
Search for "saed"
Conformal(R) Logic ...
Mapping Manager

Power:

```
Instance: /risc_v
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total     Row%
  ------------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
    register     6.26777e-07  1.03365e-04  0.00000e+00  1.03991e-04   28.66%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
       logic     1.51429e-06  2.57331e-04  0.00000e+00  2.58845e-04   71.34%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
       clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00    0.00%
  ------------------------------------------------------------------------------
    Subtotal     2.14107e-06  3.60695e-04  0.00000e+00  3.62836e-04  100.00%
  Percentage           0.59%       99.41%        0.00%      100.00%  100.00%
  ------------------------------------------------------------------------------
```

Area:

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Nov 07 2023  05:00:29 pm
  Module:                 risc_v
  Operating conditions:   slow
  Interconnect mode:      global
  Area mode:              physical library
============================================================

             Instance                       Module          Cell Count  Cell Area  Net Area   Total Area
-------------------------------------------------------------------------------------------------------
risc_v                                                          19277  71332.460     0.000    71332.460
  mycore                              core                      18651  59897.901     0.000    59897.901
    C                                 controller                  128    655.996     0.000      655.996
      MainDec                         maindec                      49    351.334     0.000      351.334
        ctl_opcode_60_10              case_box                     24     76.490     0.000       76.490
        mux_controls_60_10            mux                          10    207.430     0.000      207.430
        ctl_funct3_67_24              case_box_1                    1      1.296     0.000        1.296
        mux_controls_67_24            mux_1                         2     10.371     0.000       10.371
        ctl_60_10                     case_box_4                    1      1.296     0.000        1.296
        mux_60_10                     mux_2                        10     51.857     0.000       51.857
      AluDec                          aludec                       18    120.568     0.000      120.568
        ctl_funct3_90_27              case_box_10                   4      7.779     0.000        7.779
        mux_alucontrol_90_27          mux_3                         3     31.114     0.000       31.114
        ctl_funct3_97_21              case_box_11                   1      1.296     0.000        1.296
        mux_alucontrol_97_21          mux_4                         1      5.186     0.000        5.186
        ctl_funct7_89_22              case_box_14                   1      2.593     0.000        2.593
        mux_alucontrol_89_22          mux_5                         4     31.114     0.000       31.114
        mux_alucontrol_83_10          bmux                          4     41.486     0.000       41.486
      mux_43_55                       bmux_20                       1      5.186     0.000        5.186
      ctl_43_30                       case_box_20                  30     72.600     0.000       72.600
      mux_43_30                       mux_21                        1     20.743     0.000       20.743
    DP                                datapath                  18523  59241.905     0.000    59241.905
      pcreg                           FFD_resettable_WIDTH32       33    291.698     0.000      291.698
      pcaddStart                      adder                      1137   2570.831     0.000     2570.831
        g1                            not_op                       32     41.486     0.000       41.486
        OUT_154_17:sub_163_28         sub_unsigned                459   1011.219     0.000     1011.219
        OUT_154_17:add_162_26         add_unsigned                188    383.745     0.000      383.745
        OUT_154_17:add_165_29         add_unsigned_24             426    968.437     0.000      968.437
        OUT_154_17:mux_OUT_159_14     bmux_22                      32    165.944     0.000      165.944
```

mux_224_21	bmux_22	32	165.944	0.000	165.944
pcJumpMux	mux_WIDTH32	32	165.944	0.000	165.944
mux_224_21	bmux_22	32	165.944	0.000	165.944
rf	regfile	1244	15209.778	0.000	15209.778
mux_regFile[readReg2]_147_54	bmux_33	32	2655.099	0.000	2655.099
mux_147_46	bmux_22	32	165.944	0.000	165.944
mux_regFile[readReg1]_146_54	bmux_33	32	2655.099	0.000	2655.099
mux_146_46	bmux_22	32	165.944	0.000	165.944
ctl_regDest_145_47	case_box_52	53	172.426	0.000	172.426
muxToWrite	mux_WIDTH32	32	165.944	0.000	165.944
mux_224_21	bmux_22	32	165.944	0.000	165.944
immg	immGenerator	43	506.906	0.000	506.906
ctl_opcode_240_10	case_box_53	12	24.632	0.000	24.632
mux_IMM_OUT_240_10	mux_37	31	482.274	0.000	482.274
muxsrcB	mux_WIDTH32	32	165.944	0.000	165.944
mux_224_21	bmux_22	32	165.944	0.000	165.944
muxsrcA	mux_WIDTH32	32	165.944	0.000	165.944
mux_224_21	bmux_22	32	165.944	0.000	165.944
alu	alu	14769	37262.142	0.000	37262.142
g1	and_op	32	82.972	0.000	82.972
g2	or_op	32	82.972	0.000	82.972
div_185_25	divide_unsigned	9947	24708.759	0.000	24708.759
mul_184_25	mult_unsigned	2869	7530.992	0.000	7530.992
sub_186_26	sub_unsigned	459	1011.219	0.000	1011.219
lt_187_27	lt_unsigned	221	482.274	0.000	482.274
eq_177_25	equal_unsigned_422	13	58.340	0.000	58.340
mux_187_27	bmux_20	1	5.186	0.000	5.186
ctl_aluctrl_180_14	case_box_56	25	59.636	0.000	59.636
mux_aluOut_180_14	mux_424	32	663.775	0.000	663.775
mux_177_25	bmux_20	1	5.186	0.000	5.186
g5	not_op_55	32	41.486	0.000	41.486
OUT_183_23:sub_199_31	sub_unsigned	459	1011.219	0.000	1011.219
OUT_183_23:add_198_29	add_unsigned	188	383.745	0.000	383.745
OUT_183_23:add_201_32	add_unsigned_24	426	968.437	0.000	968.437
OUT_183_23:mux_OUT_195_17	bmux_22	32	165.944	0.000	165.944
imem	instructionMemory	32	5310.199	0.000	5310.199
mux_RAM[address]_267_22	bmux_426	32	5310.199	0.000	5310.199
dmem	dataMemory	596	6124.360	0.000	6124.360
mux_RAM2[address]_257_22	bmux_427	32	1327.550	0.000	1327.550
ctl_address_259_21	case_box_73	36	108.901	0.000	108.901

Timing:

```
====================================================================
  Generated by:           Genus(TM) Synthesis Solution 20.11-s111_1
  Generated on:           Nov 15 2023  03:06:40 pm
  Module:                 core
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
====================================================================


Path 1: MET (0 ps) Setup Check with Pin DP_pcreg_q_reg[28]/CLK->D
          Group: clock
     Startpoint: (F) DP_rf_regFile_reg[20][21]/CLK
          Clock: (F) clock
       Endpoint: (R) DP_pcreg_q_reg[28]/D
          Clock: (R) clock

                     Capture       Launch
        Clock Edge:+   20000        10000
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=   20000        10000

             Setup:-      43
       Uncertainty:-     200
     Required Time:=   19757
      Launch Clock:-   10000
         Data Path:-    9757
             Slack:=       0

#-------------------------------------------------------------------------------------------------------------------
#         Timing Point          Flags    Arc    Edge   Cell     Fanout  Load Trans Delay Arrival Instance
#                                                                (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------------------------
  DP_rf_regFile_reg[20][21]/CLK -       -       F     (arrival)   1024     -   100     0   10000    (-,-)
  DP_rf_regFile_reg[20][21]/Q   -       CLK->Q  F     SDFFNX1        3   5.2    41   230   10230    (-,-)
  g128320/Q                     -       IN1->Q  F     AO22X1         1   2.1    44    76   10306    (-,-)
  g60818__4319/QN               -       IN1->QN R     NOR2X0         1   2.8    56    32   10338    (-,-)
  g60576__8428/QN               -       IN1->QN F     NAND2X1        1   2.1    38    27   10364    (-,-)
  g60431__4733/QN               -       IN1->QN R     NOR2X0         1   2.4    52    29   10393    (-,-)
  g129118/QN                    -       IN1->QN F     NAND3X0        1   5.1    61    39   10432    (-,-)
  g60369__7098/QN               -       IN1->QN R     NOR2X2         2   7.8    56    30   10462    (-,-)
  g60271__4319/QN               -       IN1->QN F     NOR2X2         1  10.0    87    35   10497    (-,-)
  g60270__6260/QN               -       IN1->QN R     NOR2X4        14  58.5   118    66   10563    (-,-)
  g60251/ZN                     -       INP->ZN F     INVX8         38 112.9    68    48   10611    (-,-)
  DP_alu_div_15_25_g126451/QN   -       IN2->QN R     NOR2X4         4   9.9    58    29   10640    (-,-)
  DP_alu_div_15_25_g126225/QN   -       IN1->QN F     NAND2X1        2   5.0    49    34   10674    (-,-)
  DP_alu_div_15_25_g125979/QN   -       IN2->QN R     NOR4X0         3   9.5   182    91   10765    (-,-)
  DP_alu_div_15_25_g125906/QN   -       IN1->QN F     NAND2X2        2   7.0    66    36   10801    (-,-)
  DP_alu_div_15_25_g125892/QN   -       IN1->QN R     NOR2X2         2   5.1    49    26   10827    (-,-)
  DP_alu_div_15_25_g125780/QN   -       IN1->QN F     NAND4X0        1   5.5    83    44   10871    (-,-)
  DP_alu_div_15_25_g125759/QN   -       IN1->QN R     NAND2X2        5  19.1    84    44   10915    (-,-)
  DP_alu_div_15_25_g125751/QN   -       IN1->QN F     NAND2X2        2  11.0    52    35   10950    (-,-)
  DP_alu_div_15_25_g125734/QN   -       IN1->QN R     NAND2X2        1   5.4    46    22   10972    (-,-)
  DP_alu_div_15_25_g125710/QN   -       IN1->QN F     NAND2X2        1   6.9    36    24   10996    (-,-)
  DP_alu_div_15_25_g125707/ZN   -       INP->ZN R     INVX2          1  11.8    35    22   11018    (-,-)
  DP_alu_div_15_25_g125690/QN   -       IN2->QN F     NOR2X4         7  18.3    47    37   11055    (-,-)
  DP_alu_div_15_25_g125643/Q    -       IN4->Q  F     OA22X1         1   1.3    29    62   11117    (-,-)
  g129051/Q                     -       IN3->Q  F     AND3X2         4  24.7    73   114   11231    (-,-)
  DP_alu_div_15_25_g125604/ZN   -       INP->ZN R     INVX4          6  20.9    41    24   11256    (-,-)
  DP_alu_div_15_25_g125595/QN   -       IN1->QN F     NAND2X1        1   5.3    62    32   11288    (-,-)
  DP_alu_div_15_25_g125535/QN   -       IN2->QN R     NAND2X2        2   8.7    48    33   11320    (-,-)
  DP_alu_div_15_25_g125523/QN   -       IN1->QN F     NOR2X2         1   5.1    49    27   11347    (-,-)
  DP_alu_div_15_25_g125521/QN   -       IN1->QN R     NOR2X2         1  11.9    65    35   11382    (-,-)
  DP_alu_div_15_25_g125509/QN   -       IN1->QN F     NOR2X4         1  10.0    55    29   11411    (-,-)
  DP_alu_div_15_25_g125505/QN   -       IN1->QN R     NOR2X4         3  14.9    52    29   11439    (-,-)
  DP_alu_div_15_25_g125494/QN   -       IN2->QN F     NAND2X2        3  11.4    55    31   11471    (-,-)
  DP_alu_div_15_25_g125456/QN   -       IN1->QN R     NAND3X0        1  10.5   108    55   11525    (-,-)
  DP_alu_div_15_25_g125453/QN   -       IN1->QN F     NAND2X4        4  28.1    65    44   11569    (-,-)
  DP_alu_div_15_25_g125397/CO   -       CI->CO  F     FADDX1         2   8.4    54   102   11671    (-,-)
  DP_alu_div_15_25_g125393/QN   -       IN1->QN R     NAND2X2        1   5.4    47    22   11693    (-,-)
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  DP_alu_div_15_25_g116394/QN   -       IN1->QN R     NAND2X1        2   4.7    58    34   18405    (-,-)
  DP_alu_div_15_25_g116235/QN   -       IN1->QN F     NAND2X1        3  10.3    99    47   18451    (-,-)
  DP_alu_div_15_25_g116198/QN   -       IN2->QN R     NAND2X2        3   6.2    53    34   18486    (-,-)
  DP_alu_div_15_25_g116181/ZN   -       INP->ZN F     INVX0          1   2.8    35    26   18512    (-,-)
  DP_alu_div_15_25_g116119/QN   -       IN1->QN R     NAND2X1        1   2.8    57    24   18536    (-,-)
  DP_alu_div_15_25_g116094/QN   -       IN1->QN F     NAND2X1        1   2.8    40    29   18564    (-,-)
  DP_alu_div_15_25_g115888/QN   -       IN1->QN R     NAND2X1        1   1.7    40    22   18586    (-,-)
  g128093/Q                     -       IN2->Q  R     OA21X1         1   5.4    46    78   18665    (-,-)
  DP_alu_div_15_25_g115704/QN   -       IN1->QN F     NAND2X2        1   2.8    30    19   18684    (-,-)
  DP_alu_div_15_25_g115665/QN   -       IN2->QN R     NAND2X1        1   5.4    48    31   18714    (-,-)
  DP_alu_div_15_25_g115649/QN   -       IN1->QN F     NAND2X2        1   5.3    34    22   18737    (-,-)
  DP_alu_div_15_25_g115614/QN   -       IN2->QN R     NAND2X2        1   5.4    35    24   18761    (-,-)
  DP_alu_div_15_25_g115612/QN   -       IN1->QN F     NAND2X2        1   5.3    32    21   18782    (-,-)
  DP_alu_div_15_25_g115603/QN   -       IN2->QN R     NAND2X2        1   5.4    35    24   18806    (-,-)
  DP_alu_div_15_25_g115602/QN   -       IN1->QN F     NAND2X2        1   5.3    29    21   18826    (-,-)
  DP_alu_div_15_25_g115597/QN   -       IN2->QN R     NAND2X2        1   5.4    33    23   18849    (-,-)
  g5101/QN                      -       IN1->QN F     NAND2X2        1  10.5    74    27   18876    (-,-)
  g5004/QN                      -       IN1->QN R     NAND2X4        3  10.6    39    24   18900    (-,-)
  g128129/Q                     -       IN1->Q  F     XOR2X1         1   2.8    37    67   18967    (-,-)
  g128128/Q                     -       IN1->Q  F     OR3X1          2  12.4    53    76   19042    (-,-)
  g19419/QN                     -       IN1->QN R     NAND2X4        2  16.1    47    26   19068    (-,-)
  g19407/QN                     -       IN2->QN F     NAND2X2        9  20.0    65    40   19108    (-,-)
  g19390/QN                     -       IN1->QN R     NOR2X0         2   4.2    72    41   19149    (-,-)
  addinc_ADD_UNS_OP_2_g5620/Q   -       IN1->Q  R     AND2X1         3   7.4    46    70   19220    (-,-)
  addinc_ADD_UNS_OP_2_g5449/QN  -       IN1->QN F     NAND2X1        2   4.4    44    31   19251    (-,-)
  g128568/QN                    -       IN3->QN R     NAND3X0        1   2.8    58    40   19290    (-,-)
  addinc_ADD_UNS_OP_2_g5400/QN  -       IN1->QN F     NAND2X1        1   2.8    41    29   19319    (-,-)
  addinc_ADD_UNS_OP_2_g5377/QN  -       IN1->QN R     NAND2X1        2   5.1    54    29   19348    (-,-)
  addinc_ADD_UNS_OP_2_g5370/ZN  -       INP->ZN F     INVX0          3   7.2    55    41   19389    (-,-)
  addinc_ADD_UNS_OP_2_g5329/QN  -       IN2->QN R     NOR2X0         1   2.5    58    34   19423    (-,-)
  addinc_ADD_UNS_OP_2_g5320/QN  -       IN1->QN F     NOR2X0         1   2.5    48    34   19457    (-,-)
  addinc_ADD_UNS_OP_2_g5291/QN  -       IN2->QN R     NAND3X0        4  10.9   101    59   19516    (-,-)
  addinc_ADD_UNS_OP_2_g5256/QN  -       IN1->QN F     NAND2X1        1   2.8    51    34   19550    (-,-)
  addinc_ADD_UNS_OP_2_g5245/QN  -       IN1->QN R     NAND2X1        1   3.9    55    28   19578    (-,-)
  addinc_ADD_UNS_OP_2_g5226/Q   -       IN1->Q  R     XOR2X1         1   1.9    34    64   19642    (-,-)
  g39551/Q                      -       IN3->Q  R     AO22X1         1   1.7    46    60   19703    (-,-)
  g39727/Q                      -       IN1->Q  R     AND2X1         1   1.7    28    54   19757    (-,-)
  DP_pcreg_q_reg[28]/D          <<<     -       R     DFFX1          1     -     -     0   19757    (-,-)
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