CS & IT ENGINEERING

Computer Organization & Architecture

1500 Series

Lecture No.- 06

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Recap of Previous Lecture

Topic Pipeline

Topic Pipeline Hazards

Topics to be Covered

- Topic: Cache Memory
- Topic: Cache mapping Technique
- Topic: Cache Replacement Algorithm
- Topic: Cache Updating Technique

[MCQ]

#Q. Consider the main memory of a computer system consisting of "2^m" blocks, and cache "2m" blocks, and cache has "2m" blocks. If the two-way set associative mapping scheme is used, the k^{th} block of main memory to be placed in _____ set?

#CM Blocks (#CM Lines) = 2M

2 Way Set Associ.

A 2^m mod 2m

B k mod 2^m

C 2^m mod m

Ans (D)

D k mod m

#SET (S) = $\frac{2M}{2}$ = M

K MOD S = i

K MOD M = i

k: MM Block No.

S: #SET

i: set Number

[NAT]

#Q. Number of chips (128 × 8 RAM) needed to provide a memory capacity of 2048 bytes is _____

Memory Size = 2048 Byte ⇒ 2048 × 8 bit

RAM CHIP Size = 128 × 8

$$\#\text{RAM CHIP} = \frac{(2^{11})\ 2048 \times 8}{(2^{7})\ 128 \times 8} \Rightarrow\Rightarrow 2^{4} = 16 \text{ RAM CHIP Ans}$$

Ans (16)

[MCQ]

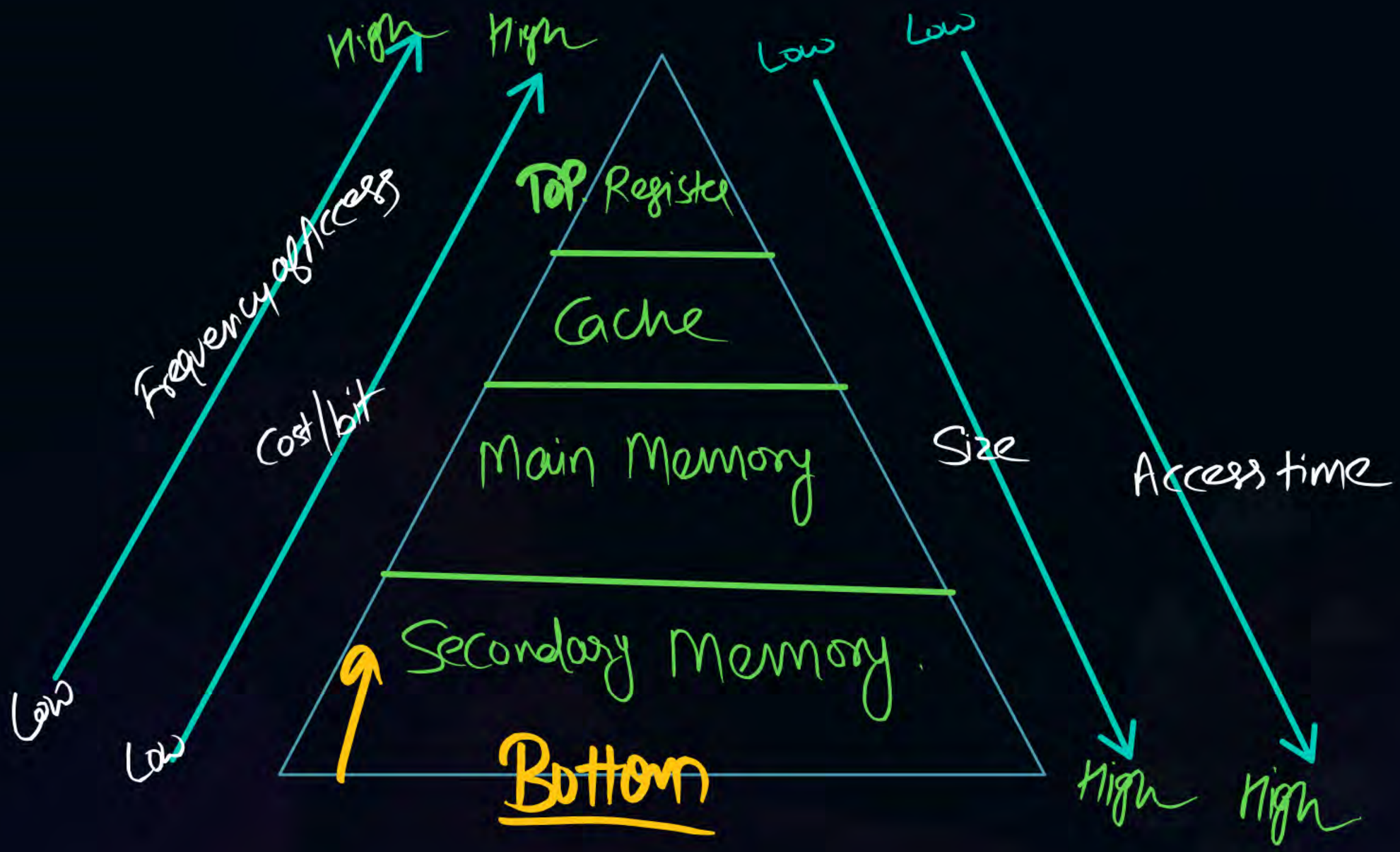
#Q. Match List-I and List-II using memory hierarchy from bottom to top and find the best suitable matching for List-I.

SM to Register.

List-I		List-II	
a.	size — 2	1.	Increase
b.	Cost/bit — 1	2.	Decrease
c.	Access time — 2	3.	No change
d.	Frequency of access — 1		

Ans (D)

	a	b	c	d
A	1	1	2	2
B	1	2	1	2
C	2	2	1	1
D	2	1	2	1


High
High
Low
Low
Frequency of Access
Cost/bit
Low
Low
TOP Register
Cache
Main Memory
Secondary Memory
Bottom
Size
Access time
High
High

[MCQ]

#Q. How many 128 × 8 bit RAMs are required to design 32K × 32 bit RAM

A 512

B 1024

C 128

D 32

Ans (B).

$$\frac{2^8(2^4)\,32K \times 32}{(2^7)\,128 \times 8} \Rightarrow 2^8 \times 4 = 2^{10}$$

1024

[MCQ]

H.W

#Q. Find the correct order of True (T) and False (F) for the following statements.

1. DRAM consists of internal flip-flops.
2. SRAM consists of capacitors.
3. SRAM is easier to use than DRAM.
4. SRAM has shorter read and write cycles than that of DRAM.

A F F T F

B T T T T

C F F T T

D T T F F

[MCQ]

#Q. Construct 128K × 16 bit RAM from 128 × 16 bit RAM chip. What is the size of decoder is required ?

A 9×512

B 11×2048

C 10×1024

D 7×128

Ans (c)

$\frac{128K \times 16}{128 \times 16} = 2^{10}$ (1K)

n bit

$n \times 2^n$

10×2^{10}

10×1024

[MCQ]

#Q. Consider a 2 way set associative cache, consisting of 4 blocks. Assume that LRU block replacement policy is used. The number of cache misses for the following sequence of block address is

10 3 5 7 3 7 12 24 10 3

#SET = #LINES / N-Way

= 4/2 = 2

A 5

B 6

C 7

D 8

Ans (D)


K mod S[2]
10 %2 = 0 M
3 %1 = 1 M
5 = 1 M
7 = 1 M
3 = 1 M
7 = 1 → HIT
12 = 0 → M
24 = 0 M
10 = 0 Miss
3 = 1 HIT
8 Miss
2 Hit
SET 0
10 24
12 10
SET 1
3 7
5 3

[NAT]

#Q. If a Cache Memory is designed as a direct mapped cache, the length of the TAG field is 10 bits. If the cache is now designed as 8-way set associative cache, the length of the TAG is __13__ bits. Ans

N-way

Tag bit in Set Associative = Tag bits in Direct Mapping $+\lceil \log_2 N \rceil$

Tag bit in 8 Way set Associative = $10 + \lceil \log_2 8 \rceil$

$\Rightarrow 10+3$

$\Rightarrow$ 13 bits Ans

Direct mapping $\Rightarrow$ Tag $= \frac{\text{MM Size}}{\text{CM Size}}$

$\Downarrow$

Tag bit $= \lceil \log_2 \text{tags} \rceil$

[MCQ]

#Q. In memory hierarchy of cache and main memory, the main memory takes 100 nsec to return the first word (32 bit) of a line and 10 nsec to return each subsequent word. The cache memory has a hit rate of 95%, 128 bytes lines and cache hit latency of 5 nsec. The T_{miss} for this cache will be _____

(Assume that the cache waits until the line has been fetched into the cache and then re-executes the memory operation, resulting in a cache hit. Neglect the time required to write the line into the cache once it has been fetched from the main memory. Also assume that the cache takes the same amount of time to detect that a miss has occurred as to handle a cache hit.)

A 410 ns

Ans (B).

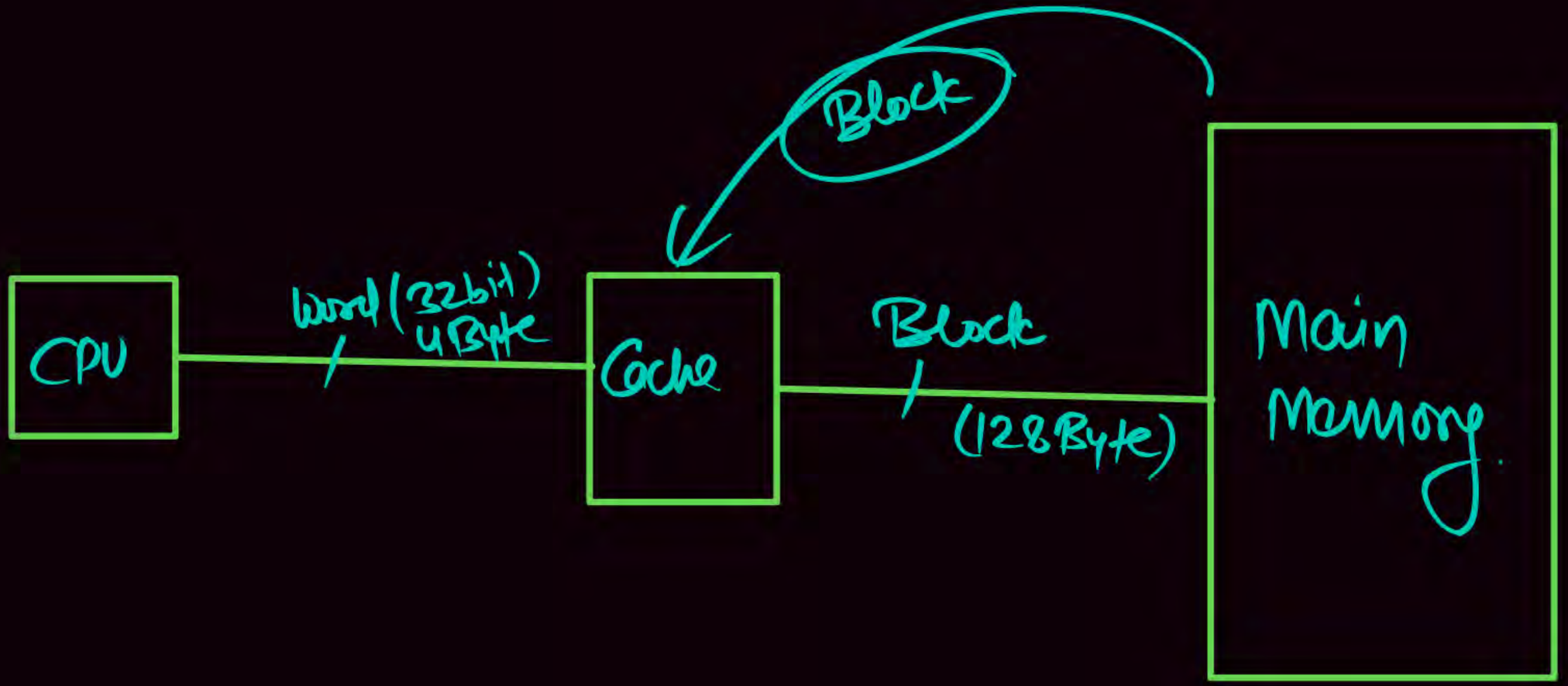
B 420 ns

C 240 ns

D 540 ns

$$T_{avg} = h * t_c + (1-h)\{t_c + t_m\}$$

Twiss


Block
CPU
Word (32bit)
4Byte
Cache
Block
(128Byte)
Main
Memory

Ma = 100nsec for 1 Word (32bit)
& 10nsec for Subsequent Word

Cache Access = 5nsec.

Hit Ratio = 95%.

Line (Block Size) = 128 Byte

Twiss ?

$$\#Words = \frac{128\,Byte}{4\,Byte(32bit)} = 32\,Words$$

$$T_{wiss} = 5 + [1(100) + 31(10)] + 5$$

$$= 5 + 410 + 5$$

$$= 420nsec.$$ Ans

[MCQ]

#Q. Which of the following is not true regarding set associative cache when cache size is kept fixed?

A. Decreasing associativity increases set index size. True.

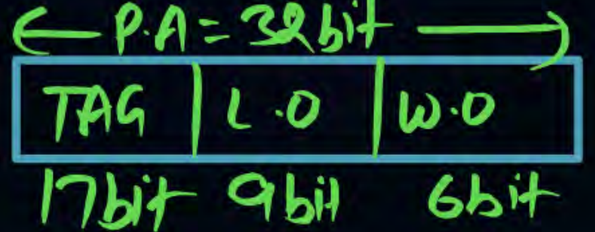
B. Decreasing associativity decreases tag metadata True

C. Increasing associativity increases tag metadata. True.

D. Increasing associativity increases number of sets False.

Ans (D).

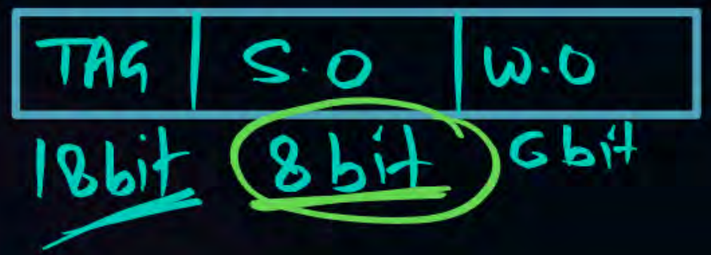
Direct map



@ 4 way ⟶ 2 way.

2 way Set Associative

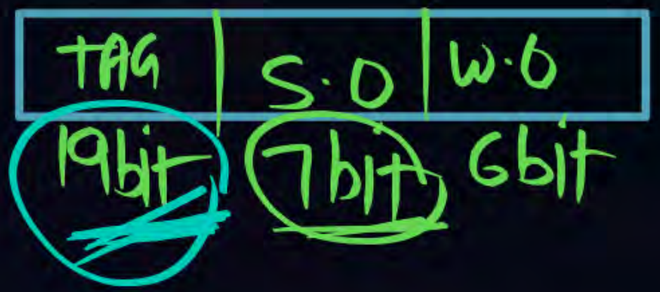
$\#SET = \frac{2^9}{2^1} = 2^8$ set



Tag memory = # Lines × Tag bit

4 way Set Associative

$\#SET = \frac{2^9}{2^2} = 2^7$ set



[MCQ]

#Q. A system uses 2-level cache. For every 100 memory accesses generated by CPU, 90 hits in L_1 cache and 8 hits in L_2 cache. Access times of L_1, L_2 and main memory are 10, 20 and 100 nanoseconds respectively. What is the average memory access time (in nanoseconds)?

A 14 ns

B 16 ns

C 21.2 ns

D None of these

Ans (A)

$1-h_1=0.1$ $\quad h_1 = \frac{90}{100} = 0.9$

$1-h_2=0.2$ $\quad h_2 = \frac{8}{10} = 0.8$

$L_1 = t_1 = 10\,ns$

$L_2 = t_2 = 20\,ns$

$M_a = 100\,ns$

$$T_{avg} = h_1 t_1 + (1-h_1) h_2 (t_2 + t_1) + (1-h_1)(1-h_2)(t_m + t_2 + t_1)$$

OR

$$T_{avg} = t_1 + (1-h_1)\left[t_2 + (1-h_2) t_m\right]$$

$$\Rightarrow 10 + 0.1\left[20 + 0.2(100)\right] \Rightarrow 10 + 0.1\left[20+20\right]$$

$$= 10 + 0.1[40]$$

$T_{avg} = 14\,nsec.$

$$T_{avg} = h * t_c + (1-h)(t_m + t_c)$$

OR

$$\cancel{h t_c} + t_m + t_c - h t_m - \cancel{h t_c}$$

$$t_c + (1-h) t_m$$

$$\boxed{T_{avg} = t_c + (1-h)\, t_m}$$

[MCQ]

#Q. If each address space represents one byte of storage space, how many address lines are needed to access RAM chips arranged in a 4 × 6 array, where each chip is 8 K × 4 bits?

A 13

B 15

C 16

D 17

Ans(D)

$8K \times 4 \Rightarrow 2^{13} \times 2^{2} = 2^{15}$ bits

Byte $\Rightarrow \frac{2^{15} \text{ bits}}{8 \text{ bits}} = 2^{12}$ Byte

12 bit

$4 \times 6 =$ 24 RAM → 5 bit

$5 + 12 = 17$ bit

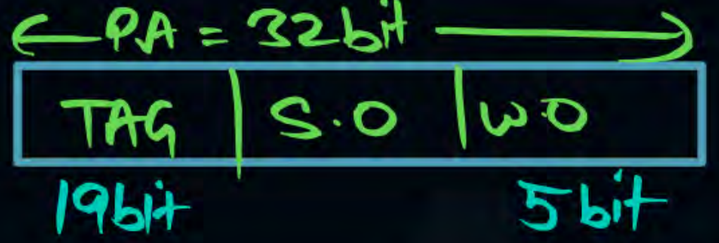
[NAT]

Consider a 64 kB (1 kB = 2^{10}Byte), N-way set associative cache with cache block size of 32 byte. Assume that the cache is Byte addressable and the address sent by the processor is of 32 bit. If the tag field size is 19 bit then the value of N is 8 Ans

Cache Size = 64kB (2^{16} Byte)

Block Size = 32B (2^5 Byte) ⇒ W.O = 5bit

P.A = 32bit, TAG = 19bit



$$\#LINES = \frac{CM\ Size}{Block\ size} = \frac{2^{16}B}{2^5B} = 2^{11}\ Lines$$

S.O = 32 − (19 + 5)

S.O = 8bit

$$\#SET = 2^8\ Sets$$

$$\#SET = \frac{\#LINES}{N\text{-}Ways}$$

$$2^8 = \frac{2^{11}}{N\text{-}Way}$$

$$N\text{-}Way = \frac{2^{11}}{2^8} = 2^3 \Rightarrow$$ 8 Way set Associative

[MCQ]

#Q. Consider an 8-way set associative cache of size 64 kB. Block size is 32 bytes CPU generates 32-bit addresses. What is the size of tag comparators?

A 17

B 18

C 19

D 20

Ans (C)

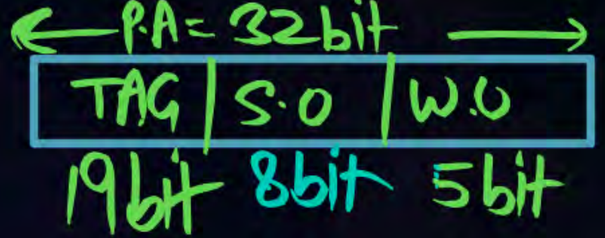
2^5

#LINE = $\frac{64\,KB}{32B}$ = 2K = 2^{11} Lines

8 way

#SET = $2^{11}/2^3 = 2^8$

S.O = 8bit



[MCQ]

If a 8 way set associative cache is made up of 64 bit words. 8 words per line and 8192 sets. What is the size of cache memory?

8 Byte

Block Size = 8 words

8 way set Associative

8192 [2^{13}] Set

Blocks size = 8 words (1 word = 64 bit [8 Byte])

Block Size = 8 × 8B = (64 Byte) = 2^6 Byte

$\#SET = \frac{\#LINES}{N\text{-ways}} \Rightarrow$

$8192\ (2^{13}) = \frac{\#LINE}{8\ (2^3)}$

$\#lines = 2^{13} \times 2^3 = 2^{16}$ lines

A 1 Mbyte

B 2 Mbyte

C 4 Mbyte

D 8 Mbyte

Ans [C].

$$\#LINES = \frac{CM\,Size}{Block\,Size}$$

$$CM\,Size = \#Lines \times Block\,Size$$

$$\Rightarrow 2^{16} \times 2^{6}\,Byte$$

$$\Rightarrow 2^{22}\,Byte \Rightarrow 4MByte$$ Ans

[MCQ]

#Q. Consider a 4-way set associative cache with block size = 64 bytes. CPU generates 32-bit addresses. Tag comparator requires 22 bits including a valid and a modified bit. What is the size of the cache?

2^6 B

A 8 KB

B 16 KB

C 32 KB

D 64 KB

Ans(B).

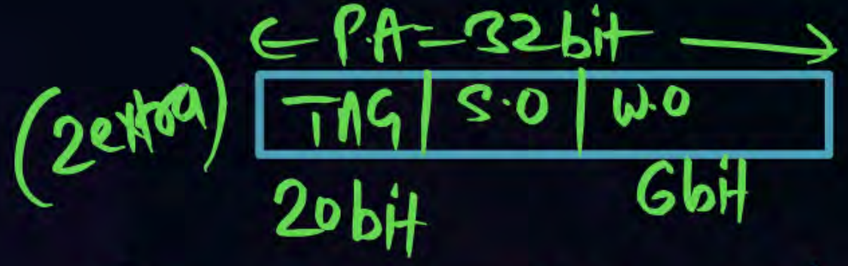
#SET = #LINES / N-ways

$2^6 = \frac{\#LINES}{4}$

$\#LINES = 2^6 \times 4 = 2^8$ Lines

$\Rightarrow 2^8 \times 2^6 B = 2^{14} B$

$= 16KB$



S.O = 32 − (20+6) = 6 bit

2^6 set

[NAT]

#Q. Consider two level-memory, contains cache and main memory. Cache access time is 10 ns and main memory access time is 120 ns/word. The size of block is 4 words. Main memory is referred 20% of time. What is the average access time ___106___ (in Nano seconds)

$t_c = 10 nsec$

$t_m = 120 nsec/word$

4 word

$T_B = 4 \times 120 = 480 nsec$

$T_{avg} = .80 \times 10 + .20(10 + 4*120)$

$\Rightarrow 8 + .20(490)$

$= 8 + 98$

$= 106 nsec$ Ans

Ans (106)

[NAT]

Consider a system with two level cache hierarchies with L_1 and L_2 cache. Program refers memory 3000 times, out of which 30 misses are in L_1 cache and 21 misses are in L_2 cache. If miss penalty of L_2 is 500 clock cycles, hit time of L_1 is 2 clock cycle and hit time of L_2 is 16 clock cycle, the average memory access time (in clock cycle) ____(upto 2 decimal places.)

L_1 Miss Rate $= \frac{30}{3000} = 0.010$

L_2 Miss Rate $= \frac{21}{30} = 0.7$

$$T_{avg} = \text{HIT time}_{L1} + \text{Miss Rate in } L1 \left[\text{Hit time in } L2 + \text{Miss Rate in } L2 \left(\text{Miss Penalty} \right) \right]$$

$$2 + 0.010 \left[16 + 0.7 (500) \right]$$

$$2 + 0.010 \left[16 + 350 \right]$$

$$2 + 0.010 \left[366 \right]$$

$$2 + 3.66$$

$$5.66 \text{ Ans}$$

[MCQ]

#Q. Suppose you want to build a memory with 4 byte words and a capacity of 2^{21} bits. What is type of decoder required if the memory is built using 2K × 8 RAM chips?

A. 5 to 32

B. 6 to 64

C. 4 to 16

D. 7 to 128

Ans (D).

1 Word = 32 bit → Word Addressable

2^{21} bits

$2^{16} \times 2^5 \Rightarrow 2^{16} \times 32$

RAM Chip = $\frac{2^{16} \times 32}{2K \times 8} \Rightarrow \frac{2^{16} \times 2^5}{2^{11} \times 2^3}$

$= 2^7$ RAM Chip

7 bit Req.

7×2^7

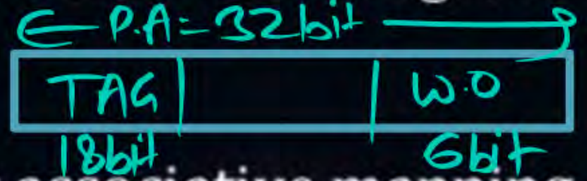
7 to 128. Ans

[NAT]

#Q. Consider a write through cache memory which is 10 times faster than the main memory. The main memory access time is 800 ns. When there is a miss in the cache memory, an 8 word block is transferred from main memory to the cache memory. Hit ratio for read and write operations are 70% and 90% respectively. System generates 70% of read request. What is the throughput of the system (in K words/sec) is _____

[MCQ]

Consider a computer system with a byte addressable main memory of size 2^{32} byte and 64K bytes data cache memory with block of size 64 byte. Tag field length is 18 bits. Which of the following cache mapping used in this system?



32 - (18+6) = 8bit

A. Fully associative mapping

B. 2-way set associative mapping

C. Direct mapping

D. 4-way set associative mapping

Ans (D)

PA = 32 bits
Block size = 64Byte
Cm Size = 64kB
Tag = 18 bit

$\#Lines = \frac{Cm\,Size}{Block\,Size} = \frac{64kB}{64B}$

$\#Lines = 2^{10}$ Lines

S.O = 8 bit $\Rightarrow$ $\#SET = 2^8$

$\#SET = \frac{\#Lines}{N\text{-way}}$

$2^8 = \frac{2^{10}}{N\text{-way}} \Rightarrow N\text{way} = \frac{2^{10}}{2^8} = 2^2 = 4\text{way}$

Home Work

[MCQ]

#Q. Consider three cache organizations each of size 16 KB, with associativity as C_1 – 2 WSA, C_2–4 WSA and C_3–8 WSA, and in all such organizations the block size is of 32 bytes and the size of physical address is 30 bits. A (4 × 1) multiplexer having latency of "0.4" nsec along with "T" bits tag comparator latency of (T/10) nsec. If the hit latencies of cache organizations C_1, C_2 and C_3 are H_1, H_2 and H_3 then the relationship that can be established between hit latencies is _____

A $H_1 > H_2 > H_3$

B $H_1 > H_3 > H_2$

C $H_1 < H_3 < H_2$

D $H_1 < H_2 < H_3$

[NAT]

#Q. Consider a direct mapped cache of size 32 KB and block size of 64 bytes. CPU generates 32- bit addresses. The difference in number of bits in tag meta(Memory) data in this organization with respect to 4-way set associative implementation is_____

[MCQ]

#Q. The main memory address is divided into three field. The least significant 'w' bits can identify a unique word or byte within a block of main memory. Main memory has 2^s blocks to represent there blocks we need ‘s’ bits. The cache logic interprets there ‘s ' bit as a tag of ‘s–r' bits and a line field of 'r' bits.

The number of lines in cache will be

A 2^r

B 2^{r+w}

C 2^{s+w}

D undetermined

[MSQ]

#Q. Consider a computer system with a byte addressable main memory of size 232 byte and 64 k Byte write back direct mapped cache with block of size 64 byte. Cache controller maintains the tag information for each cache block comprising of the following 1 bit for valid/invalid and 1 modified bit.

A. Tag memory size is 16 K bits.

B. Tag memory size is 18 k bits.

C. A total of 2^{16} main memory block map to each cache line

D. A total of 2^{18} main memory block map to each cache line.

[MCQ]

#Q. Consider a p-way set associative cache with (8*p) blocks. Assume that main memory has (16*p) blocks. What is the tag size in this organization?

A $\text{Log}_2 P + 4$

B $\text{Log}_2 P - 1$

C $\text{Log}_2 P + 1$

D None of these

Ans [C].

Cache Size = 8P Block

MM Size = 16P Blocks

$$\text{Tag} = \frac{\text{MM Size}}{\text{CM Size}} = \frac{16P}{8P} = 2$$

TAG = 2

Tag bit = 1bit

P way set Associative

$$\text{Tag bits} = 1 + \lceil \log_2 P \rceil$$ Ans

[MSQ]

5 Consider a computer system which has 4GB, byte addressable main memory and cache size 8MB, 4way set associative cache memory with block size 4096 byte. Consider the following six physical addresses represented in a hexadecimal notation.

$A_1 = 0 \times 47\ CA4\ ABC$

$A_2 = 0 \times 56\ ECF\ 38D$

$A_3 = 0 \times 29\ FDB\ 4CF$

$A_4 = 0 \times 38\ 8A4\ DAC$

$A_5 = 0 \times C3\ EFC\ A47$

$A_6 = 0 \times AB\ 9DB\ 128$

Which of the following is correct ?

A A_1 and A_4 are mapped to the same cache set.

B A_2 and A_5 are mapped to the same cache set.

C A_2 and A_5 are mapped to the different cache set.

D A_3 and A_6 are mapped to the same cache set.

[MCQ]

#Q. 6 Consider a 4 way set associative cache of size 16 KB and having block size 1024 byte. Assume cache is initially empty. Consider least recently used (LRU) policy for replacement. What is the miss ratio (in %) for the below memory access request?

OXA25BC8DF, OX FBCDFBAB, OX ABCDE9DF
OXFDADC8DF, OXFBCDFA3D, OX44A11C25
OXA25BCBAE, OXBCADE19F, OXA25BC92D
OXFBCDF849, OX 44A11FFF, OX FDADCA13

A 40%

B 50%

C 60%

D 100%

2 mins Summary

- Topic: Cache Memory
- Topic: Cache mapping Technique
- Topic: Cache Replacement Algo
- Topic: Cache Updating Technique

THANK - YOU