COMPUTER SCIENCE

Computer Organization and Architecture

ALU & Control unit

Lecture_05

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01 Control Unit

02 CPU Time Calculation

Working
Micro operation & Program.

Control Unit

Hardwired Control Unit Design

- S.O.P (Sum of Product) Expression
- Logic functions
- Fastest CU.

Dis Adv.

It is Not Flexible

Not Support New Operation.

Control Unit

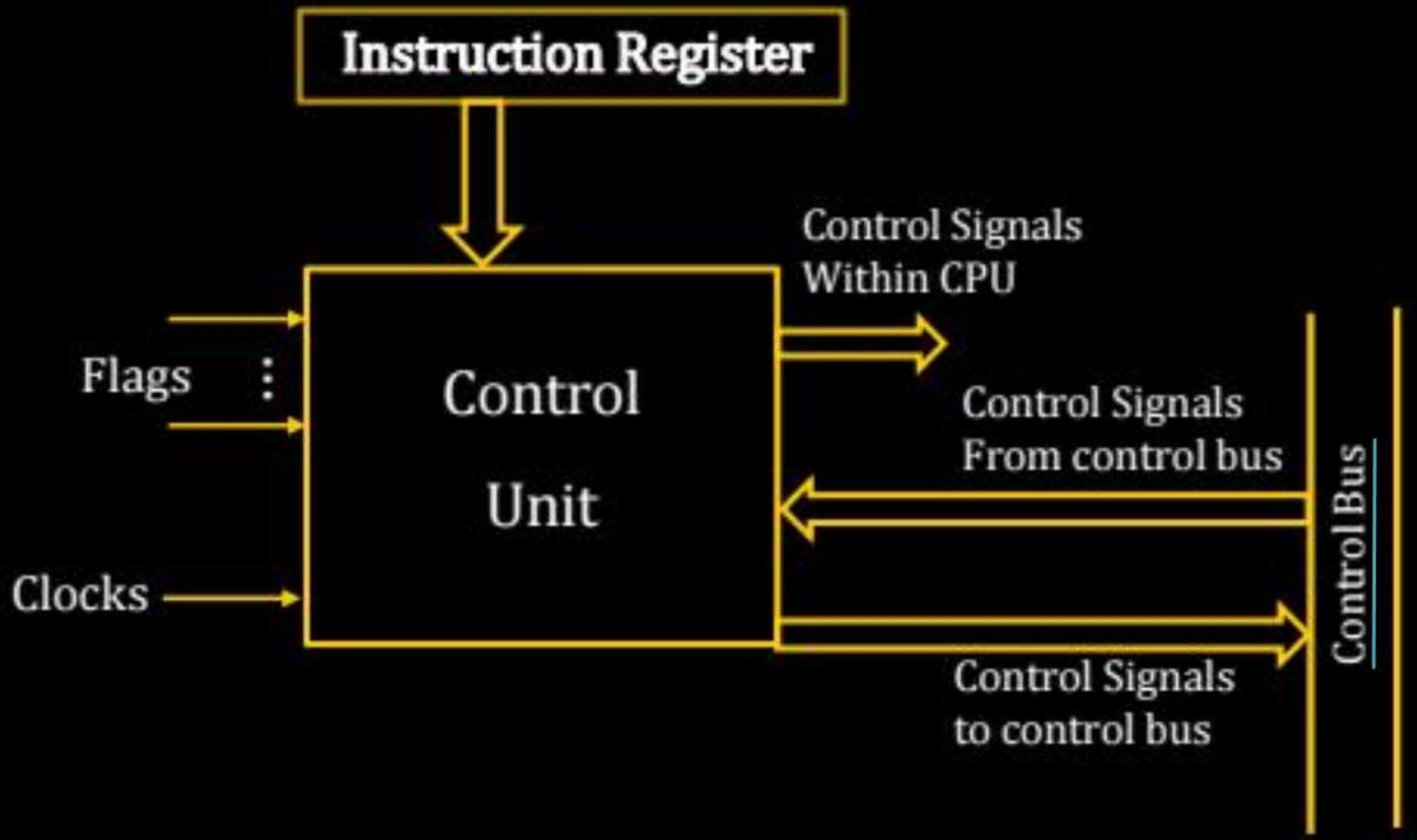
Control unit is the Supervisor in the System that control each & every activity.

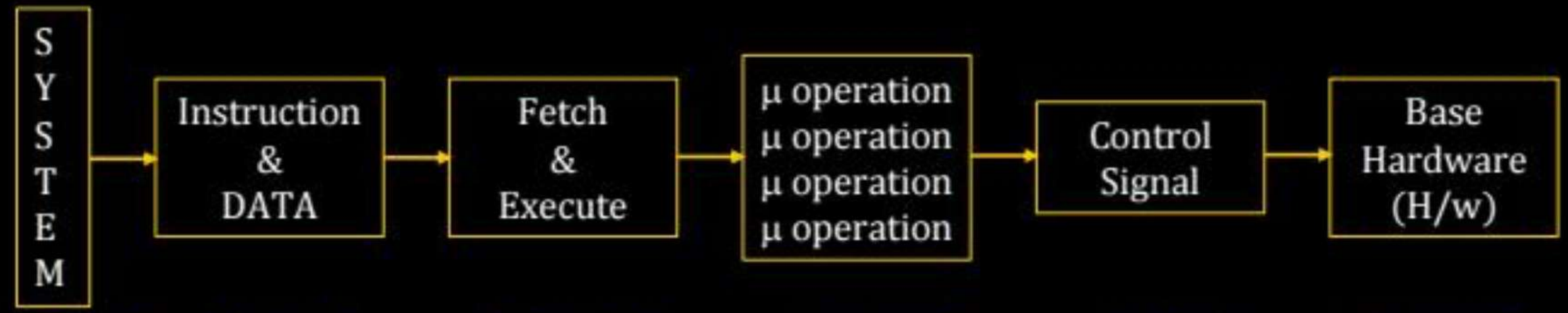
- Control Signals are implement in a Control Unit.
- Control Signal are Required to execute the micro operation.
- Micro operation is the elementary operation in the hardware.
- Control unit generates the sequence of control Signal.
- Control Signal are Directly executed on a Base Hardware (H/W)

  So H/W generate the desired Response.

Computer System Functionality is Program Execution.

Block Diagram of the Control Unit

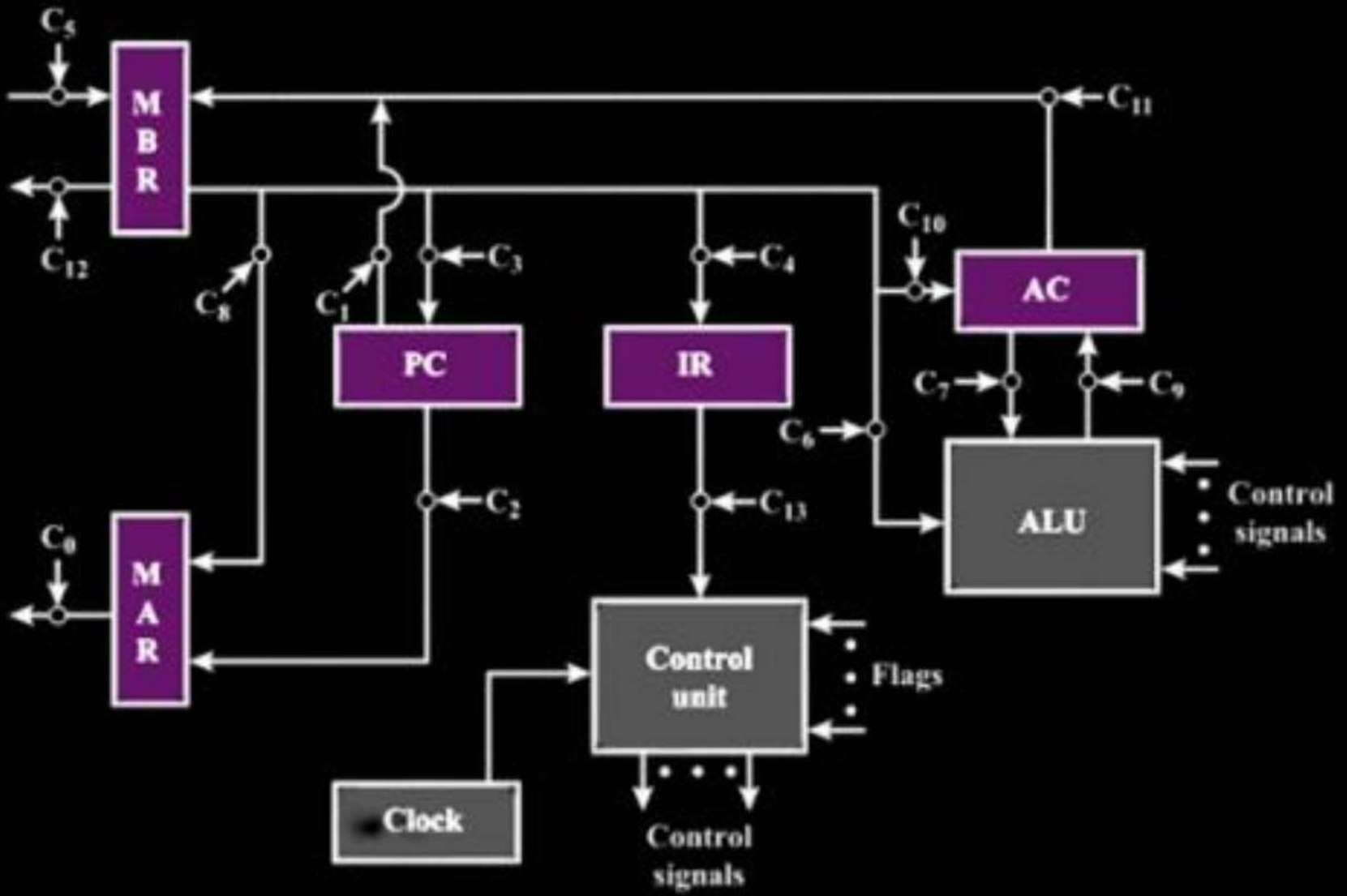



SYSTEM
Instruction & DATA
Fetch & Execute
μ operation
μ operation
μ operation
μ operation
Control Signal
Base Hardware (H/w)
Program Execution
Program
Instruction Cycle
μ program
Control Unit
Program Output

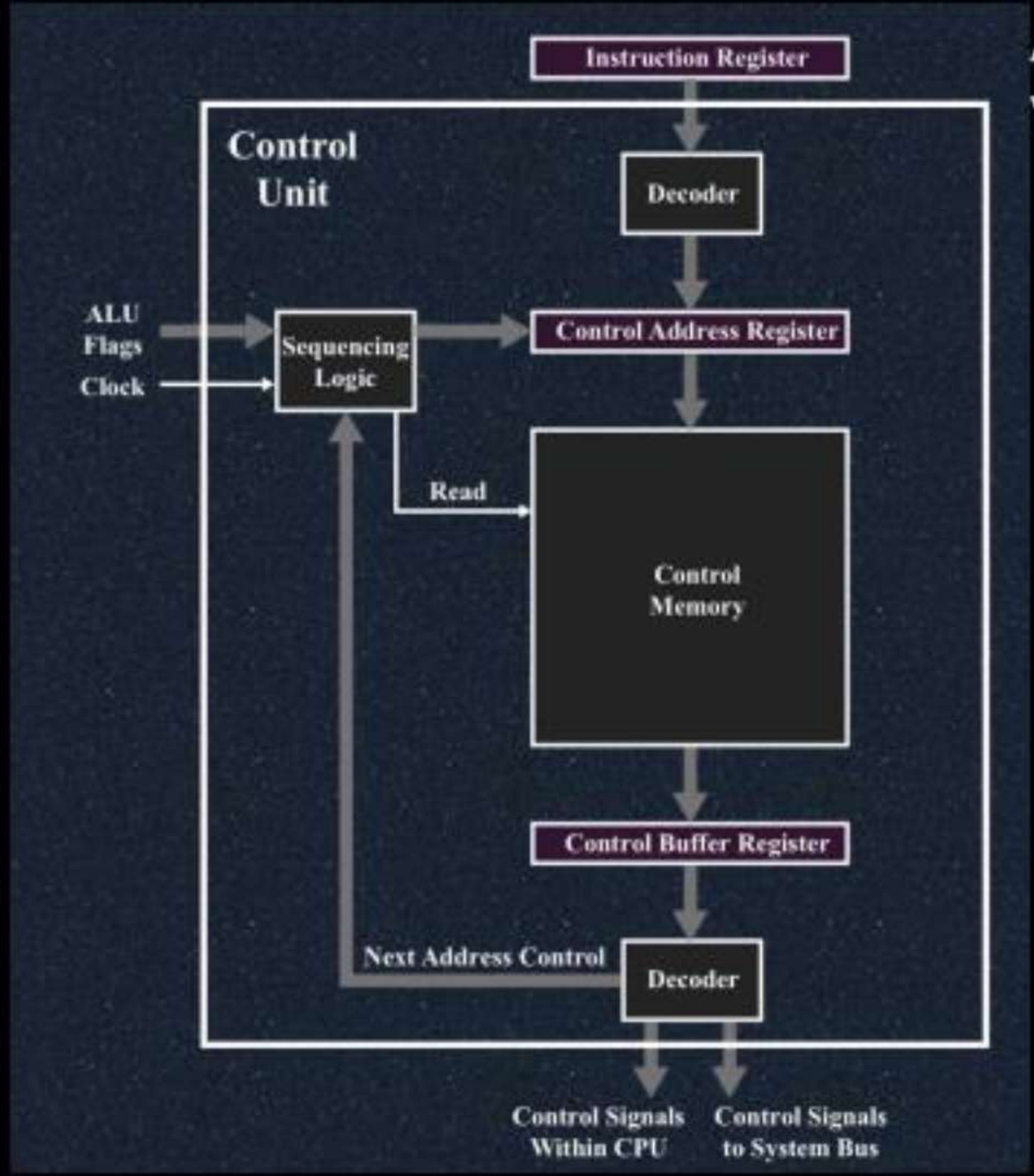
Micro-operations & Control Signals

	Micro-operations	Active-control Signals
Fetch:	T_1: MAR $\Re$ (PC) (or) PC $\rightarrow$ MAR	C_2
	T_2: MBR $\Re$ Memory PC $\Re$ (PC) + 1	C_5, C_R
	T_3: IR $\Re$ (MBR)	C_4
Indirect:	T_1: MAR $\Re$ (IR(Address))	C_8
	T_2: MBR $\Re$ Memory	C_5, C_R
	T_3: IR(Address) $\Re$ (MBR (Address))	C_4
Interrupt:	T_1: MBR $\Re$ (PC)	C_1
	T_2: MAR $\Re$ Save-address PC $\Re$ Routine-address	
	T_3: Memory $\Re$ (MBR)	C_{12}, C_W

Data Paths & Control Signals



Functioning of Microprogrammed Control Unit



Pre Requirement of the CU Design is as follow

1) How many Control Lines are present in the Hardware [S0, S1, S2, S3...]

2) How many Instruction are implemented in the Hardware [I1, I2, I3....]

3) How many Micro operation are required for each Instruction [T1, T2, T3...]

4) What the control Signal Required for each micro operation for each Instruction.

Control Signals will be Implemented into the Control Unit by using following Approach:

1) HARDWIRED CU Design

2) MICRO-PROGRAMMED CU Design

Q.

Consider the following hypothetical CPU which uses 3 data register A, B & C and supports 3 instruction I_1, I_2 & I_3. Obtain the logic function that will generate the hardwired control for the signal Ain & Bout with the following data.

	I_1	I_2	I_3
T_1	Ain, Bout	Ain, Cin, Bout	Bin, Bout
T_2	Bin, Cin, Aout	Ain, Aout	Ain, Bin, Cout
T_3	Bin, Bout	Bin, Bout	Bin, Bout
T_4	Cin, Aout	Bin, Aout	Ain, Aout
T_5	End	End	End

Step 1 : Search where the control signals Ain & Bout are present.

Step 2 : Options are in I.T format or T.I format.

Step 3 : For any particular time interval. Is the control signal presents for all the instructions?

Step 1 : Search where the control signals Ain & Bout are present.

Step 2 : Options are in I.T format or T.I format.

Step 3 : For any particular time interval. Is the control signal presents for all the instructions?

$\underline{\text{Ain}} = T_1\ I_1 + (T_1 + T_2)\ I_2 + (T_2 + T_4)\ I_3$

$\underline{\text{Bout}} = T_1 + T_3$

↓

Bout is present for all instruction during T_1 & T_3

Q.

A hardwired CPU use 10 control signals SI to S10 in various time steps T1 to T5 implement 4 instructions I1 to I4 as shown below.

	T1	T2	T3	T4	T5
I1	S1, S3, S5	S2, S4, S6	S1, S7	S10	S3, S8
I2	S1, S3, S5	S8, S9, S10	S5, S6, S7	S6	S10
I3	S1, S3, S5	S7, S8, S10	S2, S6, S9	S10	S1, S3
I4	S1, S3, S5	S2, S6, S7	S5, S10	S6, S9	S10

Which of the following pairs of expressions represent the circuit for generating control signals S5 and S10 respectively [(IJ + Ik) Tn indicates that the control signal should be generated in time step Tn if the instruction being executed is [IJ to IK]?

(a) S5 = TI + I2.T3 and S10 = (I1 + I3).T4 + (I2 + I4).T5

(b) S5 = TI + (I2 + I4).T3 and S10 = (I1 + I3).T4 + (I2 + I4).T5

(c) S5 = T1 + (I2 + I4).T3 and S10 = (I2 + I3 + I4).T2 + (I1 + I3).T4 + (I2 + I4).T5

(d) S5 = T1 + (I2 + I4).T3 and S10 = (I2 + I3).T2 + I4.T3 + (I1+I3).T4 + (I2+ I4).T5

Q.

A CPU has only three instructions I1, 12 and 13, which use the following signals in time steps T I—T5:

I1: Tl : Ain, Bout, Cin
T2 : PCout, Bin
T3 : Zout, Ain
T4 : PCin, Bout
T5 : End

I2: T1 : Cin, Bout, Din
T2 : Aout, Bin
T3 : Zout, Ain
T4 : Bin, Cout
T5 : End

I3: T1: Din, Aout
T2 : Ain, Bout
T3 : Zout, Ain
T4 : Dout, Ain
T5 : : End

Which of the following logic functions will generate the hardwired control for the signal Ain? [GATE CSE 2004]

(a) T1. I1 + T2. I3 + T4.I3 +T3

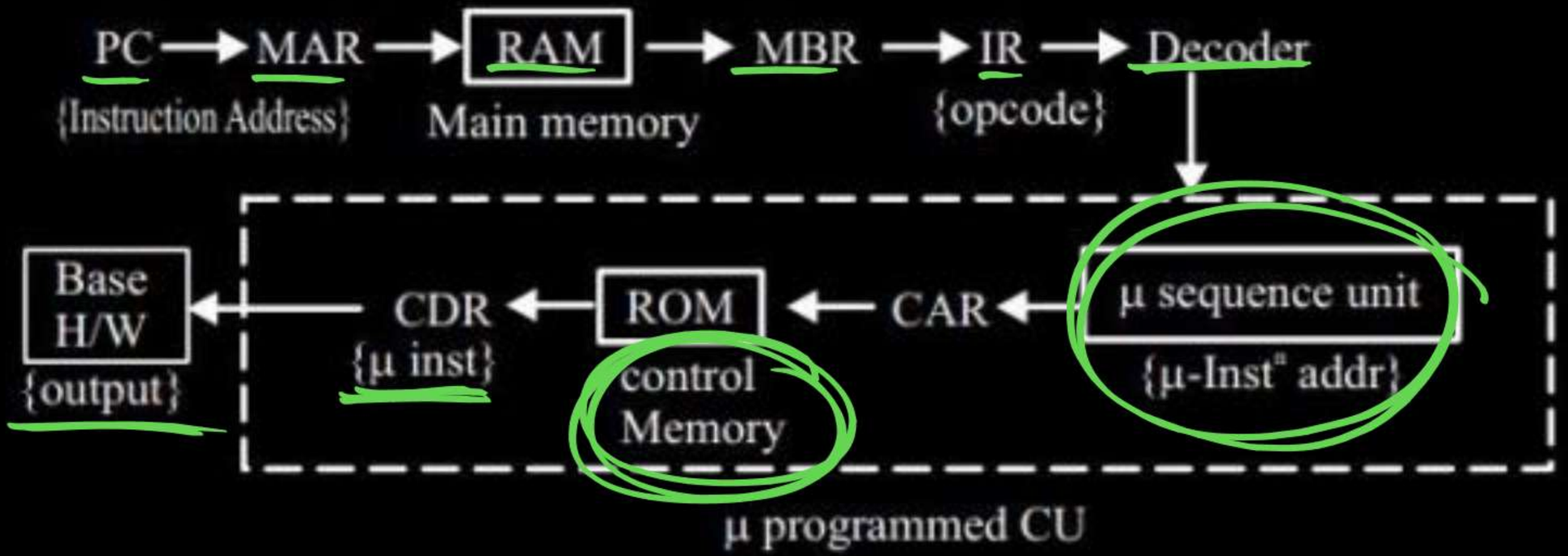
(b) (T1 + T2 + T3).I3 + T1.I1

(c) (T1 + T2).I1 + (T2 + T4).I3 + T3

(d) (T1 + T2).I2 + (T1 + T3). I1 + T3

Micro Programmed CU Design

MICRO-PROGRAMED CU DESIGN



Control unit

① Hardwired CU Design

- S.O.P expression
- Logic function
- Fastest (RISC)

Not Flexible

② Microprogrammed CU Design

[Uprog Stored in CM (Control Memory)]

Decoded Format

[Horizontal uprog]

4CS ⇒ 4bit

4bit = 4CS

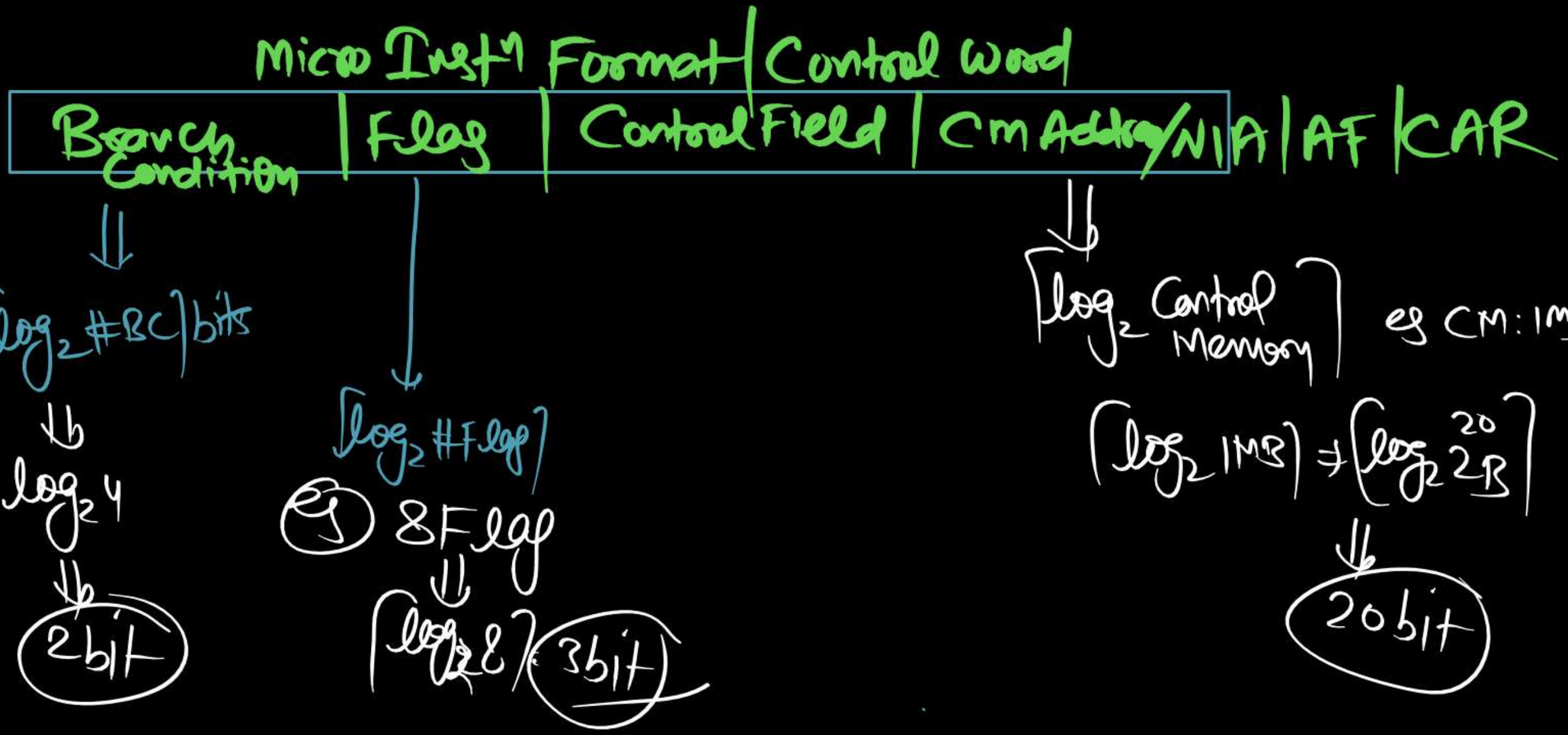
Encoded Format

[Vertical uprog]

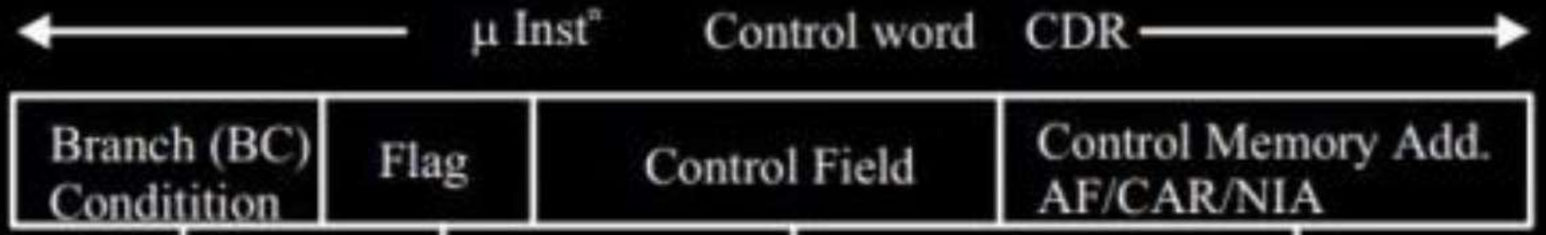
4CS ⇒ $\log_2 4 = 2$ bit

4bit ⇒ $2^4 = 16$ C.S.

MICRO-PROGRAMED CU DESIGN



MICRO INSTRUCTION FORMAT



CM: Control Memory

One of a system Supported Branch Condition

$[\log_2 \#\ BC's]$

Eg. 4 BC

NZ
Z
C
NC

$\log_2 4$ ⇓ 2 bit

One of the system Supported flags

$[\log_2 \#\ Flags]$

Eg. 8 Flag

$\log_2 8$ ⇓ 3 bit

Control Signal

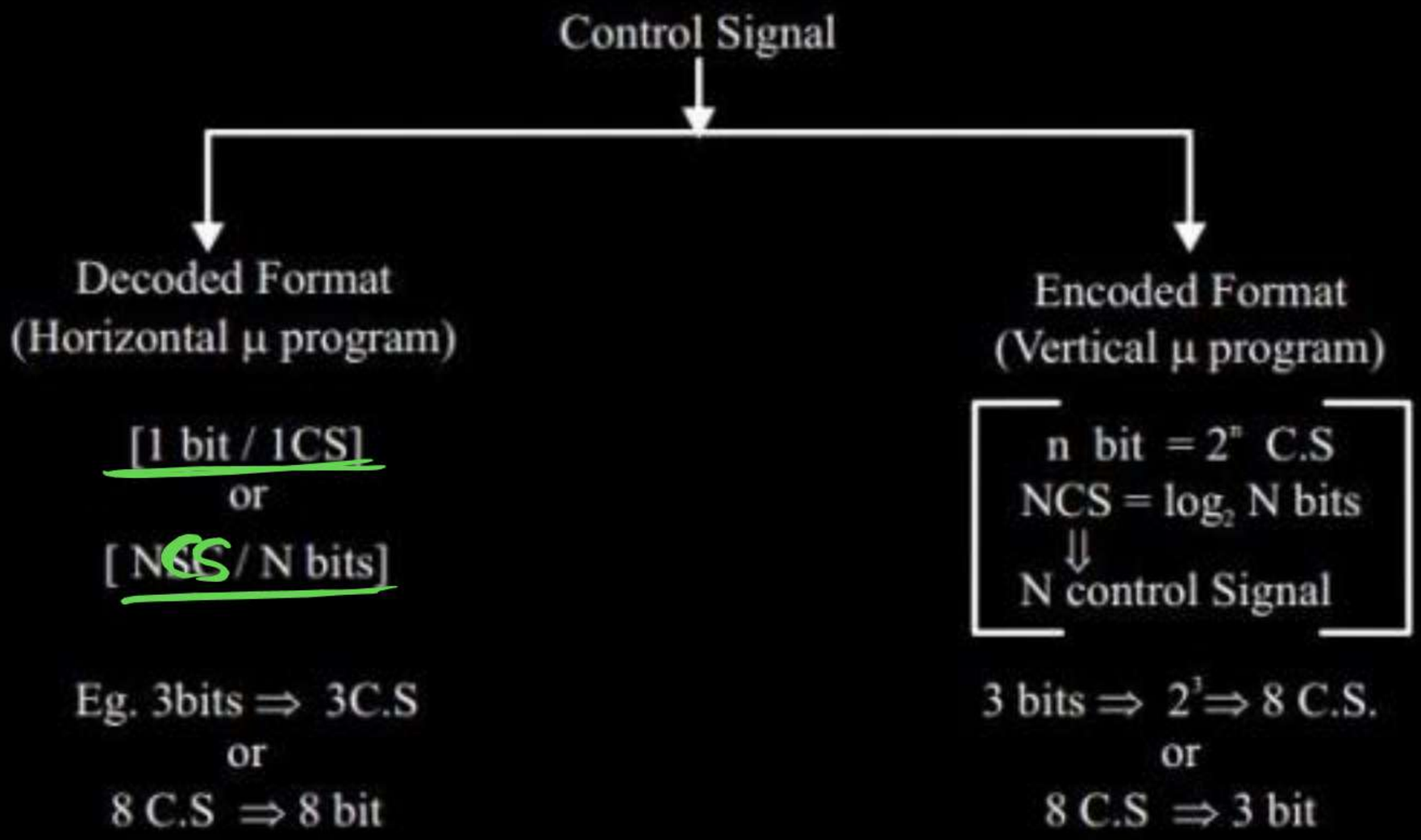
Control Signal

Decoded Format (Horizontal μ program)

Encoded Format (Vertical μ program)

Control Signal

- Decoded Format (Horizontal uprog)
  - 1 bit ⇒ 1 CS
  - NCS ⇒ N bit
- Encoded Format (Vertical uprog.)
  - n bit = 2^n CS
  - NCS = $\log_2$ N bit


Control Signal
Decoded Format
(Horizontal μ program)
[1 bit / 1CS]
or
[NCS / N bits]
Eg. 3bits ⇒ 3C.S
or
8 C.S ⇒ 8 bit
Encoded Format
(Vertical μ program)
n bit = 2^n C.S
NCS = log2 N bits
⇓
N control Signal
3 bits ⇒ 2^3 ⇒ 8 C.S.
or
8 C.S ⇒ 3 bit

Based on the way of Representing, μInstⁿ is divided into 2 Type

① Horizontal μInstⁿ (Decoded format)

② Vertical μInstⁿ (Encoded format)

(I) Horizontal Microprogramming

(1) # Control signal in the Hardware : $S_0\ S_1\ S_2\ S_3$

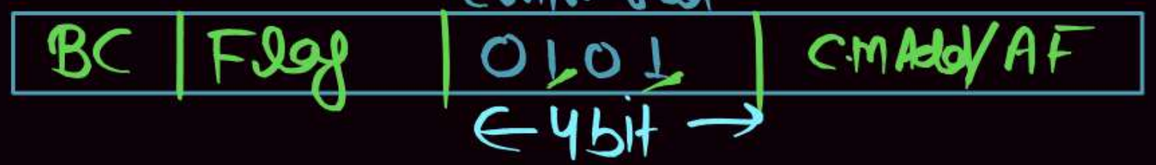
[4CS ⇓ 4bit]

(2) Decoded format of C.S :

0 : Disable

1 : Enable

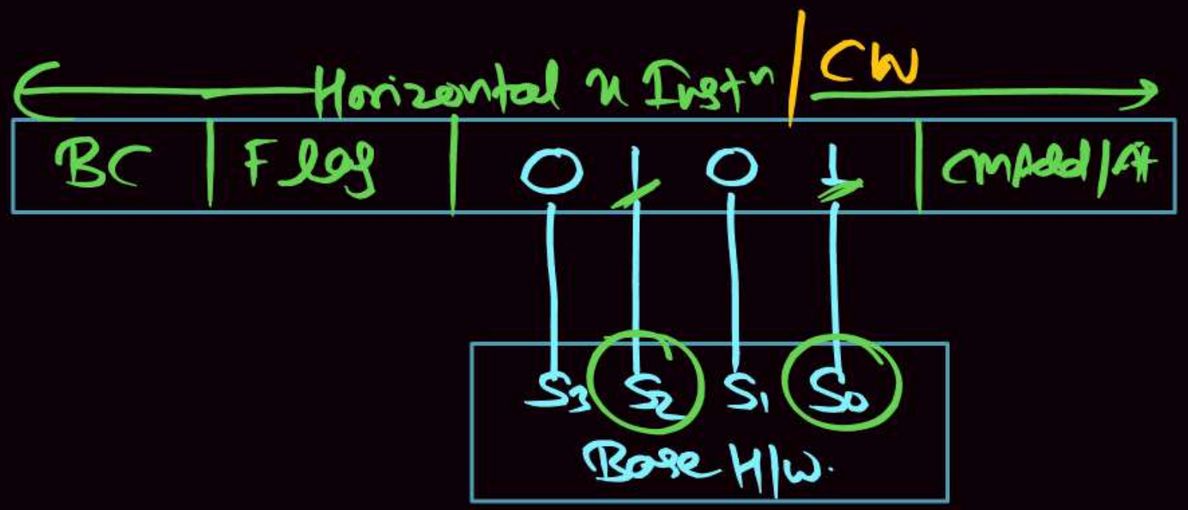
(3) Design a Horizontal m Instⁿ for C.S = [S_0, S_2]

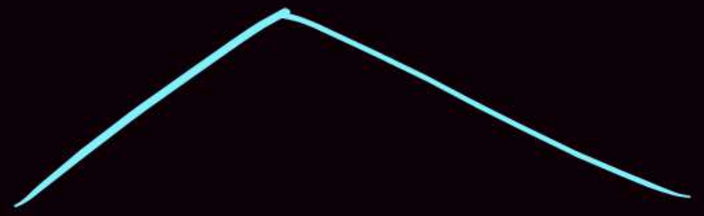


S_3 S_2 S_1 S_0

0 1 0 1

(4) Operational State





Horizontal
[Decoded Format]

1bit ⇒ 1 CS
4bit ⇒ 4 CS
4 CS ⇒ 4bit

Vertical
[Encoded Format]

n bit $= 2^r$ CS

NCS ⇒ $\log_2 N$ bit

Eg

4 CS ⇒ $\log_2 4$ = 2bit

Vertical Uprogramming:

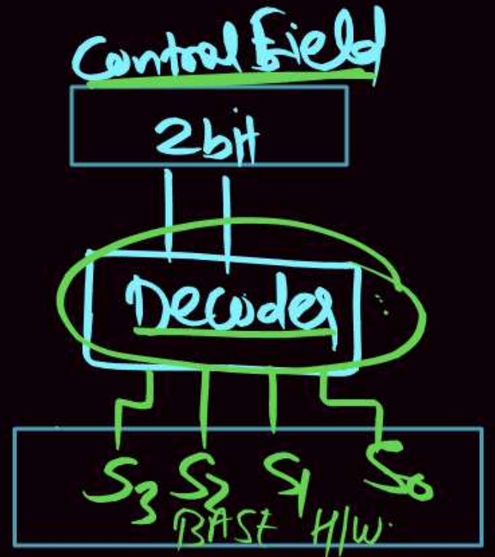
① # Control Signal in H/w : $[S_0\ S_1\ S_2\ S_3]$

② Encoded format of CS : $\lceil \log_2 4 \rceil$ = 2bit

UCS ⇒ $\log_2 4$ = 2bit

Control Field = 2bit

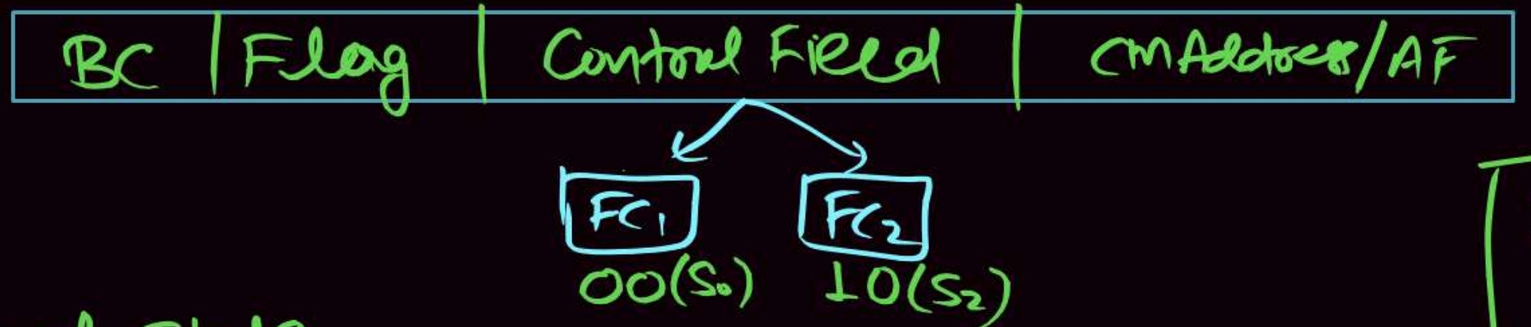
00 – S_0
01 – S_1
10 – S_2
11 – S_3



(In Vertical External Decoder is Required)

∴

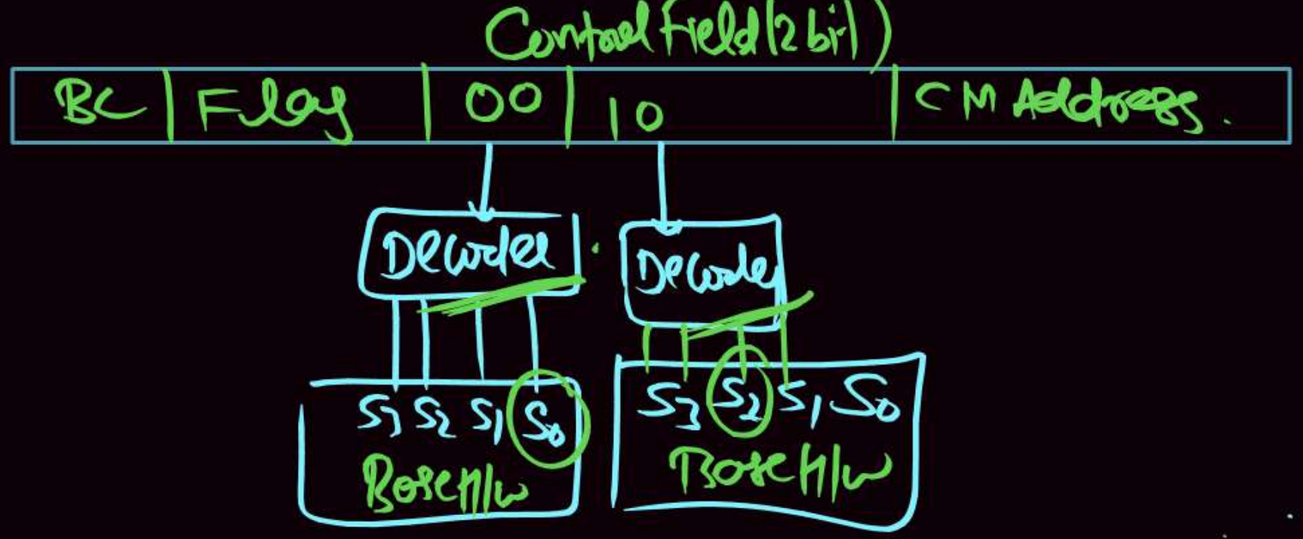
③ Design a Vertical μ Instn for CS = [S_0, S_2]



S_0 : 0 0

S_2 : 1 0

④ Operational State



FC: Function Code.

⇓

generated by the control unit to give signal to CPU to perform operation

Horizontal Programming

① In this CS are expressed in Decoded format

② n bit ⇒ n CS

N CS ⇒ N bit

eg 200 CS ⇒ 200 bits

③ Longer Control Word

④ No External Decoder is Required to generate the CS

Vertical Microprogramming

① In this CS are expressed into Encoded format.

② n bit ⇒ 2^n CS

N CS ⇒ $\log_2 N$ bit

eg for 200 CS ⇒ 8 bit

③ Shorter Control Word

④ External Decode is Required to generate the CS.

⑤ It is Flexible compared to Hardwired CU.

⑥ It Support High Degree of Parallelism (None / More than One)

⑤ It is More flexible compared to Horizontal μ prog.

⑥ It Support Low Degree of Parallelism. (None / One)

Note: Default Microprogrammed is vertical μprogrammed CU [Used in CISC].

V.V.V. Imp.

SPEED: Hardwired > Horizontal > Vertical.

TimeConsume: Vertical > Horizontal > Hardwired.

Flexibility: Vertical > Horizontal > Hardwired.

Q.1

GATE

Arrange the following configuration for CPU in decreasing order of operating speeds: Hardwired control, vertical micro-programming, horizontal micro-programming.

(a) Hardwired control, vertical micro programming, horizontal micro programming.

(b) Hardwired control, horizontal micro programming, vertical microprogramming

(c) Horizontal micro programming, vertical micro programming. Hardwired control

(d) Vertical micro programming, horizontal micro programming, hardwired control

Q.2

GATE

Horizontal microprogramming.

(a) does not require use of signal decoders

(b) Results in larger sized microinstructions than vertical microprogramming

(c) use one bit each control signal

(d) All of the above

Q.3

GATE 2-Marks

An instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows:

Group 1 : 20 signals. Group 2 : 70 signals, Groups 3 : 2 signals. Groups 4 : 10 signals, Groups 5 : 23 signals.

How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming?

(a) 0

(b) 103

(c) 22

(d) 55

	Horizontal	Vertical
G_1 : 20 CS →	20	5
G_2 : 70 CS →	70	7
G_3 : 2 CS →	2	1
G_4 : 10 CS →	10	4
G_5 : 23 CS →	23	5
	125	22

#bit Saved = 125 - 22 = 103 Ans

Q.4 Consider a Hypothetical CU it has 1024 control words memory. Is support 48 control signals & 16 Flags. What is the size of the control words in bits & control memory in byte using

(i) Horizonal Programming?

(ii) Vertical Programming?

Control Memory = 1024 CW $\Rightarrow$ CM = 2^{10} CW $\Rightarrow$ AF/NIA/CAR = 10 bit

Control Signal = 48 CS

Flag = 16 = 2^4 or $\log_2 16$

Flag = 4 bit

Horizontal Microprogramming

48 Control Signal = 48 bits

$\longleftarrow$ CW | uInstn

FLAG	C.F	CAR(AF/NIA)
4bit	48bit	10bit

Vertical Microprogramming.

48 CS = $\log_2 48$ = 6 bit

FLAG	CF	CAR(AF)
4bit	6bit	10bit

Q.4 Consider a Hypothetical CU it has 1024 control words memory. Is support 48 control signals & 16 Flags. What is the size of the control words in bits & control memory in byte using

(i) Horizonal Programming?

(ii) Vertical Programming?

Horizontal uprog:

Control Word = 4+48+10 = 62 bits Ans

Control memory = 1024 CW ⇒ 1024 × 62 bit ⇒ $\frac{1024 \times 62}{8}$ Byte ≈ 8K B Ans

Vertical uprog:

Control Word = 4+6+10 = 20bit

Control memory = 1024 CW ⇒ 1024 × 20 bits ⇒ $\frac{1024 \times 20}{8}$ Byte ≈ 3K B Ans

Q.5

Control field of a micro Instruction support 2 groups of control signal in which Group 1 Indicate None/One of 400 control signal & Group 2 (Horizontal) Indicate 6 signals. Hardwire contain 16 Flags & 32 Branch condition.

If CAR Register size is 20 bit then what is CDR in bits & control memory in bits?

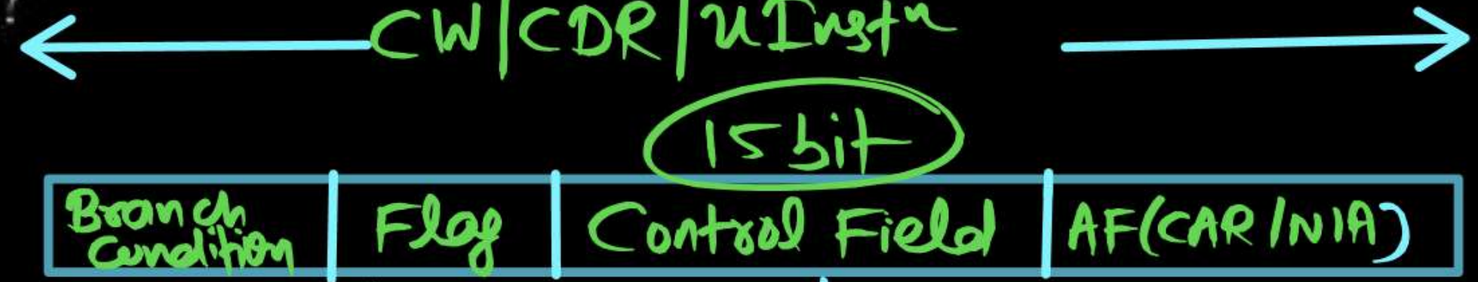
$\log_2 32$

or 2^n

32 Branch Condition $\Rightarrow$ 5bit

16 Flag = 4bit

CAR = 20bit



Control Word [CDR] Size = 5 + 4 + 15 + 20

CDR = 44 bit

CAR / AF = 20

Control memory = 2^{20} CW

$= 2^{20} \times 44$ bits Ans

(OR)

$= 44$ M bits Ans

Q. GATE

Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125 control signals are needed to be generated by the control unit. While designing the horizontal micro-programming control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?

(a) 125, 7
(b) 125, 10
(c) 135, 7
(d) 135, 10

[GATE IT 2008]

Total # Instruction = 140.

#Cycle/Instn = 7 Cycle.

Total # μoperation/μInstn = 140×7 = 980 μInstn / CW.

Control Memory = 980 CW.

Ans (D)

Control Memory = 980 CW. $= 2^{10}$ CW

AF/CAR = 10 bit

Horizontal μprog: 125 CS ⇒ 125 bits.

Control Word = 125 + 10

= 135 bit Ans & CAR = 10 bit

Control Memory = 980 × CW

⇒ 980 × 135 bits.

Q.

A Hypothetical processor contain word length of 12 bits. It support 1 word opcode. Each Instruction takes 8 cycles to compete the execution. Processor contain 256 control signal & 16 flags. Processor used Horizontal Control Unit. 64 Branch is used then what is the size of CAR & CDR in bits of control memory?

Word length

1 Word = 12 bit

OPCODE = 1 Word

= 12 bit

Total # Instruction = 2^{12} Instn

Each Instruction takes = 8 Cycle

Total # μoperⁿ / μInstⁿ = $2^{12} \times 8 = 2^{15}$ μInstⁿ / μoperⁿ / CW

= 2^{15} CW

Control Memory = 2^{15} CW.

CAR (AF) = 15 bit Ans

16 Flag ⇒ Flag = 4 bit

64 BC ⇒ BC = 6 bit

Horizontal = 256 CS ⇒ 256 bits

Control Word [CDR] Size = 6 + 4 + 256 + 15

= 281 bits Ans

Control Memory = 2^{15} CW

= 2^{15} X 281 bits Ans

RISC Reduced Instruction set computer	CISC Complex Instruction set computer
1. It support less number of addressing Mode (AM)	1. It support more number of AM.
2. It support smaller Instruction set	2. It support larger Instruction set.
3. It support more number of Register	3. It support less number of Register
4. It support fixed length Instruction	4. It support variable length Instruction
5. It support 1 Instruction per cycle (CPI=1) (Cycle per Instruction =1) CPI = 1	5. It support number 1 Instruction Per cycle (CPI ≠ 1) NOT
6. It support pipeline successfully	6. It support unsuccessful Pipeline
7. It is the expensive processor used in Real Time application	7. It is the low expensive processor
8. It is a super computer	8. General Purpose computer
9. It uses hardwired control unit. (Motorola processor, power processer, ARM processor)	9. It uses microprogrammed (vertical) control unit (Pentium processer)

THANK YOU!