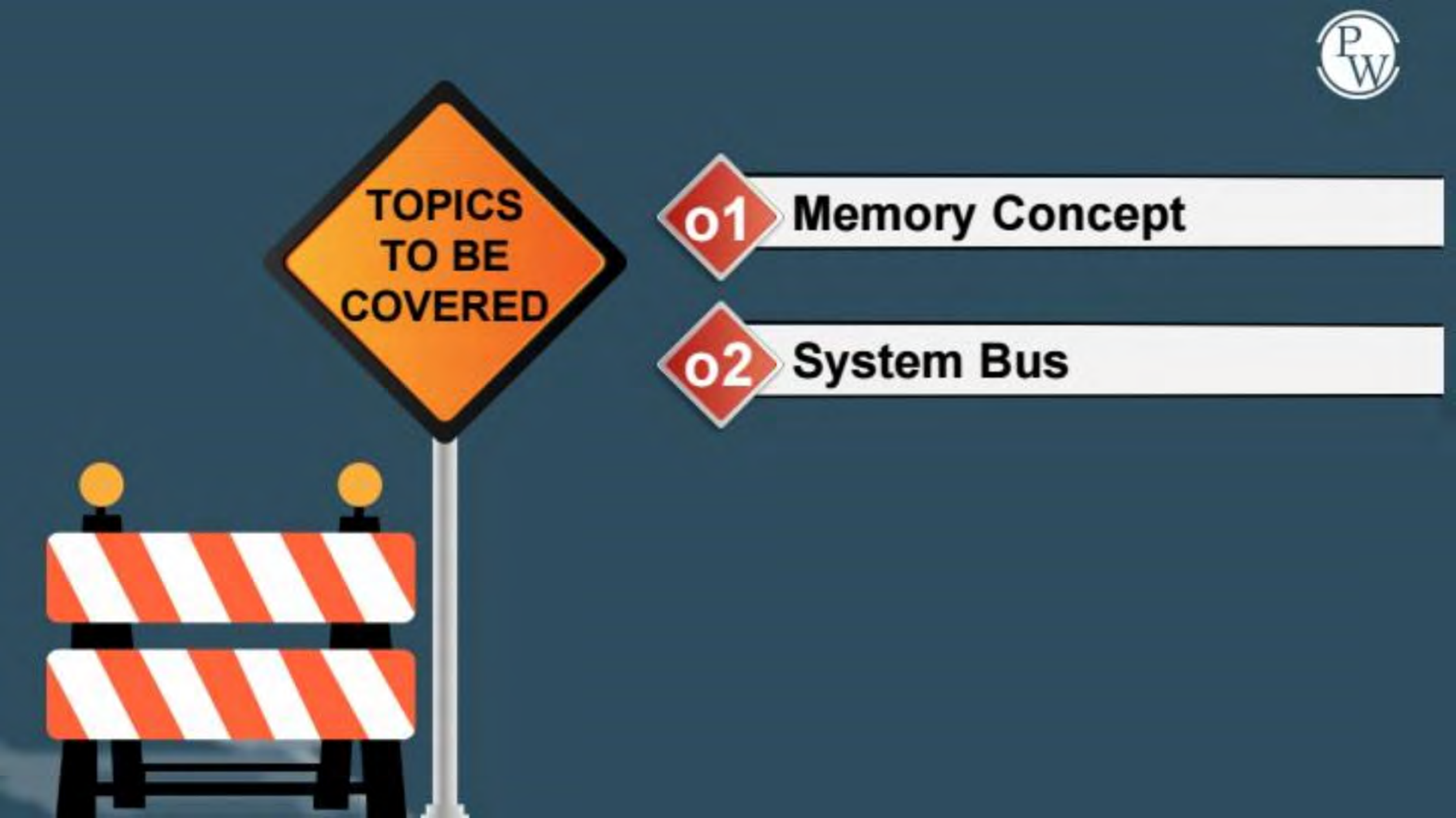
COMPUTER SCIENCE

Computer Organization and Architecture

Introduction of COA

Lecture_03

Vijay Agarwal sir

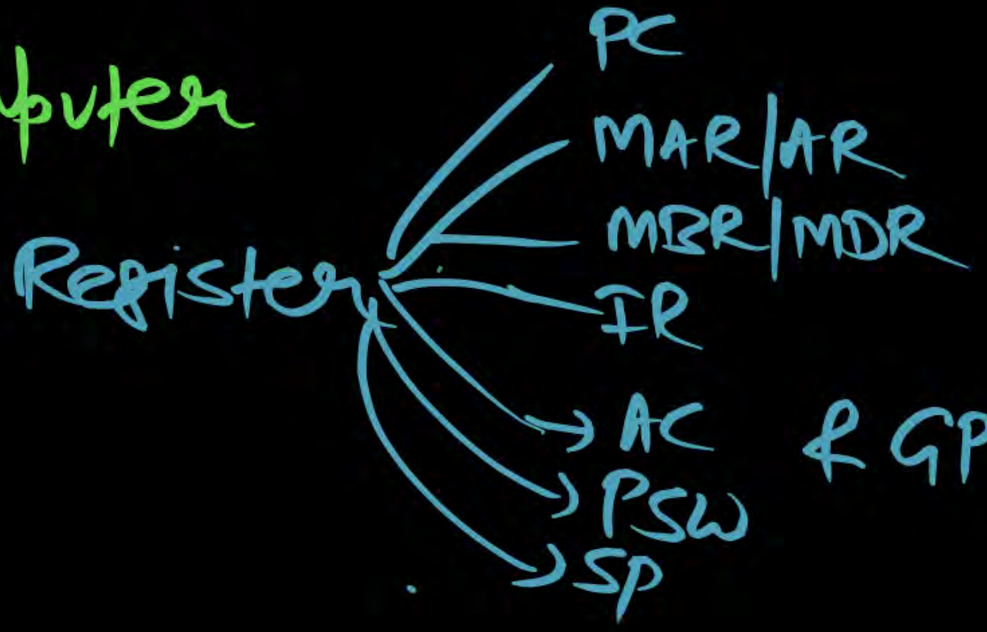


01 Memory Concept

02 System Bus

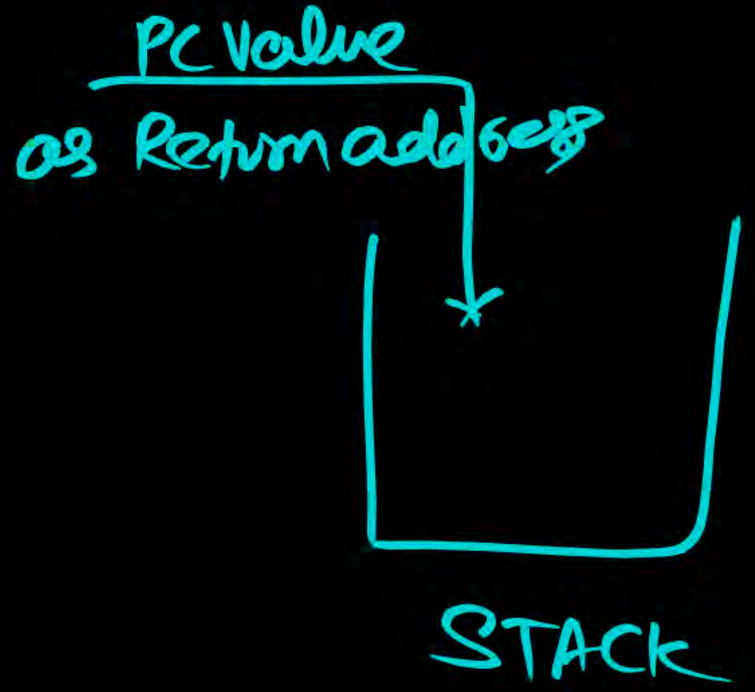
Introduction of COA

- Computer Generation
- CO & CA
- Compent of the Computer
  - CPU
  - Memory
  - I/O



Instruction cycle

1. Fetch cycle [MEM to CPU (IR)]
2. Execute cycle
   - Decode
   - Execute
3. Instruction cycle with interrupt



& Control transfer to ISR.

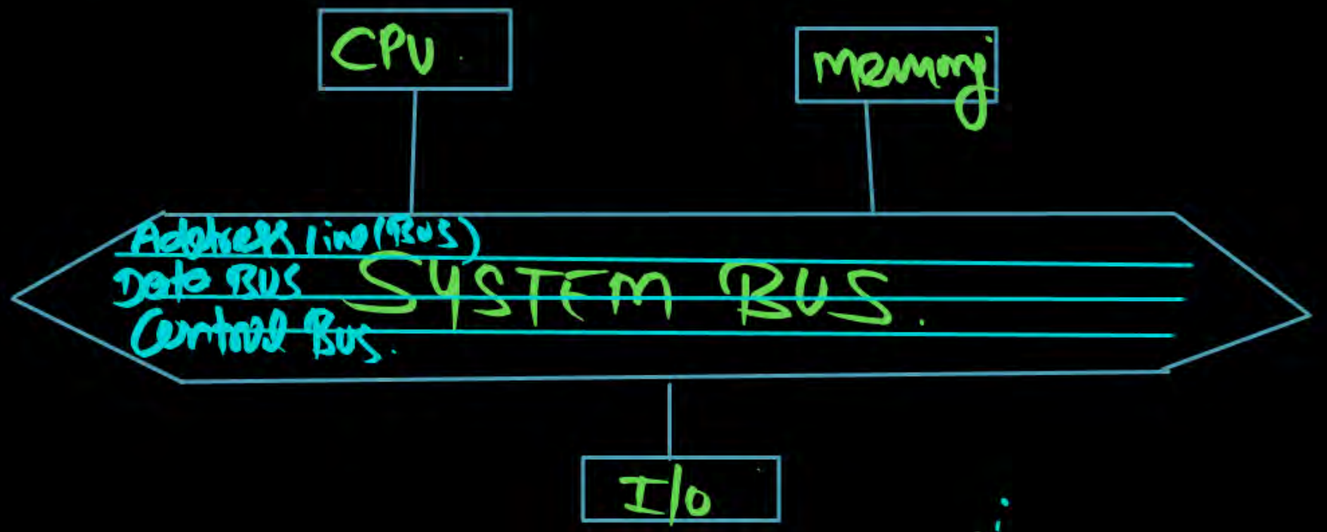
& GATE Question.

Content of the Computer

1. CPU
2. Memory
3. I/O

SYSTEM BUS :

System Bus is Collection of Lines which are Used to Provide the Communication between Major Content of the Computer. [CPU , Memory , I/O]

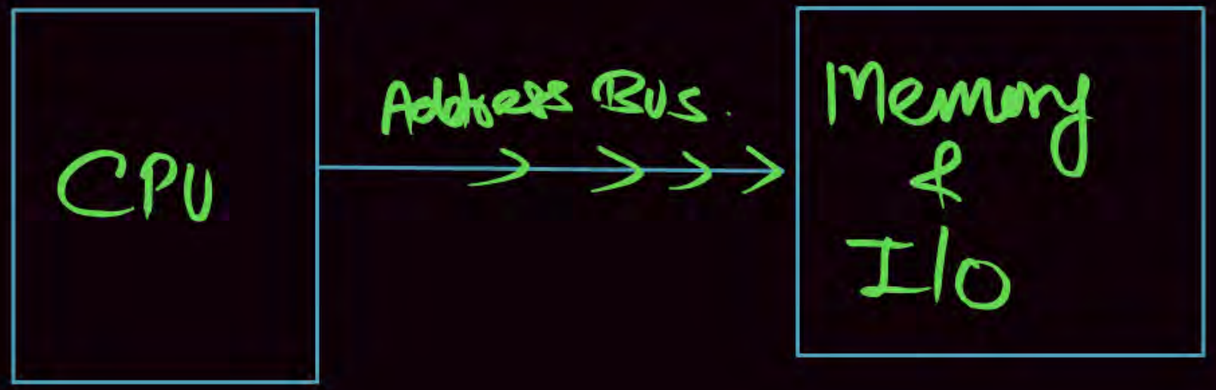


System Bus Contain 3 type of Lines(Bus).

1. Address Line / Address Bus.
2. Data Line / Data Bus
3. Control Line / Control Bus

① Address Bus : Address Bus is used to Carry the Carry the Address towards Memory & IO.

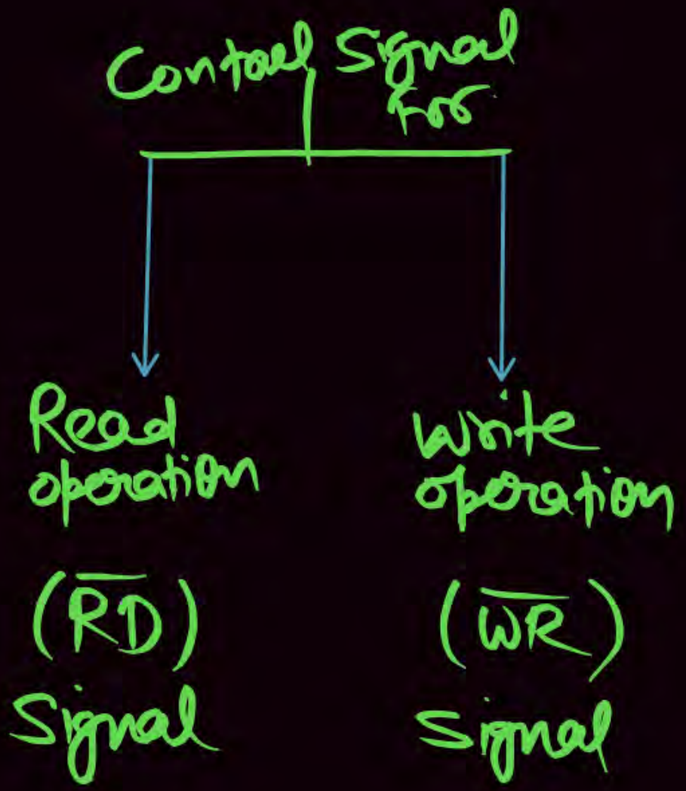
Note
- Address Line are Unidirectional.



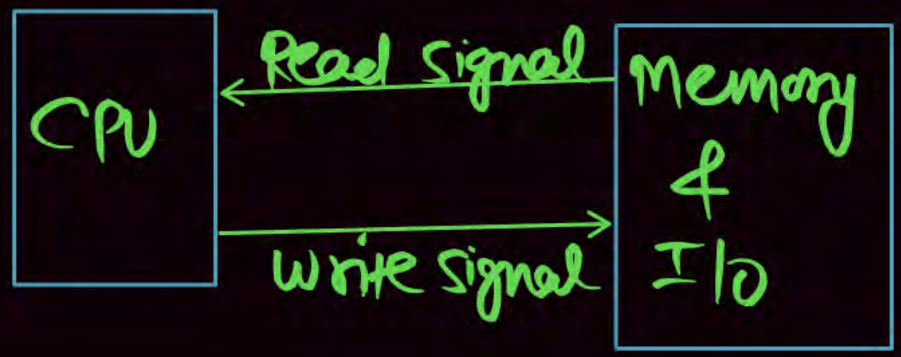
② Data Line : Data Line are Used to Carry the Data (Binary Sequence)

Note Data Bus are Bi directional.

③ Control Bus : Control lines are used to carry the Control Signal.



Control Lines are indidually unidirectional & collectively Bidirectional

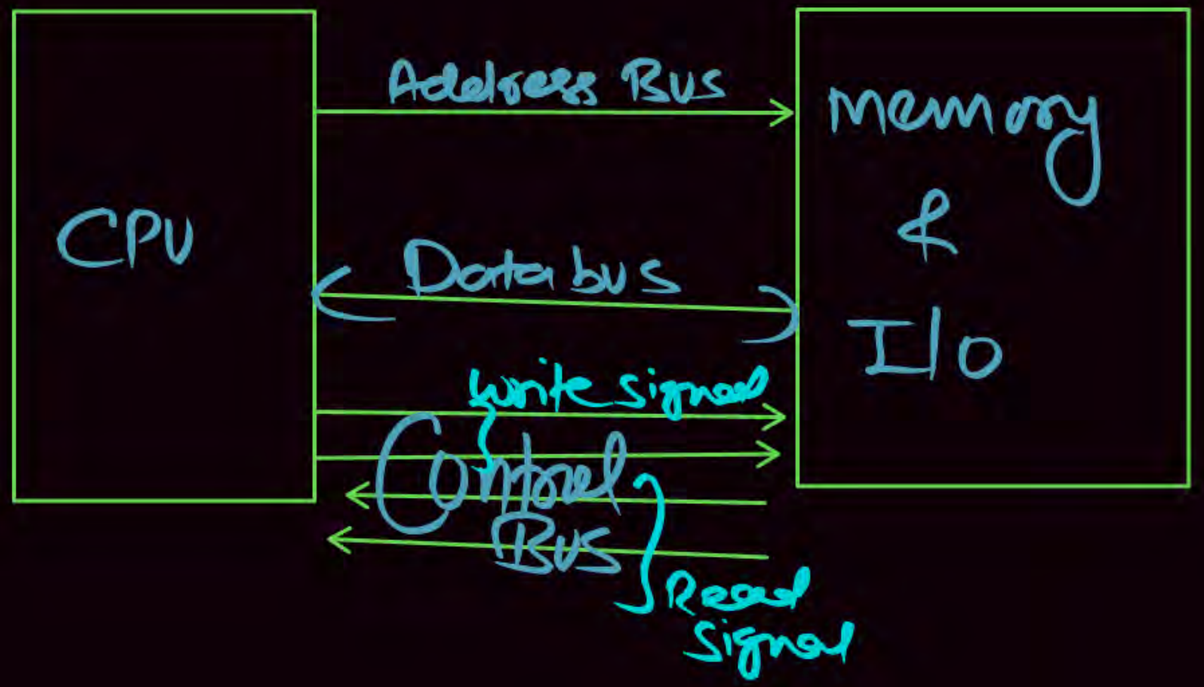


Memory

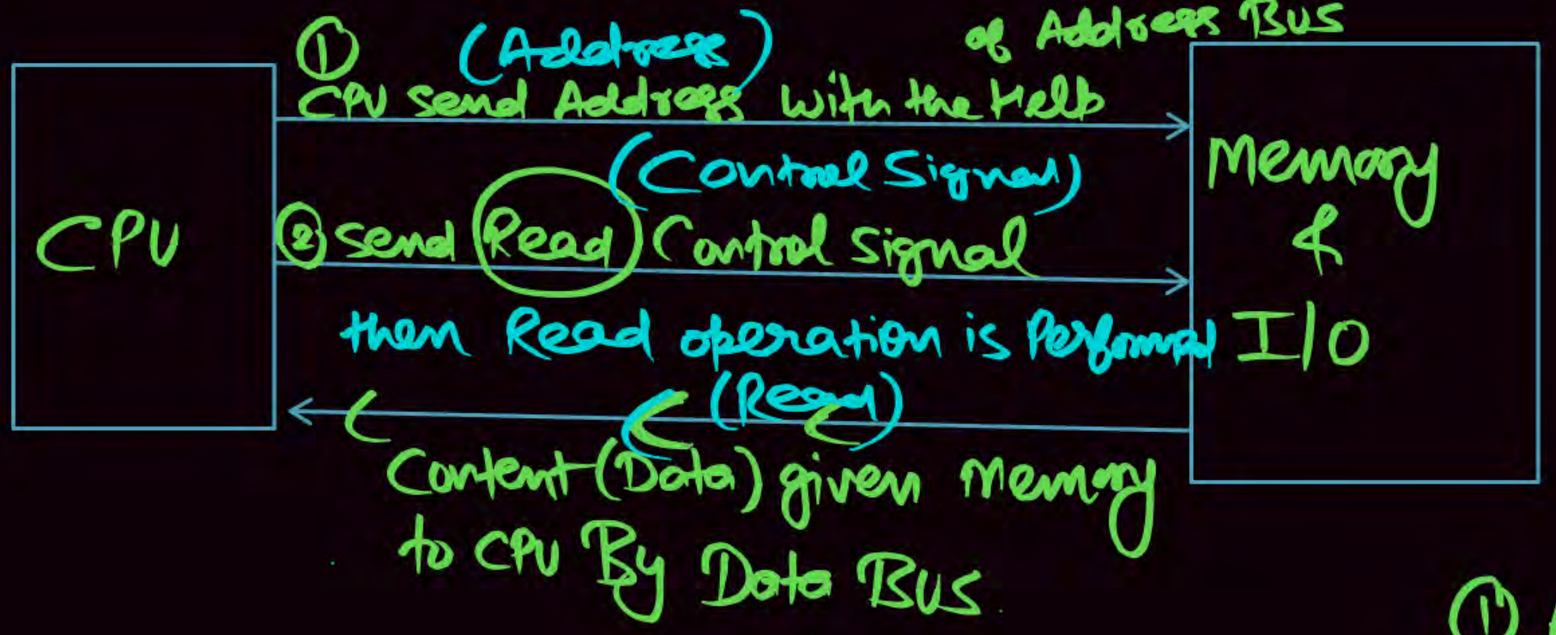
Read ⇒ memory to CPU.

Write ⇒ CPU to Memory.

System Bus

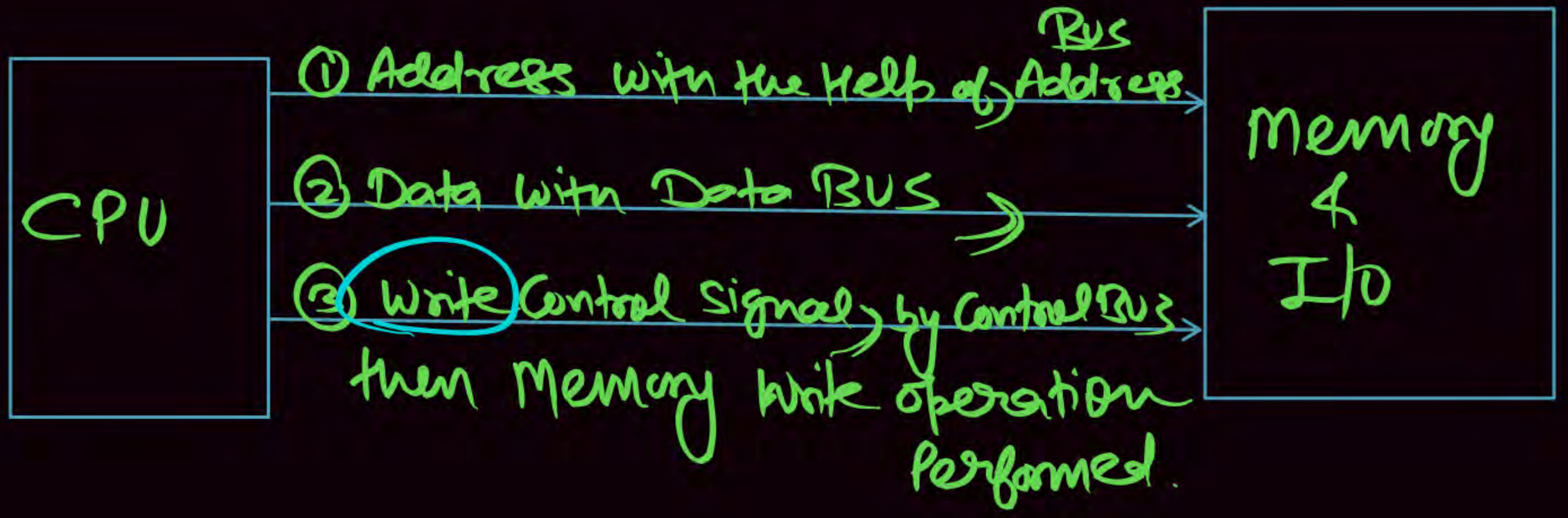

CPU
Address Bus
Data bus
write signal
Control Bus
Read Signal
memory & I/O

Read operation (memory Read)



① Address Bus
② Data Bus
③ Control Bus

Write operation (Memory Write)



(eg) MEMORY Read

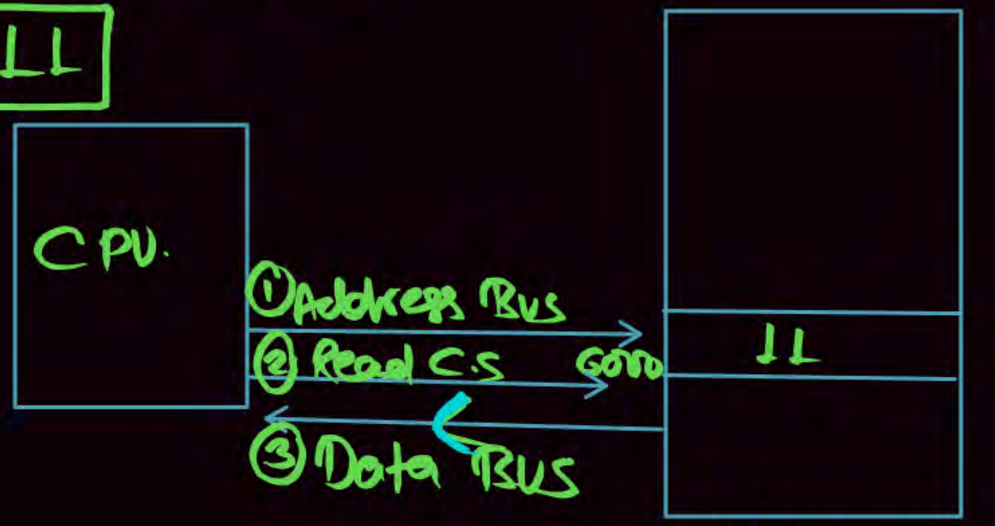
LDA

memory Read

LOAD r_0 [6000]

$r_0 \leftarrow M[6000]$

$r_0 = 11$



Assume M[6000] = 11

Memory write

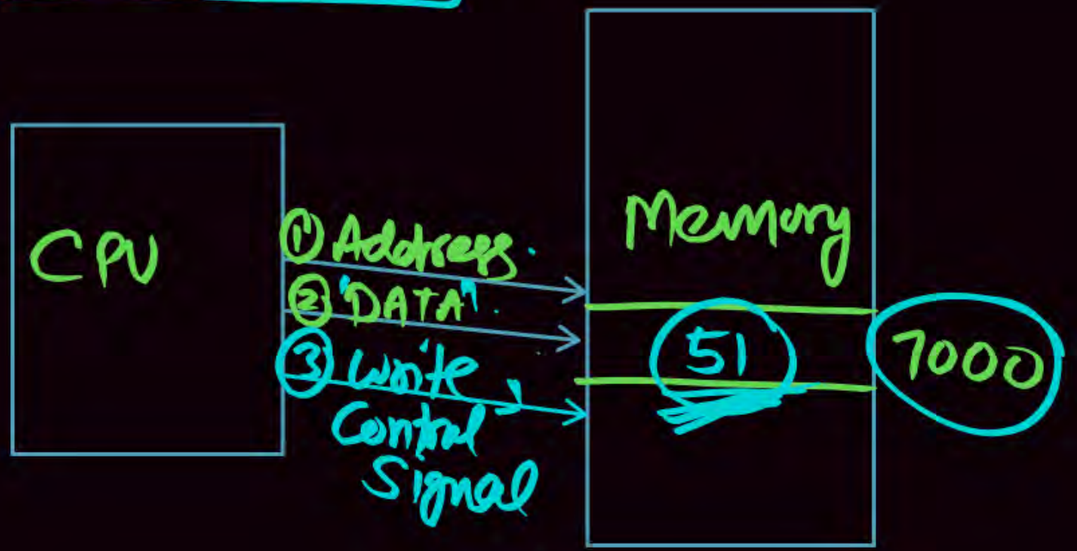
STA

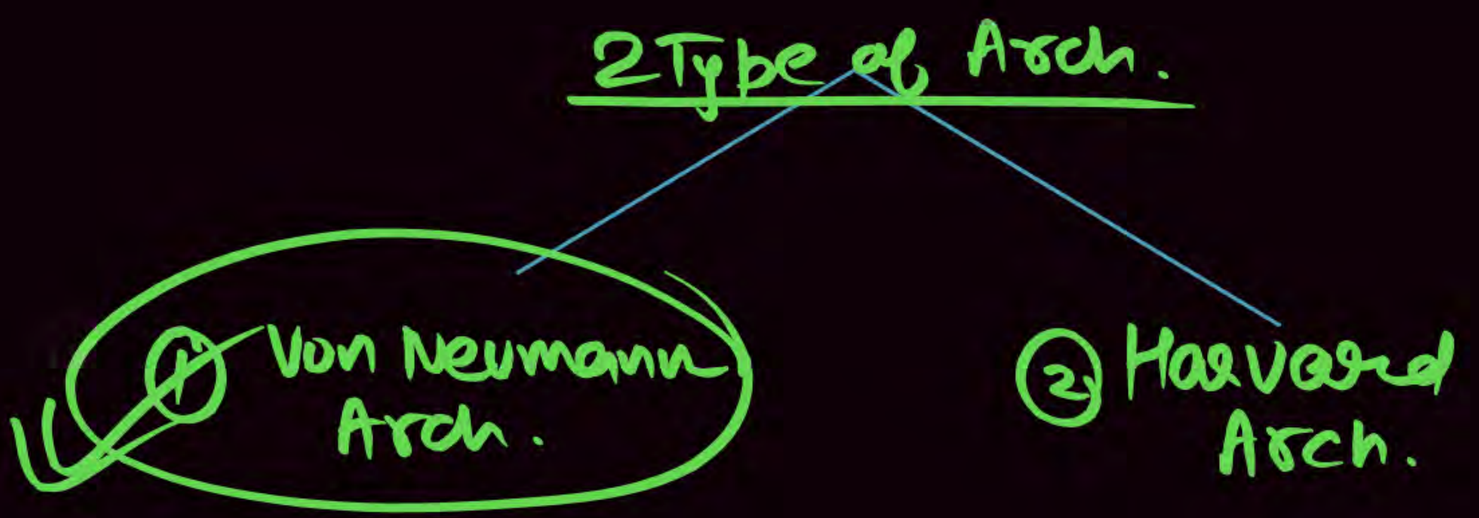
STORE [7000]

Assume AC = 51

$M[7000] \leftarrow AC$

$M[7000] \leftarrow 51$



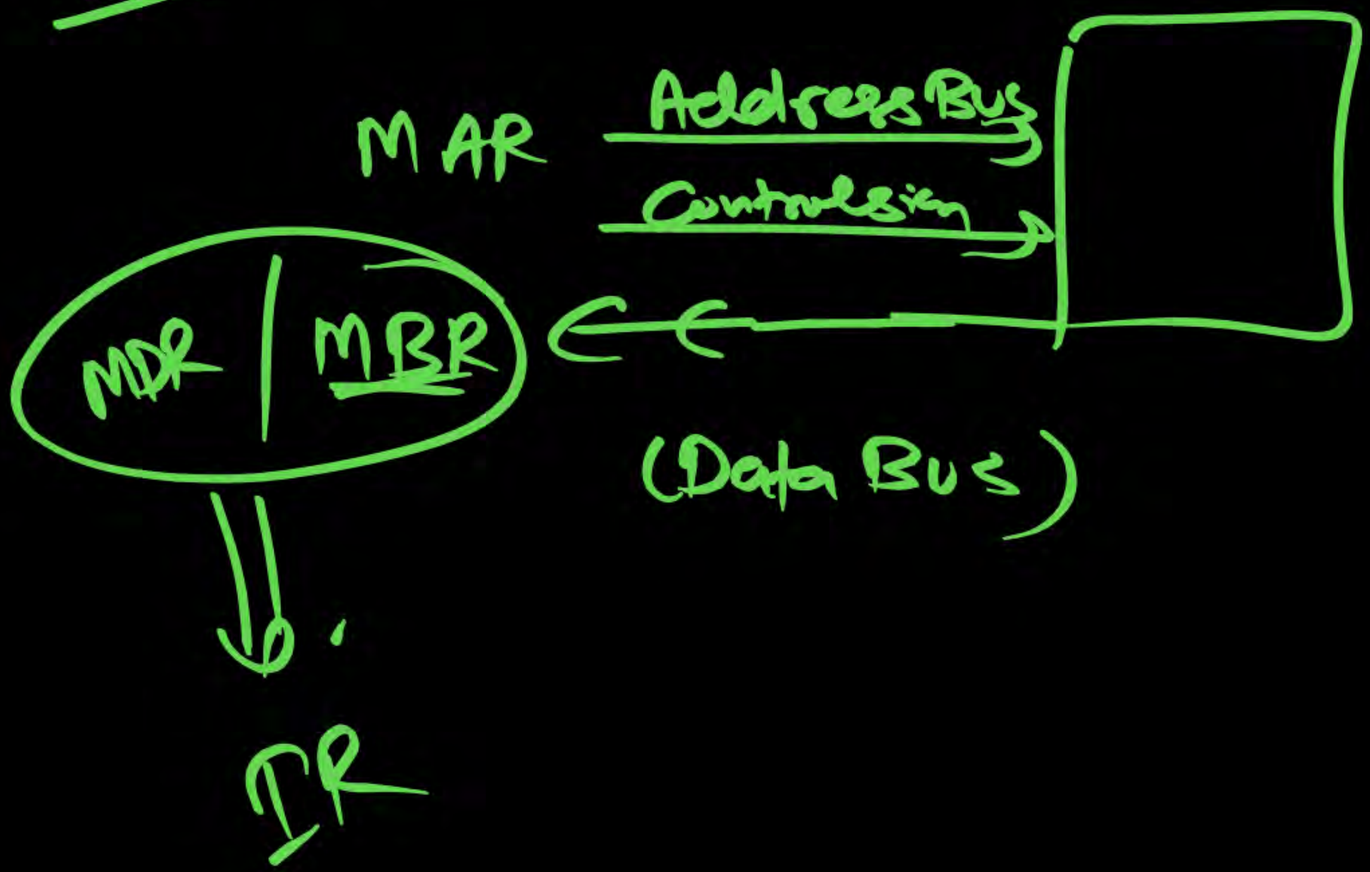

2 Type of Arch.
1 Von Neumann Arch.
2 Harvard Arch.

Computer Works on Stored Program Concept

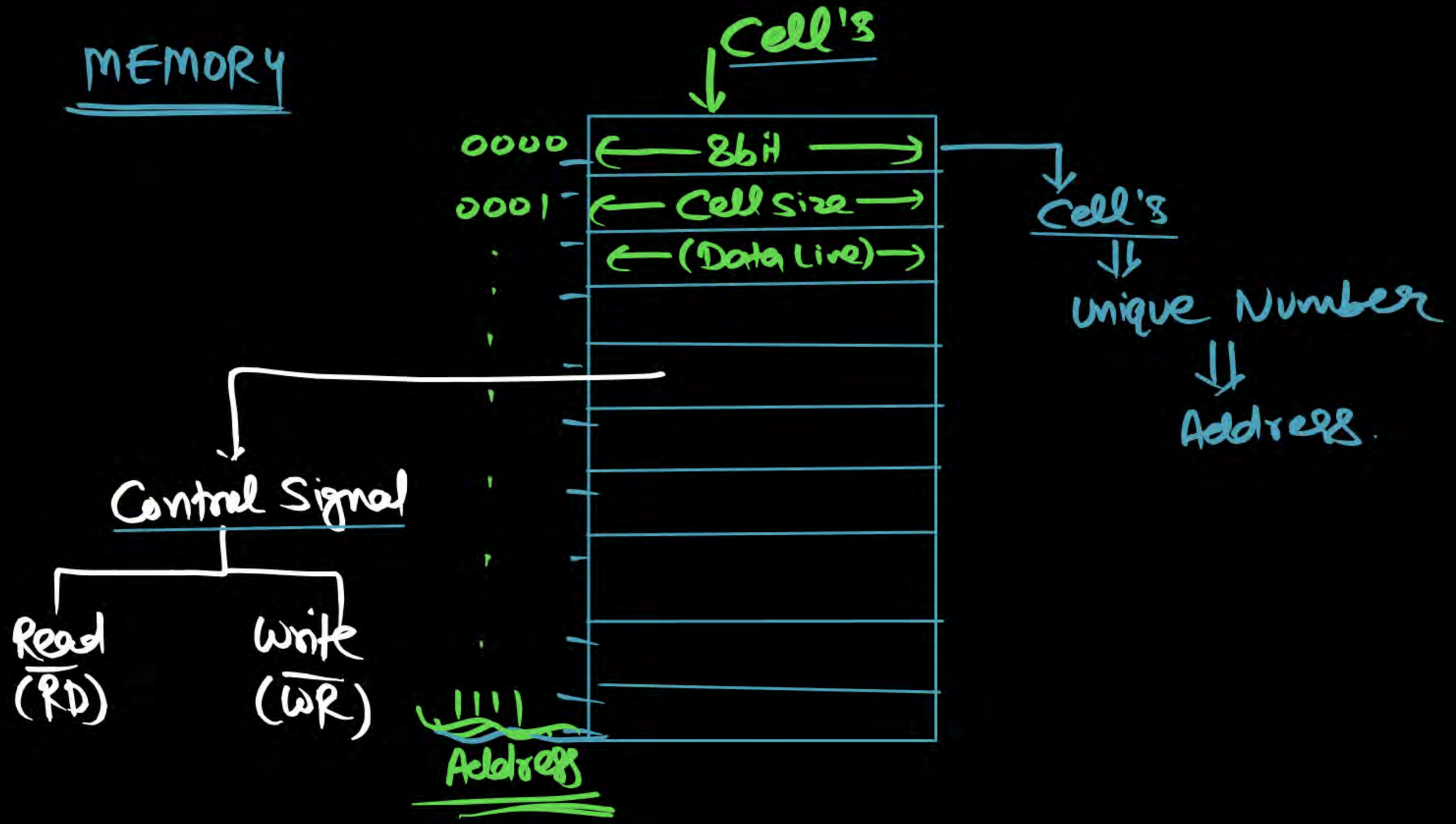
Von Neumann Arch. (Stored Program Concept)

- Main memory Contain Program & Data.
- ALU operating on Binary Data.
- Control Unit Interpreting the Instruction from Memory & Executing.
- Input Output equipment operated by Control Unit.

Instruction Fetch:



MEMORY


Cell's
0000
8bit
0001
Cell Size
(Data Line)
Cell's
Unique Number
Address
Control Signal
Read
(RD)
Write
(WR)
Address

MEMORY

- Memory is organized into equal parts, each parts is called as Cells.
- Each cell is identified by a Unique Number called as address.

Memory is Represented in the form of $2^n \times m$

$2^n \times m$

n: # of Address Line (A.L)

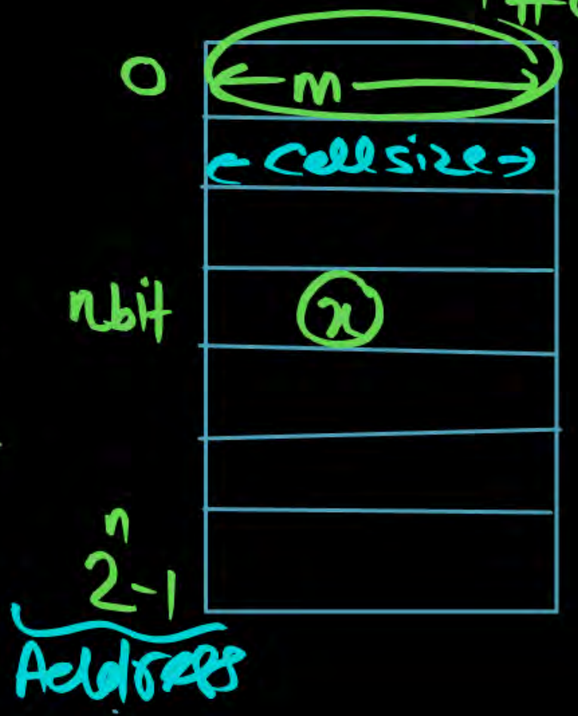
m: # of Data Line (D.L)
(Word length)

A.L ⇒ Specify the Capacity of the Memory.

D.L ⇒ Specify the Capacity of Data / Cell Size.

n bit Address Line Can Represent 2^n Memory Cells

Range (0 to $2^n - 1$) Bcz Memory start from '0'.



#ID: Number

→ Immediate Arm.

N x m

Total # Cells

$2^1 = 2$

$2^2 = 4$

$2^3 = 8$

$2^4 = 16$

$2^5 = 32$

$2^6 = 64$

$2^7 = 128$

$2^8 = 256$

$2^9 = 512$

$2^{10} = 1024$ (1 kilo)

$2^{10} = 1$ Kilo (k)

$2^{20} = 1$ Mega (M) [1024 kB]

$2^{30} = 1$ Giga (G) [1024 MB]

$2^{40} = 1$ Tera (T) [1024 GB]

$2^{50} = 1$ Peta (P) [1024 TB]

$2^{60} = 1$ Exa (E) [1024 PB]

$2^{70} = 1$ Zeeta (Z) [1024 EB]

$2^{80} = 1$ yotta (y) [1024 ZB]

1 Byte = 8 bit

1 Nibble = 4 bit

9 Byte

⇓

4 bit Required

Rc2 3bit ⇒ 0 to $2^3 - 1$

(0 to 7) ⇒ Total '8'

① 8 Byte

$2^3 \times 8$ bit

3 bit Address Line

8 bit Data line

3 bit A.L Represent 2^3 Memory Cells.

Range (0 to $2^3 - 1$)

3bit

000 ⇒ 0

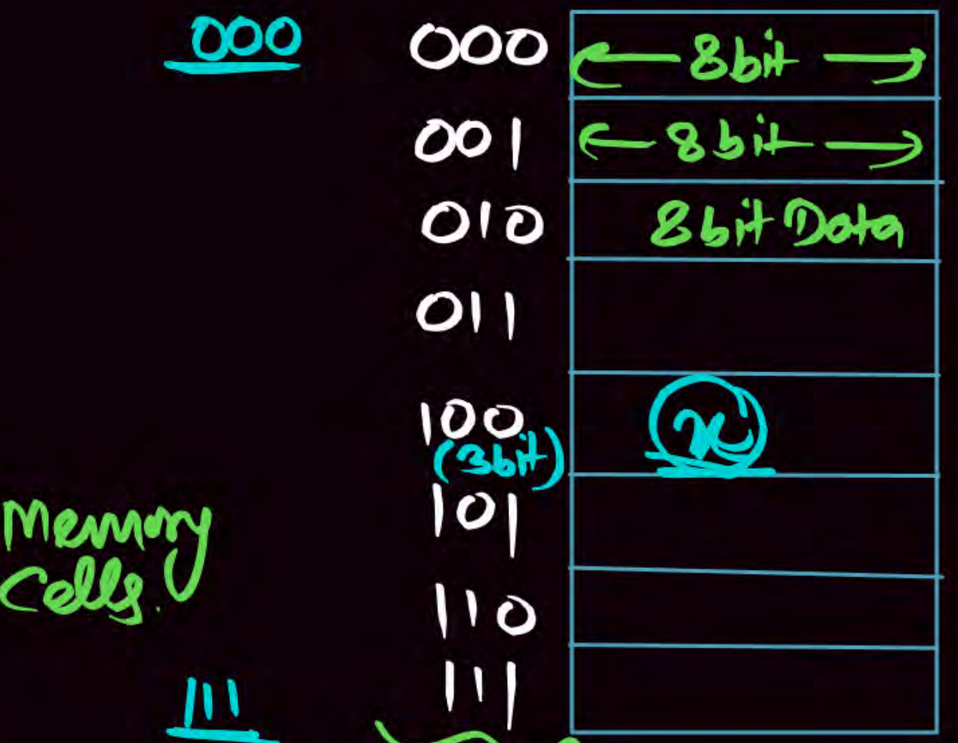
⋮ to

111 ⇒ 7

Total '8'

000

111



N X M

8 Cells x 8bit

8 Byte

2^3 Memory cells.

2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0

128 64 32 16 8 4 2 1

1 1 → '3'

000 → 0
001 → 1
010 → 2
011 → 3
100 → 4
101 → 5
110 → 6
111 → 7

② 16 Byte

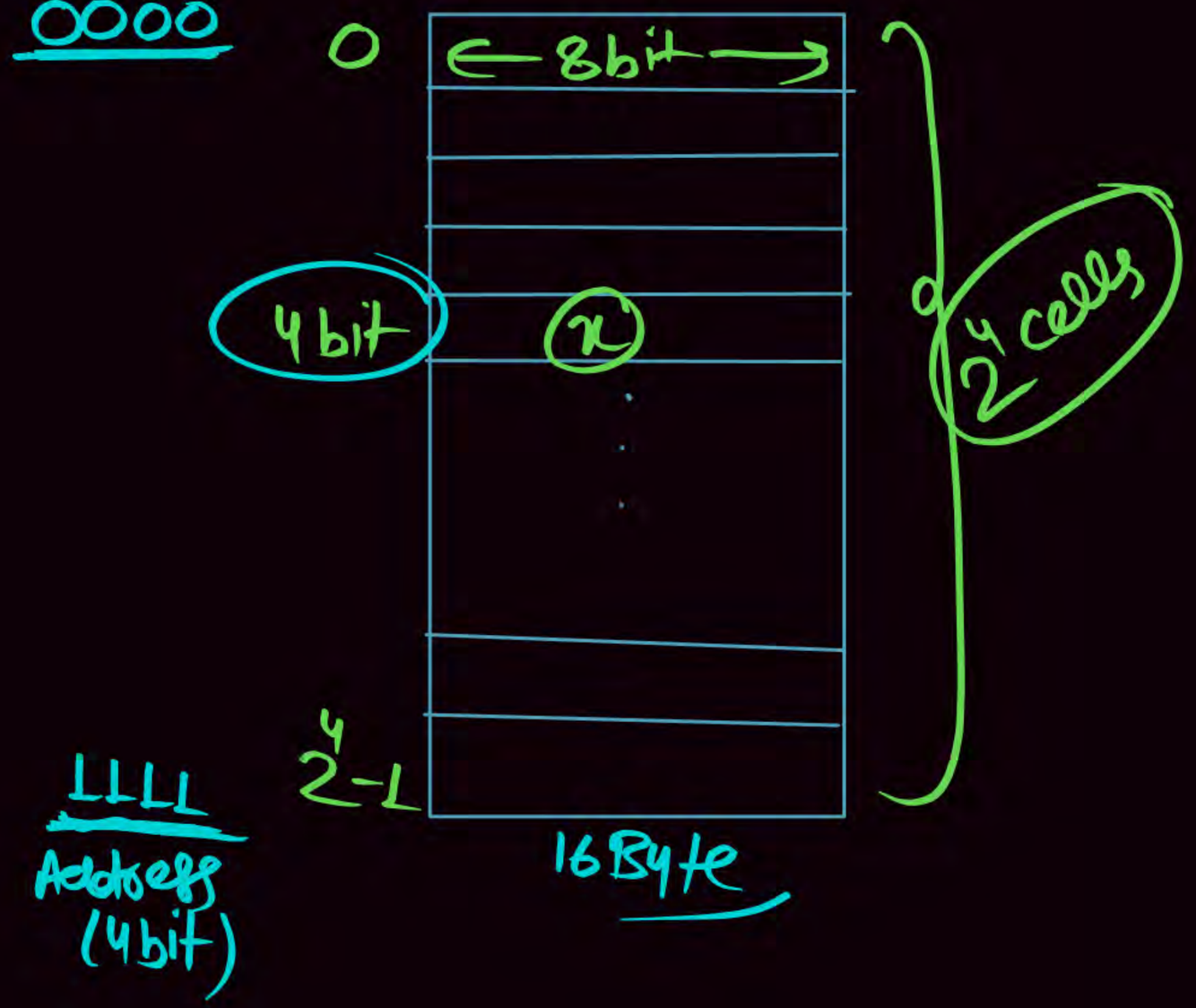
↓

$2^4 \times 8bit$

4 bit Address line

8 bit Data line

2^4 memory cells



③ 1K Byte (1024 × 8bit)

$2^{10} \times 8$ bit

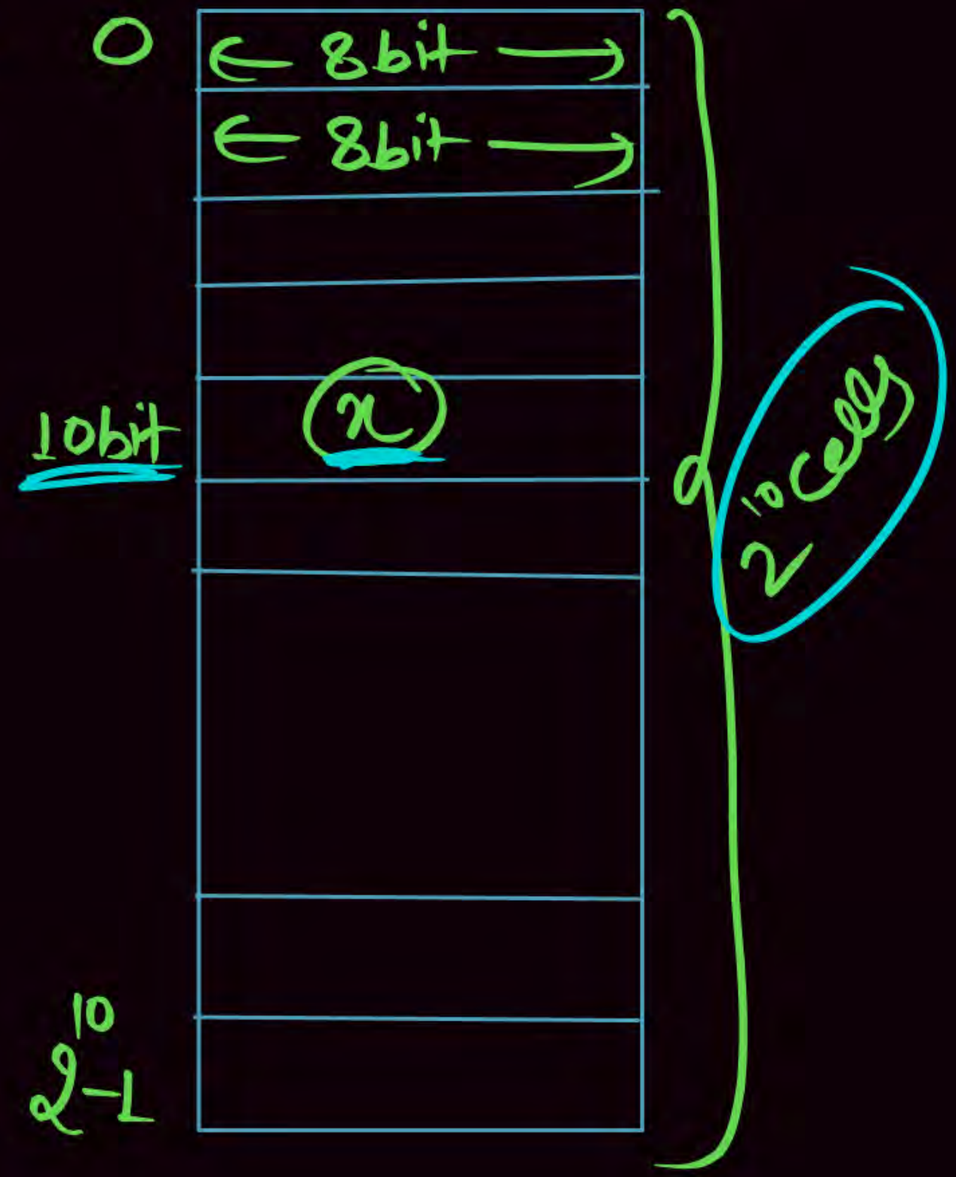
10 bit Address line

8 bit Data line

10 bit Address line can Represent

2^{10} Memory cells.

0000000000 ⟵ A I→ 10bit ⟶ 3FF



④ 64kB (8085 up)

2^6 2^{10}

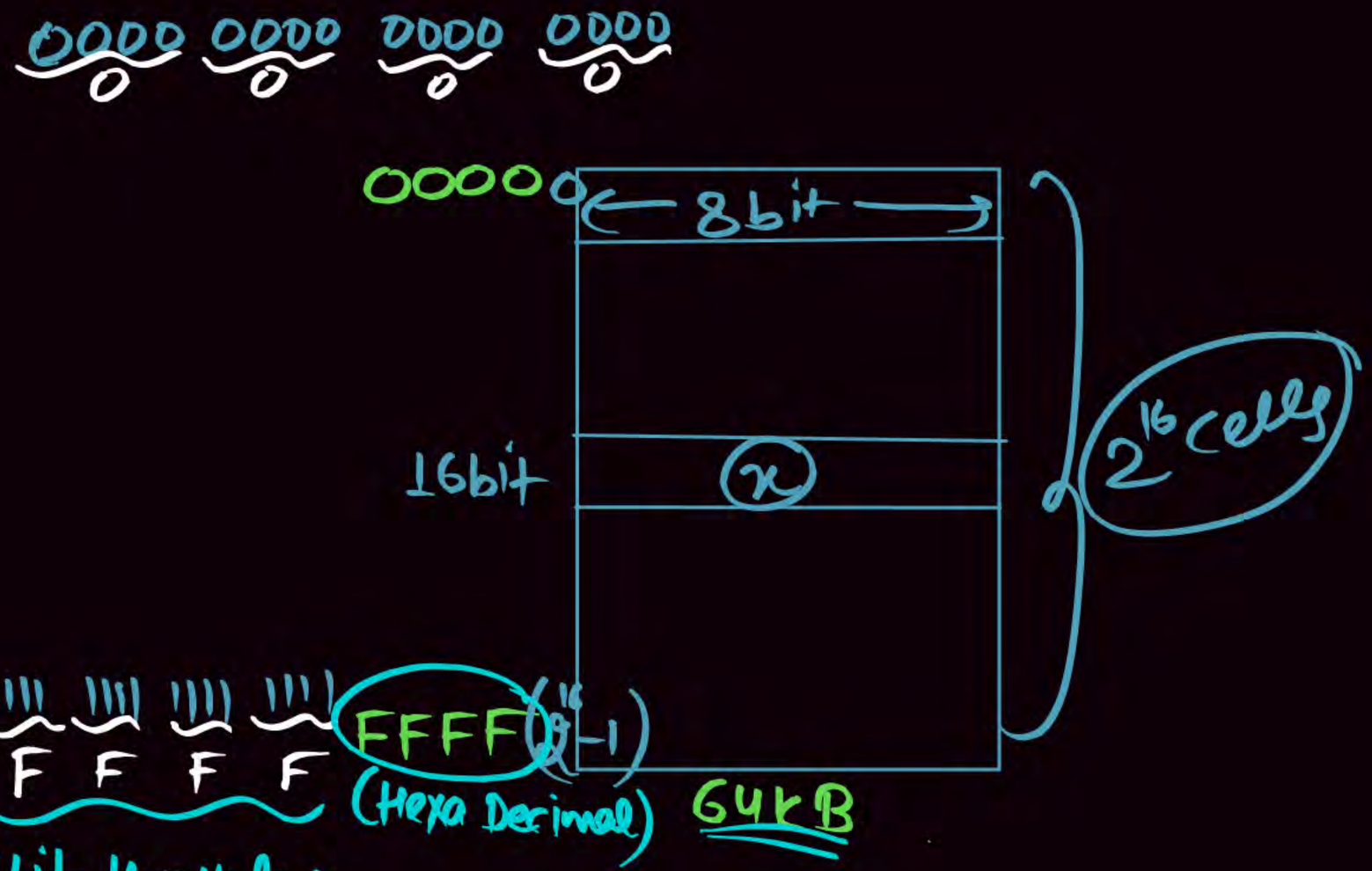
$2^{16} \times 8$ bit

16 bit Address line

8 bit Data line

2^{16} Memory cells

$(0 \text{ to } 2^{16}-1)$



for 4bit ⟶ 1 Hex Value.

⑤ 1 MByte

$2^{20} \times 8$ bit

20 bit Address line

8 bit Data.

2^{20} memory cells.

(20 bit) 0000 0000 0000 0000 0000

(in Hex) 00000

FFFFF

20 bit Hex Value

⑥ 4GB

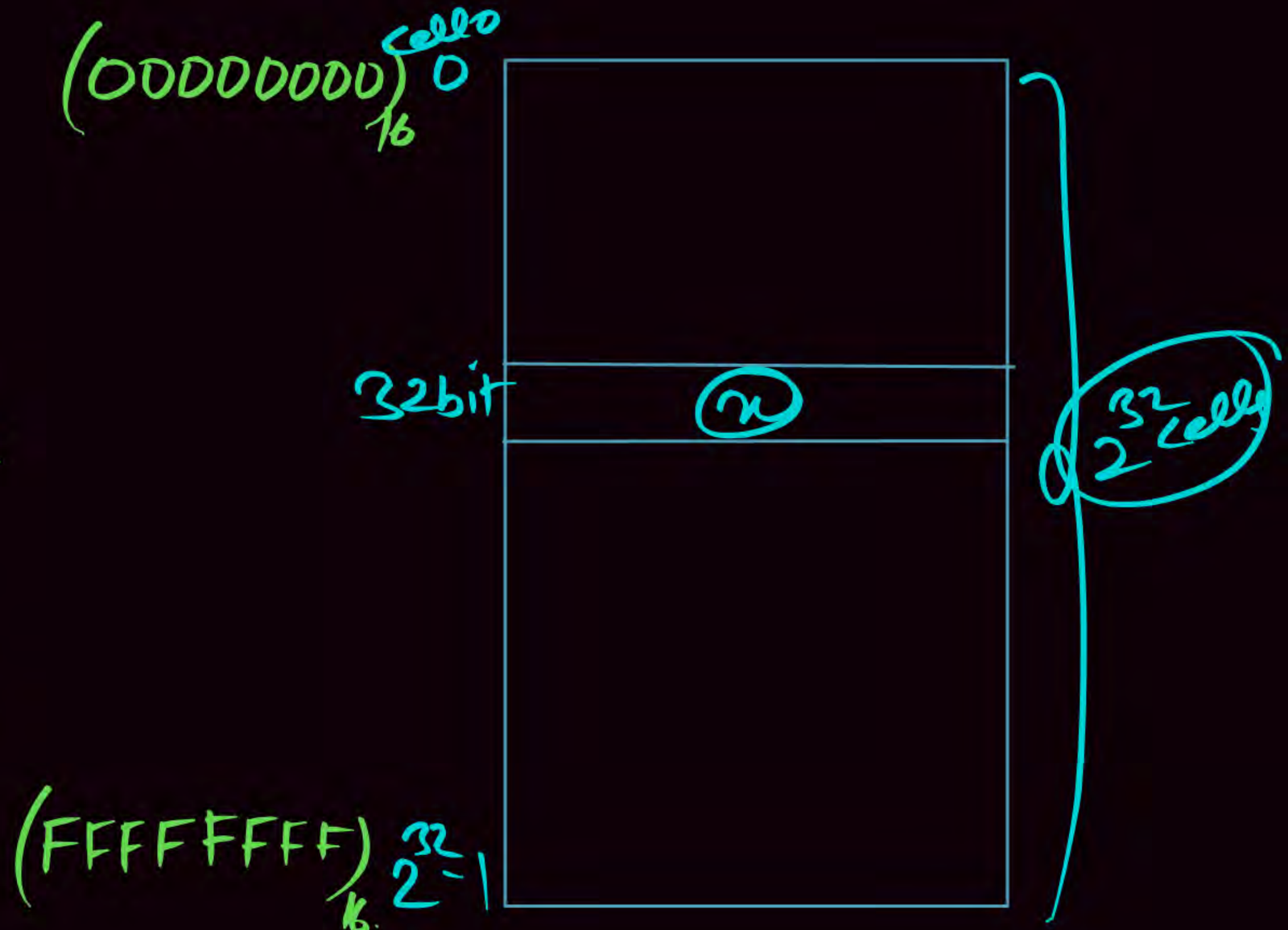
2^{4} 2^{30}

$2^{32} \times 8$bit

32 bit Address line

8bit Data line.

2^{32} Memory Cells



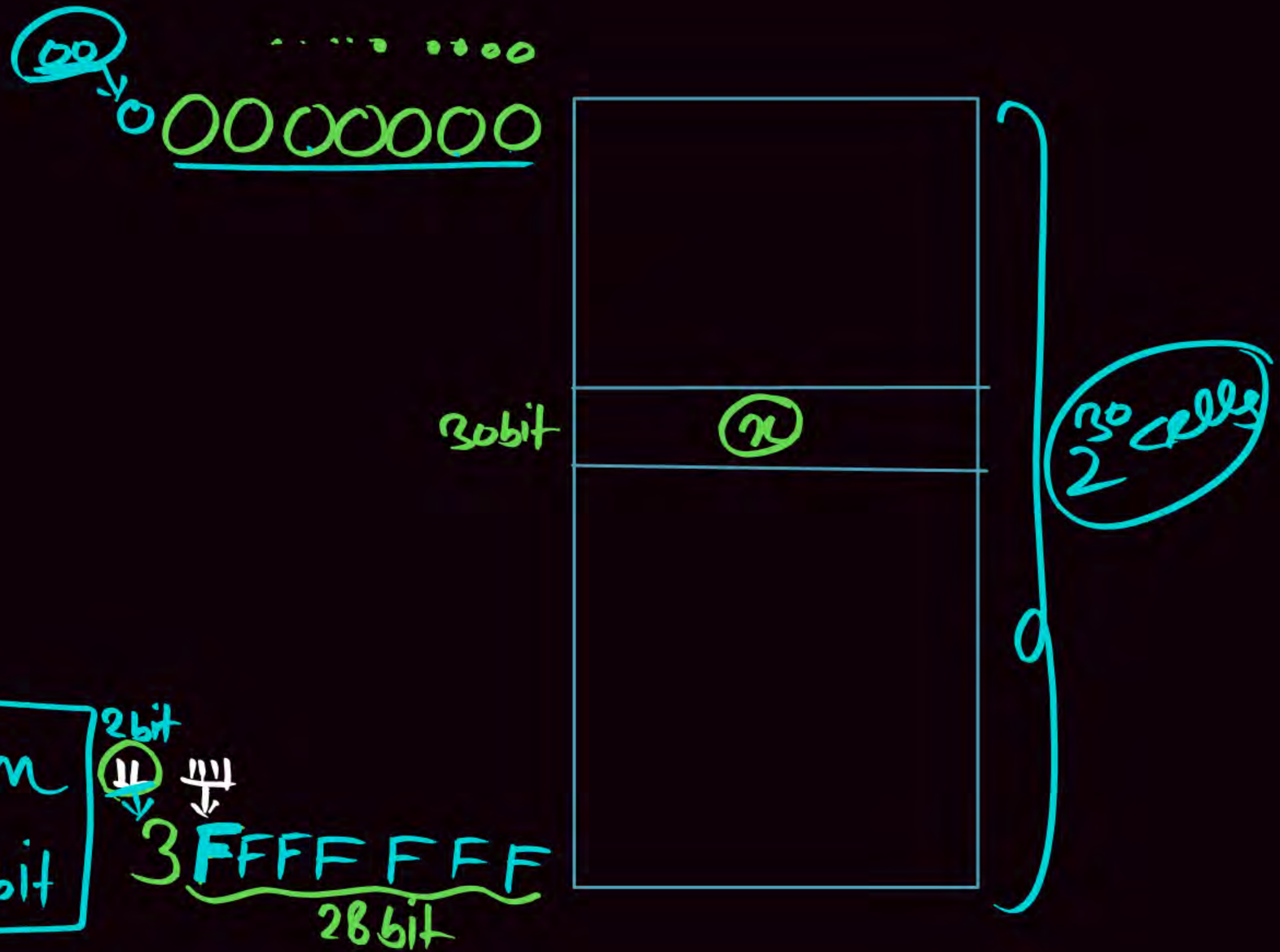
⑦ 1GB

2^{30} x 8bit

30 bit Address line

8 bit Data Line

2^{30} Memory cells



Q. The Capacity of a memory unit is defined by the Number of word Multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of 64K×16?

(a) 8 address, 8 data line

(b) 16 address, 8 Data line

(c) 15 address, 16 Data line

(d) 16 address, 16 Data line ✓

64k × 16 $[2^n \times m]$

$2^{16} \times 16$

16 bit Address line

16 bit Data line.

Q. Consider a system which has 1024 k words. Each word has the size of 32 bits then what is the capacity of memory in MB (Mega Byte) _____

Soln

1024 K Words

1024 K X 4Byte

$2^{10} \times 2^{10} \times 2^{2}$

2^{22} Byte

$2^{2} \times 2^{20}$ Byte

4MByte Ans

1 Word = 32 bit

1 Word = 4 Byte

Q. The Capacity of a memory unit is defined by the Number of word Multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of 4K×16?

(a) 10 address, 16 data line

(b) 11 address, 8 Data line

(c) 12 address, 16 Data line

(d) 12 address, 12 Data line

[GATE-2 Marks]

$4K \times 16$

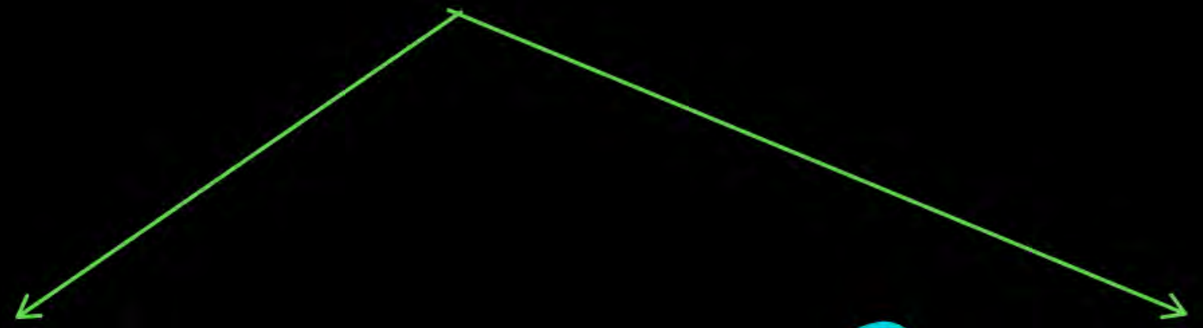
$\Downarrow$

$2^{12} \times 16$

12 bit A.L

16 bit D.L

Based on the cell size memory are 2 Type of Addressable.



① Byte Addressable

[When 1 cell size is 8 bit]

② Word Addressable.

[When 1 cell size is 1 Word]

THANK YOU!