COMPUTER SCIENCE

Computer Organization and Architecture

ALU & Control unit

Lecture_02

Vijay Agarwal sir

01 Micro Operation

- ✓ Introduction of COA
- ✓ Mic Instn & AM
- ✓ Floating Point Representation.

Micro operation, Micro program
DATA Path & Control Unit

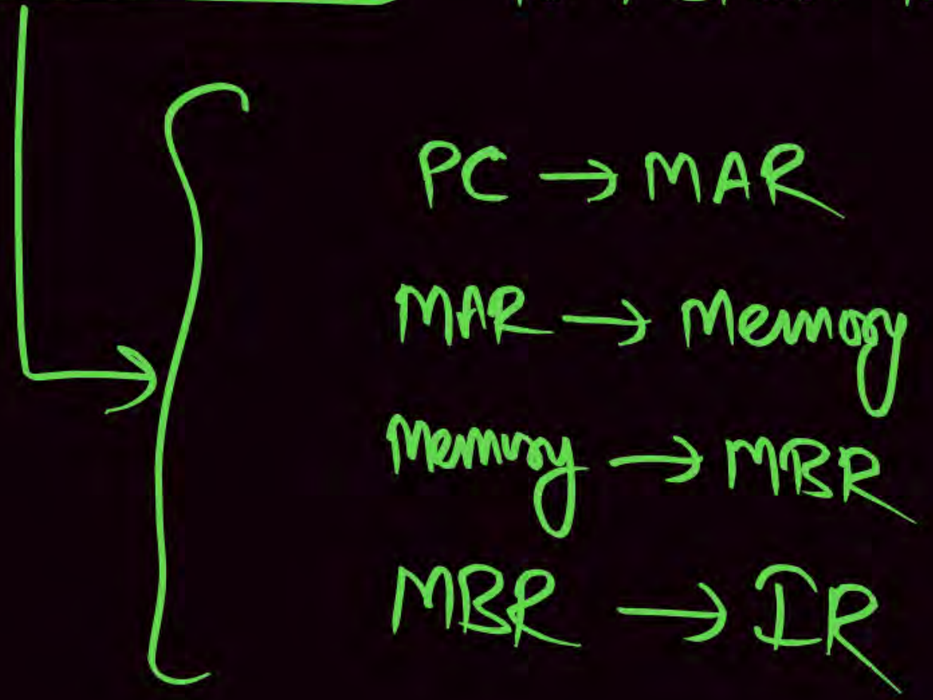
Micro operation

Instruction Cycle

Subcycle

- ① Fetch cycle
- ② Execute cycle
  - Decode
  - Execute

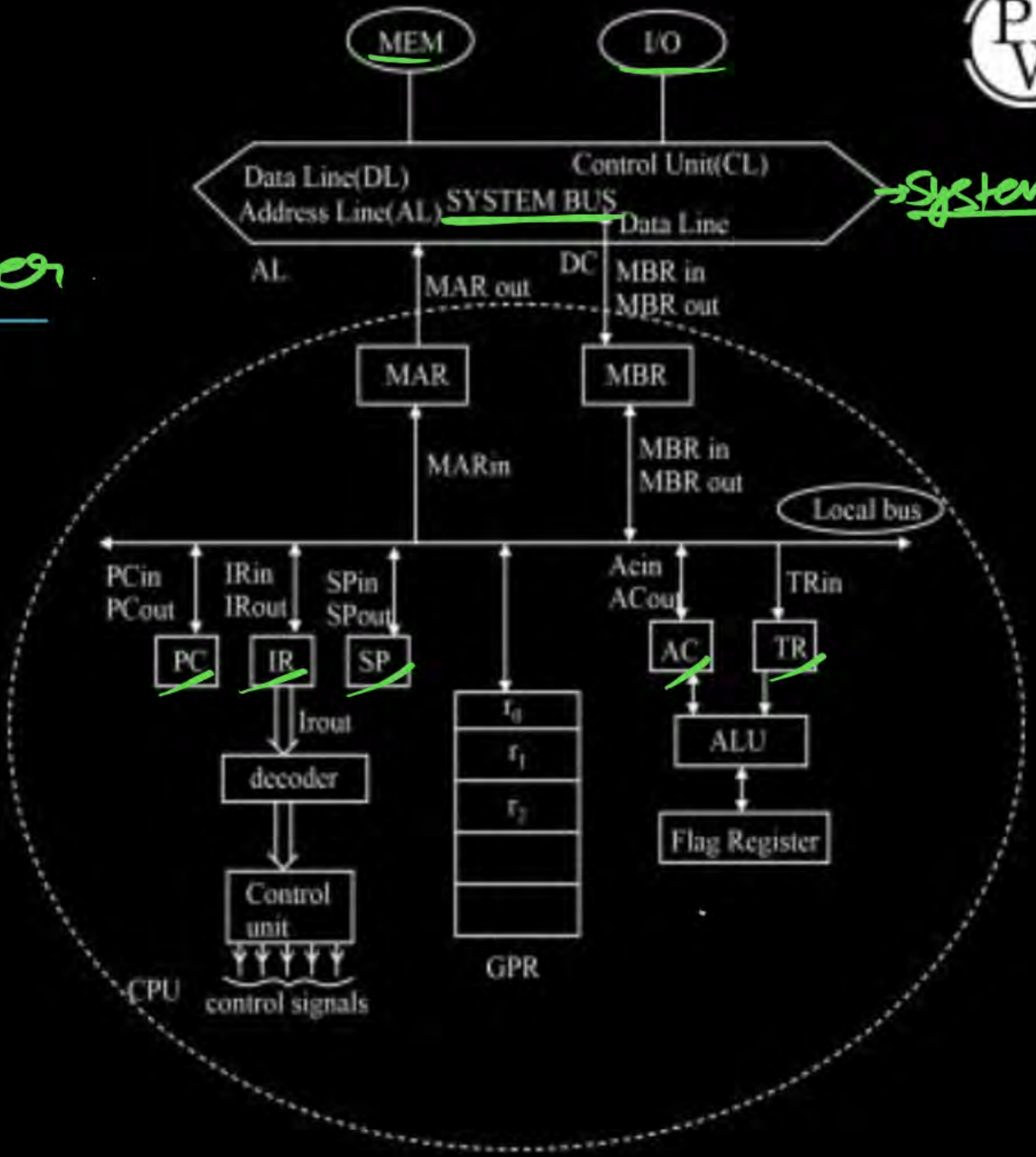
Fetch cycle : To Fetch the Instn from Mem to CPU(IR)



Structure of Computer

Component of the Computer

1. Memory
2. CPU
3. I/O

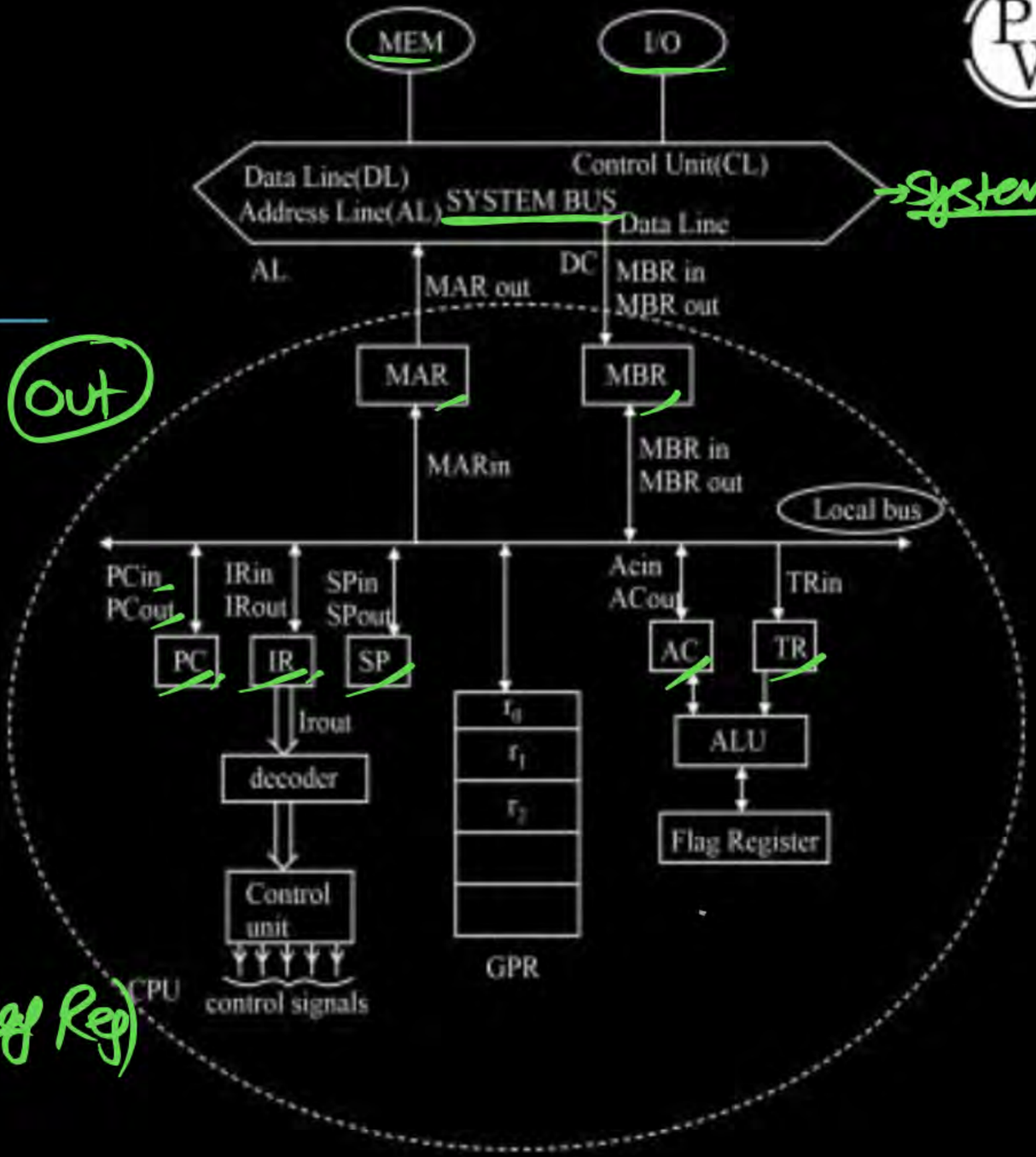


Structure of Computer

CPU ORG.

1. Register
2. ALU
3. Control Unit

PC (in) (out)
MAR
MBR
IR
AC
TR
SP
PSW (Flag Reg)
GPR

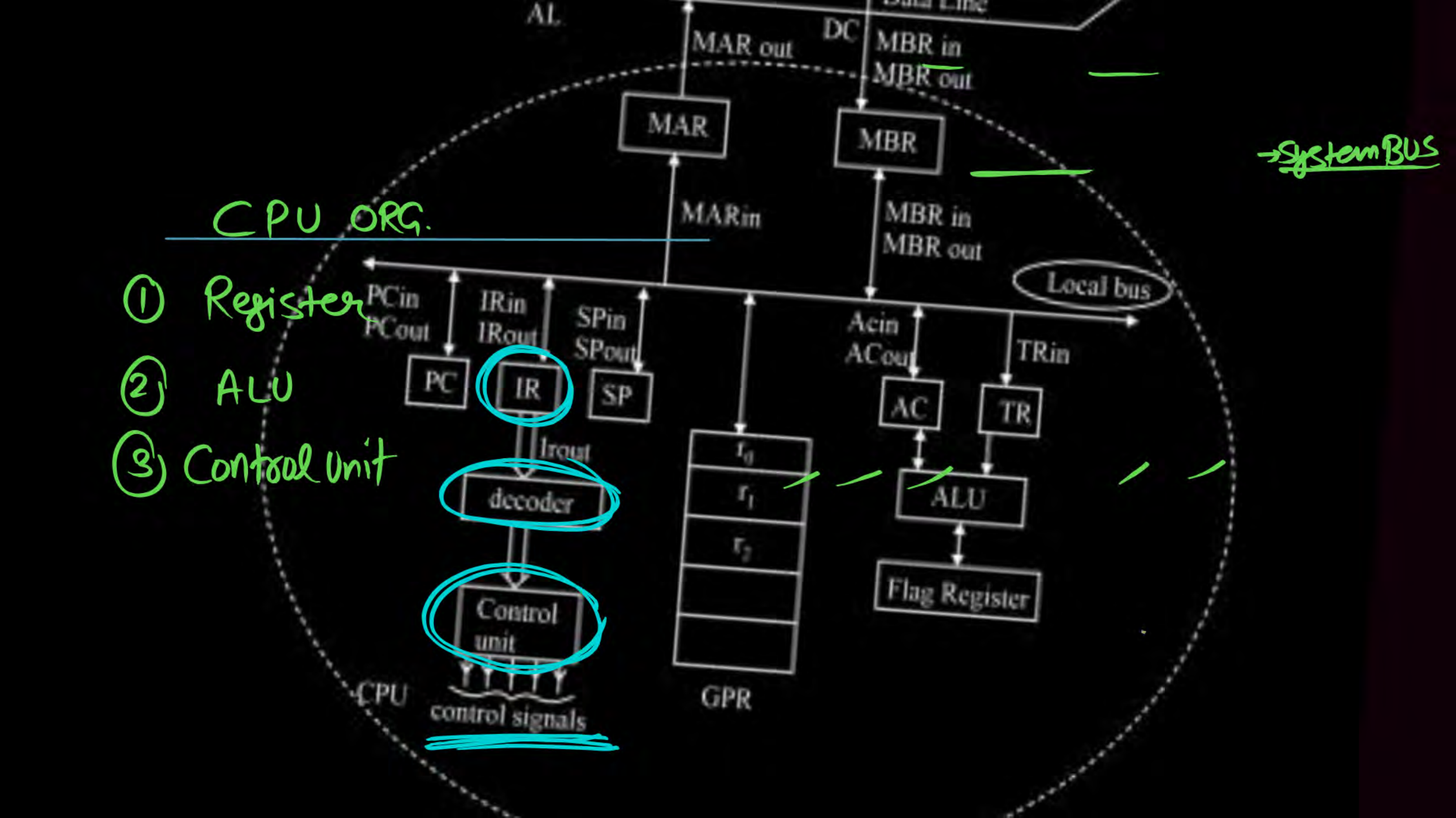


AR / MAR (Memory Address Register): Connected to Address line of the System Bus.

DR / MDR (Memory Data Register): Connected to the Data line of the System Bus.

$R_o \longrightarrow R_L$

R_{out} $R_{L\,in}$



CPU ORG.

① Register

② ALU

③ Control unit

→ System BUS

Component of Computer

1. CPU , 2. Memory & 3. IO

Memory
Register
ALU
Timing Signals, Control signals
Flags(PSW)

Component of Computer

1. CPU , 2. Memory & 3. IO

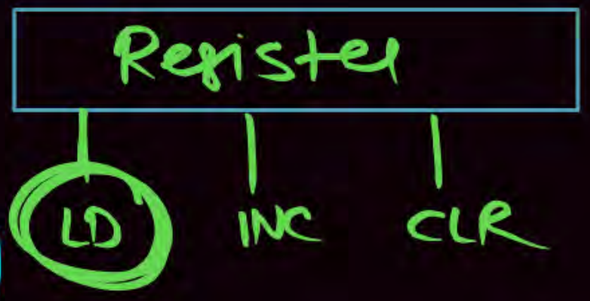
- Memory
- Register
- ALU
- Timing Signals, Control signals
- Flags(PSW)

Why Common Bus ?

Register: (Flip Flop) is collection of bit | Sequence of bits & each bit Stored in Flip Flop.

General & Special Purpose Register

Special Register.



Register is Temporary Storage.

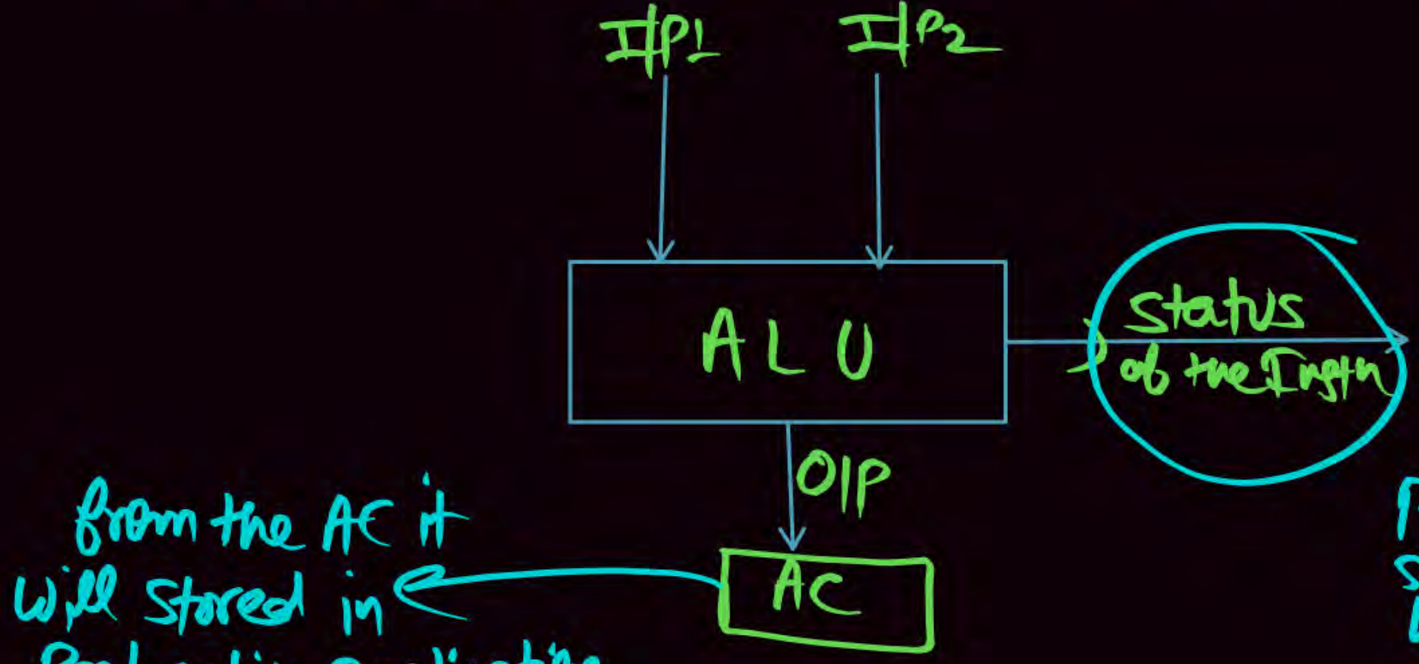
LD : Load

INC : Increment (Binary Counter)

CLR : Clear.

ALU : (Perform Arithmatic & Logical operations, Condition Checking & etc) → Hardware.

↳ Perform Multiple type operation.



Conditional Flag.

1. Carry
2. Sign
3. Auxillary Flag
4. Zero
5. Parity
6. Overflow Flag.

Control Unit

Timing Signal & Control Signal

Timing Signal: To Execute the Instruction in Proper sequence.

(a) (i) Fetch
(ii) Decode
(iii) Execute

In Fetch

T_1: PC → MAR

T_2: M[MAR] → MBR

T_3: MBR → IR

Control Signal: How & WHAT to do

Each & every thing Coroodinate.

eg.

Non Technical example.

III Exam writting
II Admit Card
I Enrollment (Registration)
IV Result.

T_1: Enrollment (Registration)
T_2: Admit Card
T_3: Exam writing
T_4: Result.

Q If we have 16 Register, 1 Memory, 1 ALU, 1 PSW & 1 other component.

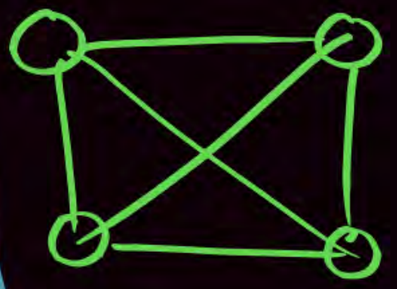
Total 20 Component (Parts)

$\hookrightarrow {}^{20}C_2 \Rightarrow$ More than 180+ Connection.

So the Solution Instead of using 180+ Connection, Connect all Component to a Common Bus (Internal BUS)

But Only 2 Parts are Communicate at a time for that (Which Parts Communicate) Control Signals are Required.

Q 4 Component (Parts)



${}^{4}C_2 = 6$

then 6 Connection

Working of Register

(eg) 4 Register A, B, C, D.

each Register of 4 bit.

V.V.V.Imp

> The Number (#) Multiplex = Number of bits in the Register.
>
> Size of Multiplex = Number of Register.

(eg) Here we have 4 Register & each Register is of 4 bits

#Mux = 4 (#bits in the Register)

Size of Mux = 4 (#Register) 4X1 mux

Q If we have m Register. each of Register Size n bits then Number of MUX & Size of MUX ?

Soln

Number of Multiplex (MUX) = n (# of bits in the Register)

Size of mux = M bit (# Registers).
mx1

④ If we have 32 Register & each Register Size is 8bit then

(i) What is Number of MUX = 8 (#bits in Register)

(ii) Size of MUX = 32X1 (#Registers)

Working of Register

(eg) 4 Register A, B, C, D.

each Register of 4 bit.

V.V.V.Imp

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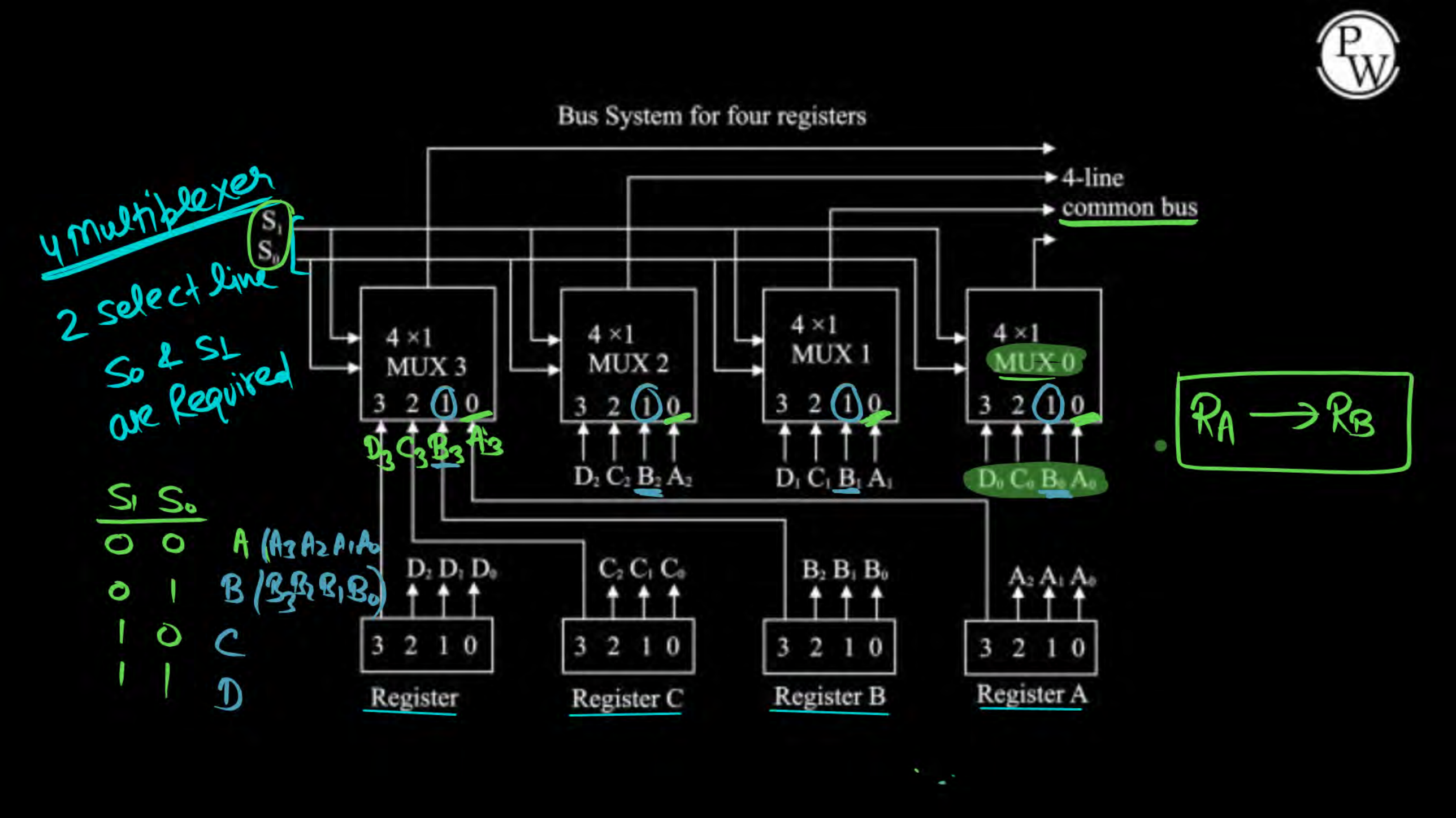

Bus System for four registers
4 Multiplexer
2 select line
S0 & S1 are Required
S1
S0
4-line common bus
4 ×1 MUX 3
4 ×1 MUX 2
4 ×1 MUX 1
4 ×1 MUX 0
3 2 1 0
D3 C3 B3 A3
D2 C2 B2 A2
D1 C1 B1 A1
D0 C0 B0 A0
RA → RB
S1 S0
0 0 A (A3 A2 A1 A0
0 1 B (B3 B2 B1 B0)
1 0 C
1 1 D
D2 D1 D0
C2 C1 C0
B2 B1 B0
A2 A1 A0
Register
Register C
Register B
Register A

$(A_3A_2A_1A_0)$; A 0 0 means input '0' will be Select across all MUX.

$(B_3B_2B_1B_0)$; B 0 1 means input '1' will be Select from all MUX.

$(C_3C_2C_1C_0)$; C 1 0 means input '2' will be Select from all MUX

$(D_3D_2D_1D_0)$; D 1 1 means input '3' will be Select from ALL MUX.

Function Table for Bus of Fig.

S_1	S_0	Register selected	
0	0	A	$(A_3 A_2 A_1 A_0)$
0	1	B	$(B_3 B_2 B_1 B_0)$
1	0	C	$(C_3 C_2 C_1 C_0)$
1	1	D	$(D_3 D_2 D_1 D_0)$

How Data is Transferred ?

Task:

Register A to Register B

$R_A \rightarrow R_B$.

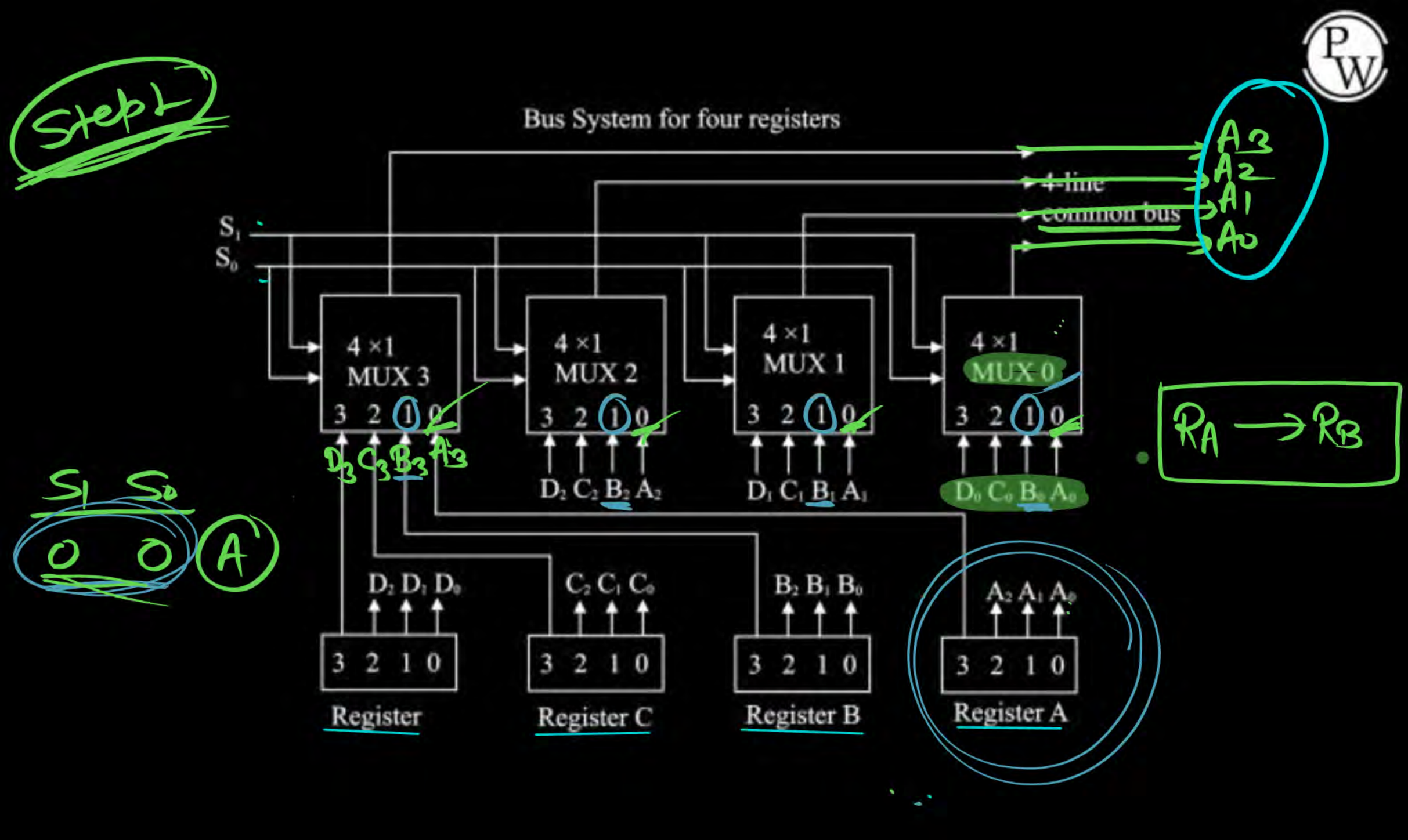
T_1: R_{Aout} R_{Bin}

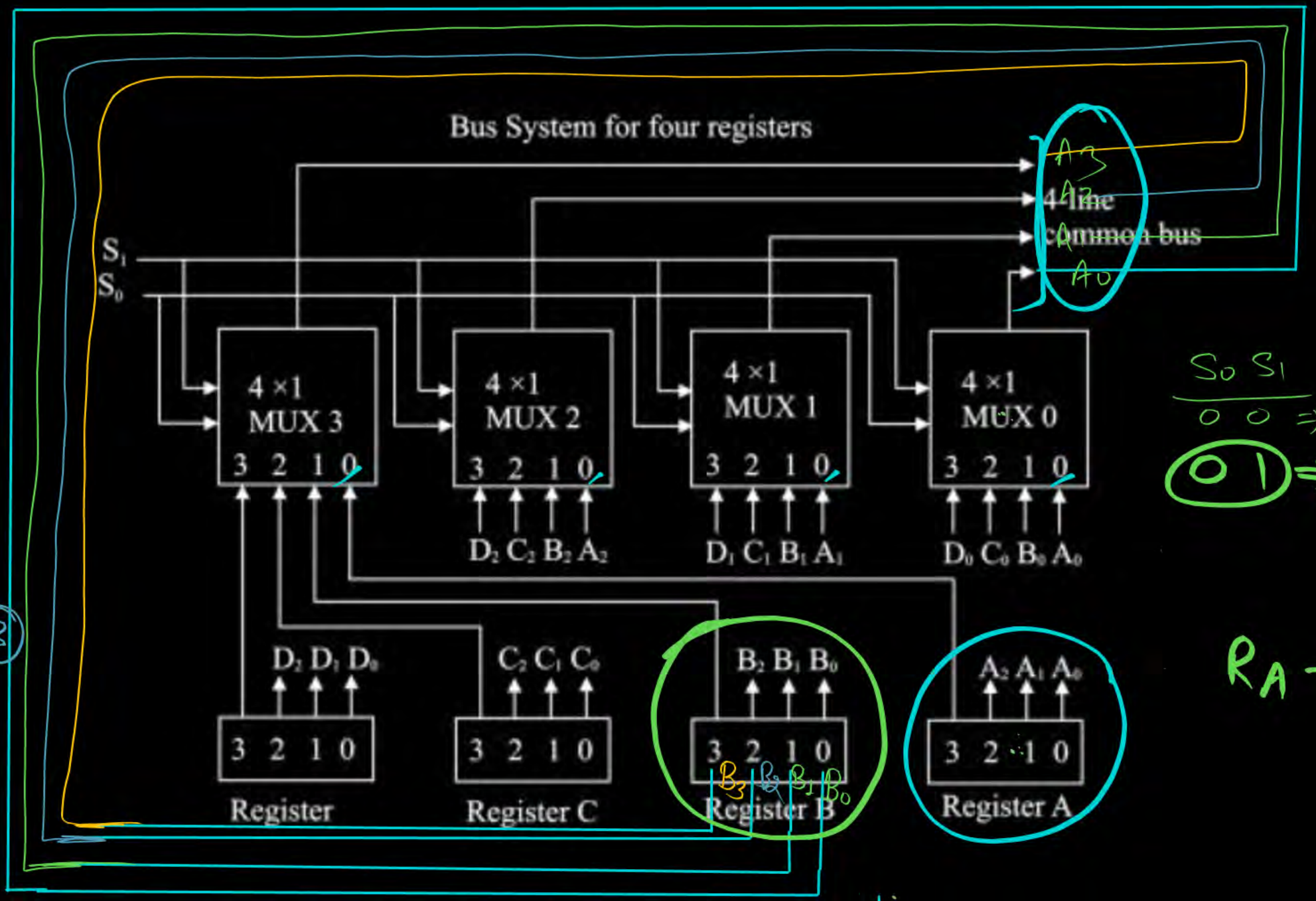
$R_A \rightarrow R_B$

Process: Register A Content given to MUX then

MUX to Common Bus then

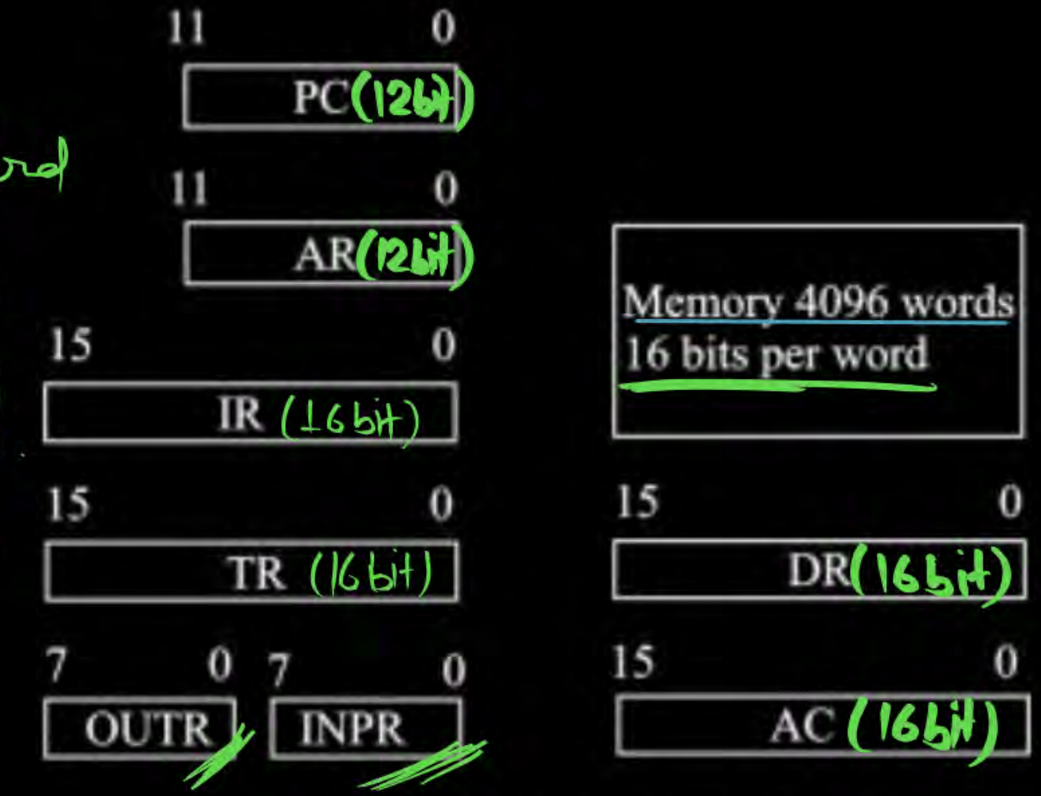
Common Bus to Load into Register B.


Step 1
Bus System for four registers
4-line common bus
S_1
S_0
4 ×1 MUX 3
4 ×1 MUX 2
4 ×1 MUX 1
4 ×1 MUX 0
3 2 1 0
D_3 C_3 B_3 A_3
D_2 C_2 B_2 A_2
D_1 C_1 B_1 A_1
D_0 C_0 B_0 A_0
A_3 A_2 A_1 A_0
$R_A \rightarrow R_B$
S_1 S_0
0 0 A
D_2 D_1 D_0
C_2 C_1 C_0
B_2 B_1 B_0
A_2 A_1 A_0
3 2 1 0
Register
Register C
Register B
Register A


Bus System for four registers
4-line common bus
S_1
S_0
4 ×1 MUX 3
4 ×1 MUX 2
4 ×1 MUX 1
4 ×1 MUX 0
3 2 1 0
D_2 C_2 B_2 A_2
D_1 C_1 B_1 A_1
D_0 C_0 B_0 A_0
D_2 D_1 D_0
C_2 C_1 C_0
B_2 B_1 B_0
A_2 A_1 A_0
Register
Register C
Register B
Register A
Step2
S_1 S_0
0 1 (B)
LOAD
(RB)
S_0 S_1
0 0 ⇒ A
0 1 ⇒ B
$R_A \rightarrow R_B$.

	S_1	S_0	
$(A_3A_2A_1A_0)$	0	0	; 0 0 means input '0' will be Select across all Mux.
$(B_3B_2B_1B_0)$	0	1	; 0 1 means input '1' will be Select from all Mux.
$(C_3C_2C_1C_0)$	1	0	; 1 0 means input '2' will be Select from all Mux
$(D_3D_2D_1D_0)$	1	1	; 1 1 means input '3' will be Select from ALL Mux.

Design a Small Computer



Basic computer registers and memory

I/P From key Board

Input Register (8bit)

Output Register (8bit)
↳ Display or output

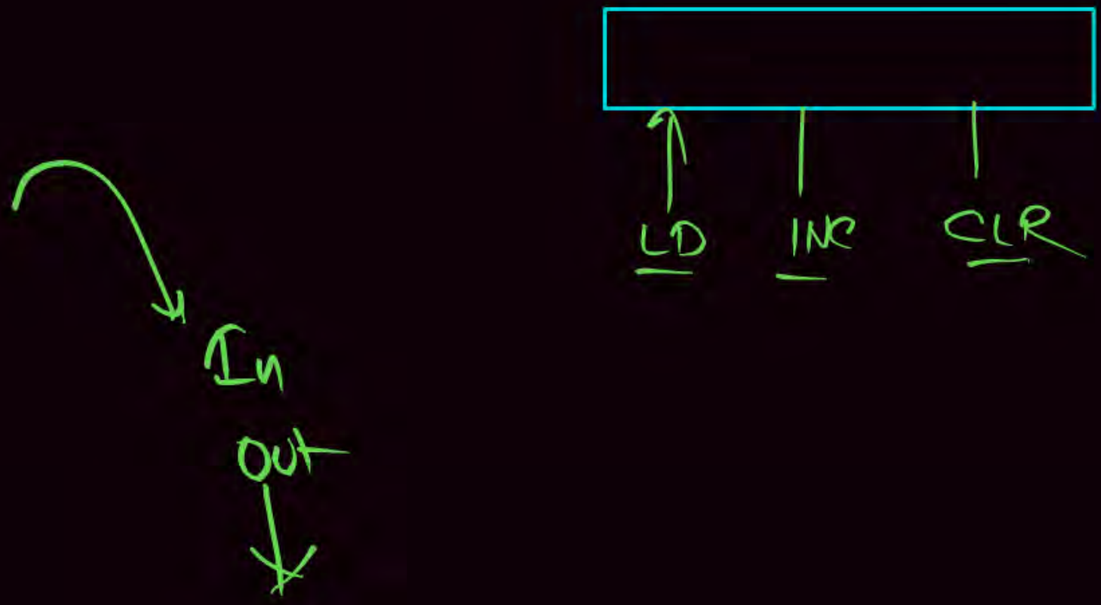
Connected to key Board

12 bit Address Line
16 bit Data Line.

Memory
4096 × 16 ⇒ $2^{12} \times 16$

A.R = 12 bit
D.R = 16 bit

16 bit word Load from the Memory.



Address Reg (AR) Connected to Address Line of the System BUS.

MBR (DR) Connected to Data line of the System BUS.

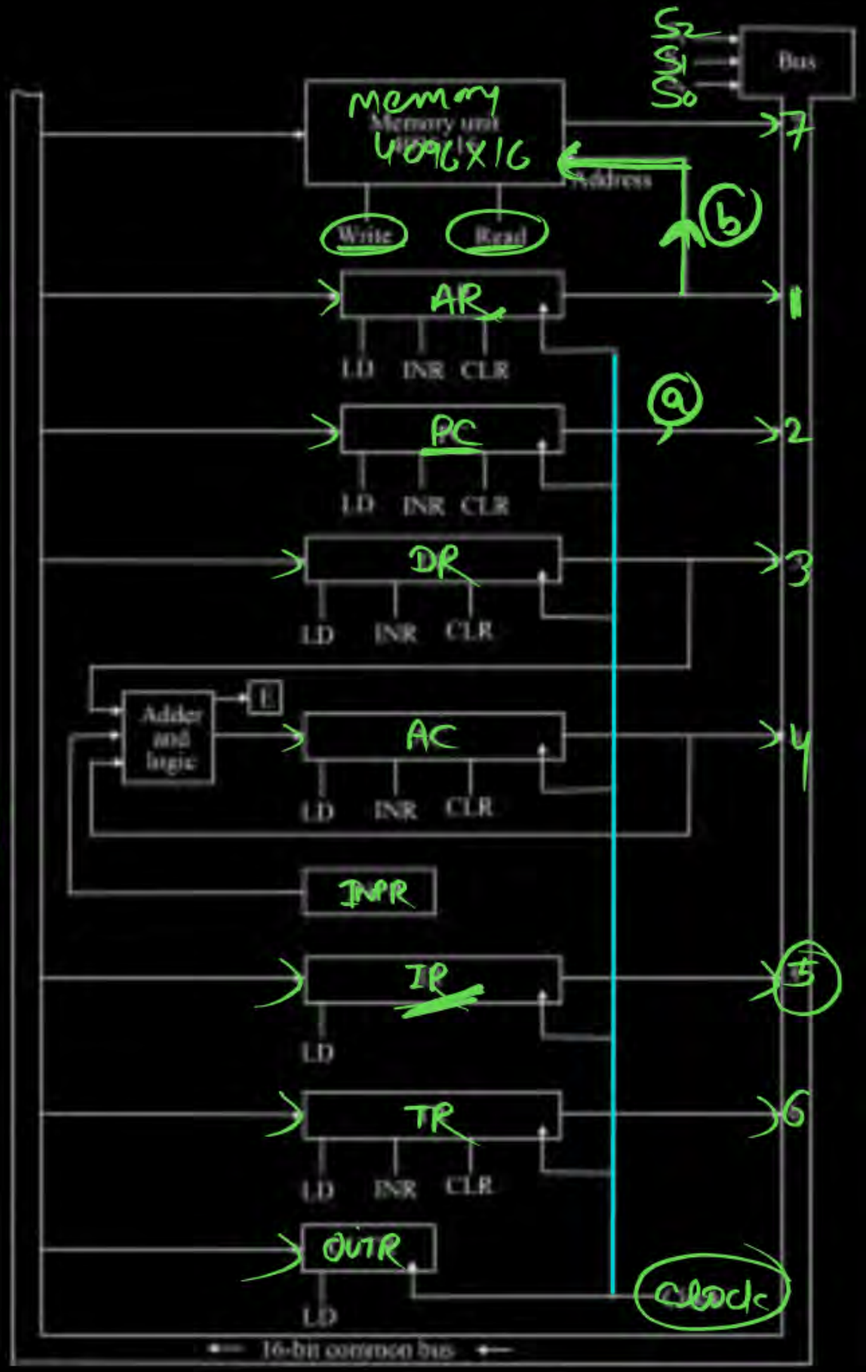
Working

Total 7 unit Connected to a Bus So

3 Select are Required.

$S_2 S_1 S_0$

1 1 1 → 7 (Memory)



Basic computer registers connected to a common bus

(Read CS)

Load from Memory.

Memory

'7' $S_2 S_1 S_0$

1 1 1 ⇒ Memory (7)

memory have n location so Which Memory Address Content (Data) Load into Bus is given by AR (Address Reg.) (MAR)

1 1 1 → Memory (7)

0 1 0 → PC (2)

1 0 1 → IR (5)

PC → MAR (AR)

010 ⇒ 2 (PC), PC will be Enable then Content of PC is Put into Common Bus & AR Register (Load (In) is set to 1 (Active) So AR get the Memory Address

---

Memory
PC
IR

} But in what Sequence (timing) which operation Performed, Done (taken) by Timing Signal.

Fetch cycle : Instn is Fetch from Memory to CPU (IR)

PC → M[MAR]

MAR → Memory

Memory → MBR

MBR → IR

T_1: PC → MAR

T_2: M[MAR] → MBR

T_3: MBR → IR

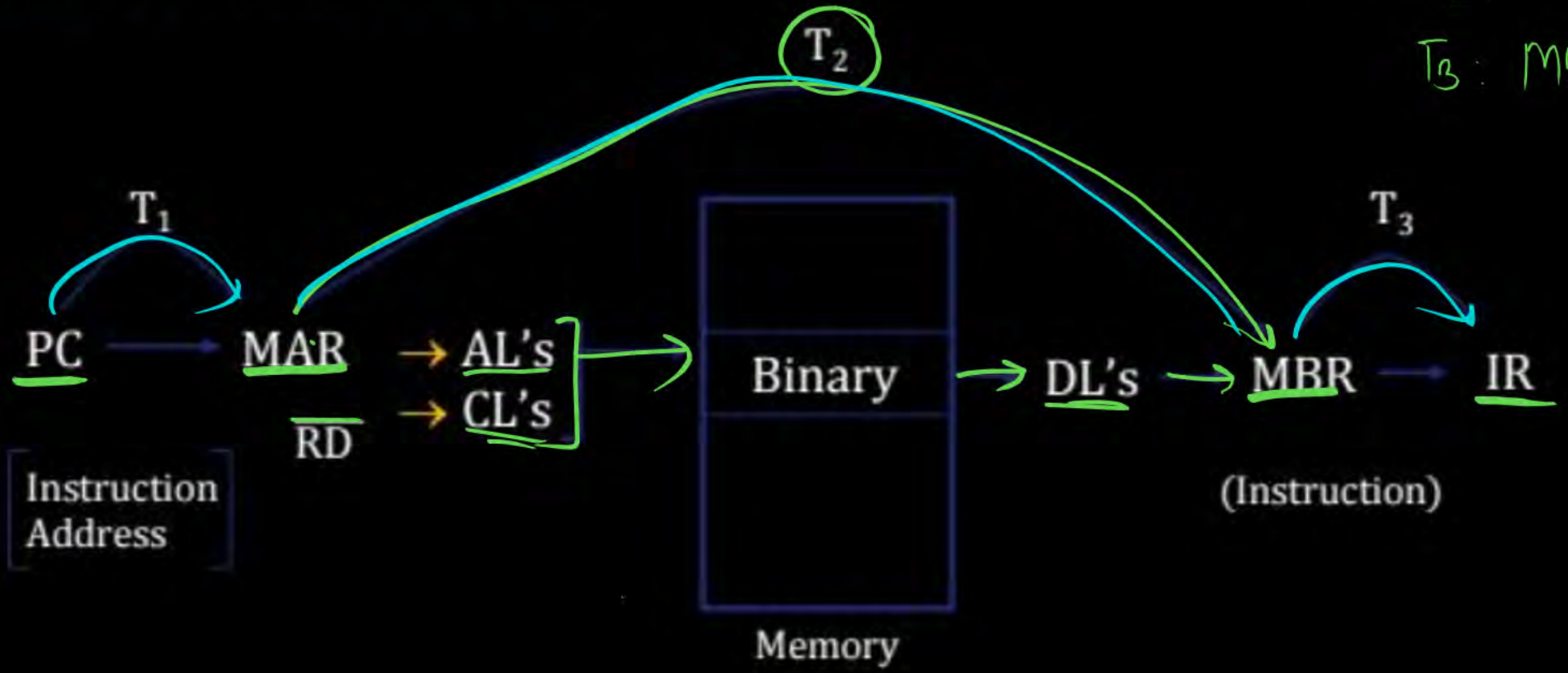
Instruction Cycle

(1) Fetch Cycle: Instruction Fetch.

Hardware Design(H/W Design)

AL: Address Line
DL: Data Line
CL: Control Line

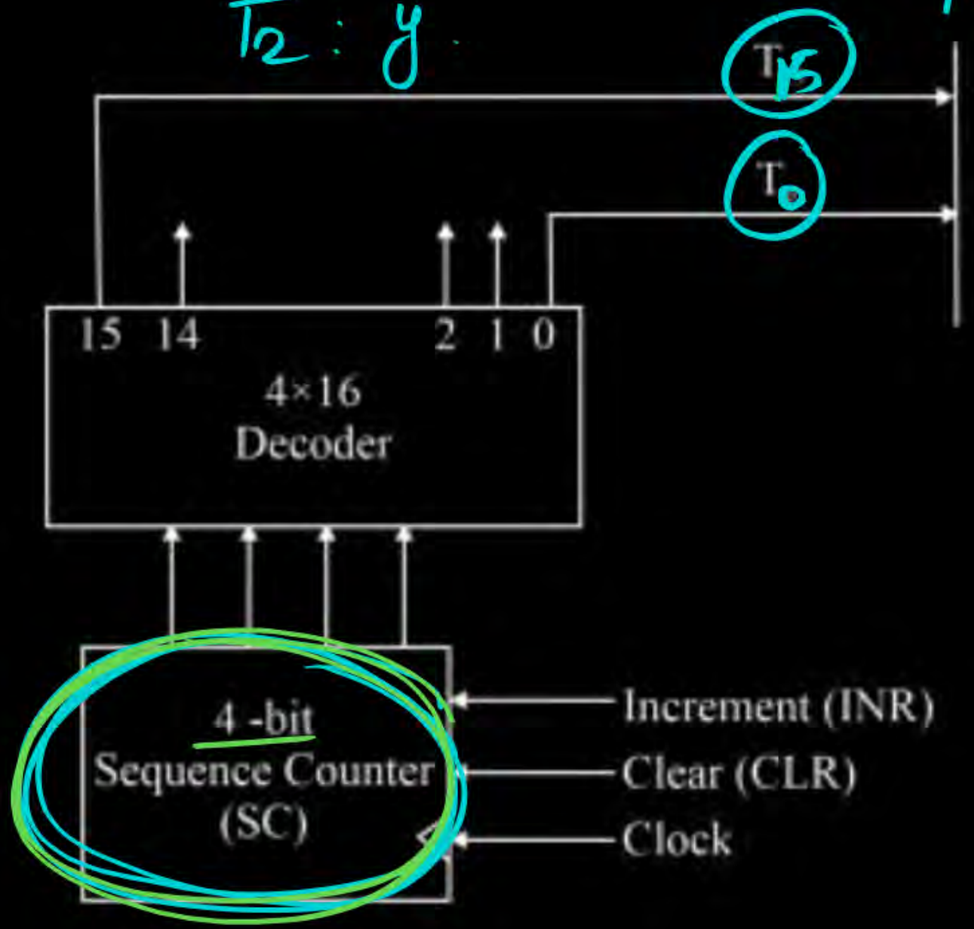
T_1: PC → MAR
T_2: M[MAR] → MBR
T_3: MBR → IR

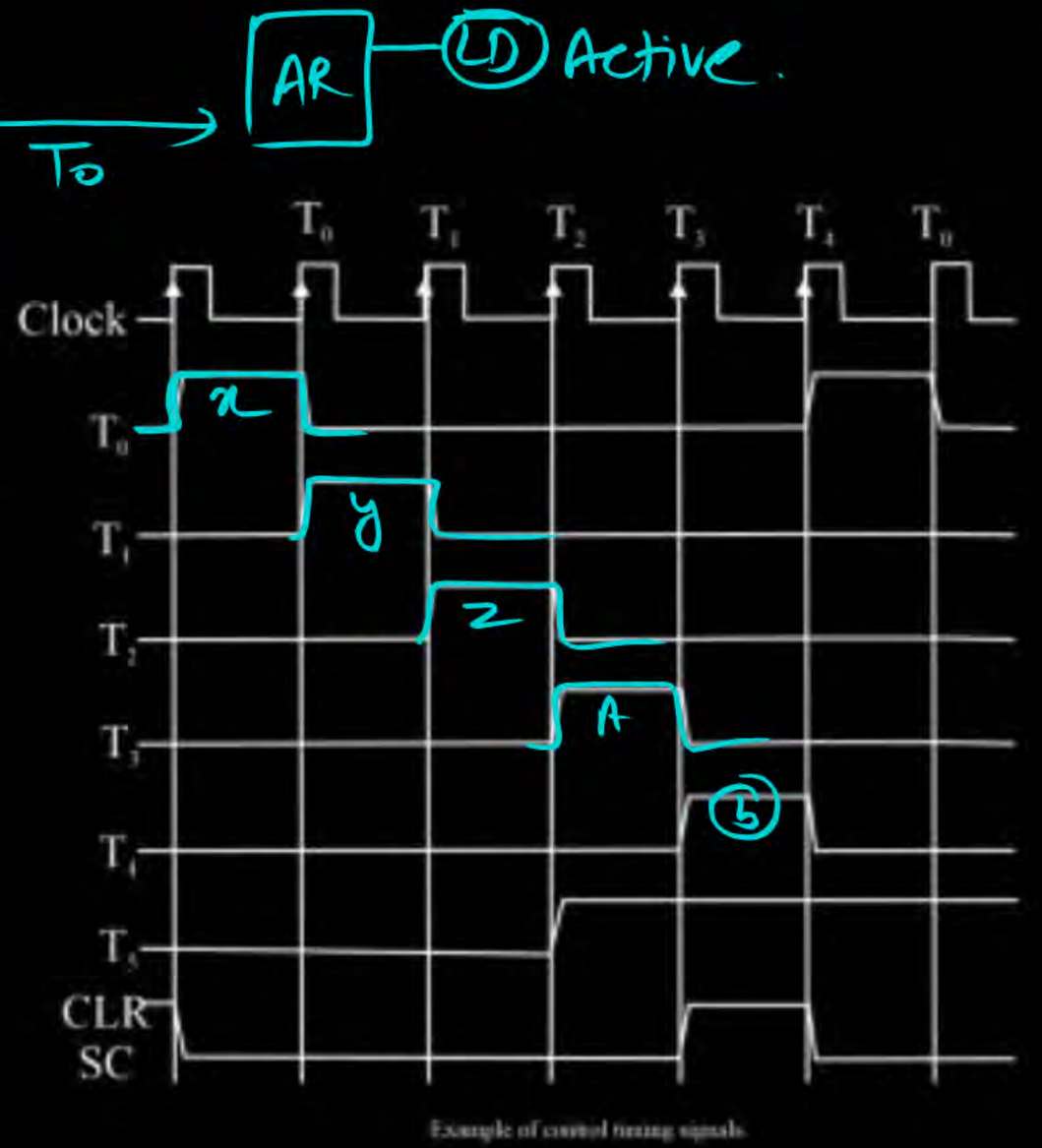


T_0: PC → MAR

T_1: x

T_2: y





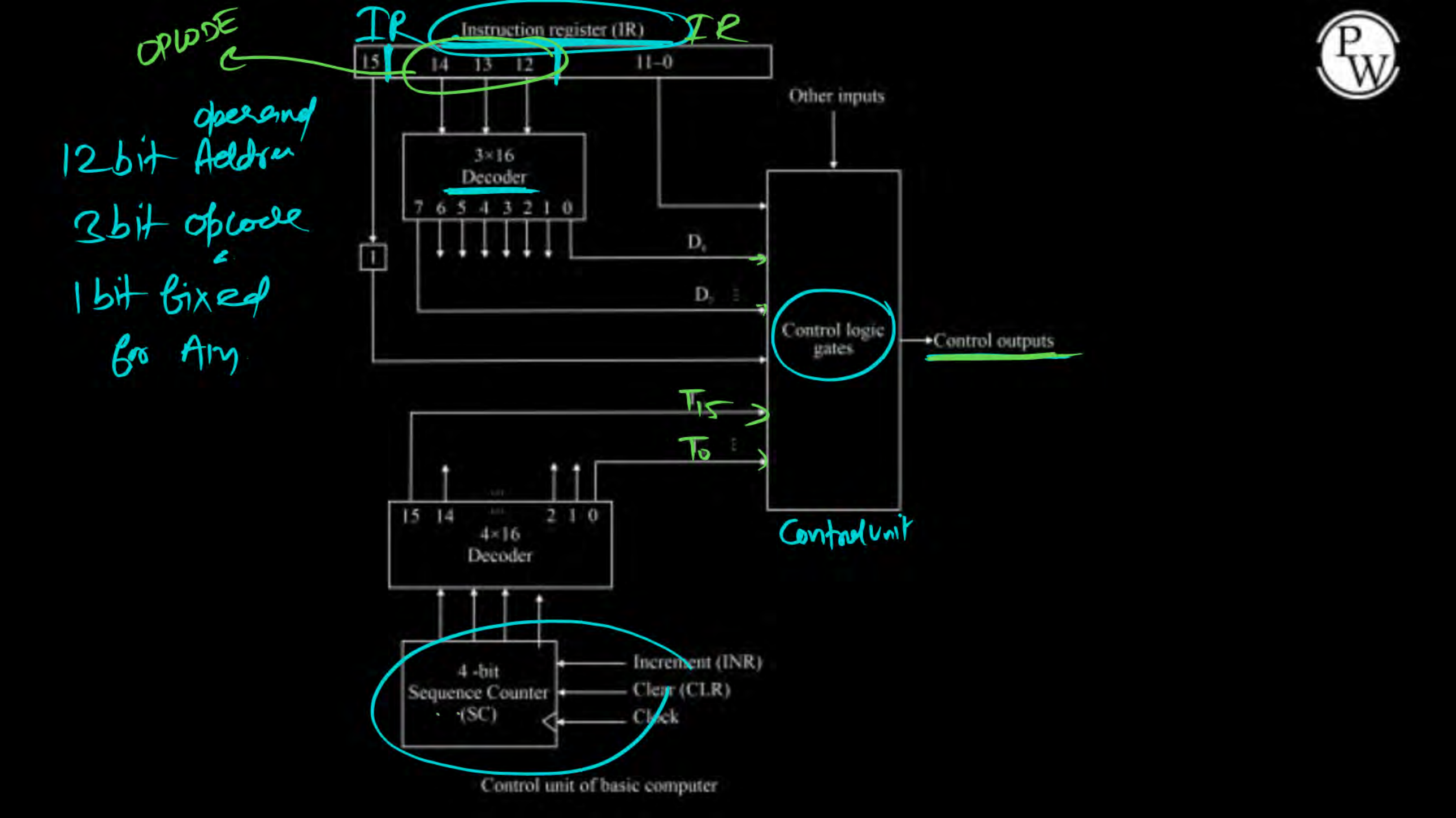
Example of control timing signals

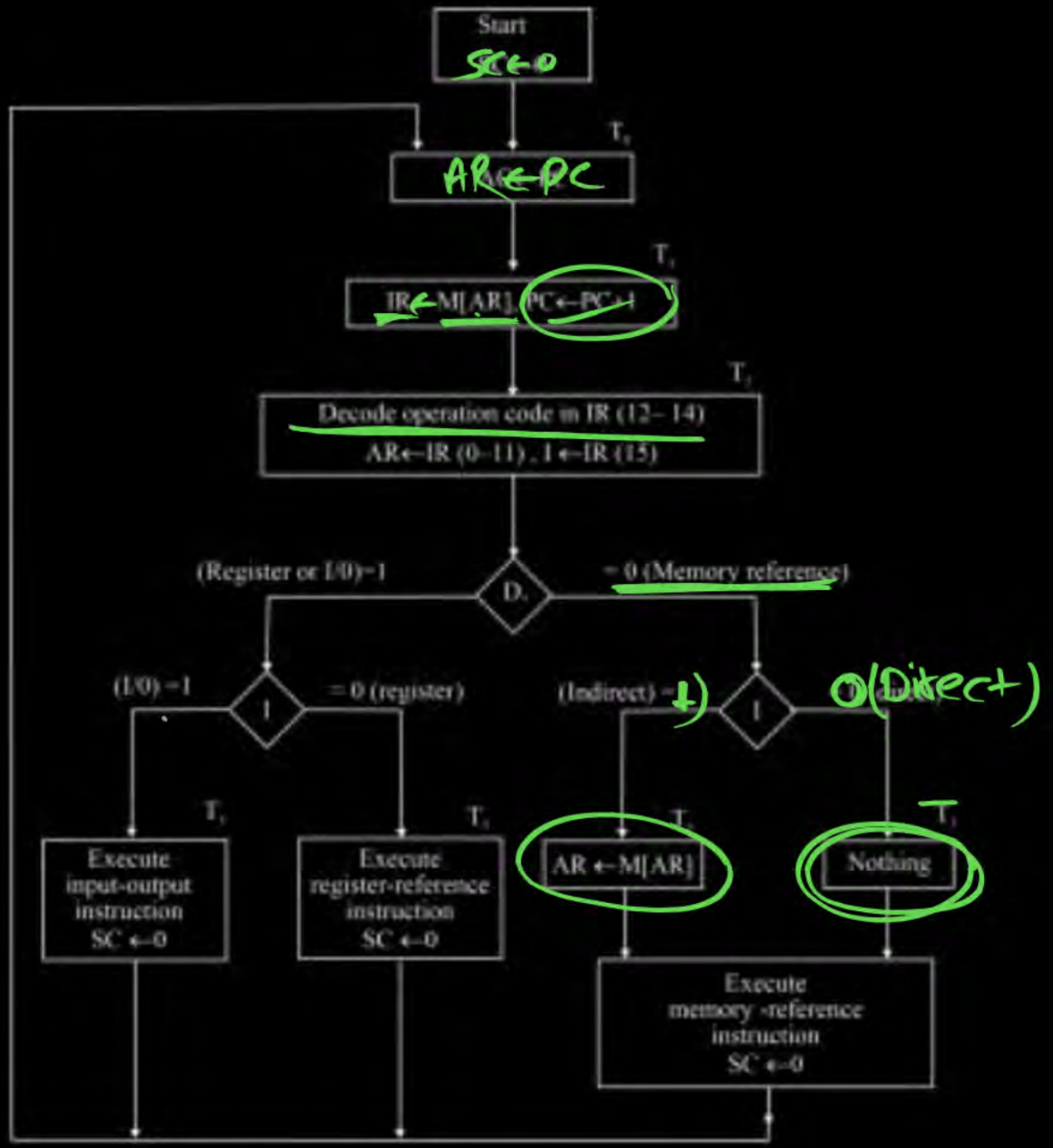
3 bit Sequence Counter

Total 8 Timing Signal (T_0 T_7)

or

(T_1 to T_8)


OPCODE
IR
Instruction register (IR)
IR
15
14
13
12
11–0
operand
12 bit Address
3 bit opcode
1 bit fixed
for Any
Other inputs
3×16
Decoder
7 6 5 4 3 2 1 0
I
D7
D0
Control logic
gates
Control outputs
T15
T0
15 14
2 1 0
4×16
Decoder
Control unit
4 -bit
Sequence Counter
(SC)
Increment (INR)
Clear (CLR)
Clock
Control unit of basic computer



Flow chart for instruction cycle (initial configuration)

THANK YOU!