

COMPUTER SCIENCE

Computer Organization and Architecture

Introduction of COA

Lecture_04



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**TOPICS
TO BE
COVERED**

- o1 Memory Concept**
- o2 System Bus**

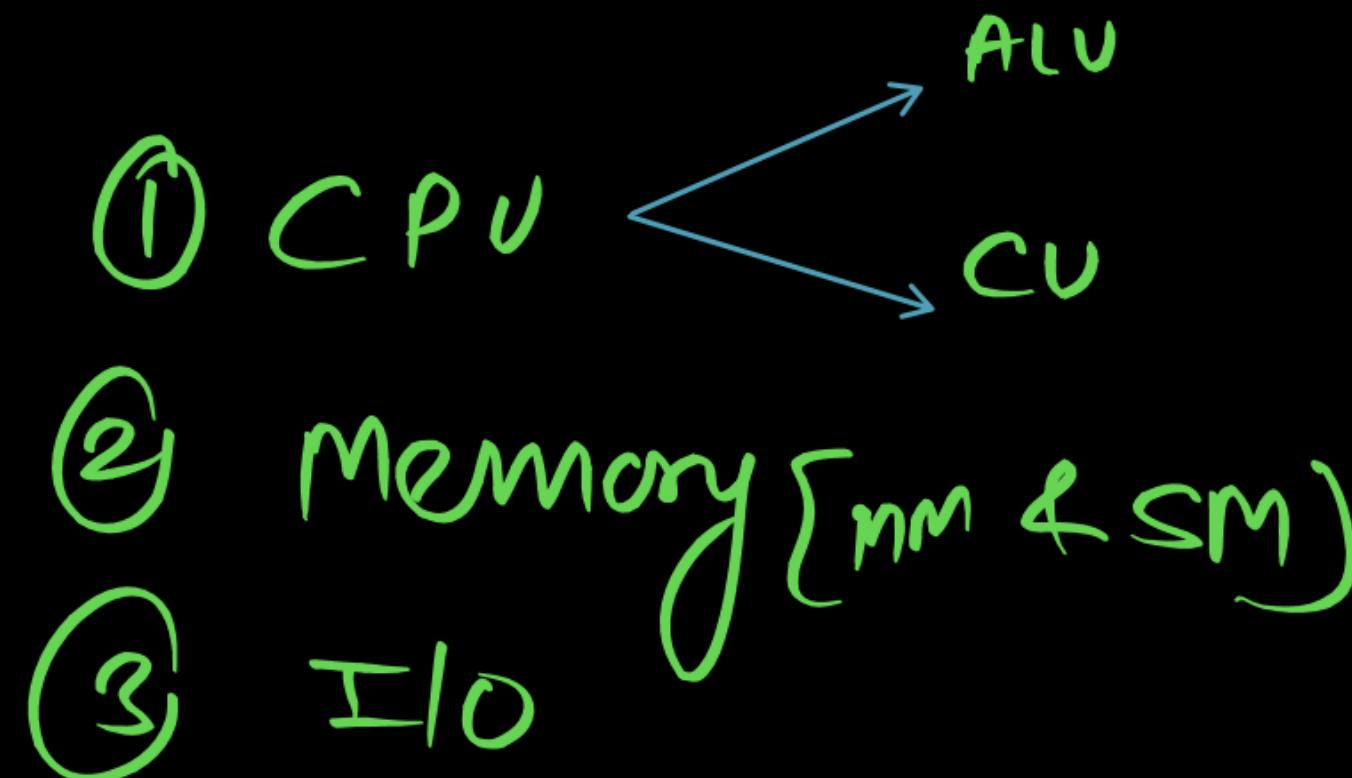
Computer Generation

Computer Arch & Comp. Org.

↓
'How'

- ③ Intel X86 having same Arch. but org. is Different.
- 80186
80286
80386
80486

Component of the Computer



Registers

- ① PC
- ② MAR / AR
- ③ MBR / MDR / DR
- ④ IR
- ⑤ AC
- ⑥ SP
- ⑦ PSW
- GPR

Stored Program Concept

↳ Von Neumann Arch.

Instruction Cycle

① Fetch Cycle

② Execute Cycle

Decode
Execute

- ① Fetch cycle : [Mem to CPU (IR)] & then PC incremented
- ② Execute cycle (To process (to execute) the Fetch Instn)

Instruction Cycle With Interrupt.

System Bus

- ① Address line | Bus
- ② Data line | Bus
- ③ Control line | Bus.

Memory

$$2^n \times m$$

n: # Address line (A.L)

m: # Data line (D.L)

A.L \Rightarrow Capacity of Memory

D.L \Rightarrow Capacity of Data (Word length)

n bit A.L Represent 2^n memory cells.

$$N \times m$$

N: # MM Cells

$$n: \lceil \log_2 N \rceil$$

~~n: 10bit
m: 8bit~~

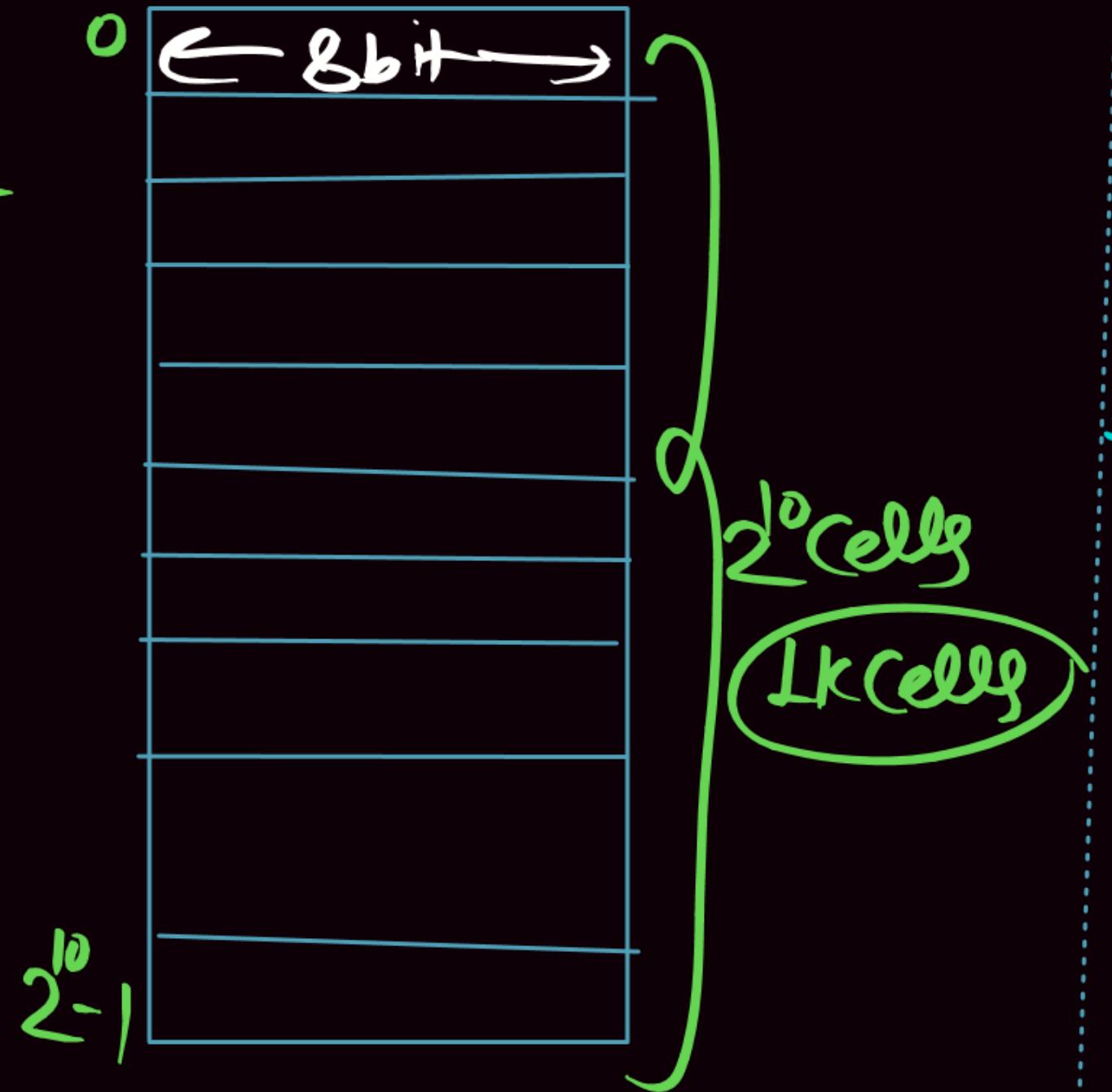
1KB

$2^{10} \times 8\text{bit}$

10 bit Address line

8 bit Data line.

10 bit A.L Can Represent
 2^{10} Memory Cells.



$N \times m$

1KB

1K X 8bit

$1k(2^{10})$ [$m=8\text{bit}$]
1k Memory Cells

#bit Required to
Represent 1k Cells

$$\lceil \log_2 1k \rceil = 10\text{bit}$$

~~n = 10bit~~

$$\lceil \log_2 50 \rceil = 2^n$$

6 bit

$$2^1 = 2$$

$$2^2 = 4$$

$$2^3 = 8$$

$$2^4 = 16$$

$$2^5 = 32 \equiv 5 \text{ bit}$$

$$2^6 = 64$$

$$2^7 = 128$$

$$2^8 = 256$$

$$2^9 = 512$$

① $70 \Rightarrow 7\text{bit}$

② $9 \Rightarrow 4\text{bit}$

$$2^8 = 256 \quad 2^9 = 512$$

③ $101 = 7\text{bit} \quad 7256 \Rightarrow 9\text{bit}$

④ $65 = 7\text{bit}$

⑤ $260 = 9\text{bit}$

⑥ $500 = 9\text{bit}$

1 MB.

$2^{20} \times 8\text{bit}$

2^{20} cells

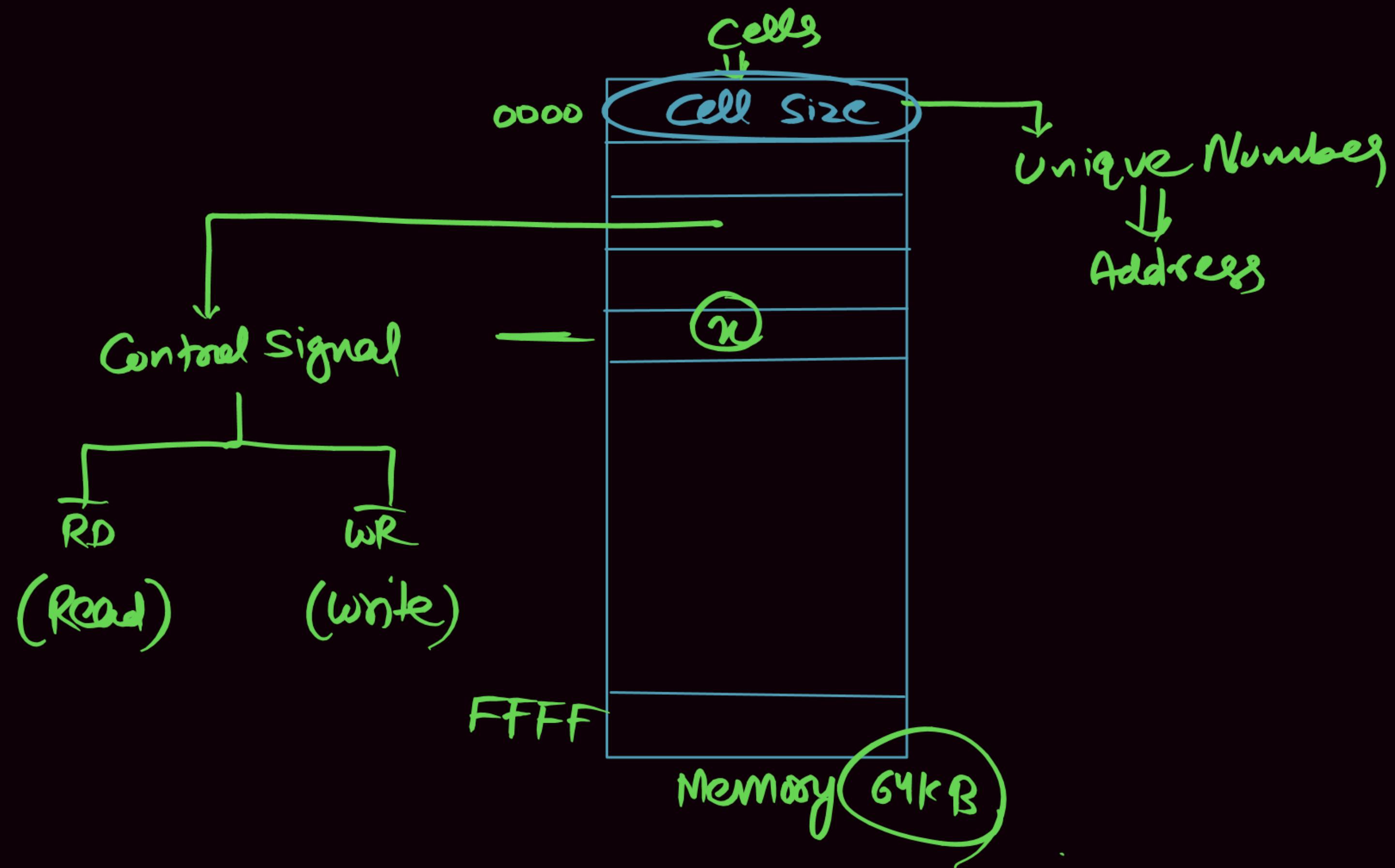
20 bit Address line.

8 bit Data line

$\underbrace{1\text{M}}_{1\text{M}} \times 8\text{bit}$

1M cells

Each cell is 8bit.



① 8 Byte

② 16 Byte

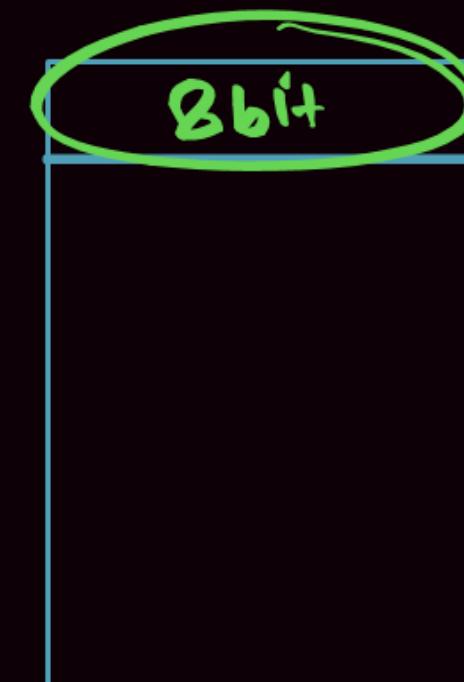
③ 64 Byte

④ 1 KB

⑤ 1 MB

⑥ 2 GB

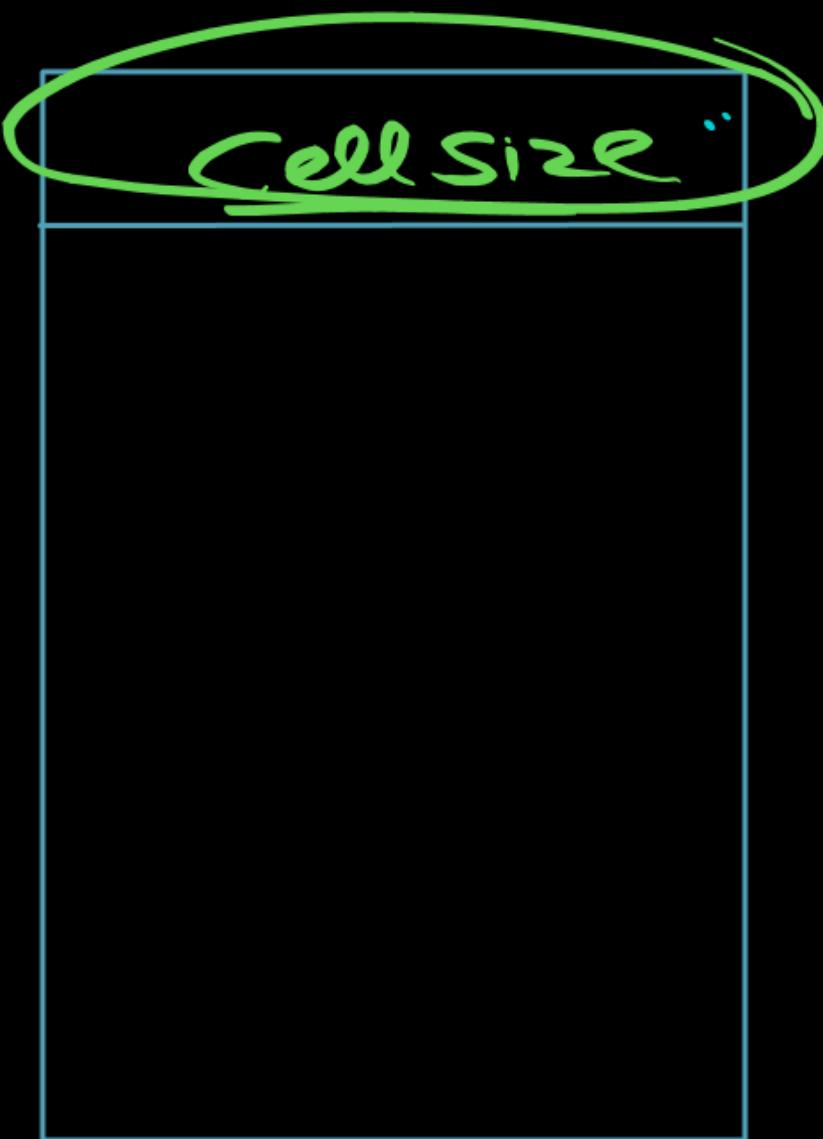
1 Byte (B) = 8 bit



P
W

Based on the cell size Memory Configuration
is Divided into 2 Type.

- ① Byte Addressable Memory
- ② Word Addressable Memory.

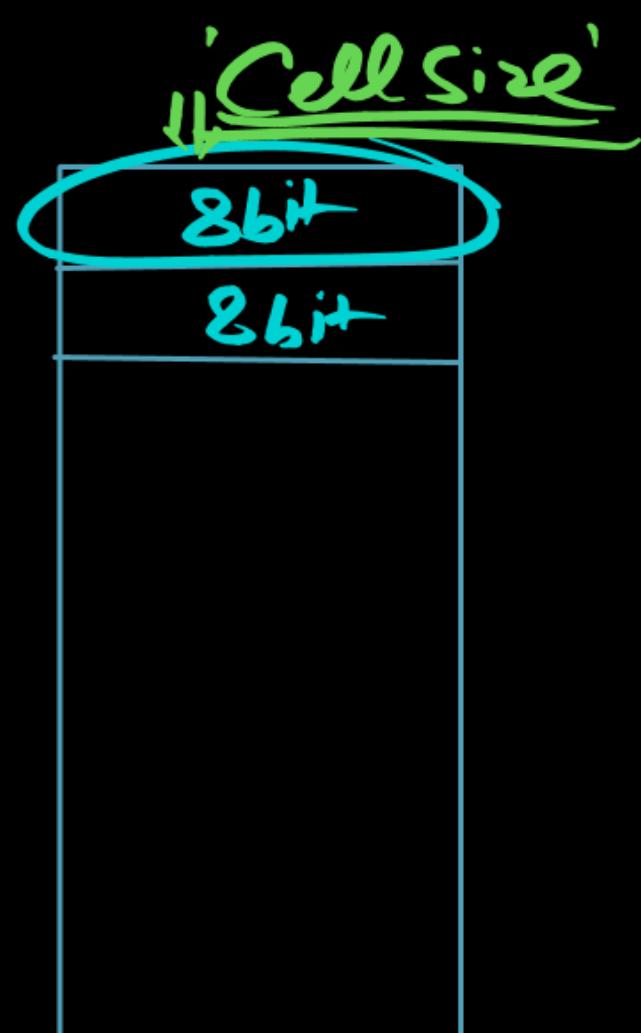


① Byte Addressable Memory : When the Cell Size is '8bit' then Corresponding Address is Byte Addressable.

- ③ $(2^2) 4 \times \underline{8}$:
- $(2^4) 16 \times \underline{8}$:
- $(2^6) 64 \times \underline{8}$:
- $(2^8) 256 \times \underline{8}$:
- $(2^{10}) 1K \times \underline{8}$:
- $2^{20} 1M \times \underline{8}$:
- $2^{30} 1G \times \underline{8}$:
- $2^n \underline{2^n \times 8}$;

- 2bit Address
- 4bit Address
- 6bit ..
- 8 bit ..
- 10bit ..
- 20bit ..
- 30bit ..
- n bit Address ← Byte Address.

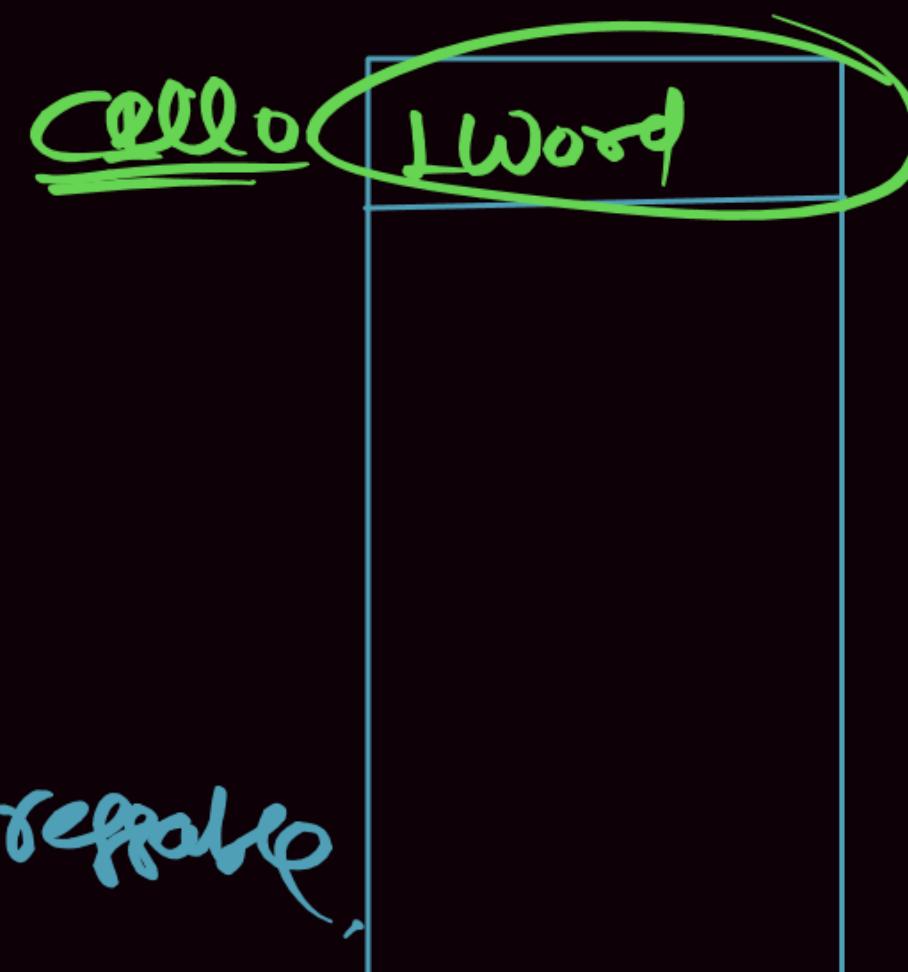
Cell size is 8 bits
So its.



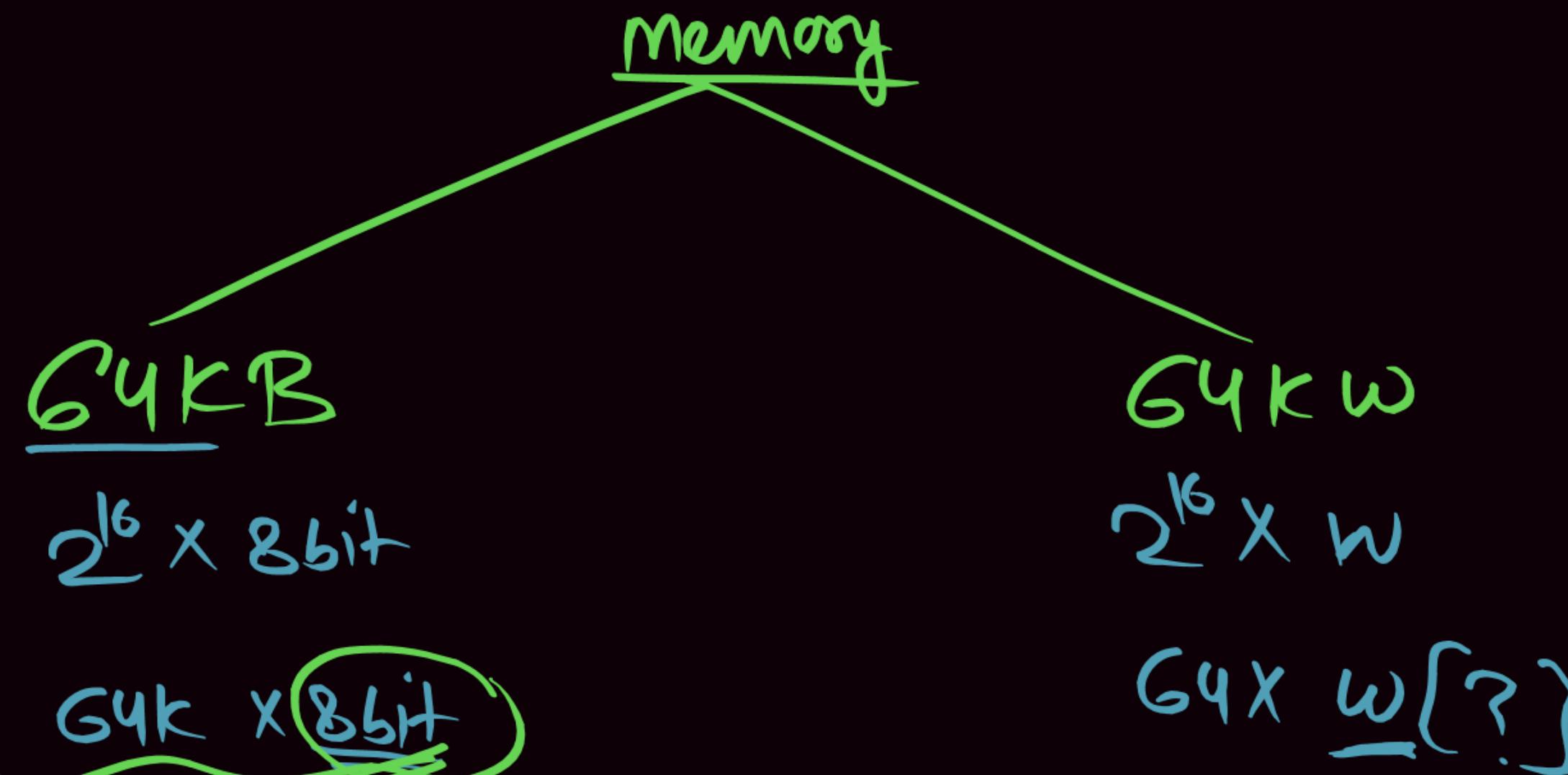
② Word Addressable Memory: When the Cell Size is given in the form of words (Depends on word length) then Corresponding Address is called Word Addressable.

- ③
- | | |
|----------------------------|---------------|
| $4 \times \underline{w}$ | 2bit Address |
| $16 \times \underline{w}$ | 4bit " |
| $64 \times \underline{w}$ | 6bit " |
| $256 \times \underline{w}$ | 8bit " |
| $1K \times \underline{w}$ | 10bit " |
| $1M \times \underline{w}$ | 20bit " |
| $1G \times \underline{w}$ | 30bit " |
| $2^n \times \underline{w}$ | n bit Address |
- ~~Cell size Must be in Word.~~

Word Addressable



(Microprocessor) μP	Byte (B)	Word <small>(Word size = word length)</small>
① 8 bit Processor	8bit	8bit
② 16 bit Processor	8bit	16bit
③ 32 bit Processor	8bit	32bit
④ 64 bit Processor	8bit	64bit
⑤ n bit Processor	<u>8bit</u> <u>unique Meaning</u> <u>No Ambiguity</u>	<u>nbit</u> <u>multiple meanings</u> <u>Ambiguity</u>



Defact : Byt in
Memory

:

Note

(Data type in memory is Byte)

Default memory configuration is Byte Addressable. So

In the Memory Data is stored 'Byte wise'.

Note

Default Data type in the CPU is 'Word'. So

the operation are performed on a CPU according to

Word format

Note

To synchronize Memory Data type with CPU Data type Memory Interfacing will be adjusted by the Designer according to a word length of the CPU, to access the Data from Memory to CPU in the form of words.

16 bit Processor

In CPU, operation

Performed on 16bit Data.

Little Endian
Big Endian

2 Byte [2 cells [each 8 bit cells]].
from MM to CPU

~~Note~~

Default memory Configuration is Byte Addressable.

In Memory Chip Data is Stored in Byte Wise.

(Microprocessor)
2¹⁶

8 bit Processor

16 bit Processor

32 bit Processor

64 bit Processor

n bit Processor

Byte (B)

8 bit

8 bit

8 bit

8 bit

8 bit

unique Meaning

No Ambiguity

word
1 word
size = word
length

8 bit

16 bit

32 bit

64 bit

n bit

Multifee meaning

Ambiguity

Cells
Interfacing

1 cells

2 cells

4 cells

8 cells

8bit = 1 Byte
16bit = 2 Byte [2 cells]

(e) 8086 Processor

16 bit Processor.

MOV Ax [1000]

Ax $\leftarrow \begin{bmatrix} m[1000] \\ m[1001] \end{bmatrix}$. 2 cells:

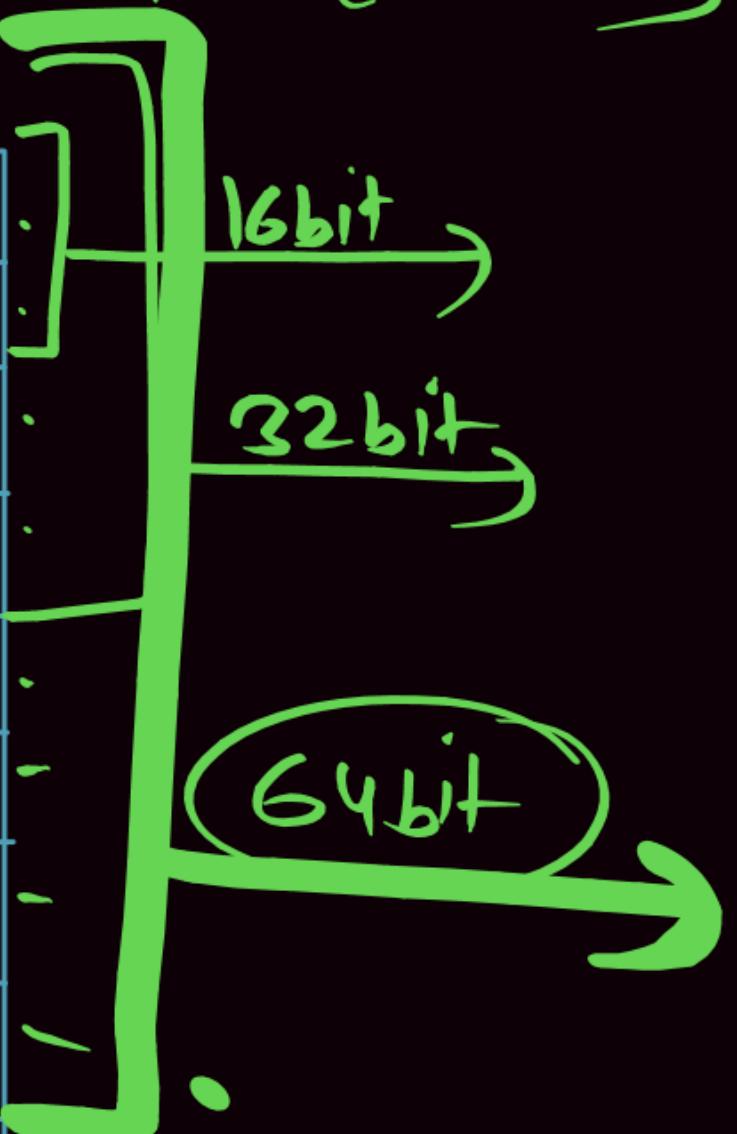
(f) 32 bit Processor

MOV δ_1 [1000]

$\delta_1 \leftarrow \begin{bmatrix} m[1000] \\ m[1001] \\ m[1002] \\ m[1003] \end{bmatrix}$

1000 Cell 0
1001 Cells
1002 Cells 2
1003 Cells 3

8bit	.



16 bit Processor

Word length = 16 bit

Q.

The Capacity of a memory unit is defined by the Number of word

P
W

Multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of $64K \times 16$?

- (a) 8 address, 8 data line
- (b) 16 address, 8 Data line
- (c) 15 address, 16 Data line
- (d) 16 address, 16 Data line

$$\underline{64K} \times \underline{16}$$

$$2^{\underline{16}} \times 16$$

Q.

Consider a system which has 1024 k words. Each word has the size of 32 bits then what is the capacity of memory in MB (Mega Byte) _____

P
W

1024 k word

1024 k \times 4Byte (32bit)

$2^{20} \times 4B$

4MB Ans

Q.

The Capacity of a memory unit is defined by the Number of word

Multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of $4K \times 16$?

- (a) 10 address, 16 data line
- (b) 11 address, 8 Data line
- (c) 12 address, 16 Data line
- (d) 12 address, 12 Data line

[GATE-2 Marks]

$4K \times 16$

$2^{12} \times 16$

Q.

A processor can support a maximum memory of 4GB, where the memory is word-addressable (a word consists of two bytes).

The size of the address bus of the processor is at least 31 bits. Ans

4G Byte

[GATE-2016]

Memory is word Addressable.

$$1\text{ Word} = 2\text{ Byte}$$

$$\text{OR } 2\text{ Byte} = 1\text{ Word}$$

2G Word
31 Word
2

31bit
RS

4G Byte

2G X 2Byte

2G Word

OR

4G Byte
2Byte Words

2G Words

2G Words
L³⁰
2² W
2³¹ W
31bit

Q.

Consider a 32 bit Hypothetical processor which support 128 MByte memory. System is enhanced (New Design) with a word addressable memory. Then how many address lines are required in the new system?

P
W

Soln 25 bit Ans

128 MByte

$2^7 \cdot 2^{20}$ Byte

2^{27} BYtE

(ii) How many bits are saved in the New Design?

Soln

$27 - 25 = 2$ bit saved

New Design (Word Addressable)

1 Word = 32 bit
= 4 Byte

OR 4B = 1W

128 MByte

$32 \text{ M} \times 4 \text{ Byte}$

32 M Words

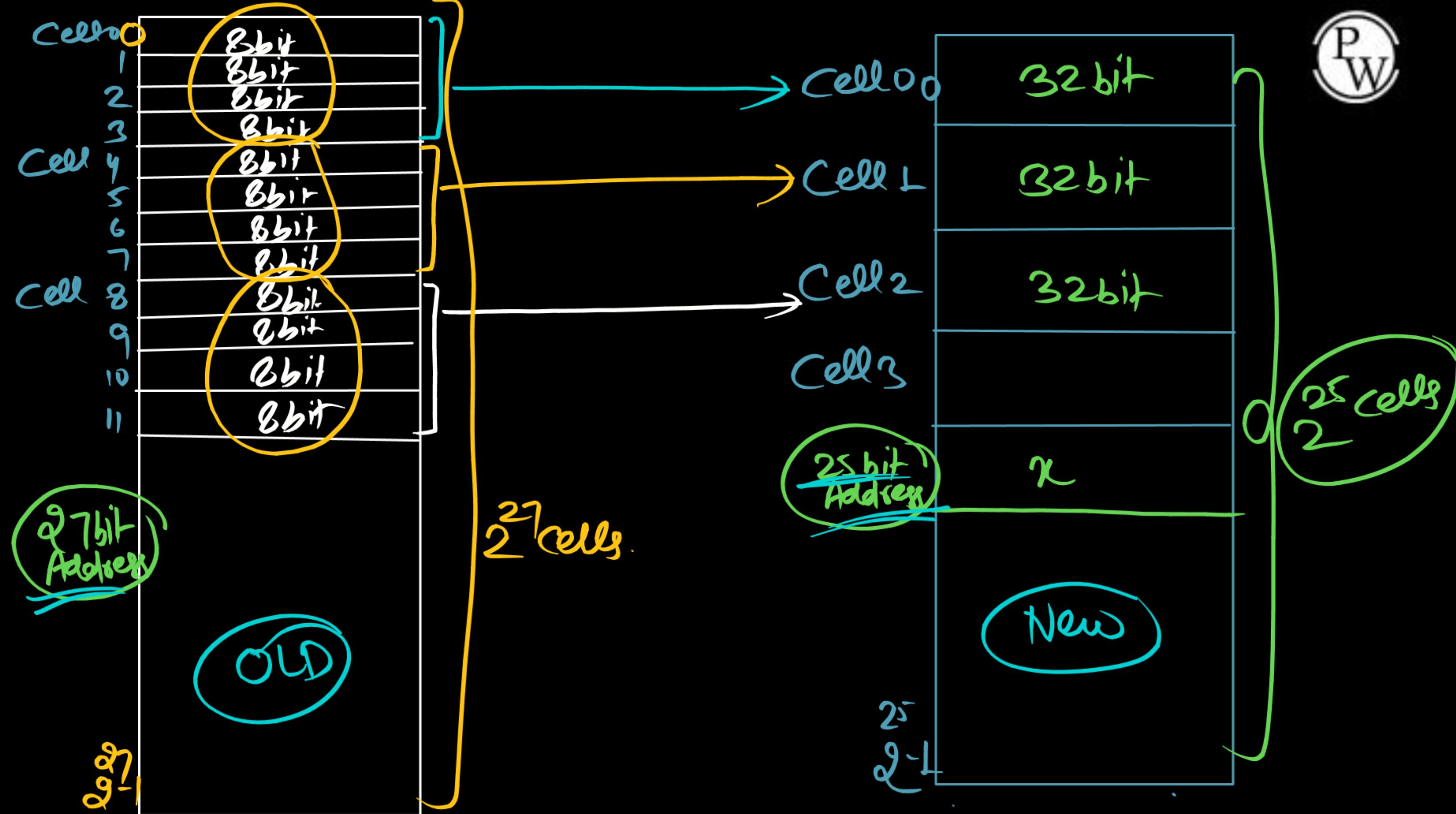
32 M Words

2^{25} Word

Add 608 = 25 bit

$\frac{128 \text{ MB}}{4 \text{ B}}$ Word

32 M Words



2^{27} Byte
 $2^{25} \times 4\text{Byte}$
 $\rightarrow 2^{25}$ Word

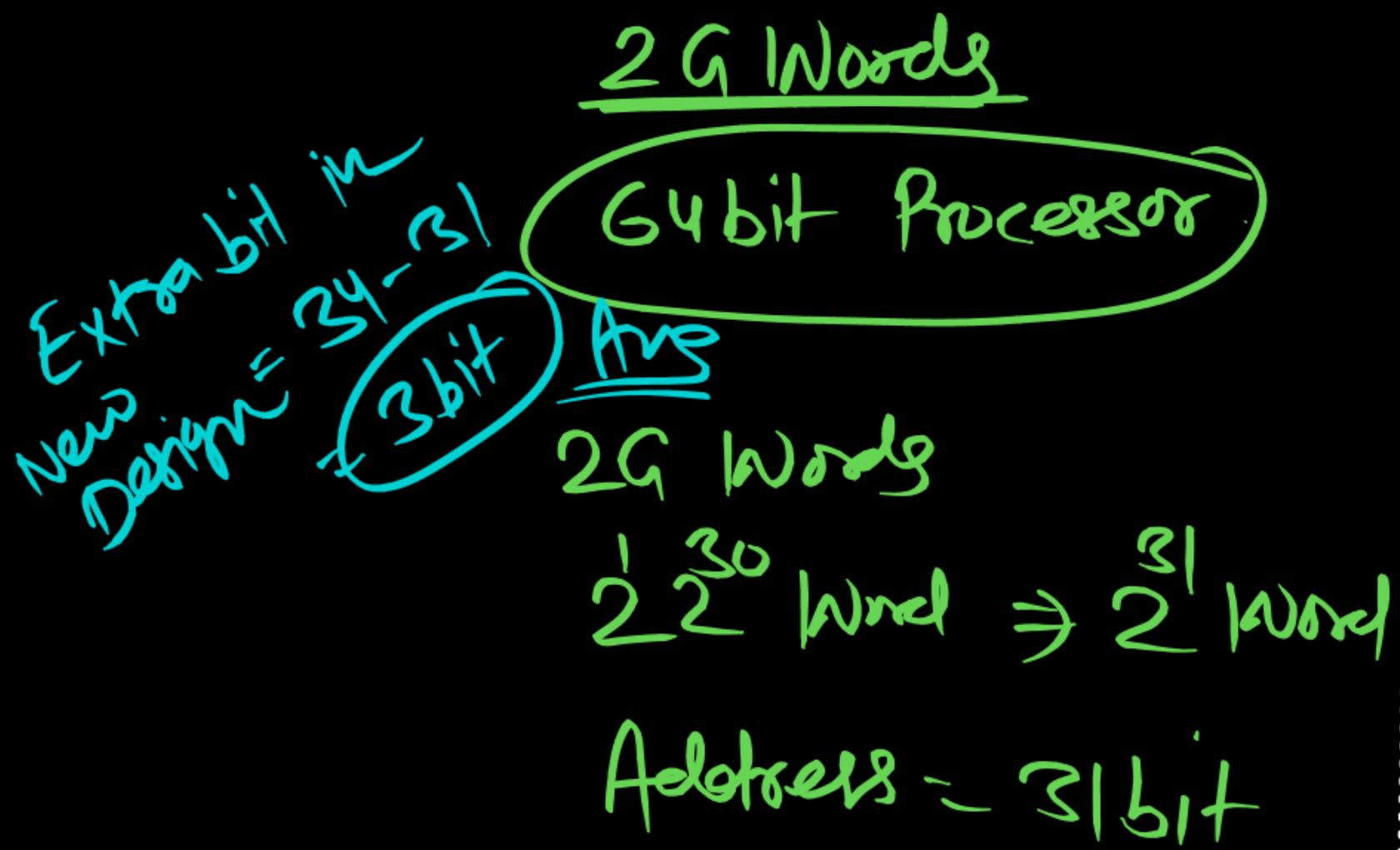
2^{25} Words.
 $2^{25} \times 4\text{Byte}$
 $2^{25} \times 2^2$ Byte
 2^{27} Byte

32bit
1Word = 4Byte

Q.

Consider a 64 bit Hypothetical processor which support 2G words memory. System is enhanced (New Design) with a Byte addressable memory. Then how many Extra address lines are required in the new system?

P
W



New Design (Byte Addressable)

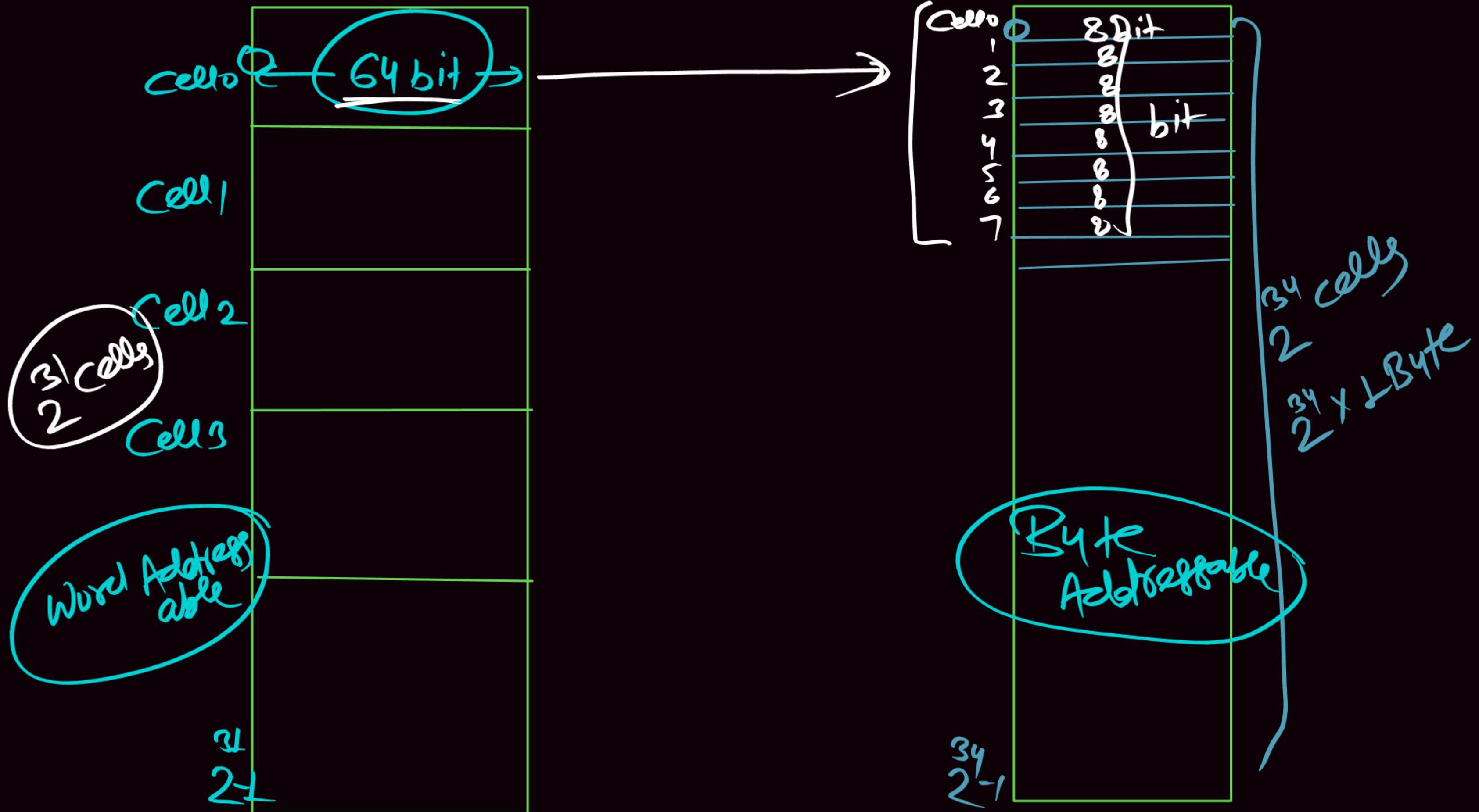
$$\begin{aligned}1 \text{ Word} &= 64 \text{ bit} \\&= 8 \text{ Byte}\end{aligned}$$

1 Word = 8 Byte

$$2^9 \text{ Words} \Rightarrow 2^9 \times 8 \text{ Byte}$$

16 G Byte
34 Byte
2³⁴ Byte

Address = 34 bit



word

(1 cell = 64 bit
8 Byte)

2^{31} cells

$2^{31} \times 8 \text{ Byte}$

$2^{31} \times 2^3 \text{ Byte}$

2^{34} Byte

Byte

2^{34} Byte

$2^{31} \times 8 \text{ Byte}$

2^{31} words

($1 \text{ Word} = 64 \text{ bit}$
or
 $8 \text{ Byte} = 1 \text{ Word}$)

Pins: Processor Contains Set of Hardware Pin to perform the operation.

Type of Pins

- ① Active Low Pin
- ② Active High Pin
-  Time Multiplex Pin.

① Active Low Pin : This pin is Enable when Input is '0', Clock Pulse is in low state.

Denoted as

Pin name

③ $\overline{\text{RD}}$, $\overline{\text{WR}}$

② Active High Pin : This pin is Enable when Input is '1'

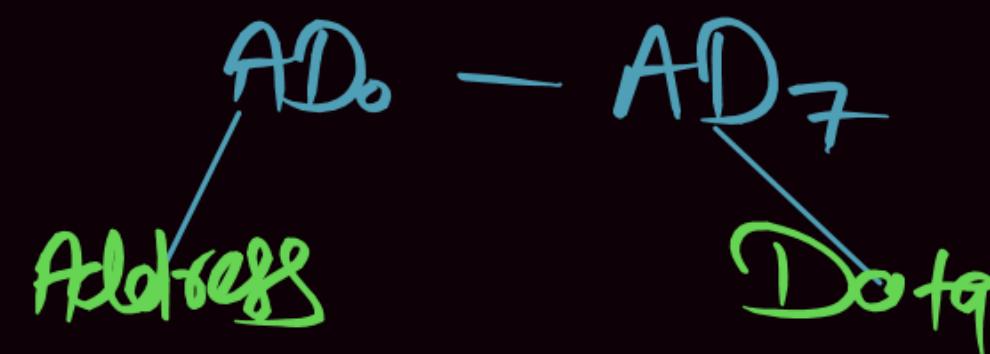
③ INTR

HLDA

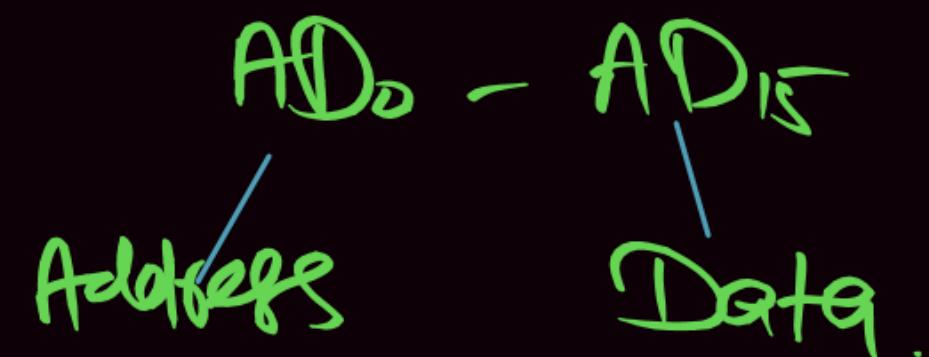
ALE

③ Time multiplexed Pin : This Pin Carries the Multiple meaning but One Only at a time.
Address Pin are time multiplexed with Data Pins to carry the Address & Data.

④ In 8085 Processor

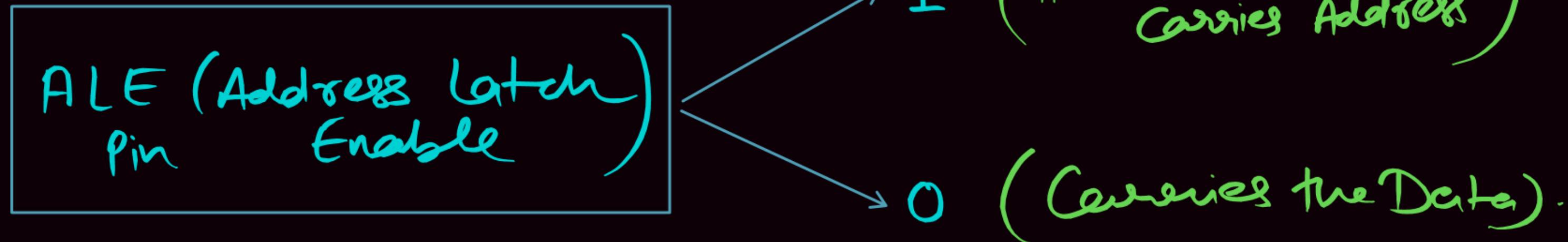


In 8086 Processor:



In 8085 : AD₀ - AD₇ Time Multiplexed Pin Contain Address & Data.

But Only One at a time.



Advantage of the time Multiplexed Pin is Number of Hardware Pins Will be Reduced.

System Bus

- ① Address Line
- ② Data Line
- ③ Control Line.

System Bus

Address Line : ① to carry the address towards Memory & I/O
② Unidirectional

Based On Address Line we can Determine the Capacity of the Memory.

③ In 8085 Processor

AD₀ - AD₇ & AB - A₁₅

16 bit address

2^{16} cells.

64K cells

64K Byte

③ In 8086

AD₀ - AD₁₅ & A₁₆ - A₁₉

20 bit Address

2^{20} cells

1M cells

1M Byte

System Bus

Data Line

- ① Carry the Data (Binary Sequence)
- ② Bidirectional

(Note) Based on the Data Line we can Determine Word length of the CPU.

(Note) Performance of CPU Determined by the Word Length of the Processor.

(ex) In 8085

AD₀ - AD₇

Word length = 8 bit

↓
Operation performed on 8 bit
Data format

(ex) In 8086

AD₀ - AD₁₅

Word length = 16 bit

Operation Performed on
16 bit Data format.

System Bus

Control Line

→ Carries the Control Signal
→ Unidirectional (individually)

Any Doubt ?

**THANK
YOU!**

