COMPUTER SCIENCE

Computer Organization and Architecture

Introduction of COA

Lecture_02

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01 Instruction Cycle

02 System Bus

Computer Generation

CO & CA

Component of the Computer.

1. CPU
2. Memory
3. I/O

Registers

- PC
- MAR | AR
- MBR | MDR | DR
- IR
- AC
- PSW
- SP
- GPR

Instruction Cycle

1. Fetch Cycle [mem to CPU (IR)]
2. Execute cycle
   - Decode
   - Execute.

Computer Works on Stored Program Concept.

⇓

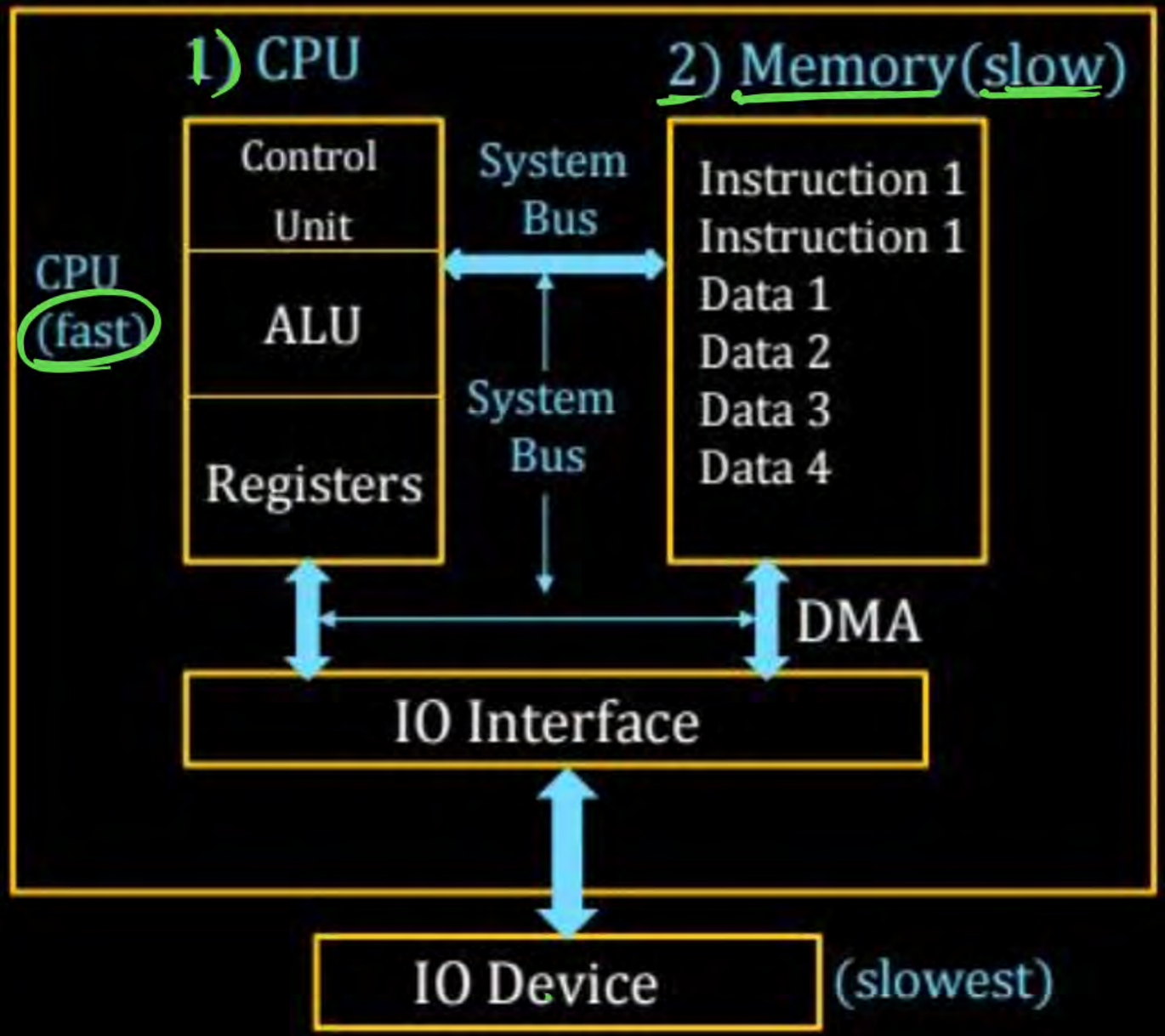
Von Neumann Architecture.

Component of Computer

(1) CPU

(2) Memory

(3) Input/output



Instruction Cycle

Instruction Cycle

The process required to execute the Instruction.

(or)

Instruction cycle describe the execution sequence of the instruction.

Instruction Cycle contain 2 sub cycle.

1) Fetch cycle
2) Execute cycle
   - Decode
   - Execute

Instruction Cycle

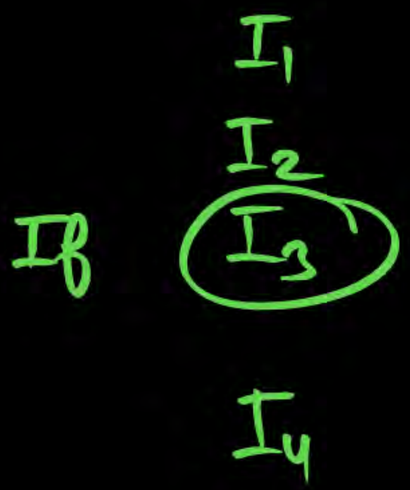
Fetch Cycle

The Objective of Fetch cycle is to Fetch the Instruction From Memory to CPU. [MEM to CPU(IR)]

V.V.Imp Note

At the End of Fetch Cycle Program Counter [PC] is update then PC Denotes the Next Instruction Stating Address.

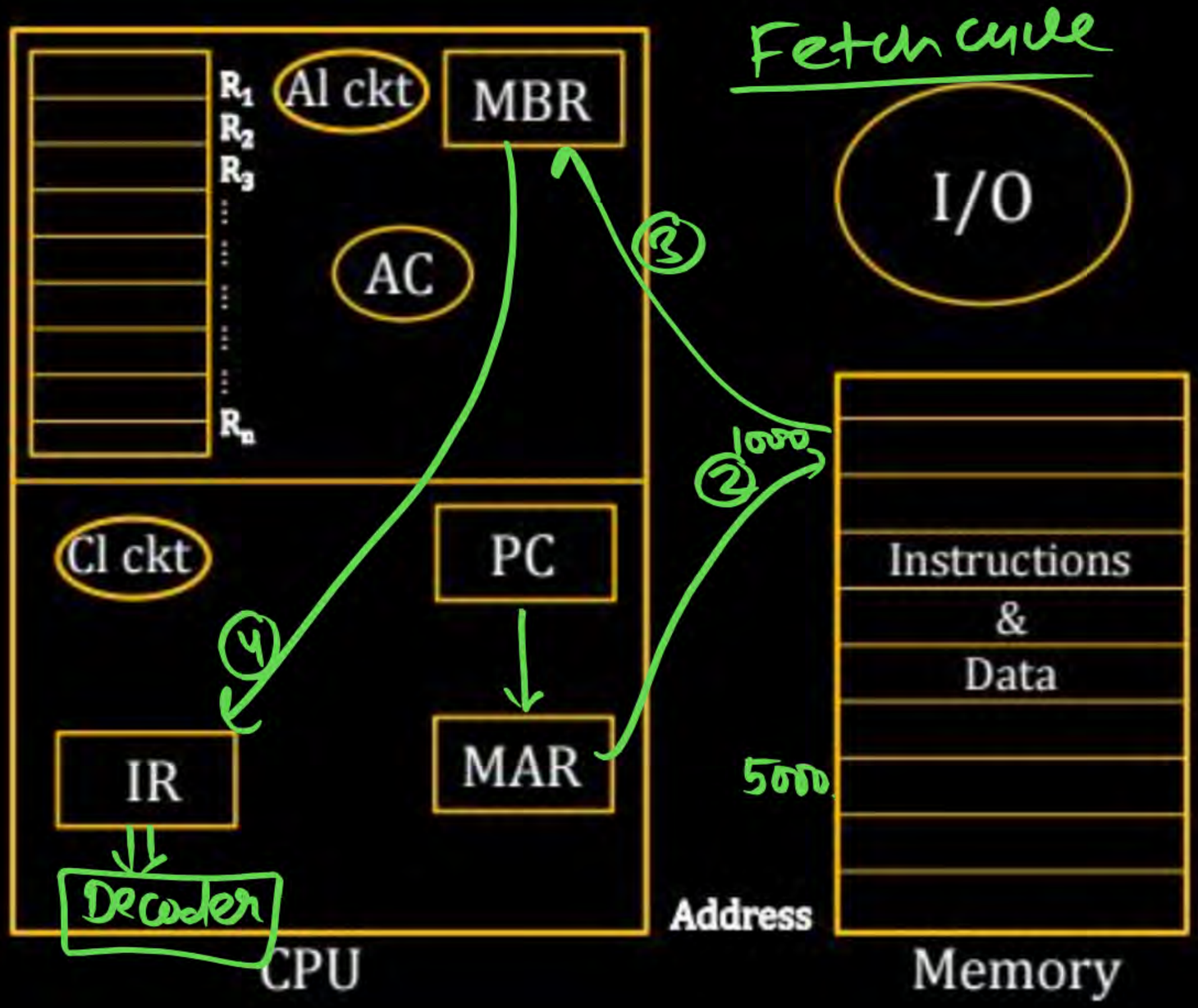
Instruction Cycle



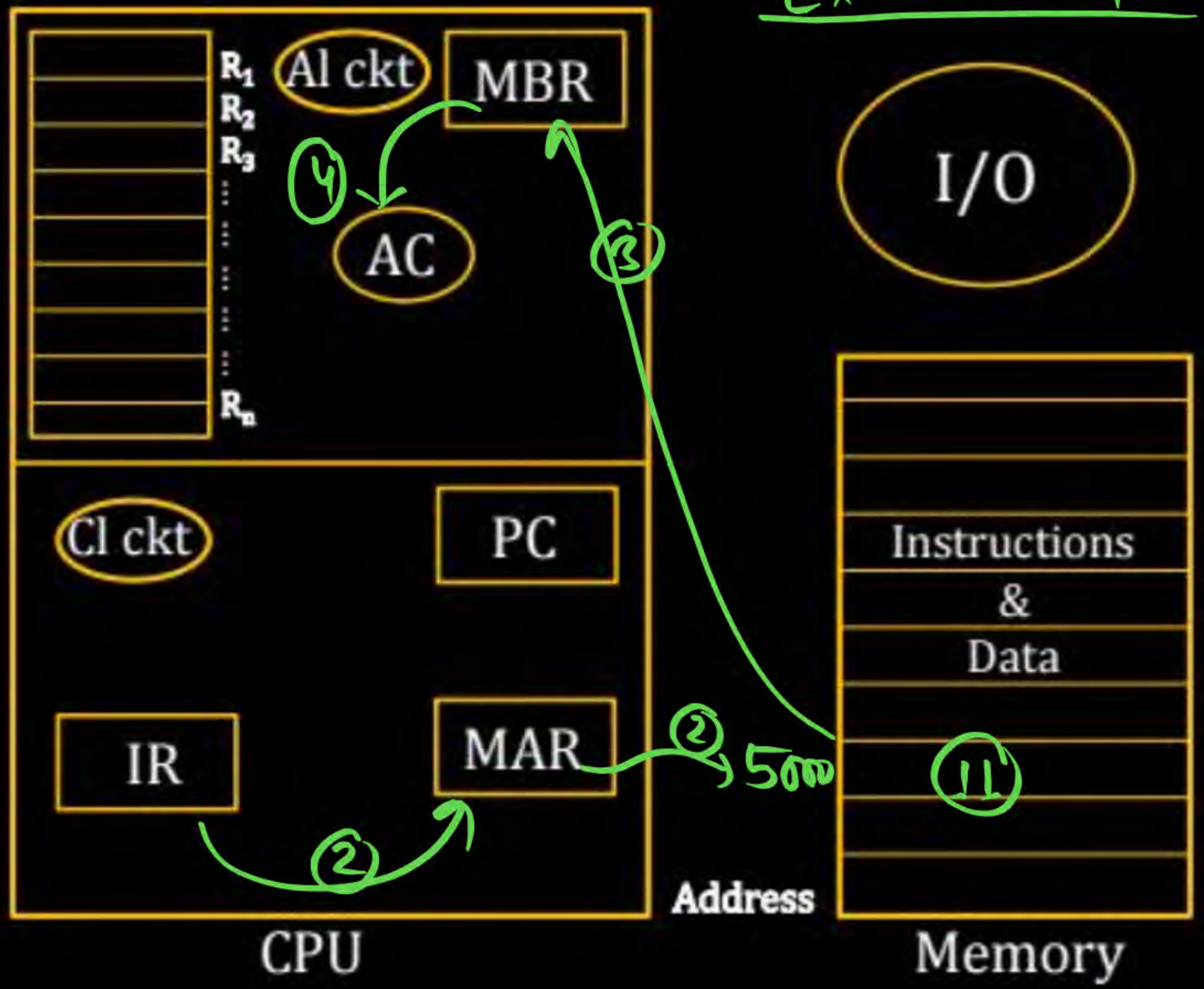
If I_3 Only Fetched then PC Denoted the Starting address of Next Instruction (I_4).

Execute Cycle

To Process (to execute) the Fetched Instruction.


Fetch cycle
R1
R2
R3
Rn
Al ckt
MBR
AC
I/O
Cl ckt
PC
IR
MAR
Decoder
Instructions
&
Data
5000
Address
CPU
Memory
1000 I1 LOAD [5000]
AC ← M(5000)

Execute cycle



1000 (I1) LOAD M[5000]

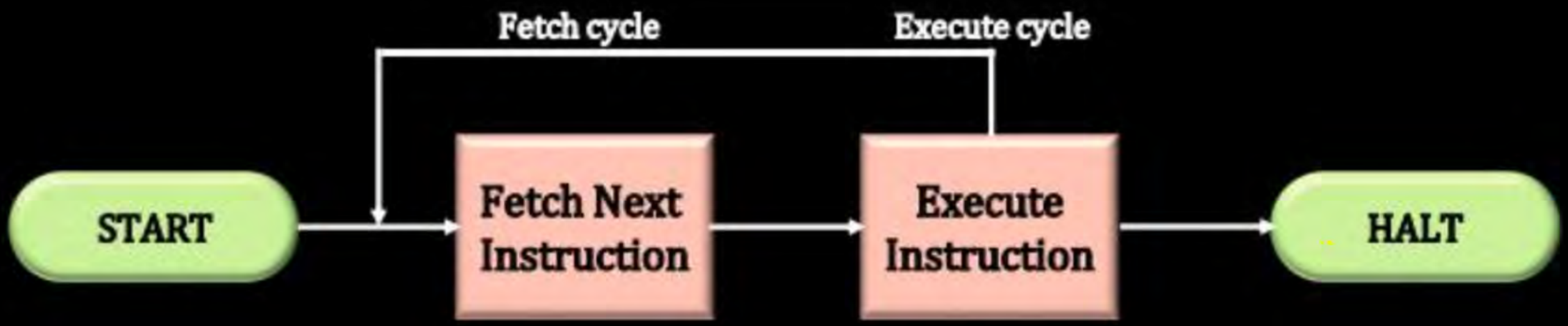
AC ← M[5000]

Steps in Instruction Cycle

- Fetch cycle
  - 1) IAC (Instruction Address Calculation)
  - 2) IF (Instruction Fetch)
- Execute cycle
  - Decode
    - 3) Decoding (Analysis of Instruction
      (What opcode, how many operand,
      where operands are available))
    - 4) OAC (Operand Address Calculation)
    - 5) OF(Operand Fetch) (DATA)
  - Execute
    - 6) DP (Data Processing)
    - 7) Result Storage

Fetch Cycle

- At the beginning of each instruction cycle the processor fetches an instruction form memory
- The program counter (PC) holds the address of the instruction to be fetched next
- The processor increments the PC after each instruction fetch so that it will fetch the next instruction in sequence
- The fetched instruction is loaded into the instruction register (IR)
- The processor interprets the instruction and performs the required action.

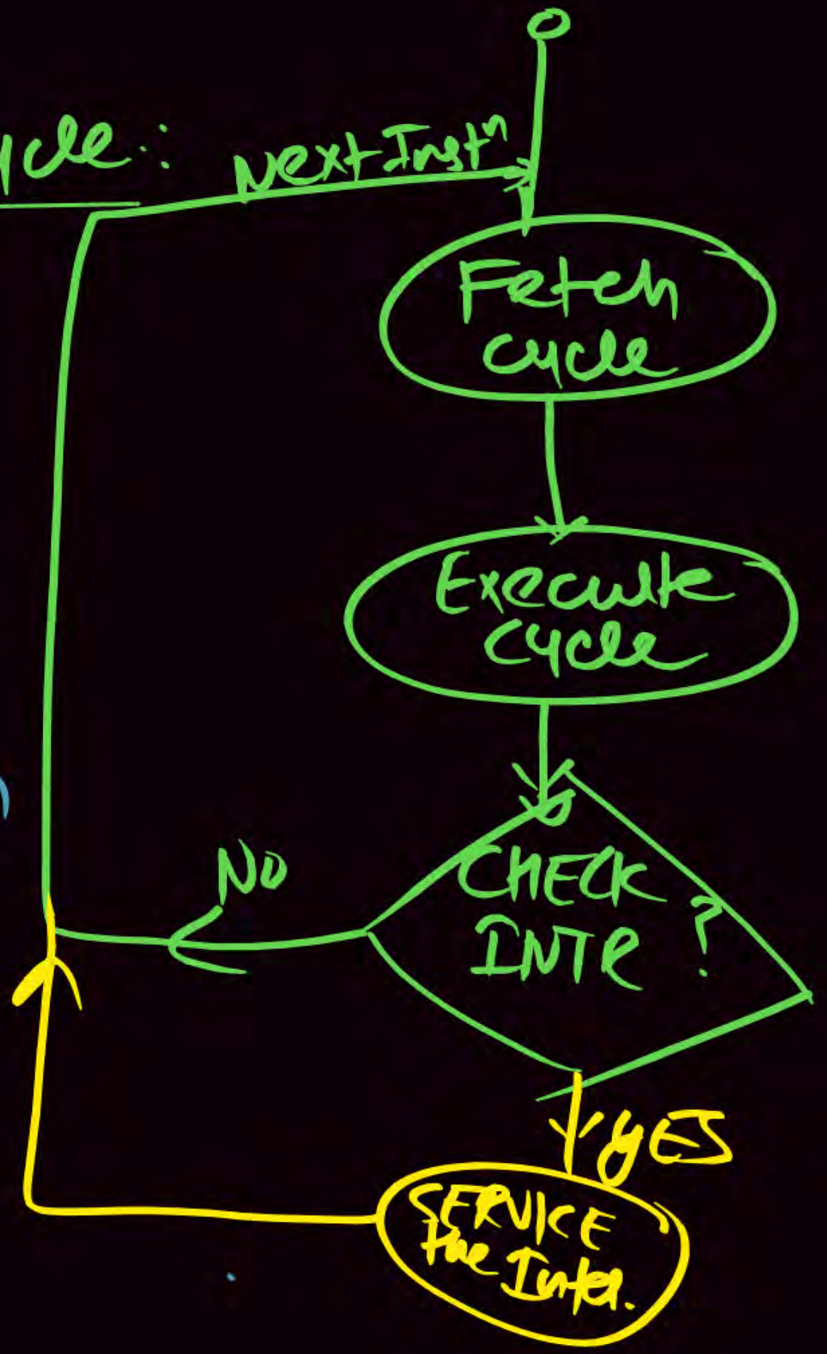


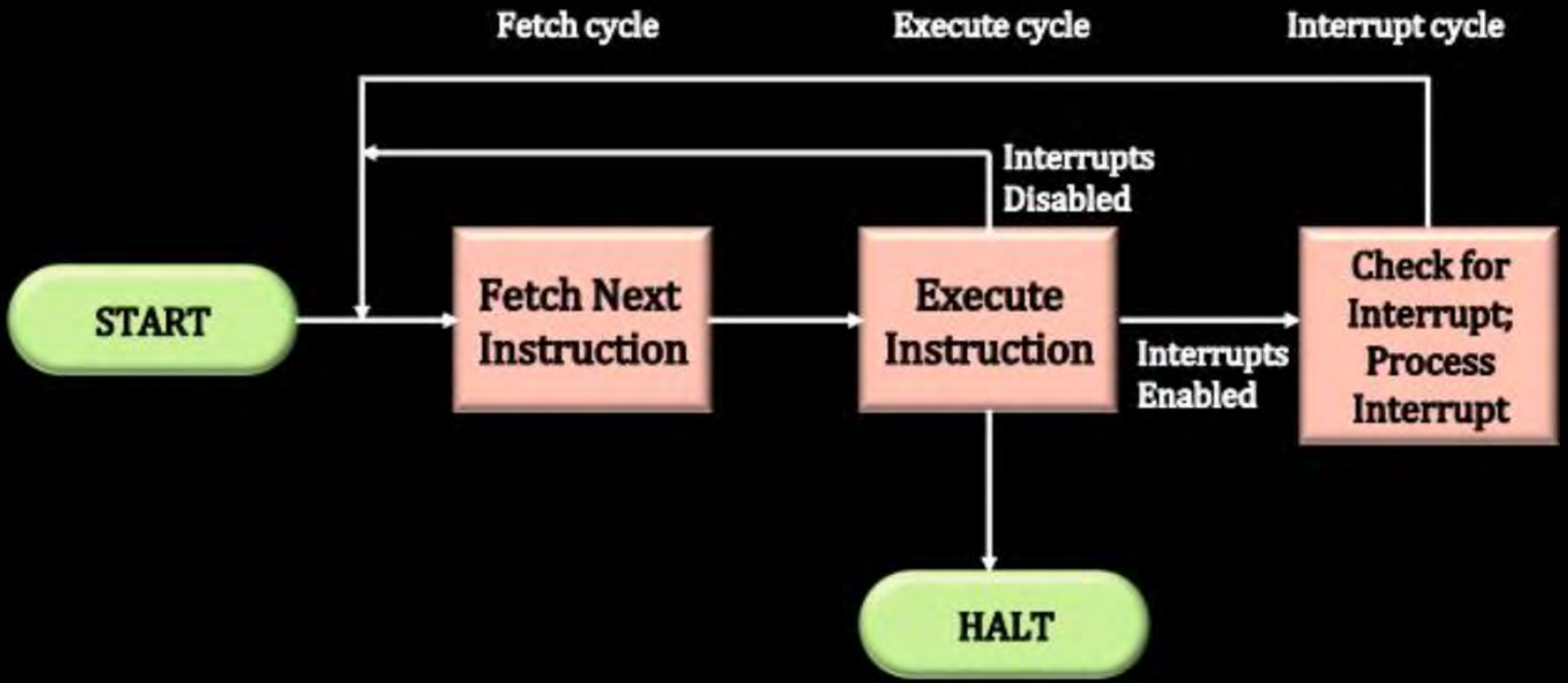
BASIC INSTRUCTION CYCLE

Instruction cycle with Interrupt cycle:

1. Fetch cycle
2. Execute Cycle
3. Interrupt cycle.

Note: After Completion of current Instruction Execution, Interrupt will be Serviced.

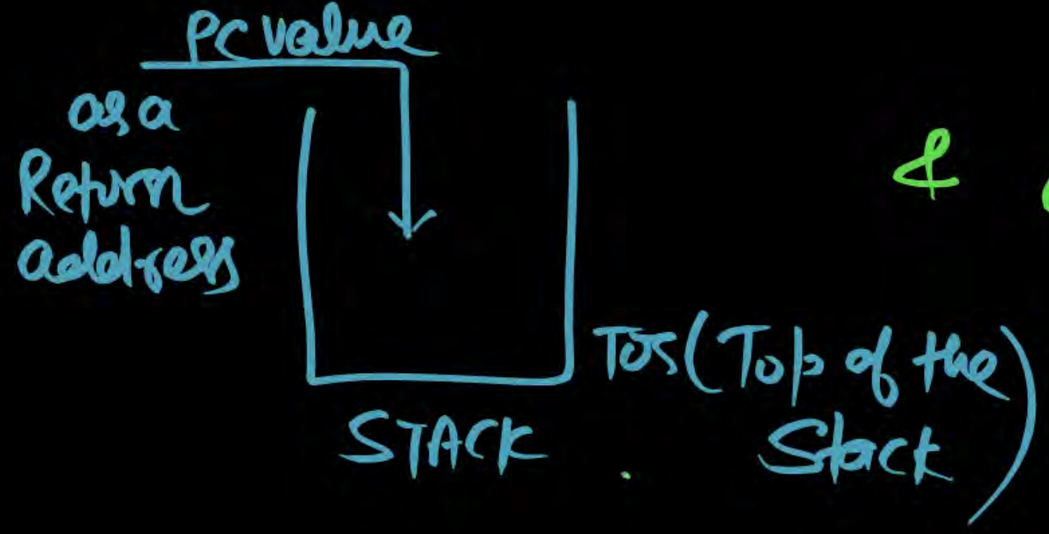




Instruction cycle with Interrupts

Note

When Interrupt occur During the execution of the Instruction then its PUSH the PC [Program Counter) value into the Stack (as a Return address) & Control transfer to ISR.



& Control Transfered to ISR.

MEMORY

① Word Addressable

1 cell = 1 Word

cells

1 Word (32 bit)
1 Word (32 bit)
1 Word (32 bit)
1 Word (32 bit)

② Byte Addressable

1 Cell = 1 Byte (8 bit)

cells

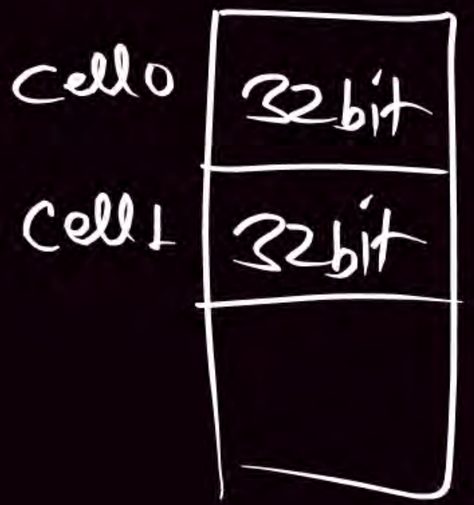
8 bit (1 Byte)
8 bit (1 B)
8 bit (1 B)
8 bit (1 B)
8 bit
8 bit
8 bit
8 bit

8 bit = 1 Byte

1 Word Size = 32 bit

If its Word Addressable then

1 Cell = 32 bits



If its Byte Addressable then 1 Cell = 8 bit

1 cell = 8 bit (1 Byte)

for 32 bit

8 bit = 1 Byte

32 bit = 4 Byte

[4 cell]

we know

In 1 kilo meter = 1000 meter

5600 meter = 5.6 km

⑨ If Word length is 32 bit

	Size
I_1 :	1 Word
I_2 :	1 Word

1 cell = 1 Word

Word

Byte

(32 bit)
1 Word = 4 Byte
→ 4 cells

& Starting address 2000 then

1 cell = 8 bit (1 Byte)

is Memory is Word Addressable

is Memory is Byte Addressable

cell 0 → 2000	I_1 (32 bit)
cell 1 → 2001	I_2 (32 bit)
2002	(32 bit)

Word Addressable [1 cell = 1 Word]

2000-2003

2000	I_1	2000 to 2003
2001	I_1	
2002	I_1	
2003	I_1	

2004-2007

2004	I_2
2005	I_2
2006	I_2
2007	I_2

1 Word = 32 bit

1 Word = 4 Byte

2000-2003 → I_1

Q.1 Consider the following program segment execute on Hypothetical processor. [4 Marks]

Assume that program is stored in the memory address 1000(Decimal) onwards. During the execution of I_6 what could be value present in the Program counter. Assume that word size is 32 bit & memory is Byte Addressable?

1 Word = 32 bit

	Instruction	Size (in words)
1000–1007	I_1	2
1008–1011	I_2	1
1012–1015	I_3	1
1016–1027	I_4	3
1028–1031	I_5	1
1032–1039	I_6	2
1040–1043	I_7	1

① ② ③ ④ ⑤ ⑥ ⑦ ⑧
1000, 01, 02, 03, 04, 05, 06, 1007

3 Word ⇒ 12 Byte

1 Word = 32 bit = 4 Byte

During Execution of I_6

↓ After Fetch cycle PC denote

Starting address of Next (I_7).

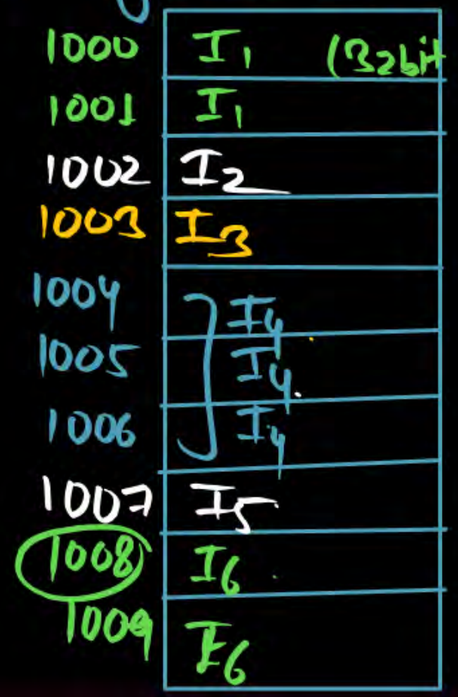
Q.2 Consider the following program segment execute on Hypothetical processor. [4 Marks]

Assume that word size is 32 bit & memory is word addressable. The program is stored in the memory at address 1000(Decimal) onwards. During the execution of I_5. What could be value present in the program counter?

Ans 1008

Instruction	Size (in words)	
I_1	2	1000 - 1001
I_2	1	1002
I_3	1	1003
I_4	3	1004 - 1005 - 1006
I_5	1	1007
I_6	2	1008 - 1009
I_7	1	1010

When I_5 executing then PC will denote starting address of Next Instn (I_6)



Q. Consider the following Program Segment for a hypothetical CN.

Instruction	Meaning	Instruction size (in words)
I_1 MOV r_0, 2000	$r_0 \leftarrow M[2000]$	3
I_2 MOV r_1, 3000	$r_1 \leftarrow M[3000]$	3
I_3 MUL r_0, r_1	$r_0 \leftarrow r_0 * r_1$	1
I_4 MOV 6000, r_0	$M[6000] \leftarrow r_0$	3
I_5 HALT	Machine Halt	1

IF & Decode + Execute

3 * 3 + 4 = 13

3 * 3 + 4 = 13

1 * 3 + 6 = 9

3 * 3 + 4 = 13

1 * 3 + = 3

51 cycle

Let the Clock Cycle required for various operation be as follows:

Instruction Fetch & Decode: 3 clock cycle per word

- MUL with both operand & stored in register: 6 Clock Cycle.
- Register to/from memory transfer: 4 clock cycle

The total number of clock cycle required to execute the program is___

Q.

GATE 6 Marks

Consider the following program segment for a hypothetical CPU Having three users registers R1, R2 and R3.

[GATE-2 Marks]

	Instruction	Operation	Instruction size (in words)	
I_1	MOV R1, 5000	R1 ← Memory[5000]	2	1000 – 1001
I_2	MOVR2, (R1)	R2 ← Memory[(R1)]	1	1002
I_3	ADD R2, R3	R2 ← R2 + R3	1	1003
I_4	MOV 6000, R2	Memory [6000] ← R2	2	1004 – 1005
I_5	HALT	Machine Halts	1	1006

Consider that the memory is word addressable with size 32 bits and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs during the ADD instruction, what will be the return address pushed on to the stack

(a) 1007 (b) 1004 (c) 1005 (d) 1016

Explanation

Soln

Interrupt occur During the Execution of ADD Instn (I_3)

When I_3 only Fetch Before the Execution then

PC having I_4 Starting Address.

So **PC Value = 1004**

When Interrupt occur During execution of I_3 then its Push the PC Value [1004] into the stack as a Return address.

Q.

Consider the following program segment for a hypothetical CPU Having three users registers R1, R2 and R3.

[GATE-2 Marks]

Instruction	Operation	Instruction size (in words)	
MOV R1, 5000	R1 ← Memory[5000]	2	1000 – 1007
MOVR2, (R1)	R2 ← Memory[(R1)]	1	1008 – 1011
ADD R2, R3	R2 ← R2 + R3	1	1012 – 1015
MOV 6000, R2	Memory [6000] ← R2	2	1016 – 1023
HALT	Machine Halts	1	1024 – 1027

I1 I2 I3 I4 I5

@ 1007
(b) 1020
(c) 1024
(d) 1028

Ans 1024

Consider that the memory is Byte addressable with size 32 bits and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the MOV 6000, R2 instruction, the return address (in decimal) saved in the stack will be

(a) 1007 (b) 1020 (c) 1024 (d) 1028

Q. Consider the following program segment for a hypothetical CPU Having three users registers R1, R2 and R3. [GATE- 2 Marks]

Instruction	Operation	Instruction size (in words)	F&D + Execute
MOV R1, 5000	R1 ← Memory[5000]	2	2×2 + 3 = 7
MOVR2, (R1)	R2 ←Memory [(R1)]	1	1×2 + 3 = 5
ADD R2, R3	R2 ← R2 + R3	1	1*2 + 1 = 3
MOV 6000, R2	Memory [6000] ← R2	2	2*2 + 3 = 7
HALT	Machine Halts	1	1×2 + 0 = 2

24 clock cycle

Let the clock cycles required for various operations be as follows:
Register to/from memory transfer:
3. Clock cycles.
ADD with both operand in register
1. Clock cycle
Instruction fetch and decode:
2. Clock cycles per word.
The total number of clock cycle required to execute the program is
(a) 29 (b) 24 (c) 23 (d) 20

COMMON DATA QUESTION (5 - 7)

Consider the following program segment, Here R1, R2 and R3 are the general purpose register.

Instruction	Operation	Instruction size (no. of words)
MOV R1, (3000)	R1←M[3000]	2
LOOP:		
MOV R2, M[R3] ADD R2, R1	R2←M[R3] R2←R1 + R2	1 1
MOV (R3), R2	M[R3] ←R2	1
INC R3	R3←R3+1	1
DEC R1	R1←R1-1	1
BNZ LOOP	Branch on not zero	2
HALT		Stop

1000 - 1007
1008 - 1011
1012 - 1015
1016 - 1019
1020 - 1023
1024 - 1027
1028 - 1031

Assume that the content of memory location 3000 is 10 and the content of the Register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the Numbers are in decimal.

Q.7 Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction "INC R3", what return address (PC value) will be pushed on to the stack?

[2 marks]

(a) 1005 (b) 1020 (c) 1024 (d) 1040

THANK YOU!