Marwadi University	Marwadi University Faculty of Technology Department of Information and Communication Technology	
Subject: Digital Design using Verilog (01CT0619)	**Aim:** Write the Verilog code for designing 16x1 Multiplexer with 2x1 multiplexer and verify.	
Experiment No: 04	**Date:**	**Enrollment No: 92100133020**

Aim: Write the Verilog code for designing 16x1 Multiplexer with 2x1 multiplexer and verify.

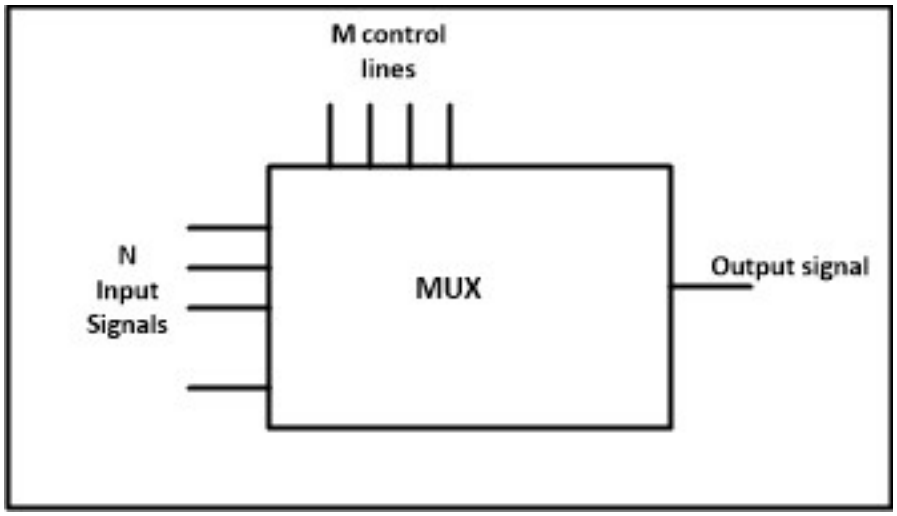
IDE: Icarus Verilog

Theory:

Multiplexer is a combinational circuit that has maximum of 2n data inputs, 'n' selection lines and single output. One of these data inputs will be connected to the output based on the values of selection lines. Since there are 'n' selection lines, there will be 2n possible combinations of zeros and ones. So, each combination will select only one data input.

Multiplexers are used in various applications where multiple-data is needed to be transmitted by using single line, for example in communication system, computer memory, transmission between satellites etc.

Multiplexers are capable of handling both analog and digital applications. In analog applications, multiplexers are made up of relays and transistor switches, whereas in digital applications, the multiplexers are built from standard logic gates. Following figure shows the general idea of a multiplexer with n input signal, m control signals and one output signal.



Types of Multiplexers: -

Multiplexer are commonly classified into the following four types: -

1) 2x1 multiplexer 2) 4x1 multiplexer 3)8x1 multiplexer 4) 16x1 multiplexer

1) 2 x 1 Multiplexer: -

In this Mux there are 2 input lines and 1 selection line. Fig. 2 shows the block diagram & logic

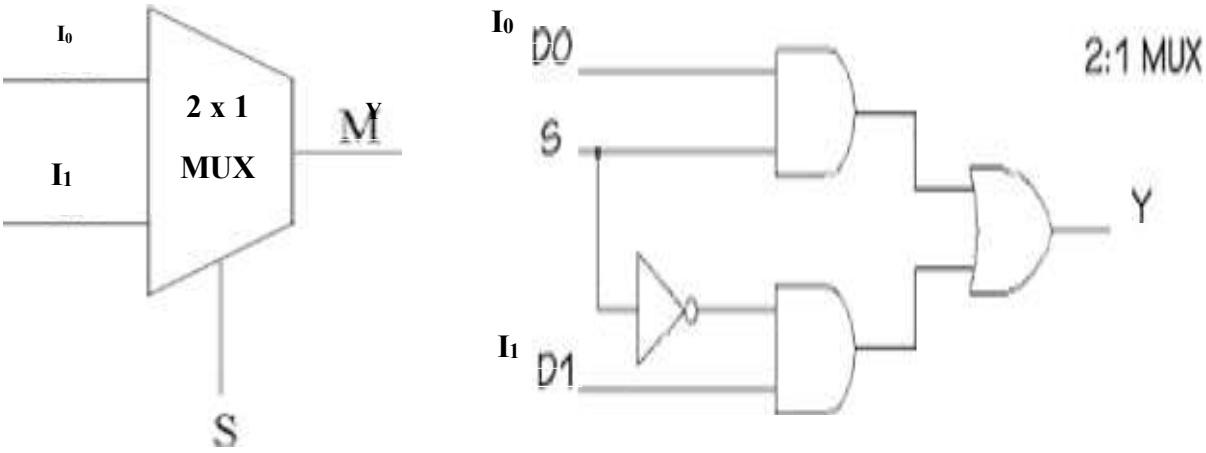


diagram of 2 x 1 mux. The IC no. of 2 x 1 mux is 74158.

Truth table for 2x1 Mux

INPUT S	OUTPUT Y
0	I_0
1	I_1

Logic function: -

$$Y = I_0S' + I_1S$$

2) 16x 1 Multiplexer: -

In this Mux there are 16 input lines and 4 selection lines. Fig. 5shows the block diagram & circuit diagram of 16 x 1 mux. The IC no. of 16 x 1 mux is 74150.

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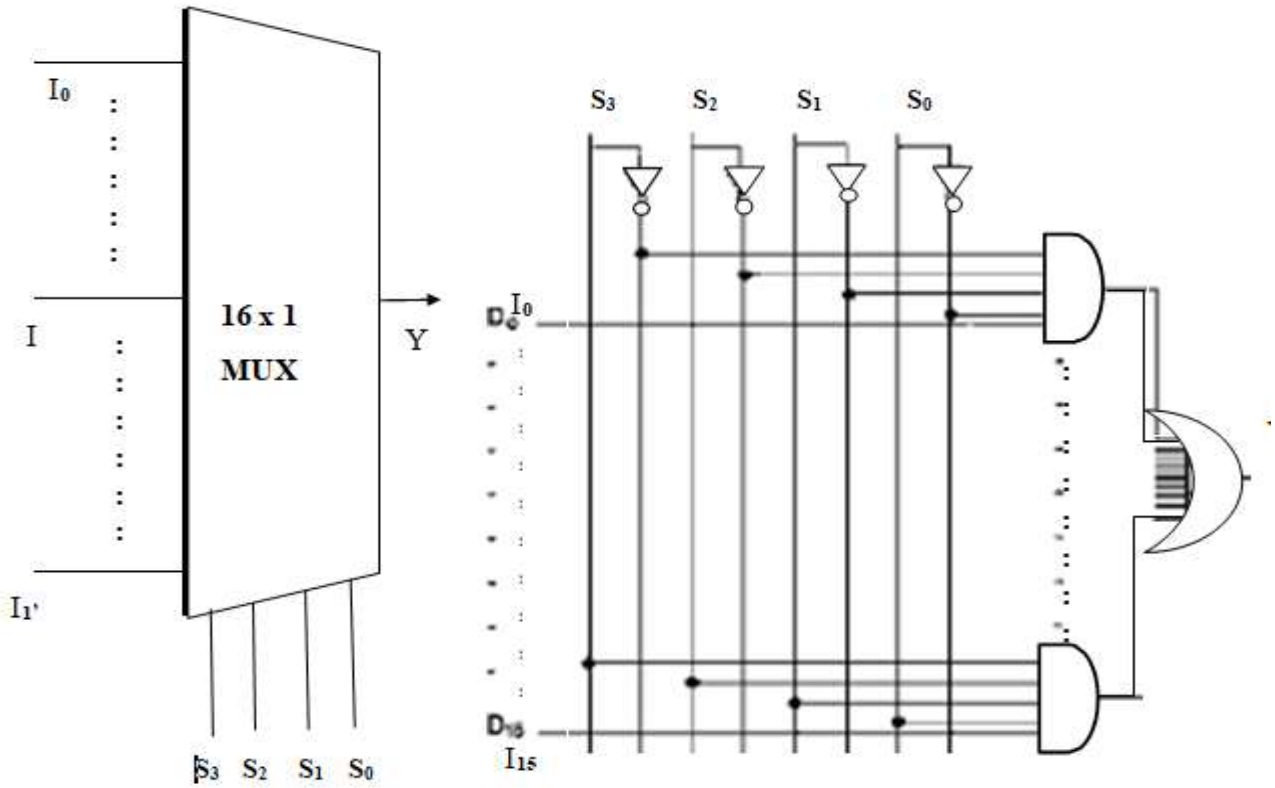

Truth table for 16 x 1 mux

Input S_3	Input S_3	Input S_3	Input S_3	Output Y
0	0	0	0	I_0
0	0	0	1	I_1
0	0	1	0	I_2
0	0	1	1	I_3

0	1	0	0	I_4
0	1	0	1	I_5
0	1	1	0	I_6
0	1	1	1	I_7
1	0	0	0	I_8
1	0	0	1	I_9
1	0	1	0	I_{10}
1	0	1	1	I_{11}
1	1	0	0	I_{12}
1	1	0	1	I_{13}
1	1	1	0	I_{14}
1	1	1	1	I_{15}

Logic function: -

$Y = I_0S_0'S_1'S_2'S_3' + I_1S_0S_1'S_2'S_3' + I_2S_0'S_1S_2'S_3' + I_3S_0S_1S_2'S_3' + I_4S_0'S_1'S_2S_3' + I_5S_0S_1'S_2S_3' + I_6S_0'S_1S_2S_3' + I_7S_0S_1S_2S_3' + I_8S_0'S_1'S_2'S_3 + I_9S_0S_1'S_2'S_3 + I_{10}S_0'S_1S_2'S_3 + I_{11}S_0S_1S_2'S_3 + I_{12}S_0'S_1'S_2S_3 + I_{13}S_0S_1'S_2S_3 + I_{14}S_0S_1S_2S_3 + I_{15}S_0S_1S_2S_3$

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Pre Lab Exercise:

a. What is major practical requirement of multiplexer?

b. Identify and Draw correct realization of Z= AB+BC+DA using 8:1 multiplxer?

c. Write formula to identify number of select line in 8x1 mux?

Verilog Code:

```
// 16 x 1 MUX using 2 x 1 MUX

module mux_2x1(input I0, input I1, input S, output R);
   wire W1, W2, S_bar;

   and(W1, I0, S);
   not(S_bar, S);
   and(W2, I1, S_bar);
   or(R, W1, W2);
endmodule

module mux_16x1(input [15:0] in, input [3:0] sel, output G);
   wire [16:0] y;

   mux_2x1 M1 (in[0], in[1], sel[3], y[0]);
   mux_2x1 M2 (in[2], in[3], sel[3], y[1]);
   mux_2x1 M3 (in[4], in[5], sel[3], y[2]);
   mux_2x1 M4 (in[6], in[7], sel[3], y[3]);
   mux_2x1 M5 (in[8], in[9], sel[3], y[4]);
```

```
    mux_2x1 M6 (in[10], in[11], sel[3], y[5]);
    mux_2x1 M7 (in[12], in[13], sel[3], y[6]);
    mux_2x1 M8 (in[14], in[15], sel[3], y[7]);

    mux_2x1 M9 (y[0], y[1], sel[2], y[8]);
    mux_2x1 M10 (y[2], y[3], sel[2], y[9]);
    mux_2x1 M11 (y[4], y[5], sel[2], y[10]);
    mux_2x1 M12 (y[6], y[7], sel[2], y[11]);

    mux_2x1 M13 (y[8], y[9], sel[1], y[12]);
    mux_2x1 M14 (y[10], y[11], sel[1], y[13]);

    mux_2x1 M15 (y[12], y[13], sel[0], y[14]);
    mux_2x1 M16 (y[14], 1'b0, 1'b0, G);  // Corrected line

endmodule
```

Test-bench:

```
module mux_16x1_tb;
  reg [15:0] in;
  reg [3:0] sel;
  wire out;

  mux_16x1 uut(in, sel, out);

  initial begin
    $display(" S3, S2, S1, S0 | In0, In1, In2, In3, In4, In5, In6, In7, In8, In9, In10, In11, In12, In13, In14, In15");
    $monitor(" %b  %b  %b  %b | %b  %b  %b  %b  %b  %b  %b  %b  %b  %b  %b  %b  %b  %b  %b  %b",
    sel[3], sel[2], sel[1], sel[0], in[0], in[1], in[2], in[3], in[4], in[5], in[6], in[7], in[8], in[9], in[10], in[11], in[12], in[13],
in[14], in[15]);

      in = 16'h0001; sel = 4'b0000;
    #50 in = 16'h0002; sel = 4'b0001;
    #50 in = 16'h0004; sel = 4'b0010;
    #50 in = 16'h0008; sel = 4'b0011;
    #50 in = 16'h0010; sel = 4'b0100;
    #50 in = 16'h0020; sel = 4'b0101;
    #50 in = 16'h0040; sel = 4'b0110;
    #50 in = 16'h0080; sel = 4'b0111;
    #50 in = 16'h0100; sel = 4'b1000;
    #50 in = 16'h0200; sel = 4'b1001;
    #50 in = 16'h0400; sel = 4'b1010;
```

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Experiment No: 04	**Date:**	**Enrollment No: 92100133020**

```
  #50 in = 16'h0800; sel = 4'b1011;
  #50 in = 16'h1000; sel = 4'b1100;
  #50 in = 16'h2000; sel = 4'b1101;
  #50 in = 16'h4000; sel = 4'b1110;
  #50 in = 16'h8000; sel = 4'b1111;
  $dumpfile("MUX_16x1.vcd");
  $dumpvars(1);
  #50 $finish;
 $finish();
 end
endmodule
```

Results:

```
PS D:\Mirror\ICT\3rd YEAR\SEM 6\DDV_Codes> iverilog 16x1_mux.v
PS D:\Mirror\ICT\3rd YEAR\SEM 6\DDV_Codes> vvp a.out
 S3, S2, S1, S0 | In0, In1, In2, In3, In4, In5, In6, In7, In8, In9, In10, In11, In12, In13, In14, In15
 0  0  0  0 |  1   0   0   0   0   0   0   0   0   0    0    0    0    0    0    0
 0  0  0  1 |  0   1   0   0   0   0   0   0   0   0    0    0    0    0    0    0
 0  0  1  0 |  0   0   1   0   0   0   0   0   0   0    0    0    0    0    0    0
 0  0  1  1 |  0   0   0   1   0   0   0   0   0   0    0    0    0    0    0    0
 0  1  0  0 |  0   0   0   0   1   0   0   0   0   0    0    0    0    0    0    0
 0  1  0  1 |  0   0   0   0   0   1   0   0   0   0    0    0    0    0    0    0
 0  1  1  0 |  0   0   0   0   0   0   1   0   0   0    0    0    0    0    0    0
 0  1  1  1 |  0   0   0   0   0   0   0   1   0   0    0    0    0    0    0    0
 1  0  0  0 |  0   0   0   0   0   0   0   0   1   0    0    0    0    0    0    0
 1  0  0  1 |  0   0   0   0   0   0   0   0   0   1    0    0    0    0    0    0
 1  0  1  0 |  0   0   0   0   0   0   0   0   0   0    1    0    0    0    0    0
 1  0  1  1 |  0   0   0   0   0   0   0   0   0   0    0    1    0    0    0    0
 1  1  0  0 |  0   0   0   0   0   0   0   0   0   0    0    0    1    0    0    0
 1  1  0  1 |  0   0   0   0   0   0   0   0   0   0    0    0    0    1    0    0
 1  1  1  0 |  0   0   0   0   0   0   0   0   0   0    0    0    0    0    1    0
VCD info: dumpfile MUX_16x1.vcd opened for output.
 1  1  1  1 |  0   0   0   0   0   0   0   0   0   0    0    0    0    0    0    1
16x1_mux.v:69: $finish called at 1250 (1s)
```

Observation and Result Analysis:

Write the final observation and Analysis

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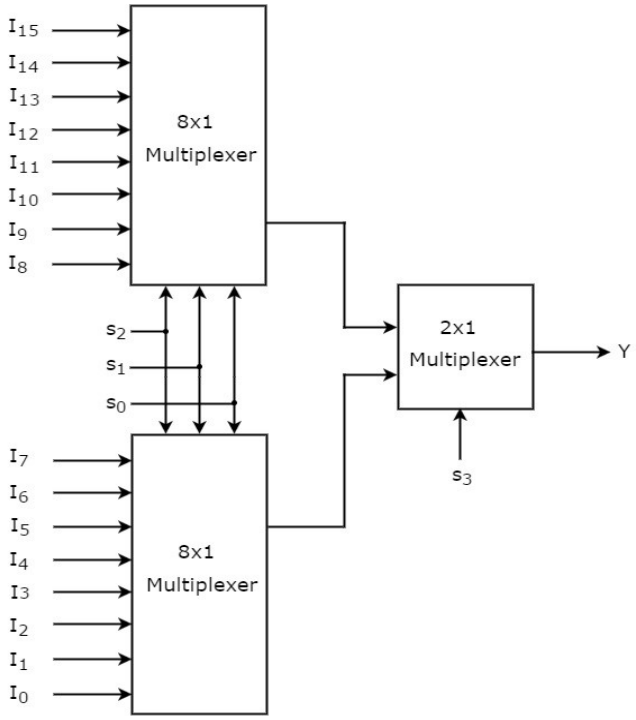
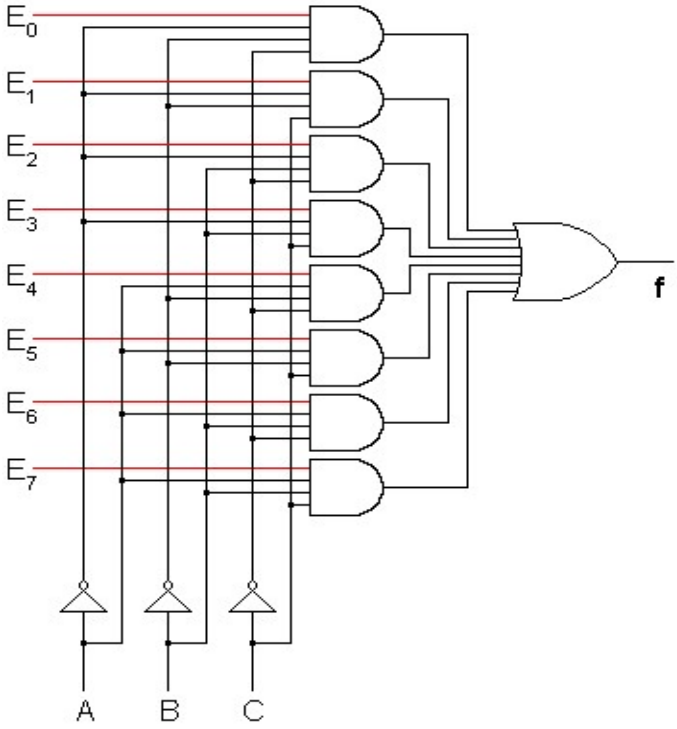
Post Lab Exercise:

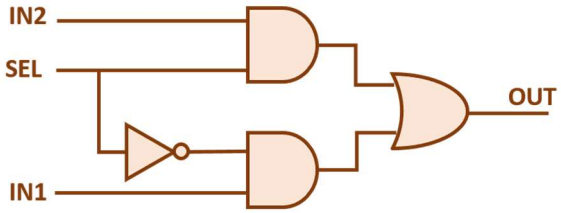
a. Implementation of 16x1 mux using 8x1 mux and 2x1 mux, Mention block diagram with screenshot of verilog code, test- bench and output.



Structure 16x1 MUX with 8x1 and 2x1 MUX



Structure of 8x1 MUX



Structure of 2x1 MUX

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Experiment No: 04	**Date:**	**Enrollment No: 92100133020**

Verilog Code:

```
module mux_2x1 (in1,in2,sel,out);
  input in1, in2, sel;
  output out;
  wire w1, w2, w3;

  and(w1, sel, in2);
  not(w3, sel);
  and(w2, w3, in1);
  or(out, w1, w2);

endmodule

module or_8_input (in1, in2, in3, in4, in5, in6, in7, in8, out);
  input in1, in2, in3, in4, in5, in6, in7, in8;
  output out;

  assign out = in1 | in2 | in3 | in4 | in5 | in6 | in7 | in8;

endmodule

module mux_8x1 (input [8:0] in, input [2:0] sel, output out);
```

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```
    wire w1, w2, w3, w4, w5, w6, w7, w8, in1_out, in2_out, in3_out, in4_out, in5_out, in6_out, in7_out,
in8_out;

    wire sel0, sel1, sel2;


    not(sel0, sel[0]);

    not(sel1, sel[1]);

    not(sel2, sel[2]);


    and(w1, in[0], sel0);

    and(w2, sel2, sel1);

    and(in1_out, w1, w2);


    and(w3, in[1], sel0);

    and(w4, sel[2], sel1);

    and(in2_out, w3, w4);


    and(w5, in[2], sel0);

    and(w6, sel2, sel[1]);

    and(in3_out, w5, w6);


    and(w7, in[3], sel0);
```

```
    and(w8, sel[2], sel[1]);
    and(in4_out, w7, w8);

    and(w9, in[4], sel[0]);
    and(w10, sel2, sel1);
    and(in5_out, w9, w10);

    and(w11, in[5], sel[0]);
    and(w12, sel[2], sel1);
    and(in6_out, w11, w12);

    and(w13, in[6], sel[0]);
    and(w14, sel2, sel[1]);
    and(in7_out, w13, w14);

    and(w15, in[7], sel[0]);
    and(w16, sel[2], sel[1]);
    and(in8_out, w15, w16);

    or_8_input a(in1_out, in2_out, in3_out, in4_out, in5_out, in6_out, in7_out, in8_out, out);

endmodule
```

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```
module mux_16x1(input [15:0] in, input [3:0] sel, output f_out);
  wire w1, w2;

  mux_8x1 a(in[8:0], sel[2:0], w1);
  mux_8x1 b(in[15:8], sel[2:0], w2);

  mux_2x1 c(w1, w2, sel[3], f_out);
endmodule
```

Test-bench:

```
module mux_16x1_using_8x1_tb;
  reg [15:0] in;
  reg [3:0] sel;
  wire out;

  mux_16x1 uut(in, sel, out);

  initial begin
    $display(" S3, S2, S1, S0 | In0, In1, In2, In3, In4, In5, In6, In7, In8, In9, In10, In11, In12, In13, In14, In15");
    $monitor(" %b %b %b %b | %b %b %b %b %b %b %b %b %b %b %b %b %b %b %b %b %b",
    sel[3], sel[2], sel[1], sel[0], in[0], in[1], in[2], in[3], in[4], in[5], in[6], in[7], in[8], in[9], in[10], in[11], in[12], in[13], in[14], in[15]);

      in = 16'h0001; sel = 4'b0000;
```

```
    #50 in = 16'h0002; sel = 4'b0001;
    #50 in = 16'h0004; sel = 4'b0010;
    #50 in = 16'h0008; sel = 4'b0011;
    #50 in = 16'h0010; sel = 4'b0100;
    #50 in = 16'h0020; sel = 4'b0101;
    #50 in = 16'h0040; sel = 4'b0110;
    #50 in = 16'h0080; sel = 4'b0111;
    #50 in = 16'h0100; sel = 4'b1000;
    #50 in = 16'h0200; sel = 4'b1001;
    #50 in = 16'h0400; sel = 4'b1010;
    #50 in = 16'h0800; sel = 4'b1011;
    #50 in = 16'h1000; sel = 4'b1100;
    #50 in = 16'h2000; sel = 4'b1101;
    #50 in = 16'h4000; sel = 4'b1110;
    #50 in = 16'h8000; sel = 4'b1111;

    $dumpfile("MUX_16x1.vcd");
    $dumpvars(1);
    #50 $finish;

  $finish();
  end
endmodule
```

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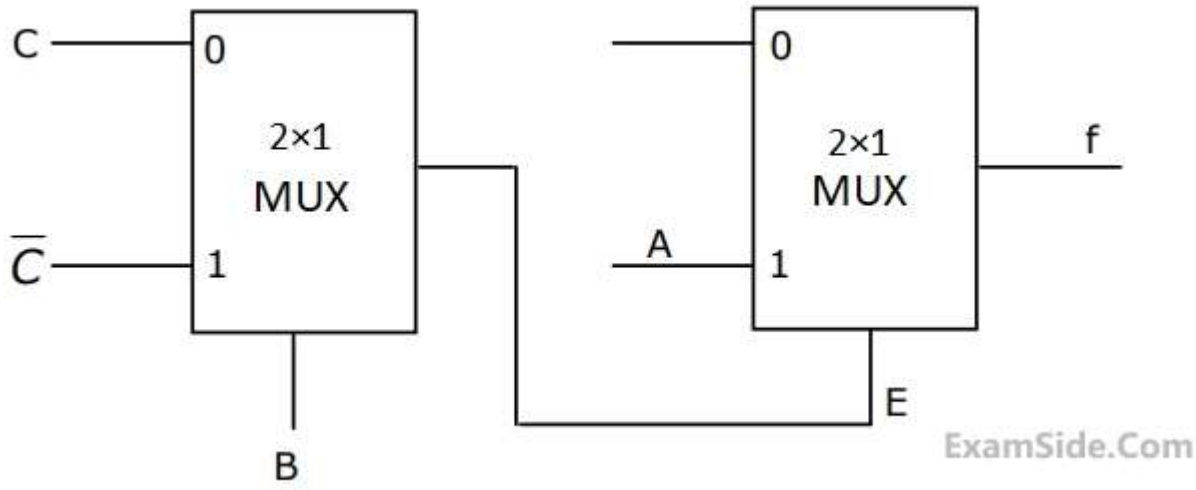
Results:

```
PS D:\Mirror\ICT\3rd YEAR\SEM 6\DDV_Codes> vvp a.out
 S3, S2, S1, S0 | In0, In1, In2, In3, In4, In5, In6, In7, In8, In9, In10, In11, In12, In13, In14, In15
 0  0  0  0 |  1   0   0   0   0   0   0   0   0   0   0    0    0    0    0    0
 0  0  0  1 |  0   1   0   0   0   0   0   0   0   0   0    0    0    0    0    0
 0  0  1  0 |  0   0   1   0   0   0   0   0   0   0   0    0    0    0    0    0
 0  0  1  1 |  0   0   0   1   0   0   0   0   0   0   0    0    0    0    0    0
 0  1  0  0 |  0   0   0   0   1   0   0   0   0   0   0    0    0    0    0    0
 0  1  0  1 |  0   0   0   0   0   1   0   0   0   0   0    0    0    0    0    0
 0  1  1  0 |  0   0   0   0   0   0   1   0   0   0   0    0    0    0    0    0
 0  1  1  1 |  0   0   0   0   0   0   0   1   0   0   0    0    0    0    0    0
 1  0  0  0 |  0   0   0   0   0   0   0   0   1   0   0    0    0    0    0    0
 1  0  0  1 |  0   0   0   0   0   0   0   0   0   1   0    0    0    0    0    0
 1  0  1  0 |  0   0   0   0   0   0   0   0   0   0   1    0    0    0    0    0
 1  0  1  1 |  0   0   0   0   0   0   0   0   0   0   0    1    0    0    0    0
 1  1  0  0 |  0   0   0   0   0   0   0   0   0   0   0    0    1    0    0    0
 1  1  0  1 |  0   0   0   0   0   0   0   0   0   0   0    0    0    1    0    0
 1  1  1  0 |  0   0   0   0   0   0   0   0   0   0   0    0    0    0    1    0
VCD info: dumpfile MUX_16x1.vcd opened for output.
 1  1  1  1 |  0   0   0   0   0   0   0   0   0   0   0    0    0    0    0    1
16x1_mux_using_8x1.v:111: $finish called at 800 (1s)
```

b. The Boolean function f implemented in the figure using two input multiplexers is



Mention procedure for obtaining Boolean function along with verilog code, testbench and output.

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Verilog:

```
module mux_2x1 (in1,in2,sel,out);
  input in1, in2, sel;
  output out;
  wire w1, w2, w3;

  and(w1, sel, in2);
  not(w3, sel);
  and(w2, w3, in1);
  or(out, w1, w2);

endmodule
```

Test-bench:

```
module mux_2x1_tb;
  reg inA, inB, inC;
  wire not_C, outE, out;
  reg [5:0] inputs;

  not(not_C, inC);
  mux_2x1 a(inC, not_C, inB, outE);
  mux_2x1 b(, inA, outE, out);

  initial begin

    for (inputs = 0; inputs < 8; inputs = inputs + 1) begin
       inA = inputs[0];
       inB = inputs[1];
       inC = inputs[2];
       #100;
```

```
    // Display inputs and corresponding outputs
    $display("A = %b | B = %b | C = %b | C' = %b | E = %b | F = %b",inA, inB, inC, not_C, outE, out);
  end
 $finish();
 end
endmodule
```

Results:

```
PS D:\Mirror\ICT\3rd YEAR\SEM 6\DDV_Codes> iverilog exp_4_post2.v
PS D:\Mirror\ICT\3rd YEAR\SEM 6\DDV_Codes> vvp a.out
A = 0 | B = 0 | C = 0 | C' = 1 | E = 0 | F = x
A = 1 | B = 0 | C = 0 | C' = 1 | E = 0 | F = x
A = 0 | B = 1 | C = 0 | C' = 1 | E = 1 | F = 0
A = 1 | B = 1 | C = 0 | C' = 1 | E = 1 | F = 1
A = 0 | B = 0 | C = 1 | C' = 0 | E = 1 | F = 0
A = 1 | B = 0 | C = 1 | C' = 0 | E = 1 | F = 1
A = 0 | B = 1 | C = 1 | C' = 0 | E = 0 | F = x
A = 1 | B = 1 | C = 1 | C' = 0 | E = 0 | F = x
exp_4_post2.v:36: $finish called at 800 (1s)
```