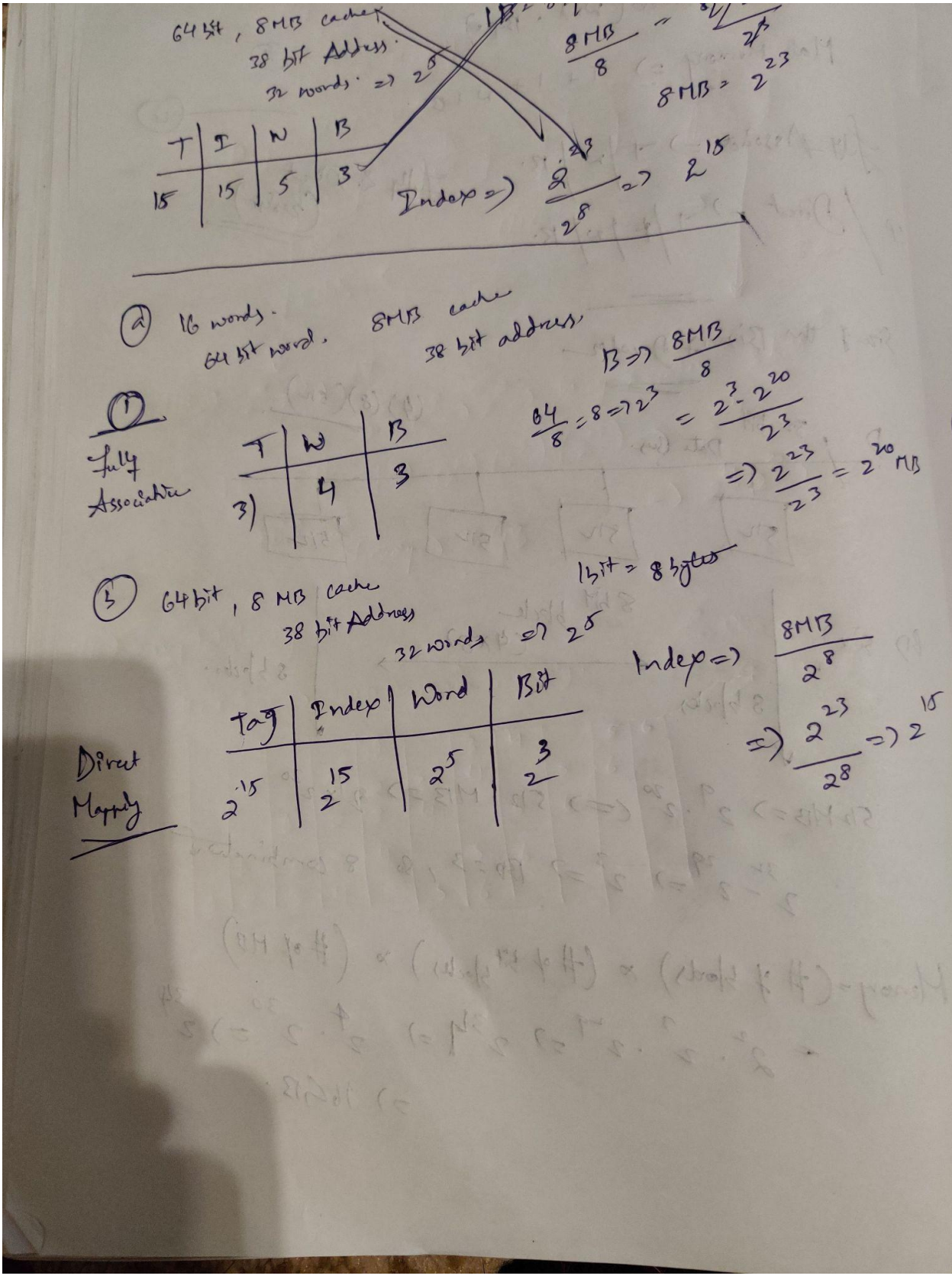
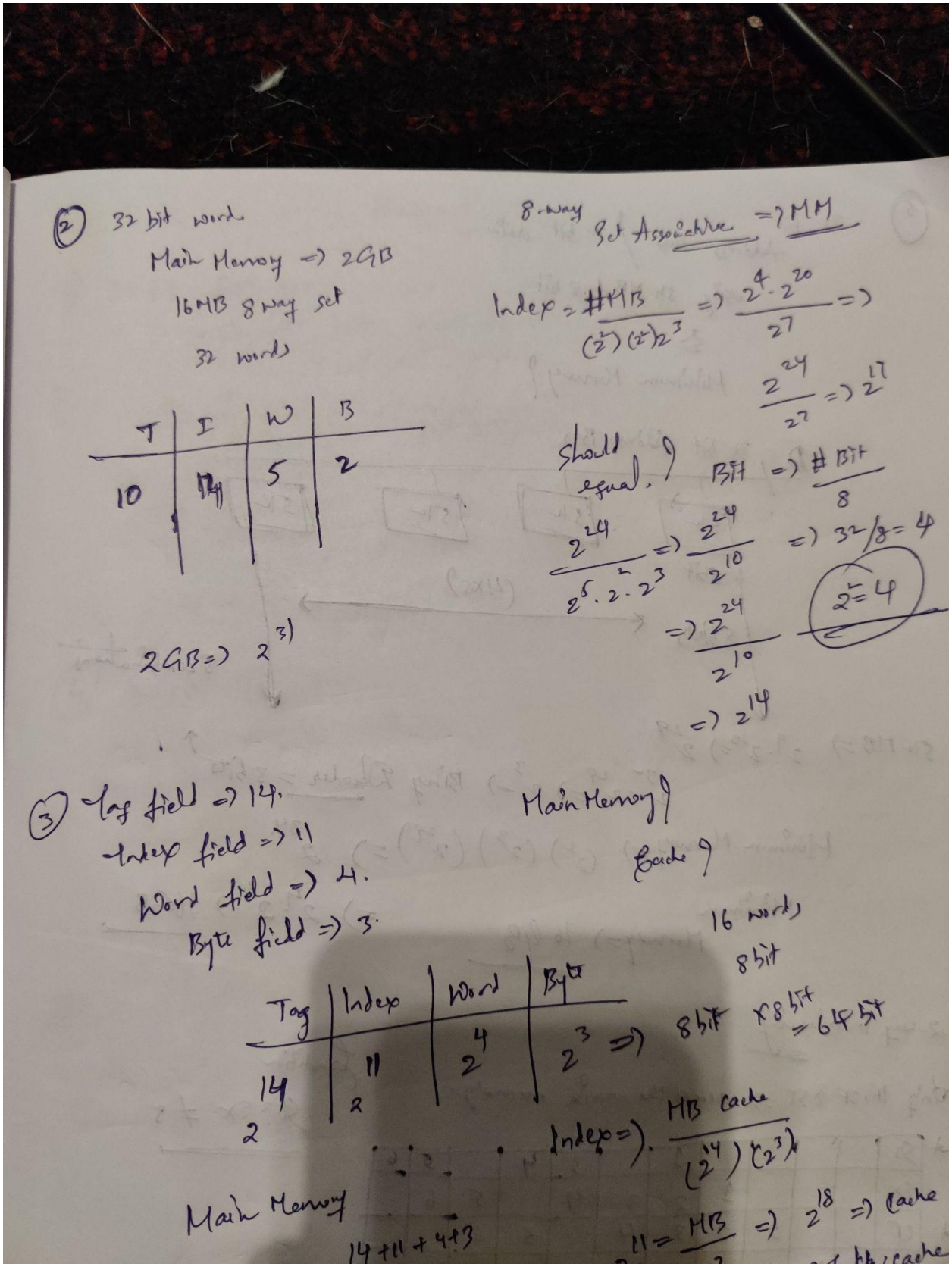
1. A 64-bit word computer system employs an 8 MB cache. The address bus in this system is 38 bits. Determine the number of bits in each field of the address to be seen in the cache using
    a. Fully associative mapping with a line size of 16 words

b. Direct mapping with a line size of 32 words



2. A 32-bit word computer system has a main memory of 2 GB, and has a 16 MB 8-way set associative cache with a line size of 32 words. How many bits is each field of the address

(Tag, Index, Word, Byte)?



3. A computer system has a main memory which is cached with a Direct Mapped cache. The memory addresses of the system have a 14-bit Tag field, an 11-bit Index field, a 4-bit word field, and a 3-bit byte field. What is the size of the main memory in bytes? What is the size of the cache in bytes? How many words are there per cache line? How many bits are the world in the system?

Main Memory => 2GB

16MB 8 way set

32 words

T	I	W	B
10	14	5	2

2GB => 2^{31}

Index = $\frac{\#MB}{(2^5)(2^2)2^3}$ => $\frac{2^4 \cdot 2^{20}}{2^7}$ =>

$\frac{2^{24}}{2^7} => 2^{17}$

Should equal. ? Blk => $\frac{\#Blk}{8}$

$\frac{2^{24}}{2^5 \cdot 2^2 \cdot 2^3} => \frac{2^{24}}{2^{10}}$ => 32/8 = 4

$2^2 = 4$

=> $\frac{2^{24}}{2^{10}}$

=> 2^{14}

(3) Tag field => 14.

Index field => 11

Word field => 4.

Byte field => 3.

Main Memory ?

Cache ?

16 words

8 bit

Tag	Index	Word	Byte
14	11	2^4	2^3 => 8 bit x 8 bit = 64 bit
2	2		

Index =). $\frac{\text{MB cache}}{(2^4)(2^3)}$

Main Memory

14 + 11 + 4 + 3

=> 32

$2^2 \cdot 2^{30}$ => 4 GB main Memory

$2^{11} = \frac{MB}{2^7}$ => 2^{18} => Cache

256 kb cache

4. According to theory, which cache organization (Direct Mapped, Set Associative, or Fully Associative) tends to have the highest average hit to miss ratio, and why? Which tends to have the lowest hit to miss ratio, and why?
   Fully Associative have the highest average Hit to Miss ratio. It is because any block can go into any line of the cache. It helps in placing the words at any place in the cache memory.

   Direct Mapped has the lowest average Hit to Miss ratio because it assigns the block to specific line of cache which leads to more miss than hit lowering the hit to miss ratio.

5. Design the memory organization of a computer system with 32 - bit address bus and 32 - bit data bus using 512 Mbyte*8 - bit memory blocks. What is the minimum size memory

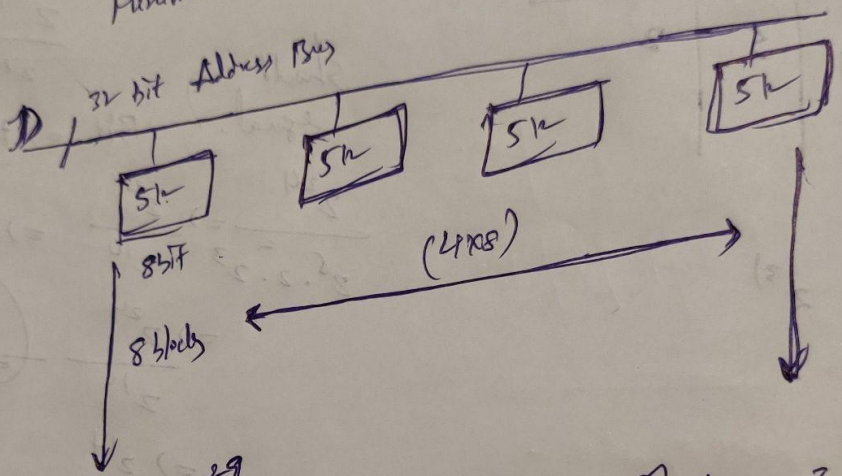
in byte that the system can have?

(5) 32 bit Address Bus / 32 bit data

using 512 MB of 8 bit

&

Minimum Memory?



512 MB $\Rightarrow 2^9 \cdot 2^{20} \Rightarrow 2^{29}$

$2^{32} - 2^{29} \Rightarrow 2^3 \Rightarrow$ Binary Decoder = 3 bits

Minimum Memory $\Rightarrow (2^2)(2^3)(2^{29}) \Rightarrow 2^{34}$

$\Rightarrow 2^4 \cdot 2^{30} \Rightarrow$ 16 GB

Minimum Memory $\Rightarrow$ 16 GB

(6) 2-way Interleaved

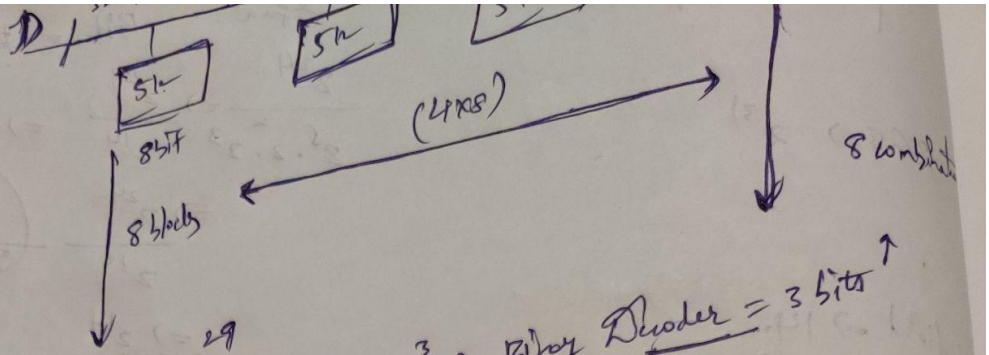
Only IF, OF & ST $\Rightarrow$ access the main memory

Condition

ST & EX ≠

*	ST					1			3	4		5	6
	EX				1	2	3	4		5	6	
*	OF			1	2	3	4		5	6		
	ID		1	2	3	4		5	6			

6. A computer system has a five-stage pipeline consisting of IF, ID, OF, EX, and ST. Assuming only IF, OF, and ST will access the main memory. Assume all instructions use every stage of the pipeline, **except 2 and 5 do not use ST**. Show the schedule for 6 instructions. There are no dependencies between any of these instructions. Assume two-way interleaving. **An instruction will spend 1 cycle in any stage it must use.**



512 MB $\Rightarrow 2^9 \cdot 2^{20} \Rightarrow 2^{29}$

$2^{32} - 2^{29} \Rightarrow 2^3 \rightarrow$ Binary Decoder = 3 bits

Minimum Memory $\Rightarrow (2^2)(2^3)(2^{29}) \Rightarrow 2^{34}$

$\Rightarrow 2^4 \cdot 2^{30} \Rightarrow$ 16 GB

Minimum Memory $\Rightarrow$ 16 GB

(6) 2-way Interleaved

Only IF, OF & ST $\Rightarrow$ access the main memory

Condition

ST & EX $\neq$ 5

*	ST				1			3	4		5	6
	EX				1	2	3	4		5	6	
*	OF			1	2	3	4		5	6		
	ID		1	2	3	4		5	6			
*	IF	1	2	3	4		5	6				