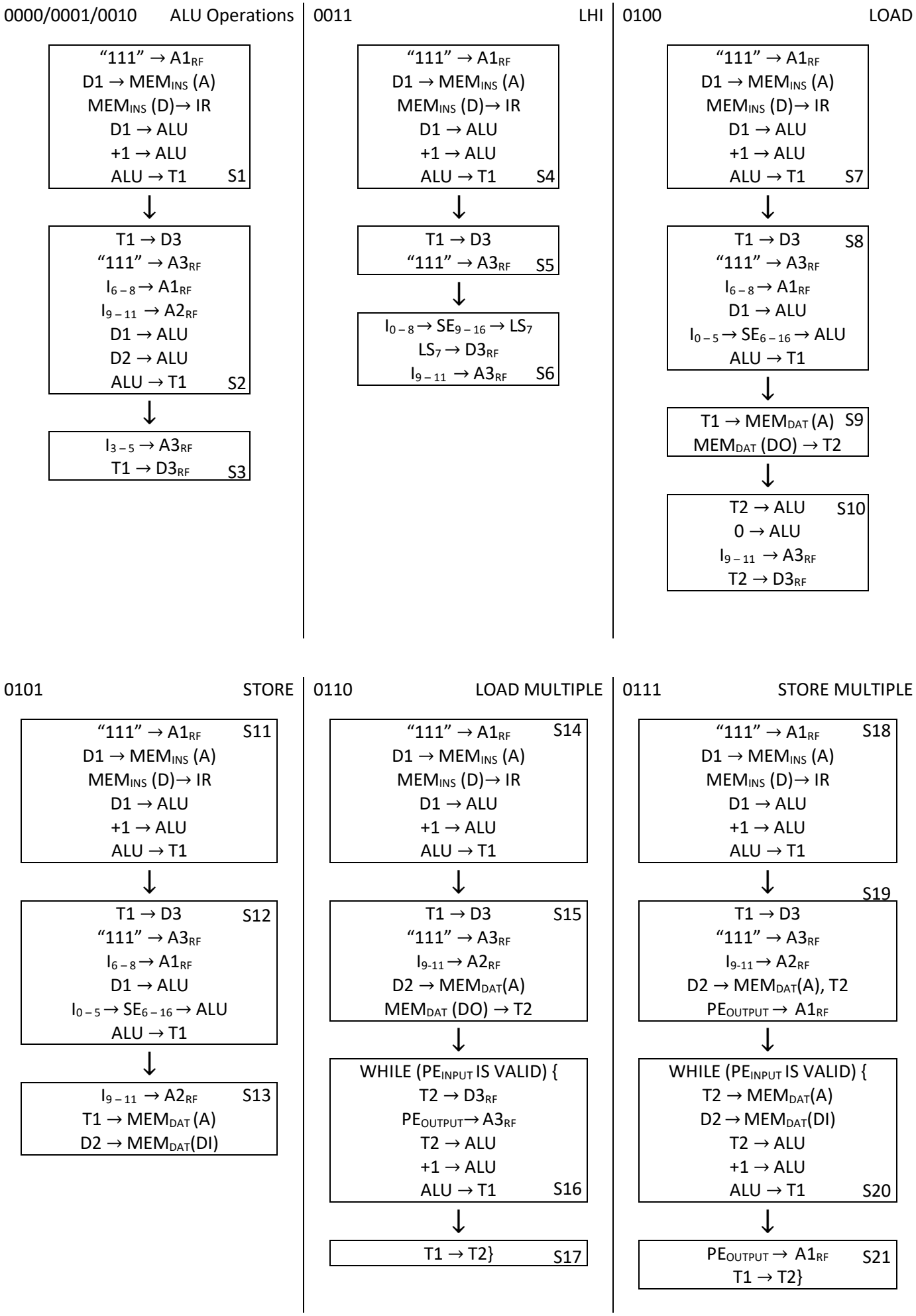
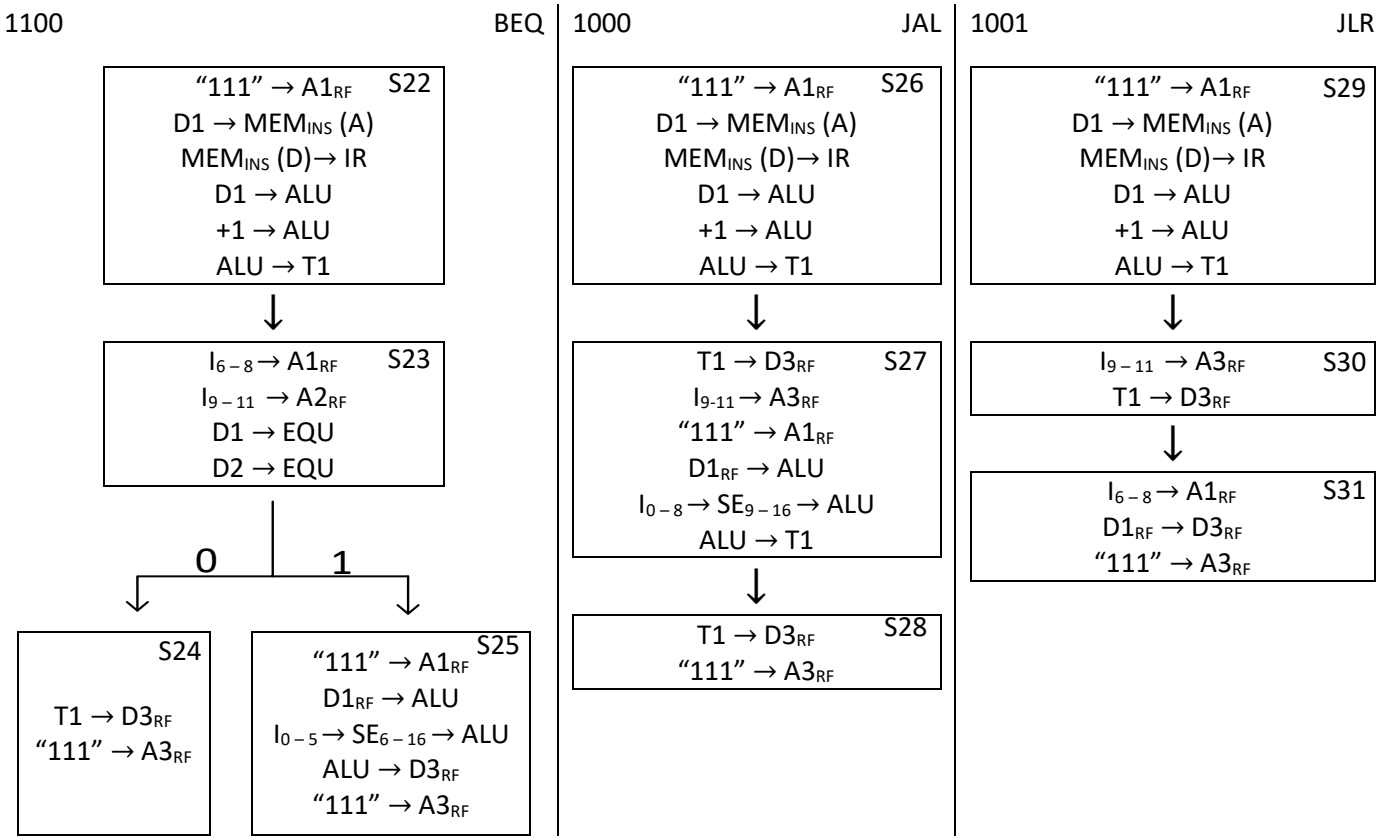

0000/0001/0010 ALU Operations
"111" → A1RF
D1 → MEMINS (A)
MEMINS (D)→ IR
D1 → ALU
+1 → ALU
ALU → T1
S1
T1 → D3
"111" → A3RF
I6 – 8 → A1RF
I9 – 11 → A2RF
D1 → ALU
D2 → ALU
ALU → T1
S2
I3 – 5 → A3RF
T1 → D3RF
S3
0011 LHI
"111" → A1RF
D1 → MEMINS (A)
MEMINS (D)→ IR
D1 → ALU
+1 → ALU
ALU → T1
S4
T1 → D3
"111" → A3RF
S5
I0 – 8 → SE9 – 16 → LS7
LS7 → D3RF
I9 – 11 → A3RF
S6
0100 LOAD
"111" → A1RF
D1 → MEMINS (A)
MEMINS (D)→ IR
D1 → ALU
+1 → ALU
ALU → T1
S7
T1 → D3
"111" → A3RF
I6 – 8 → A1RF
D1 → ALU
I0 – 5 → SE6 – 16 → ALU
ALU → T1
S8
T1 → MEMDAT (A)
MEMDAT (DO) → T2
S9
T2 → ALU
0 → ALU
I9 – 11 → A3RF
T2 → D3RF
S10
0101 STORE
"111" → A1RF
D1 → MEMINS (A)
MEMINS (D)→ IR
D1 → ALU
+1 → ALU
ALU → T1
S11
T1 → D3
"111" → A3RF
I6 – 8 → A1RF
D1 → ALU
I0 – 5 → SE6 – 16 → ALU
ALU → T1
S12
I9 – 11 → A2RF
T1 → MEMDAT (A)
D2 → MEMDAT(DI)
S13
0110 LOAD MULTIPLE
"111" → A1RF
D1 → MEMINS (A)
MEMINS (D)→ IR
D1 → ALU
+1 → ALU
ALU → T1
S14
T1 → D3
"111" → A3RF
I9-11 → A2RF
D2 → MEMDAT(A)
MEMDAT (DO) → T2
S15
WHILE (PEINPUT IS VALID) {
T2 → D3RF
PEOUTPUT→ A3RF
T2 → ALU
+1 → ALU
ALU → T1
S16
T1 → T2}
S17
0111 STORE MULTIPLE
"111" → A1RF
D1 → MEMINS (A)
MEMINS (D)→ IR
D1 → ALU
+1 → ALU
ALU → T1
S18
T1 → D3
"111" → A3RF
I9-11 → A2RF
D2 → MEMDAT(A), T2
PEOUTPUT → A1RF
S19
WHILE (PEINPUT IS VALID) {
T2 → MEMDAT(A)
D2 → MEMDAT(DI)
T2 → ALU
+1 → ALU
ALU → T1
S20
PEOUTPUT → A1RF
T1 → T2}
S21



STATE MERGING AND EQUIVALENCE

$$S1 \equiv S4 \equiv S7 \equiv S11 \equiv S14 \equiv S18 \equiv S22 \equiv S26 \equiv S29$$

$$S2 \equiv S5 \equiv S8^{*} \equiv S12^{*} \equiv S24 \equiv S30 \equiv S28$$

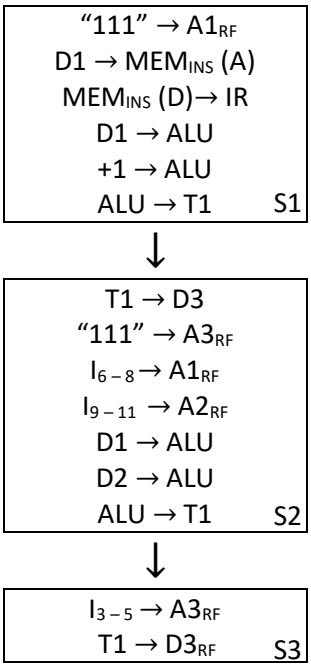
//Note: S12 and S8 will require an additional signal from the Instruction Decoder. It differs from the other states in one input to the ALU. Can be modelled as a multiplexer. Also only S2 must cause a change in the flags. //

If a mealy machine is to be implemented, then that control signal can also be generated from the FSM. That can be decided over the weekend… The Data Path can also be edited suitably then.

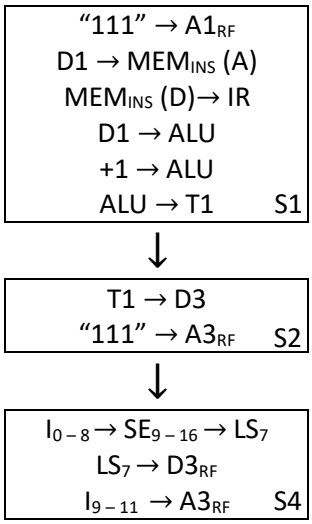
$$S17 \equiv S21$$

This leaves us with about 16 states.

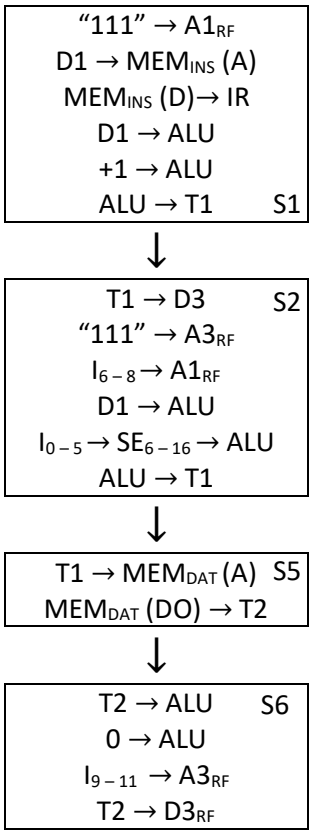
0000/0001/0010 ALU Operations



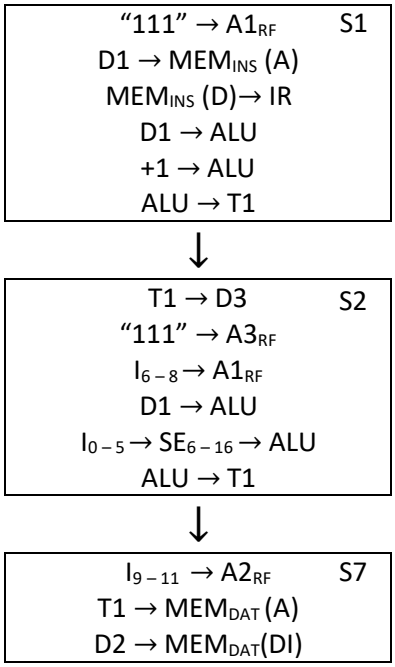
0011 LHI



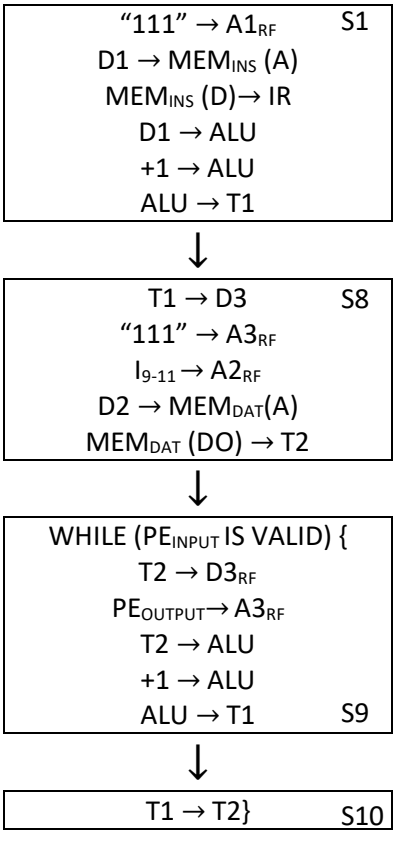
0100 LOAD



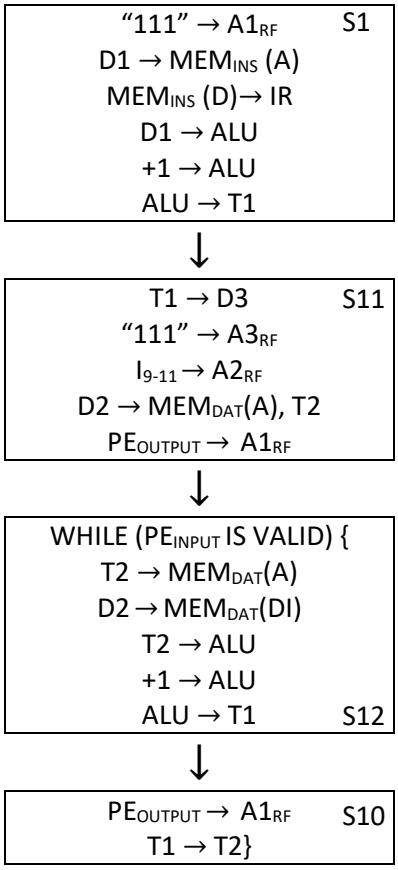
0101 STORE

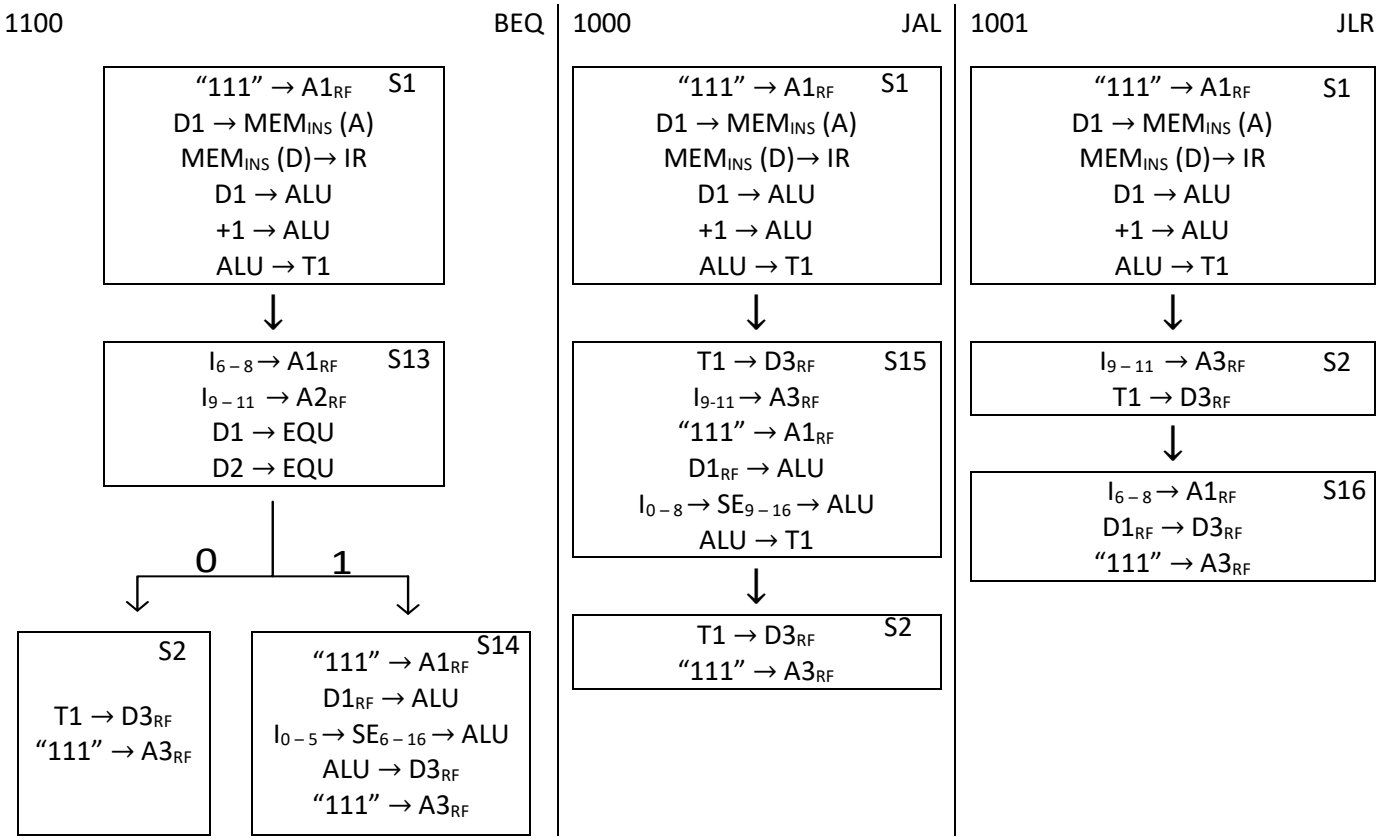


0110 LOAD MULTIPLE



0111 STORE MULTIPLE




1100
BEQ
"111" → A1RF
S1
D1 → MEMINS (A)
MEMINS (D)→ IR
D1 → ALU
+1 → ALU
ALU → T1
I6 – 8 → A1RF
S13
I9 – 11 → A2RF
D1 → EQU
D2 → EQU
0
1
S2
T1 → D3RF
"111" → A3RF
"111" → A1RF
S14
D1RF → ALU
I0 – 5 → SE6 – 16 → ALU
ALU → D3RF
"111" → A3RF
1000
JAL
"111" → A1RF
S1
D1 → MEMINS (A)
MEMINS (D)→ IR
D1 → ALU
+1 → ALU
ALU → T1
T1 → D3RF
S15
I9-11 → A3RF
"111" → A1RF
D1RF → ALU
I0 – 8 → SE9 – 16 → ALU
ALU → T1
T1 → D3RF
S2
"111" → A3RF
1001
JLR
"111" → A1RF
S1
D1 → MEMINS (A)
MEMINS (D)→ IR
D1 → ALU
+1 → ALU
ALU → T1
I9 – 11 → A3RF
S2
T1 → D3RF
I6 – 8 → A1RF
S16
D1RF → D3RF
"111" → A3RF