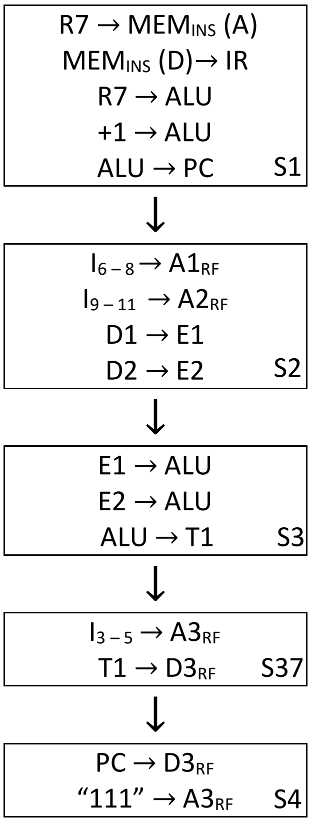
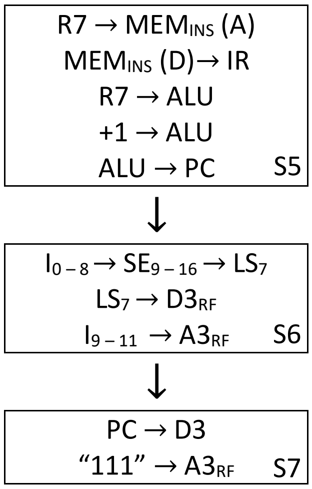
0000/0001/0010 ALU Operations



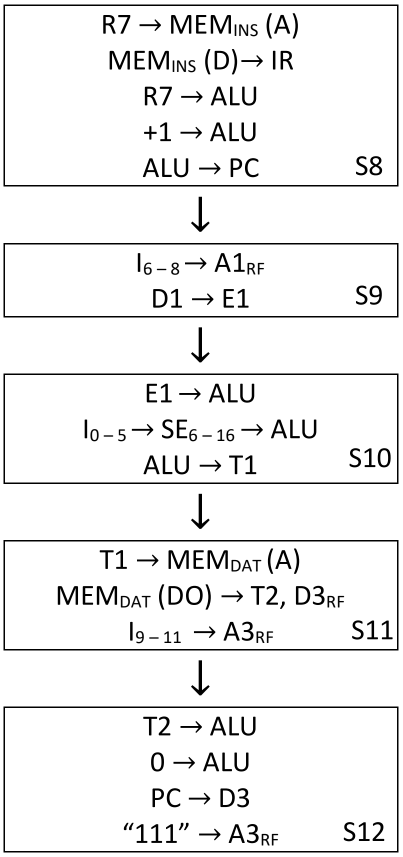
$R7 \rightarrow MEM_{INS}$ (A)
$MEM_{INS}$ (D)→ IR
R7 → ALU
+1 → ALU
ALU → PC
S1
$I_{6-8} \rightarrow A1_{RF}$
$I_{9-11} \rightarrow A2_{RF}$
D1 → E1
D2 → E2
S2
E1 → ALU
E2 → ALU
ALU → T1
S3
$I_{3-5} \rightarrow A3_{RF}$
$T1 \rightarrow D3_{RF}$
S37
$PC \rightarrow D3_{RF}$
“111” $\rightarrow A3_{RF}$
S4

0011 LHI



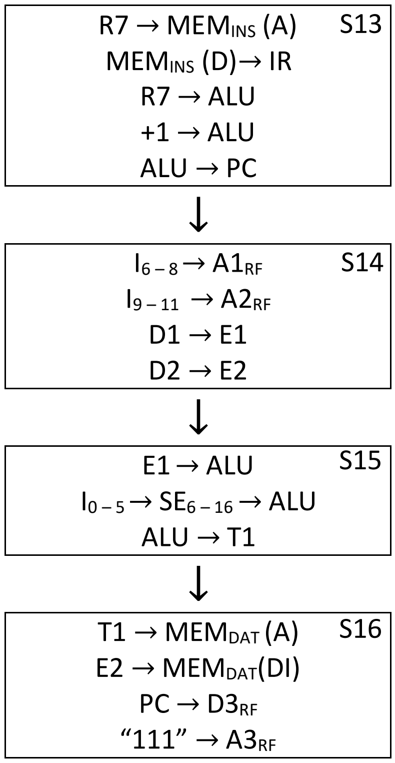
$R7 \rightarrow MEM_{INS}$ (A)
$MEM_{INS}$ (D)→ IR
R7 → ALU
+1 → ALU
ALU → PC
S5
$I_{0-8} \rightarrow SE_{9-16} \rightarrow LS_7$
$LS_7 \rightarrow D3_{RF}$
$I_{9-11} \rightarrow A3_{RF}$
S6
PC → D3
“111” $\rightarrow A3_{RF}$
S7

0100 LOAD



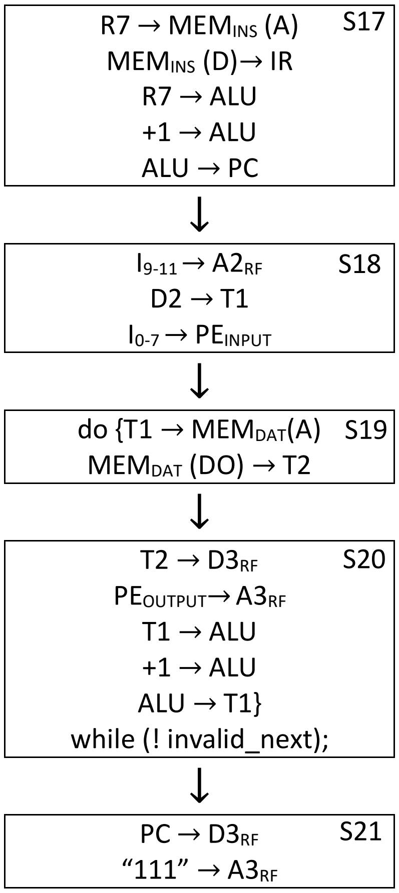
$R7 \rightarrow MEM_{INS}$ (A)
$MEM_{INS}$ (D)→ IR
R7 → ALU
+1 → ALU
ALU → PC
S8
$I_{6-8} \rightarrow A1_{RF}$
D1 → E1
S9
E1 → ALU
$I_{0-5} \rightarrow SE_{6-16} \rightarrow ALU$
ALU → T1
S10
$T1 \rightarrow MEM_{DAT}$ (A)
$MEM_{DAT}$ (DO) $\rightarrow T2, D3_{RF}$
$I_{9-11} \rightarrow A3_{RF}$
S11
T2 → ALU
0 → ALU
PC → D3
“111” $\rightarrow A3_{RF}$
S12

0101 STORE



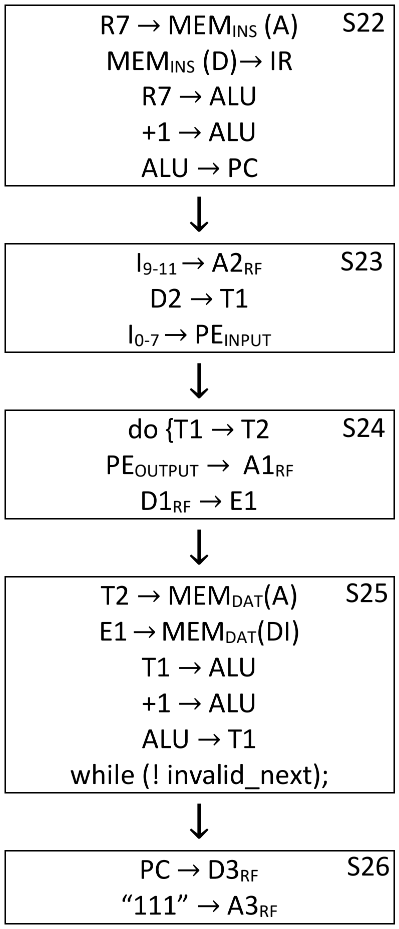
$R7 \rightarrow MEM_{INS}$ (A)
S13
$MEM_{INS}$ (D)→ IR
R7 → ALU
+1 → ALU
ALU → PC
$I_{6-8} \rightarrow A1_{RF}$
S14
$I_{9-11} \rightarrow A2_{RF}$
D1 → E1
D2 → E2
E1 → ALU
S15
$I_{0-5} \rightarrow SE_{6-16} \rightarrow ALU$
ALU → T1
$T1 \rightarrow MEM_{DAT}$ (A)
S16
$E2 \rightarrow MEM_{DAT}$(DI)
$PC \rightarrow D3_{RF}$
“111” $\rightarrow A3_{RF}$

0110 LOAD MULTIPLE



$R7 \rightarrow MEM_{INS}$ (A)
S17
$MEM_{INS}$ (D)→ IR
R7 → ALU
+1 → ALU
ALU → PC
$I_{9-11} \rightarrow A2_{RF}$
S18
D2 → T1
$I_{0-7} \rightarrow PE_{INPUT}$
do {$T1 \rightarrow MEM_{DAT}$(A)
S19
$MEM_{DAT}$ (DO) → T2
$T2 \rightarrow D3_{RF}$
S20
$PE_{OUTPUT} \rightarrow A3_{RF}$
T1 → ALU
+1 → ALU
ALU → T1}
while (! invalid_next);
$PC \rightarrow D3_{RF}$
S21
“111” $\rightarrow A3_{RF}$

0111 STORE MULTIPLE



$R7 \rightarrow MEM_{INS}$ (A)
S22
$MEM_{INS}$ (D)→ IR
R7 → ALU
+1 → ALU
ALU → PC
$I_{9-11} \rightarrow A2_{RF}$
S23
D2 → T1
$I_{0-7} \rightarrow PE_{INPUT}$
do {T1 → T2
S24
$PE_{OUTPUT} \rightarrow A1_{RF}$
$D1_{RF} \rightarrow E1$
$T2 \rightarrow MEM_{DAT}$(A)
S25
$E1 \rightarrow MEM_{DAT}$(DI)
T1 → ALU
+1 → ALU
ALU → T1
while (! invalid_next);
$PC \rightarrow D3_{RF}$
S26
“111” $\rightarrow A3_{RF}$

1100 BEQ

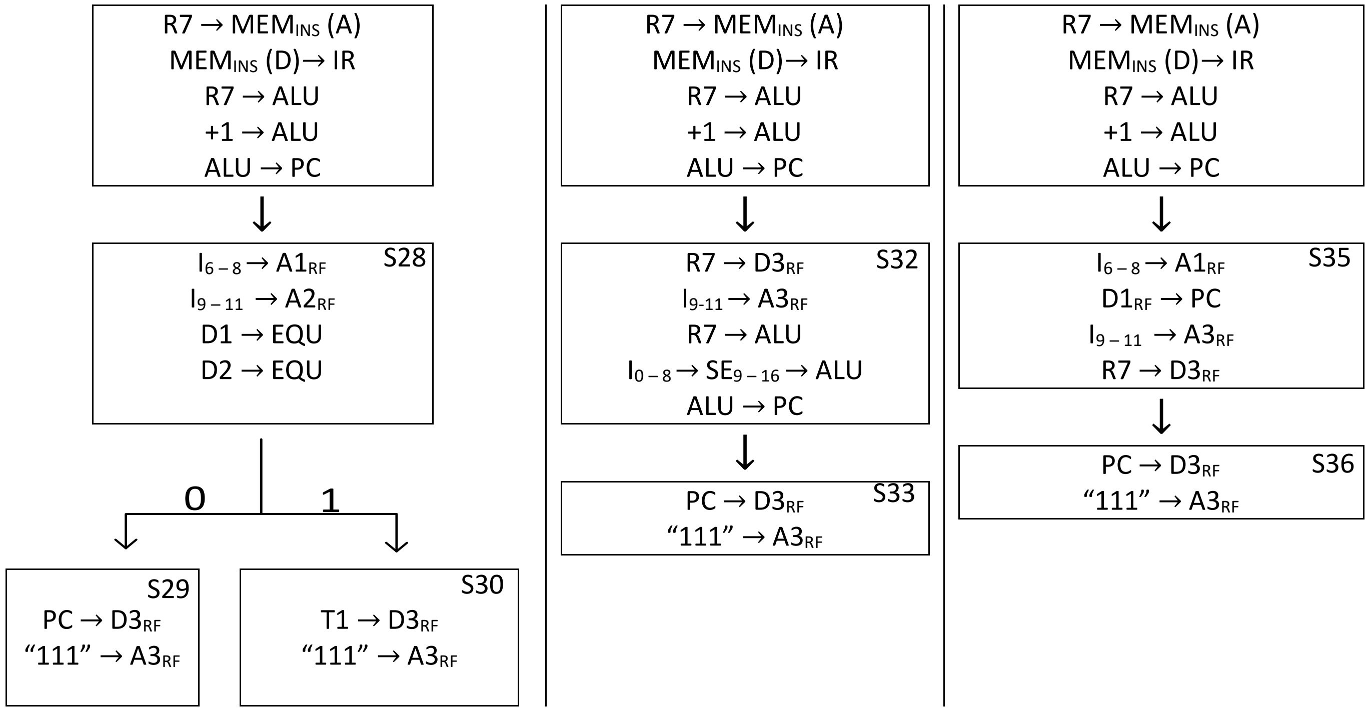
S27

1000 JAL

S31

1001 JLR

S34



## STATE MERGING AND EQUIVALENCE

$$S1 \equiv S5 \equiv S8 \equiv S13 \equiv S17 \equiv S22 \equiv S27 \equiv S31 \equiv S34$$

$$S4 \equiv S7 \equiv S12^{*}(Superset) \equiv S21 \equiv S26 \equiv S29 \equiv S33 \equiv S36$$

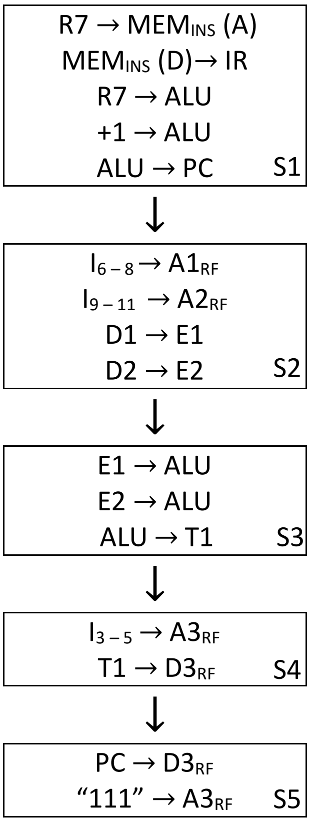
$$S2 \equiv S9 \equiv S14 \equiv S18 \equiv S23 \equiv S28(Superset)$$

$$S10 \equiv S15$$

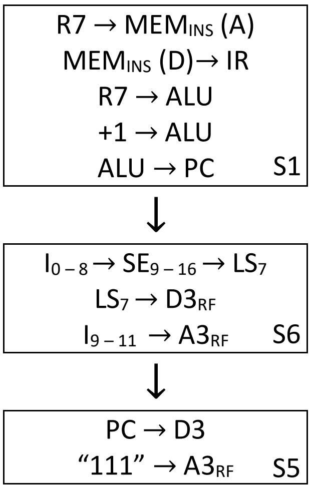
//Note: S12 will require an additional signal from the Instruction Decoder. It differs from the other states in one input to the ALU. Can be modelled as a multiplexer. Also only S2 must cause a change in the flags. //

This leaves us with 16 states in total.

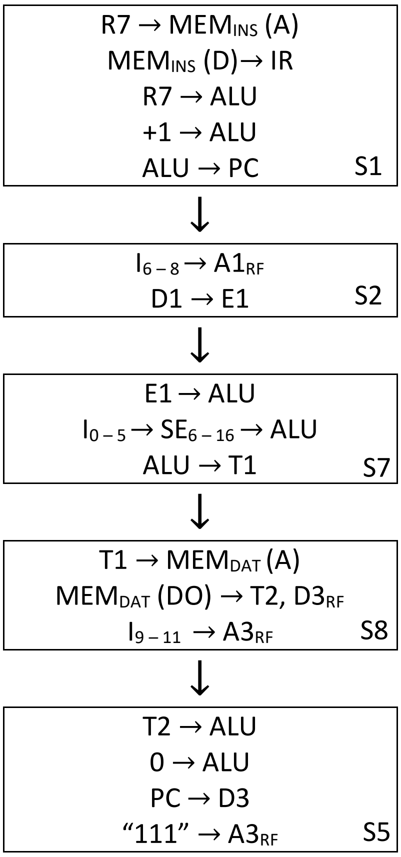
0000/0001/0010 ALU Operations



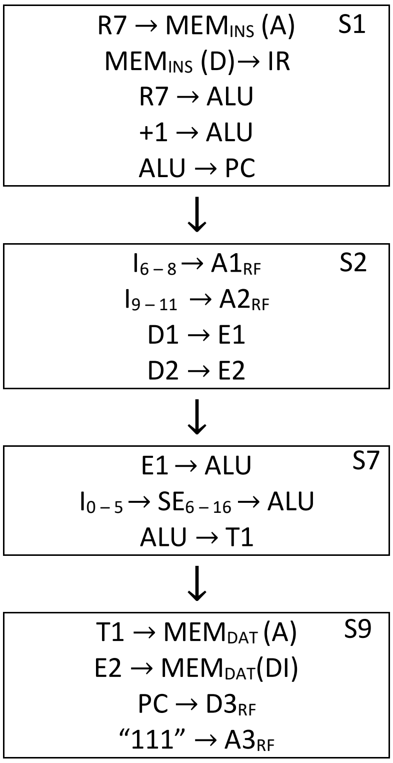
0011 LHI



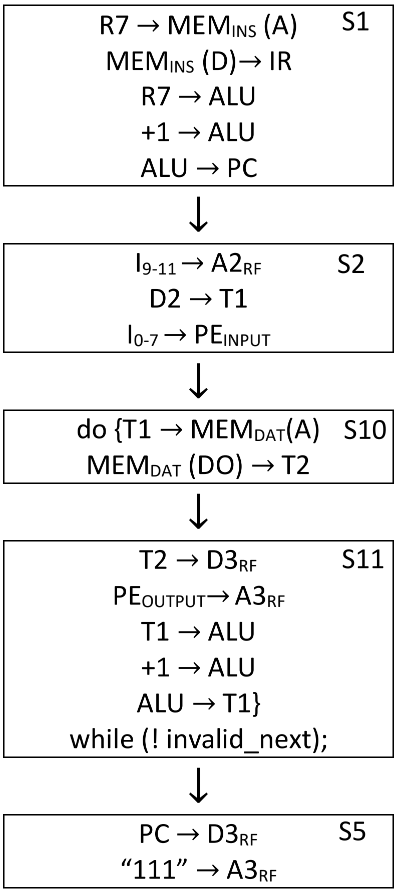
0100 LOAD



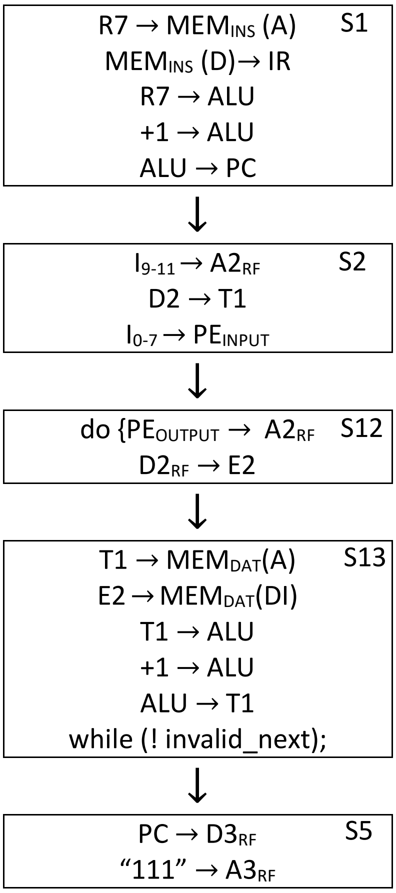
0101 STORE

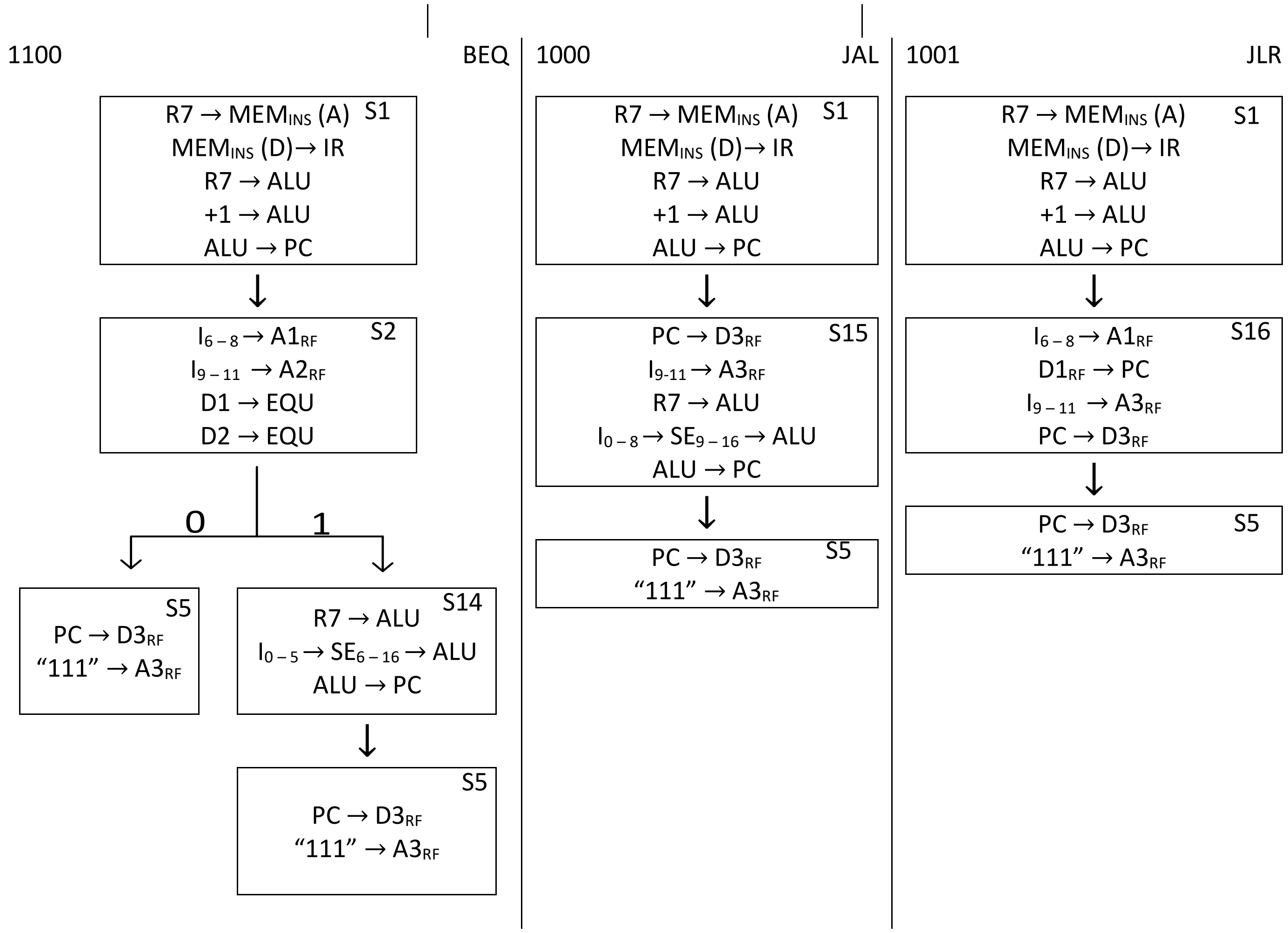


0110 LOAD MULTIPLE



0111 STORE MULTIPLE





1100
BEQ
R7 → $MEM_{INS}$ (A)
$MEM_{INS}$ (D)→ IR
R7 → ALU
+1 → ALU
ALU → PC
S1
$I_{6-8}$ → $A1_{RF}$
$I_{9-11}$ → $A2_{RF}$
D1 → EQU
D2 → EQU
S2
0
1
S5
PC → $D3_{RF}$
“111” → $A3_{RF}$
S14
R7 → ALU
$I_{0-5}$ → $SE_{6-16}$ → ALU
ALU → PC
S5
PC → $D3_{RF}$
“111” → $A3_{RF}$
1000
JAL
R7 → $MEM_{INS}$ (A)
$MEM_{INS}$ (D)→ IR
R7 → ALU
+1 → ALU
ALU → PC
S1
PC → $D3_{RF}$
$I_{9-11}$ → $A3_{RF}$
R7 → ALU
$I_{0-8}$ → $SE_{9-16}$ → ALU
ALU → PC
S15
PC → $D3_{RF}$
“111” → $A3_{RF}$
S5
1001
JLR
R7 → $MEM_{INS}$ (A)
$MEM_{INS}$ (D)→ IR
R7 → ALU
+1 → ALU
ALU → PC
S1
$I_{6-8}$ → $A1_{RF}$
$D1_{RF}$ → PC
$I_{9-11}$ → $A3_{RF}$
PC → $D3_{RF}$
S16
PC → $D3_{RF}$
“111” → $A3_{RF}$
S5