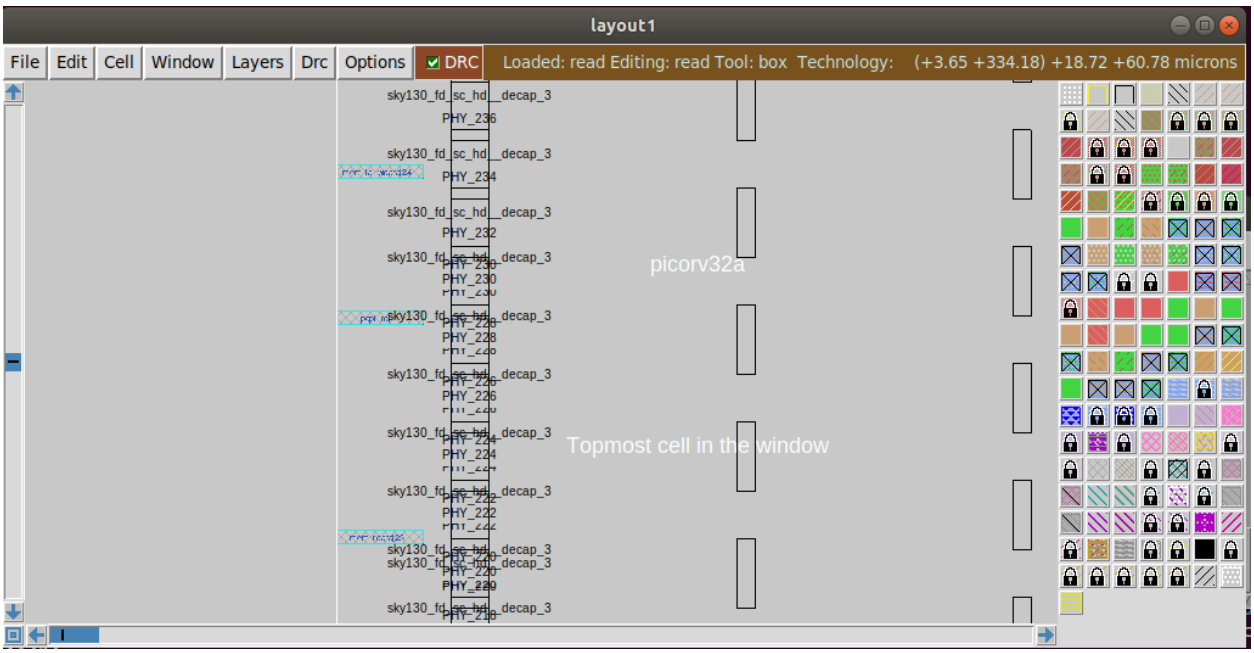
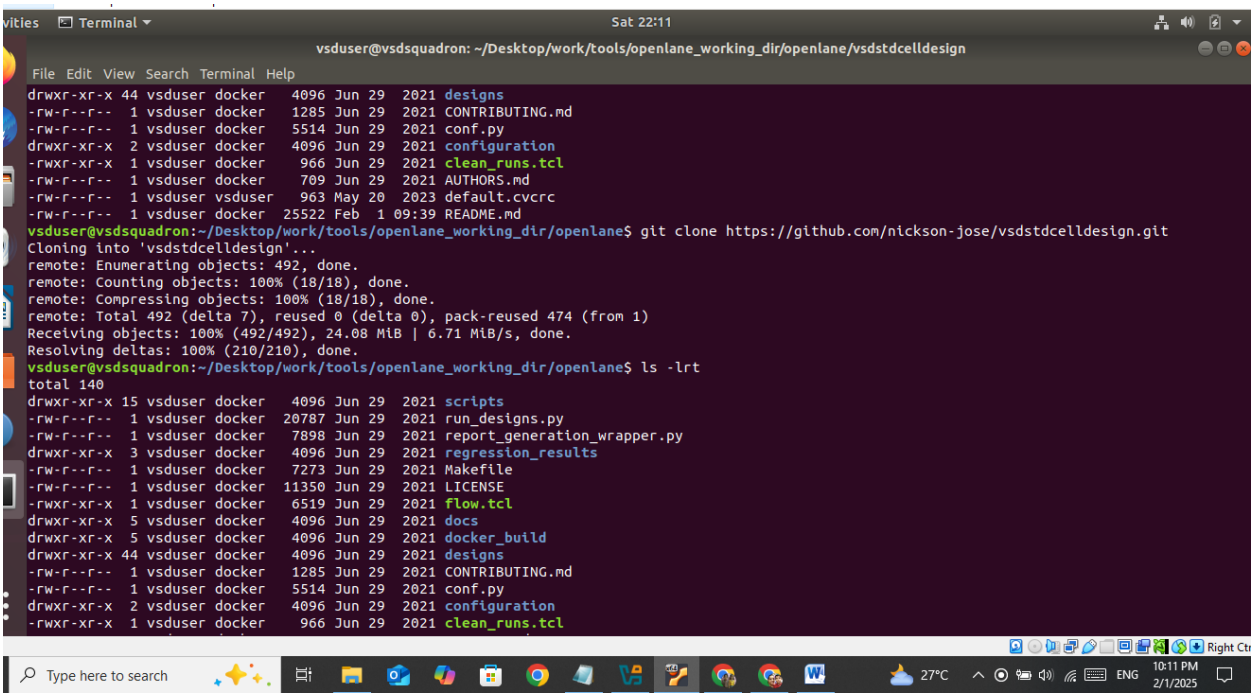
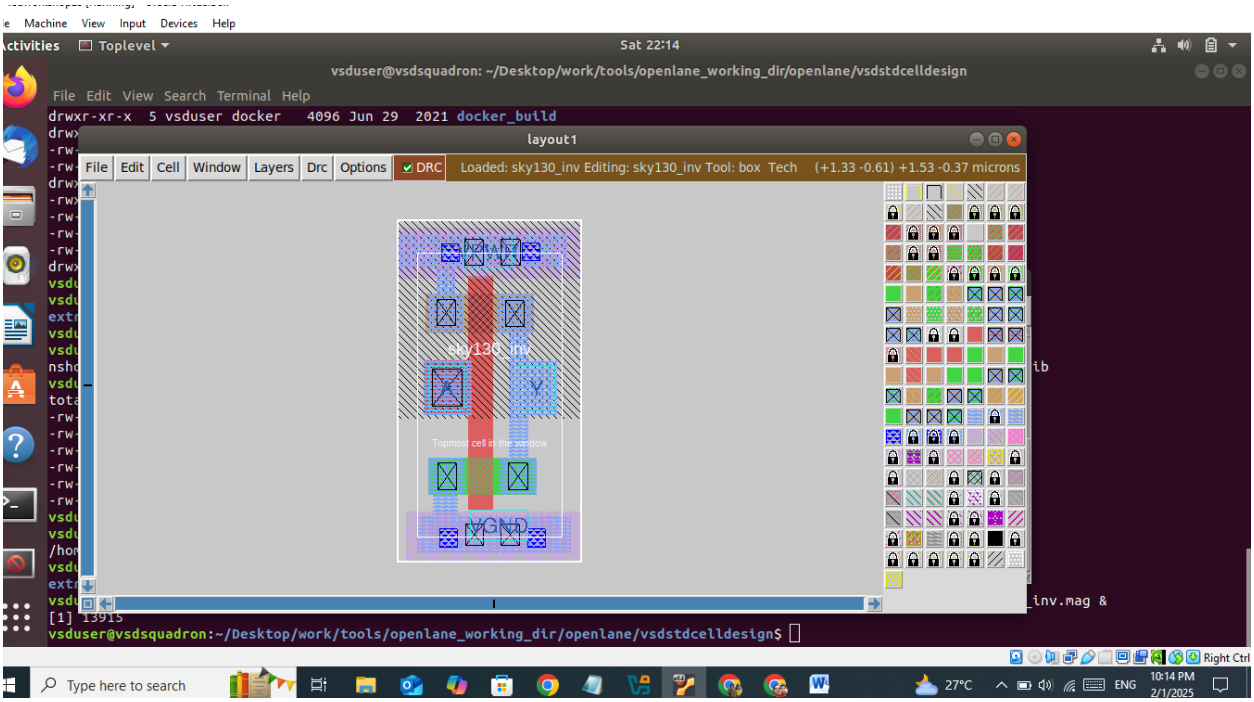
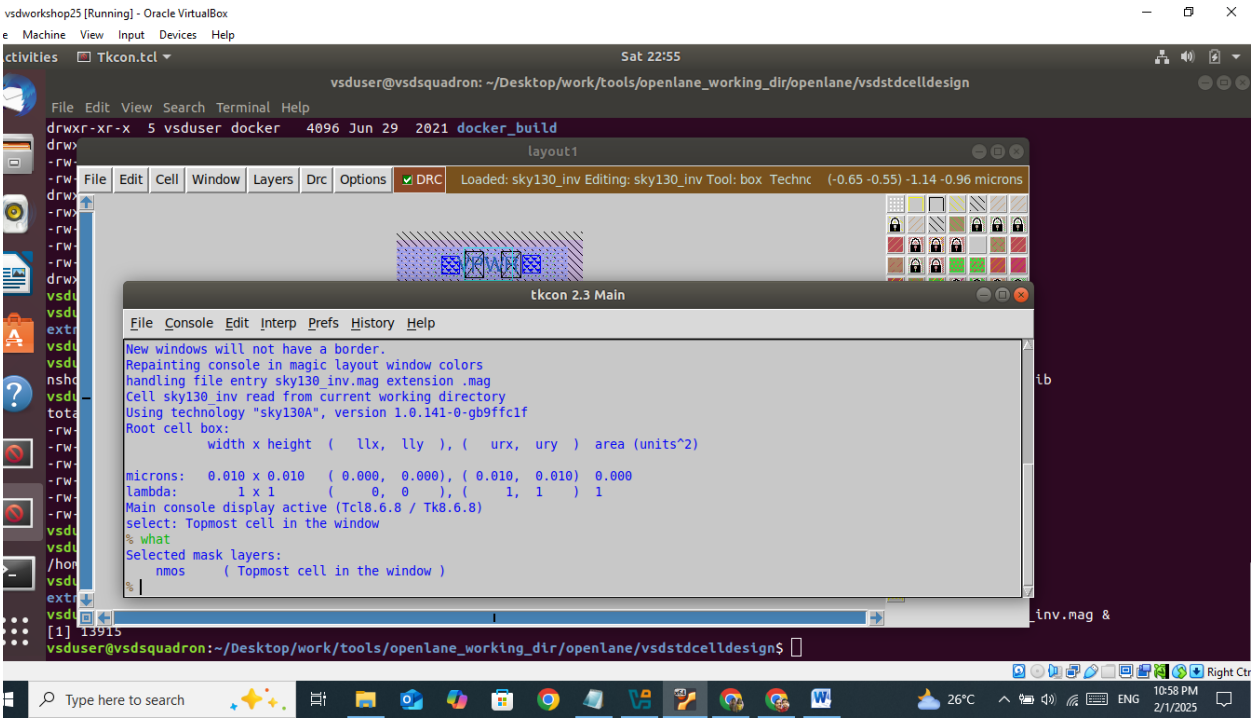
Day 3

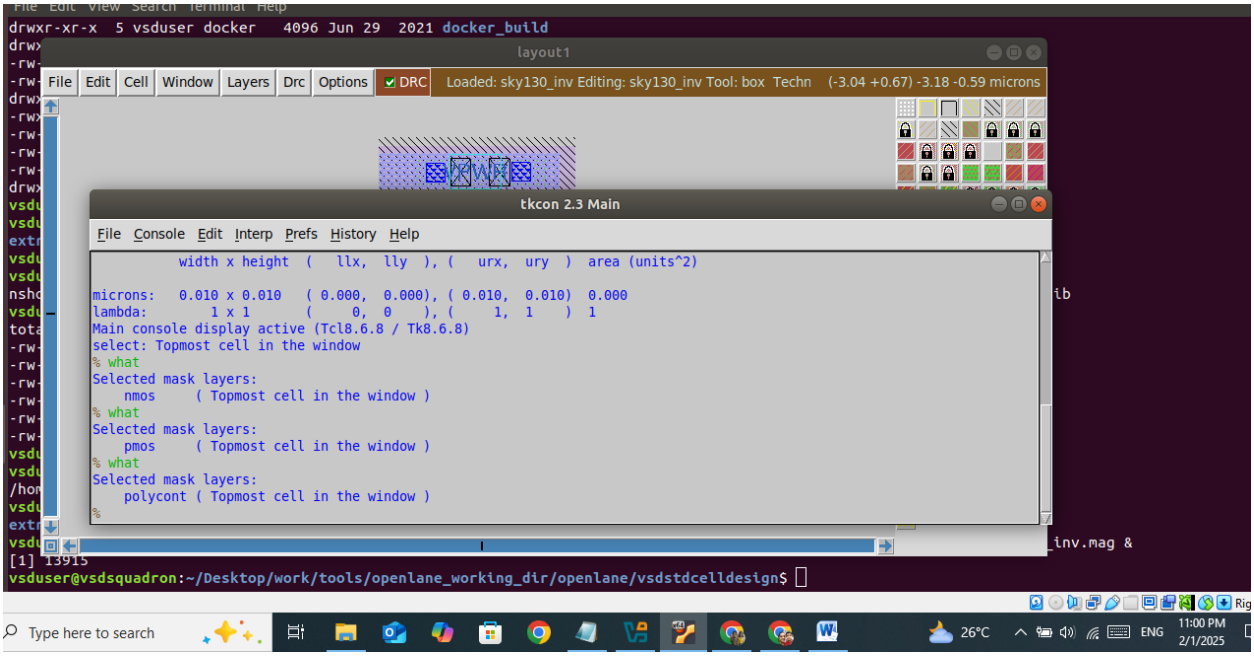
Lab

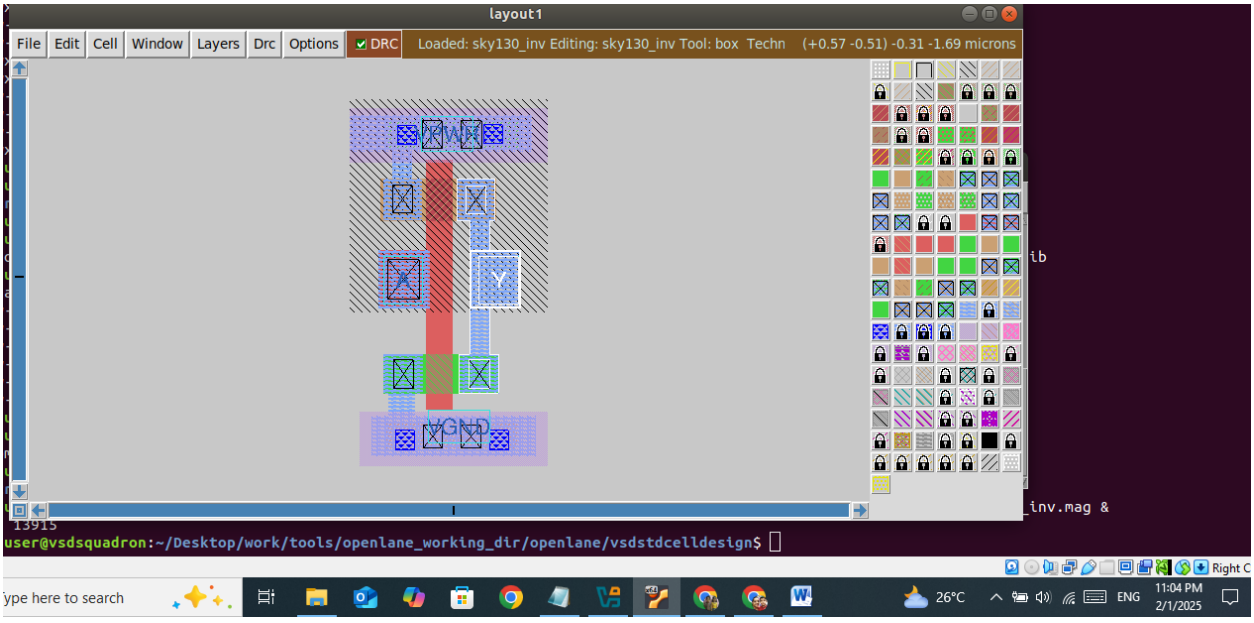

layout1
File
Edit
Cell
Window
Layers
Drc
Options
DRC
Loaded: read Editing: read Tool: box Technology:
(+3.65 +334.18) +18.72 +60.78 microns
picorv32a
Topmost cell in the window

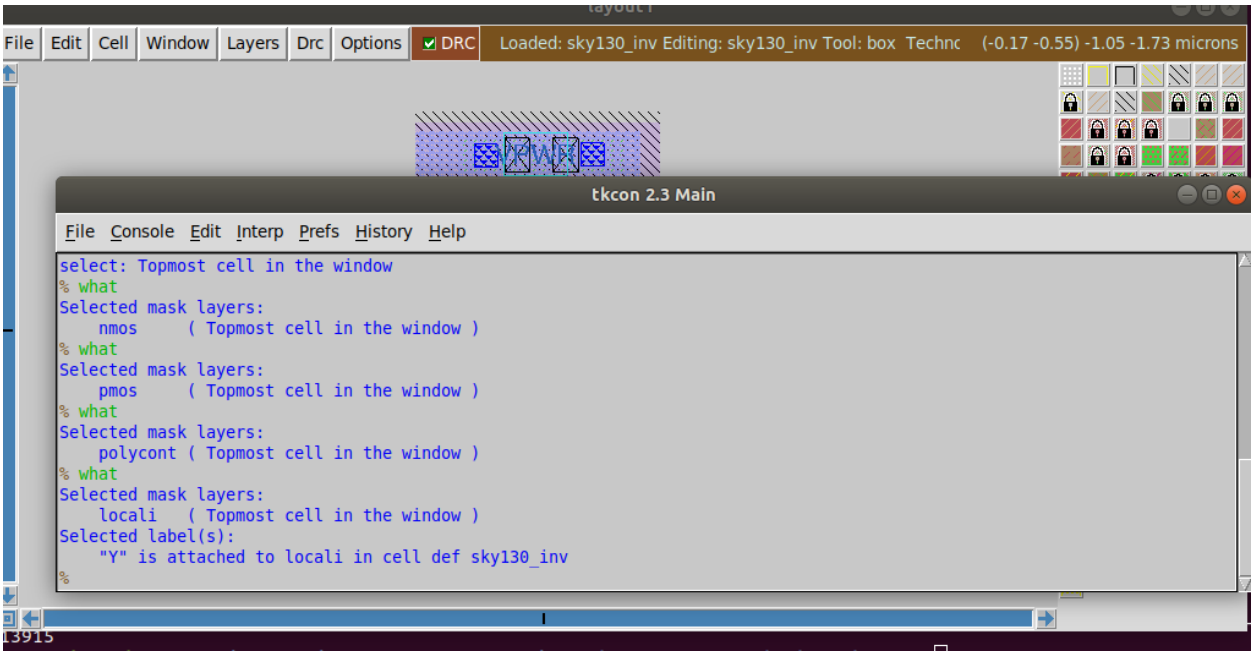

Terminal
Sat 22:11
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
File Edit View Search Terminal Help
drwxr-xr-x 44 vsduser docker 4096 Jun 29 2021 designs
-rw-r--r-- 1 vsduser docker 1285 Jun 29 2021 CONTRIBUTING.md
-rw-r--r-- 1 vsduser docker 5514 Jun 29 2021 conf.py
drwxr-xr-x 2 vsduser docker 4096 Jun 29 2021 configuration
-rwxr-xr-x 1 vsduser docker 966 Jun 29 2021 clean_runs.tcl
-rw-r--r-- 1 vsduser docker 709 Jun 29 2021 AUTHORS.md
-rw-r--r-- 1 vsduser vsduser 963 May 20 2023 default.cvcrc
-rw-r--r-- 1 vsduser docker 25522 Feb 1 09:39 README.md
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ git clone https://github.com/nickson-jose/vsdstdcelldesign.git
Cloning into 'vsdstdcelldesign'...
remote: Enumerating objects: 492, done.
remote: Counting objects: 100% (18/18), done.
remote: Compressing objects: 100% (18/18), done.
remote: Total 492 (delta 7), reused 0 (delta 0), pack-reused 474 (from 1)
Receiving objects: 100% (492/492), 24.08 MiB | 6.71 MiB/s, done.
Resolving deltas: 100% (210/210), done.
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ ls -lrt
total 140
drwxr-xr-x 15 vsduser docker 4096 Jun 29 2021 scripts
-rw-r--r-- 1 vsduser docker 20787 Jun 29 2021 run_designs.py
-rw-r--r-- 1 vsduser docker 7898 Jun 29 2021 report_generation_wrapper.py
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 regression_results
-rw-r--r-- 1 vsduser docker 7273 Jun 29 2021 Makefile
-rw-r--r-- 1 vsduser docker 11350 Jun 29 2021 LICENSE
-rwxr-xr-x 1 vsduser docker 6519 Jun 29 2021 flow.tcl
drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docs
drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docker_build
drwxr-xr-x 44 vsduser docker 4096 Jun 29 2021 designs
-rw-r--r-- 1 vsduser docker 1285 Jun 29 2021 CONTRIBUTING.md
-rw-r--r-- 1 vsduser docker 5514 Jun 29 2021 conf.py
drwxr-xr-x 2 vsduser docker 4096 Jun 29 2021 configuration
-rwxr-xr-x 1 vsduser docker 966 Jun 29 2021 clean_runs.tcl
Type here to search
27°C
ENG
10:11 PM
2/1/2025

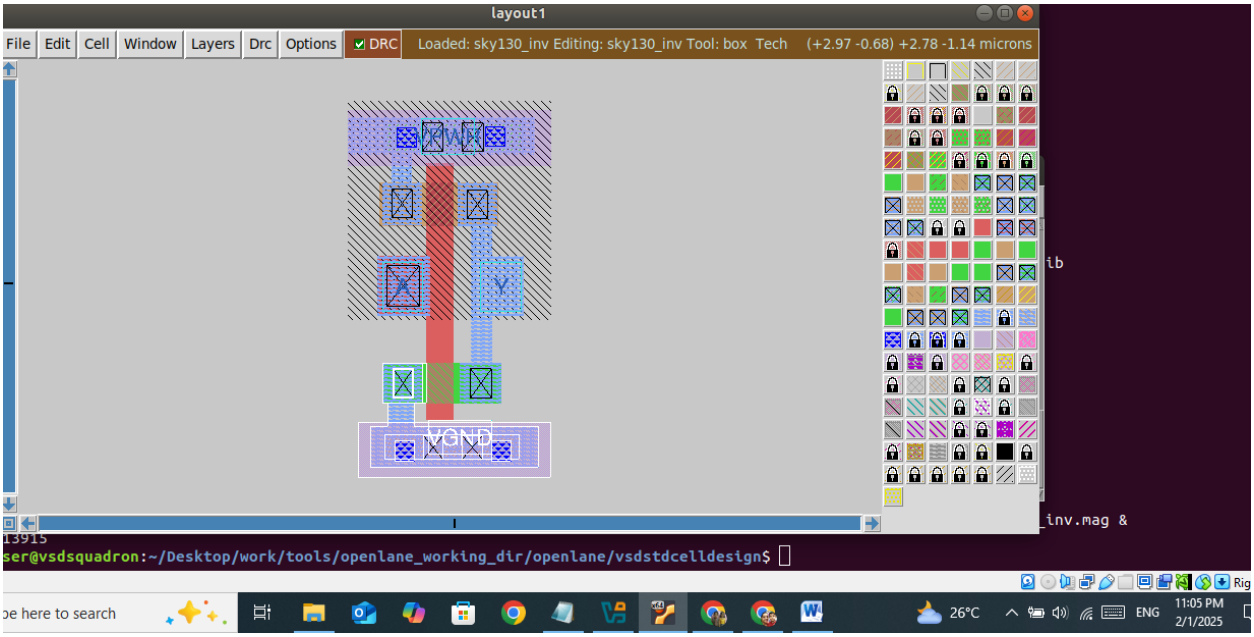

Machine View Input Devices Help
Activities
Toplevel
Sat 22:14
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
File Edit View Search Terminal Help
drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docker_build
layout1
File Edit Cell Window Layers Drc Options DRC
Loaded: sky130_inv Editing: sky130_inv Tool: box Tech (+1.33 -0.61) +1.53 -0.37 microns
sky130_inv
VGND
Topmost cell in the window
inv.mag &
[1] 13915
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
Type here to search
27°C
ENG
10:14 PM
2/1/2025

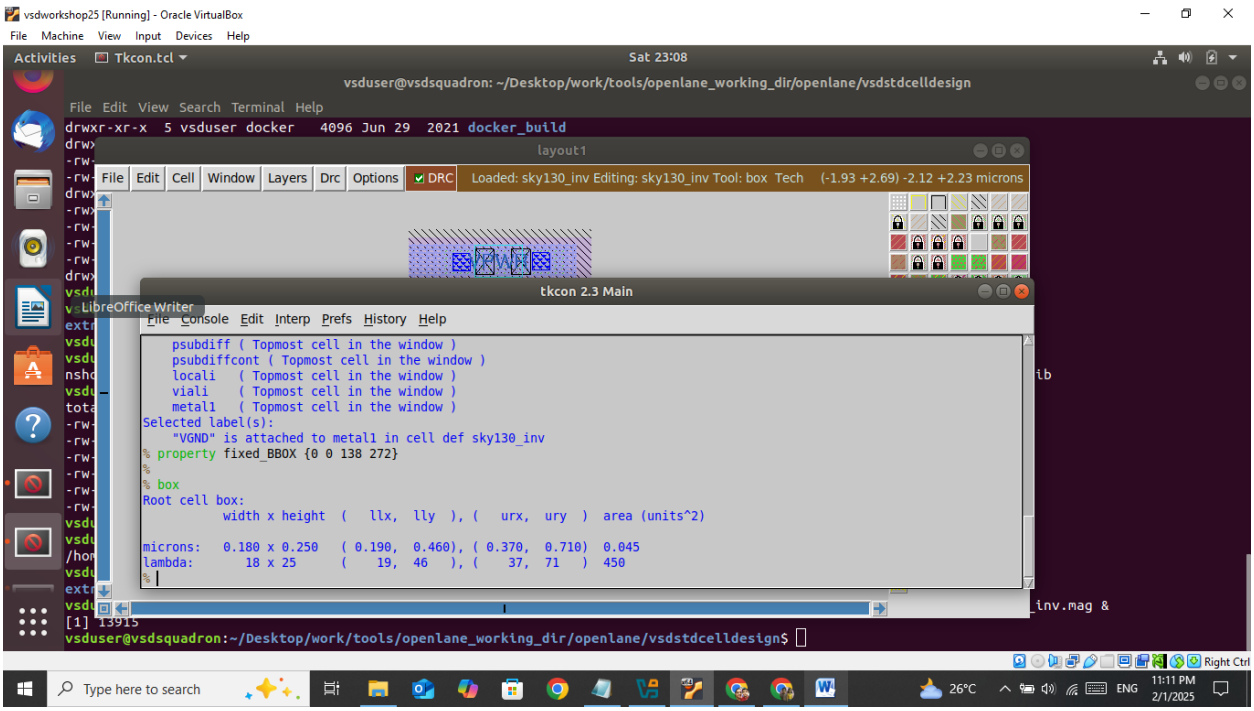

vsdworkshop25 [Running] - Oracle VirtualBox
Machine View Input Devices Help
Activities
Tkcon.tcl
Sat 22:55
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
File Edit View Search Terminal Help
drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docker_build
layout1
File Edit Cell Window Layers Drc Options DRC
Loaded: sky130_inv Editing: sky130_inv Tool: box Techno (-0.65 -0.55) -1.14 -0.96 microns
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
New windows will not have a border.
Repainting console in magic layout window colors
handling file entry sky130_inv.mag extension .mag
Cell sky130_inv read from current working directory
Using technology "sky130A", version 1.0.141-0-gb9ffc1f
Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)
microns: 0.010 x 0.010 (0.000, 0.000), (0.010, 0.010) 0.000
lambda: 1 x 1 (0, 0), (1, 1) 1
Main console display active (Tcl8.6.8 / Tk8.6.8)
select: Topmost cell in the window
% what
Selected mask layers:
nmos (Topmost cell in the window)
% |
inv.mag &
[1] 13915
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
Type here to search
26°C
ENG
10:58 PM
2/1/2025

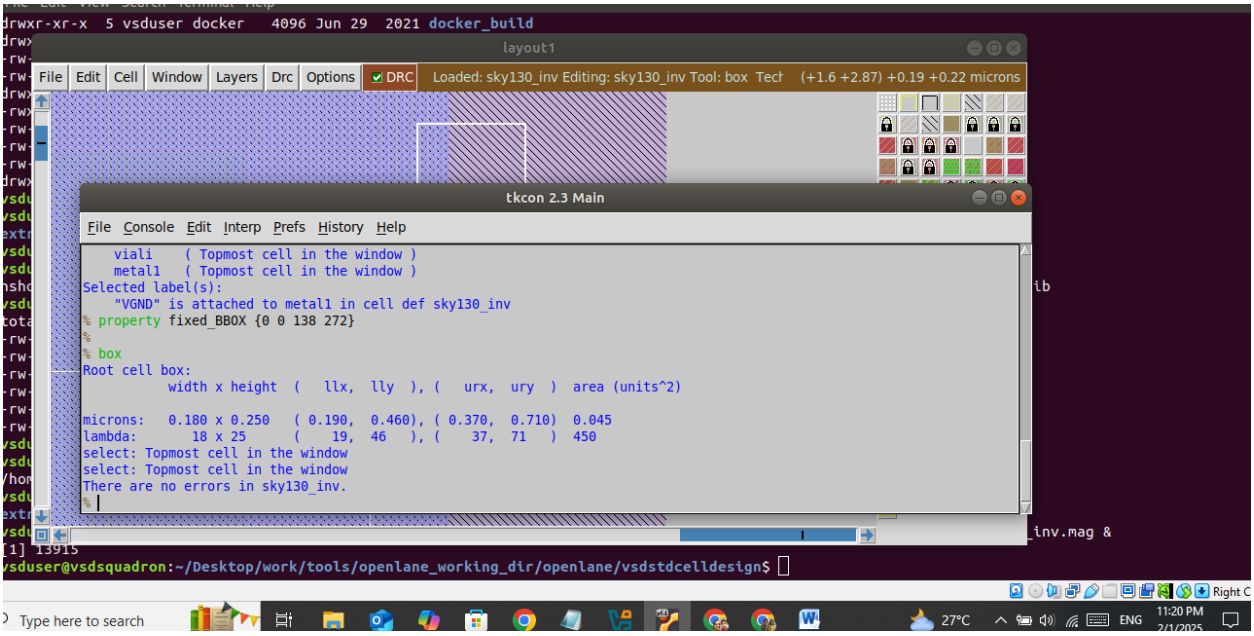

drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docker_build
layout1
File Edit Cell Window Layers Drc Options DRC Loaded: sky130_inv Editing: sky130_inv Tool: box Techn (-3.04 +0.67) -3.18 -0.59 microns
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
width x height (llx, lly), (urx, ury) area (units^2)
microns: 0.010 x 0.010 (0.000, 0.000), (0.010, 0.010) 0.000
lambda: 1 x 1 (0, 0), (1, 1) 1
Main console display active (Tcl8.6.8 / Tk8.6.8)
select: Topmost cell in the window
% what
Selected mask layers:
nmos (Topmost cell in the window)
% what
Selected mask layers:
pmos (Topmost cell in the window)
% what
Selected mask layers:
polycont (Topmost cell in the window)
%
[1] 13915
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
Type here to search
26°C
ENG
11:00 PM
2/1/2025

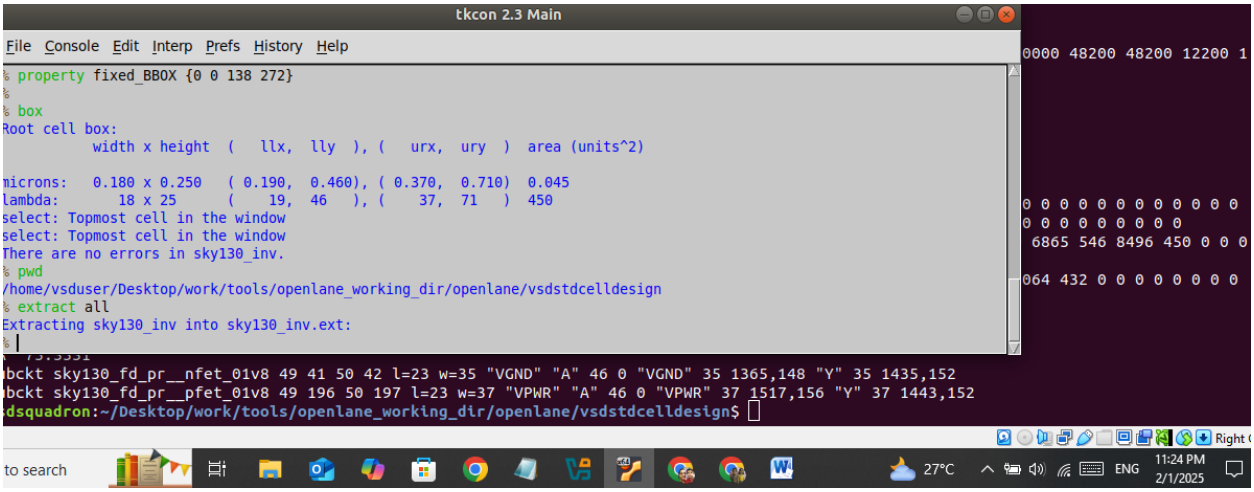

layout1
File Edit Cell Window Layers Drc Options DRC Loaded: sky130_inv Editing: sky130_inv Tool: box Techn (+0.57 -0.51) -0.31 -1.69 microns
VPWR
A
Y
VGND
inv.mag &
user@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
26°C
ENG
11:04 PM
2/1/2025

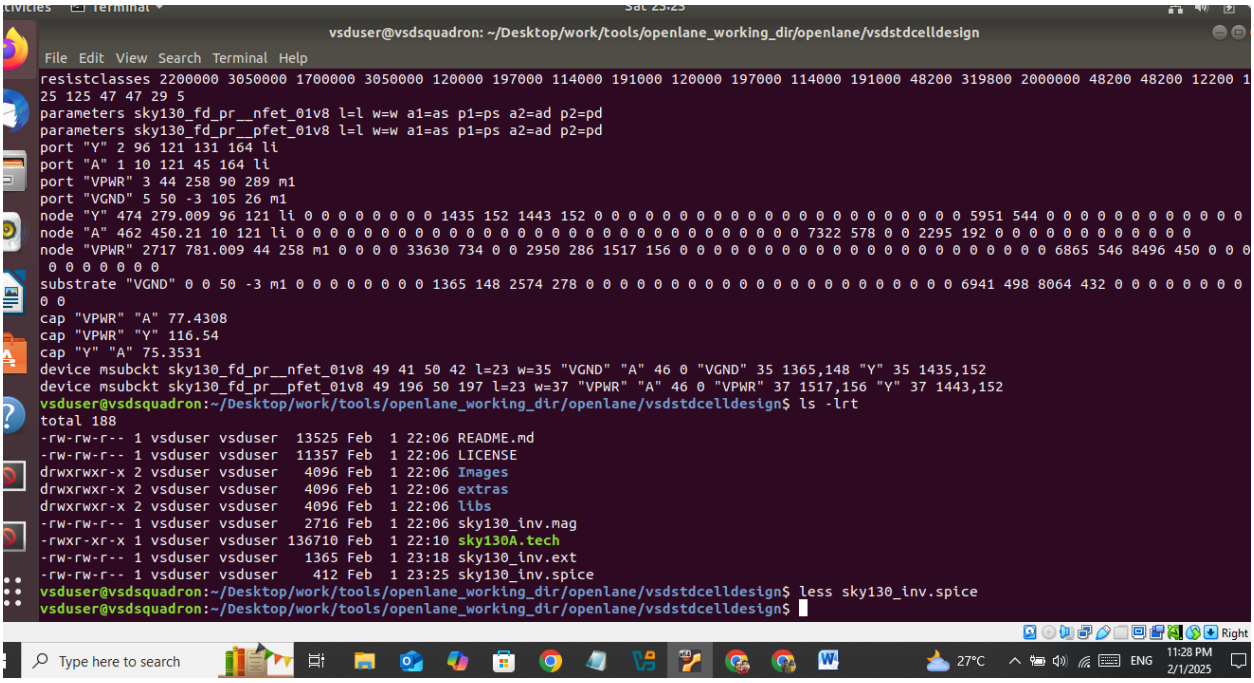

File Edit Cell Window Layers Drc Options DRC
Loaded: sky130_inv Editing: sky130_inv Tool: box Techno
(-0.17 -0.55) -1.05 -1.73 microns
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
select: Topmost cell in the window
% what
Selected mask layers:
nmos (Topmost cell in the window)
% what
Selected mask layers:
pmos (Topmost cell in the window)
% what
Selected mask layers:
polycont (Topmost cell in the window)
% what
Selected mask layers:
locali (Topmost cell in the window)
Selected label(s):
"Y" is attached to locali in cell def sky130_inv
%


layout1
File Edit Cell Window Layers Drc Options DRC
Loaded: sky130_inv Editing: sky130_inv Tool: box Tech
(+2.97 -0.68) +2.78 -1.14 microns
A
Y
VGND
ib
inv.mag &
ser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
26°C
ENG
11:05 PM
2/1/2025


vsdworkshop25 [Running] - Oracle VirtualBox
File Machine View Input Devices Help
Activities
Tkcon.tcl
Sat 23:08
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
File Edit View Search Terminal Help
drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docker_build
layout1
File Edit Cell Window Layers Drc Options DRC
Loaded: sky130_inv Editing: sky130_inv Tool: box Tech (-1.93 +2.69) -2.12 +2.23 microns
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
psubdiff (Topmost cell in the window)
psubdiffcont (Topmost cell in the window)
locali (Topmost cell in the window)
viali (Topmost cell in the window)
metal1 (Topmost cell in the window)
Selected label(s):
"VGND" is attached to metal1 in cell def sky130_inv
% property fixed_BBOX {0 0 138 272}
%
% box
Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)
microns: 0.180 x 0.250 (0.190, 0.460), (0.370, 0.710) 0.045
lambda: 18 x 25 (19, 46), (37, 71) 450
%
LibreOffice Writer
[1] 13915
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
Type here to search
26°C
ENG
11:11 PM
2/1/2025


drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docker_build
layout1
File Edit Cell Window Layers Drc Options DRC
Loaded: sky130_inv Editing: sky130_inv Tool: box Tech (+1.6 +2.87) +0.19 +0.22 microns
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
viali (Topmost cell in the window)
metal1 (Topmost cell in the window)
Selected label(s):
"VGND" is attached to metal1 in cell def sky130_inv
% property fixed_BBOX {0 0 138 272}
%
% box
Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)
microns: 0.180 x 0.250 (0.190, 0.460), (0.370, 0.710) 0.045
lambda: 18 x 25 (19, 46), (37, 71) 450
select: Topmost cell in the window
select: Topmost cell in the window
There are no errors in sky130_inv.
%
[1] 13915
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
Type here to search
27°C
ENG
11:20 PM


tkcon 2.3 Main
File Console Edit Interp Prefs History Help
% property fixed_BBOX {0 0 138 272}
%
% box
Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)
microns: 0.180 x 0.250 (0.190, 0.460), (0.370, 0.710) 0.045
lambda: 18 x 25 (19, 46), (37, 71) 450
select: Topmost cell in the window
select: Topmost cell in the window
There are no errors in sky130_inv.
% pwd
/home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
% extract all
Extracting sky130_inv into sky130_inv.ext:
% 75.3531
bckt sky130_fd_pr__nfet_01v8 49 41 50 42 l=23 w=35 "VGND" "A" 46 0 "VGND" 35 1365,148 "Y" 35 1435,152
bckt sky130_fd_pr__pfet_01v8 49 196 50 197 l=23 w=37 "VPWR" "A" 46 0 "VPWR" 37 1517,156 "Y" 37 1443,152
dsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
0000 48200 48200 12200 1
0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0
6865 546 8496 450 0 0 0
064 432 0 0 0 0 0 0 0 0
to search
27°C
ENG
11:24 PM
2/1/2025


vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
File Edit View Search Terminal Help
resistclasses 2200000 3050000 1700000 3050000 120000 197000 114000 191000 120000 197000 114000 191000 48200 319800 2000000 48200 48200 12200 1
25 125 47 47 29 5
parameters sky130_fd_pr__nfet_01v8 l=l w=w a1=as p1=ps a2=ad p2=pd
parameters sky130_fd_pr__pfet_01v8 l=l w=w a1=as p1=ps a2=ad p2=pd
port "Y" 2 96 121 131 164 li
port "A" 1 10 121 45 164 li
port "VPWR" 3 44 258 90 289 m1
port "VGND" 5 50 -3 105 26 m1
node "Y" 474 279.009 96 121 li 0 0 0 0 0 0 0 0 1435 152 1443 152 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 5951 544 0 0 0 0 0 0 0 0 0 0
node "A" 462 450.21 10 121 li 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 7322 578 0 0 2295 192 0 0 0 0 0 0 0 0 0 0
node "VPWR" 2717 781.009 44 258 m1 0 0 0 0 33630 734 0 0 2950 286 1517 156 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 6865 546 8496 450 0 0 0
0 0 0 0 0 0 0
substrate "VGND" 0 0 50 -3 m1 0 0 0 0 0 0 0 0 1365 148 2574 278 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 6941 498 8064 432 0 0 0 0 0 0 0 0
0 0
cap "VPWR" "A" 77.4308
cap "VPWR" "Y" 116.54
cap "Y" "A" 75.3531
device msubckt sky130_fd_pr__nfet_01v8 49 41 50 42 l=23 w=35 "VGND" "A" 46 0 "VGND" 35 1365,148 "Y" 35 1435,152
device msubckt sky130_fd_pr__pfet_01v8 49 196 50 197 l=23 w=37 "VPWR" "A" 46 0 "VPWR" 37 1517,156 "Y" 37 1443,152
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -lrt
total 188
-rw-rw-r-- 1 vsduser vsduser 13525 Feb 1 22:06 README.md
-rw-rw-r-- 1 vsduser vsduser 11357 Feb 1 22:06 LICENSE
drwxrwxr-x 2 vsduser vsduser 4096 Feb 1 22:06 Images
drwxrwxr-x 2 vsduser vsduser 4096 Feb 1 22:06 extras
drwxrwxr-x 2 vsduser vsduser 4096 Feb 1 22:06 libs
-rw-rw-r-- 1 vsduser vsduser 2716 Feb 1 22:06 sky130_inv.mag
-rwxr-xr-x 1 vsduser vsduser 136710 Feb 1 22:10 sky130A.tech
-rw-rw-r-- 1 vsduser vsduser 1365 Feb 1 23:18 sky130_inv.ext
-rw-rw-r-- 1 vsduser vsduser 412 Feb 1 23:25 sky130_inv.spice
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ less sky130_inv.spice
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
Type here to search
27°C
ENG
11:28 PM
2/1/2025

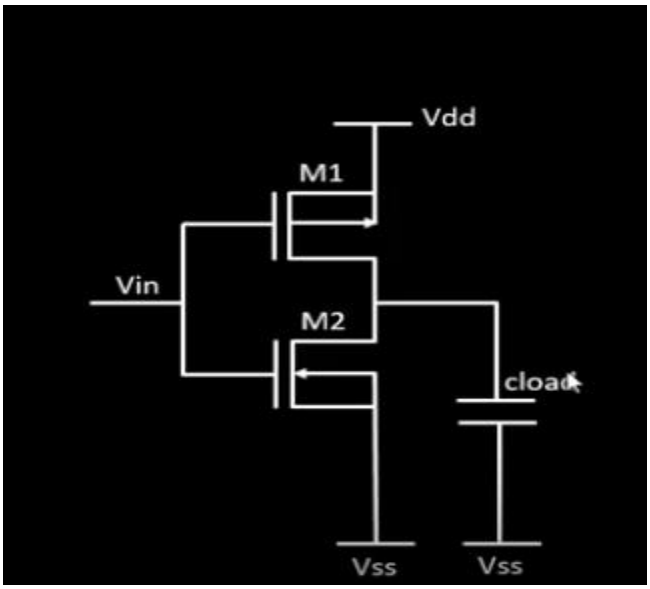
```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ less sky130_inv.spice
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ vim sky130_inv.spice
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cat sky130_inv.spice
* SPICE3 file created from sky130_inv.ext - technology: sky130A

.option scale=10n

.subckt sky130_inv A Y VPWR VGND
X0 Y A VGND VGND sky130_fd_pr__nfet_01v8 ad=1.43k pd=152 as=1.37k ps=148 w=3.5e+07 l=2.3e+07
X1 Y A VPWR VPWR sky130_fd_pr__pfet_01v8 ad=1.44k pd=152 as=1.52k ps=156 w=3.7e+07 l=2.3e+07
C0 VPWR A 0.0774f
C1 Y A 0.0754f
C2 VPWR Y 0.117f
C3 Y VGND 0.279f
C4 A VGND 0.45f
C5 VPWR VGND 0.781f
.ends
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ vim sky130_inv.spice
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```



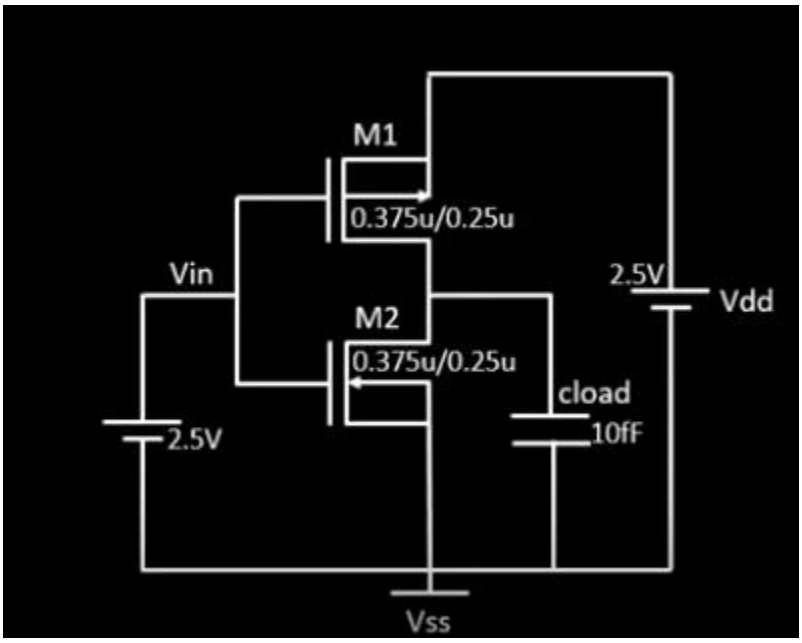
```
exttospice finished.
% box
Root cell box:
          width x height  (   llx,  lly  ), (   urx,  ury  )  area (units^2)

microns:   0.170 x 0.200   ( 0.680,  1.430), ( 0.850,  1.630)  0.034
lambda:       17 x 20      (    68,  143  ), (    85,  163  )  340
%
vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ vim sky130_inv.spice
vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```


Spice deck

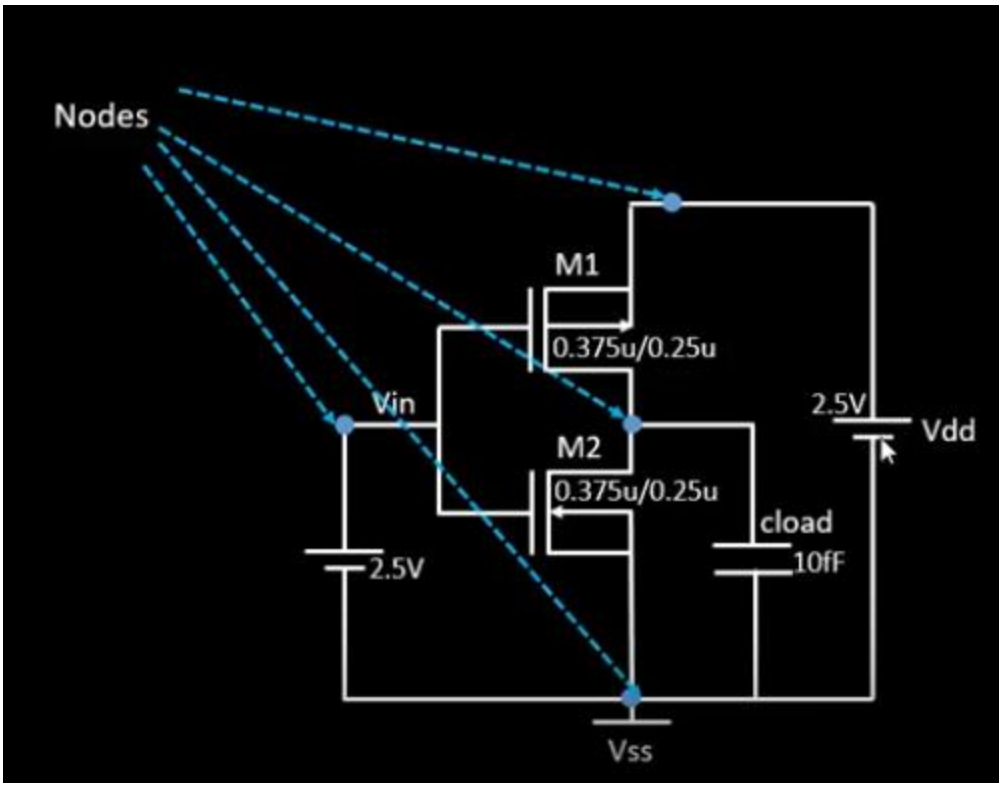
1)Component connectivity.



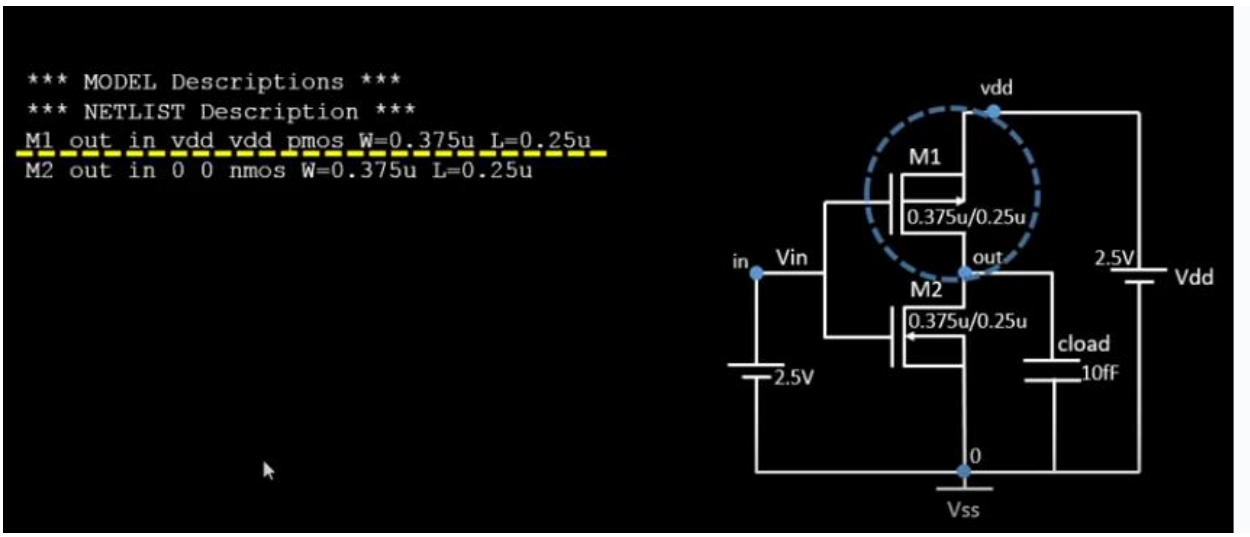
2)Component values



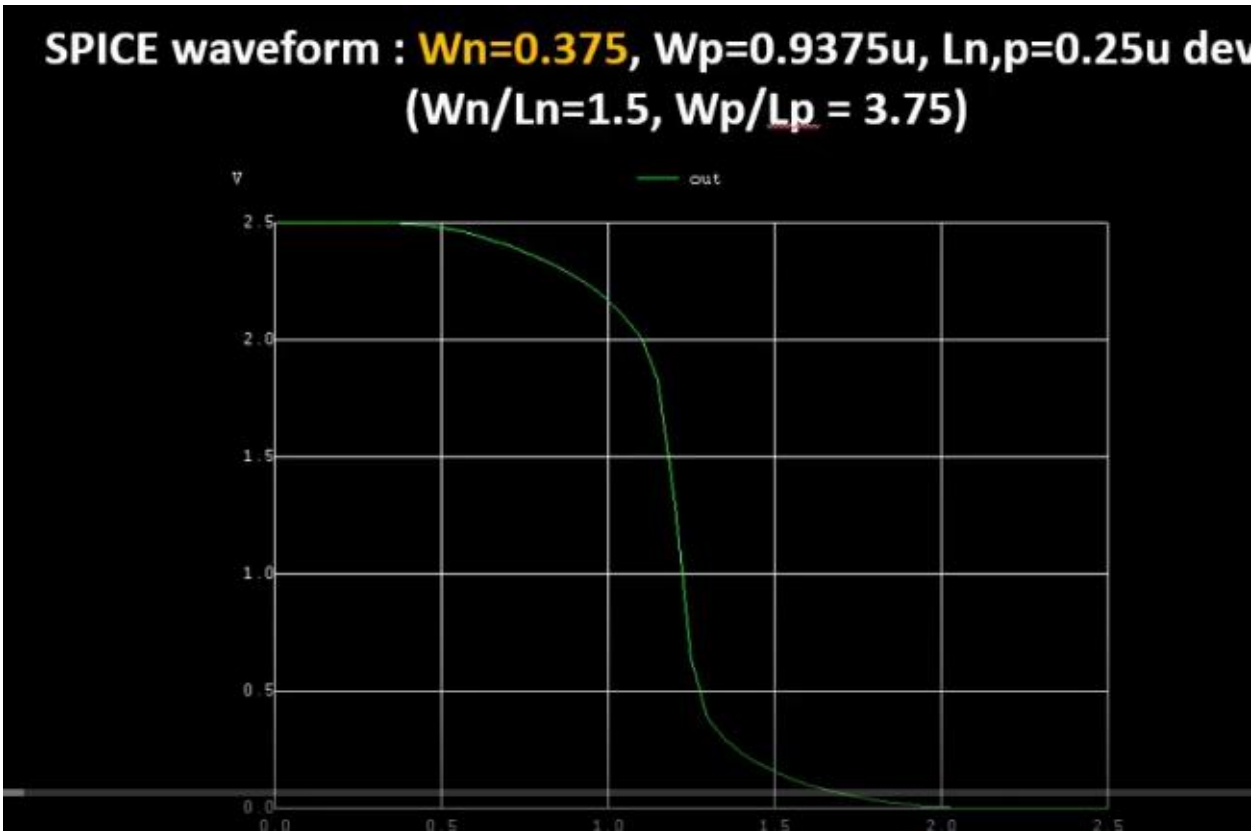
3)Identify nodes:

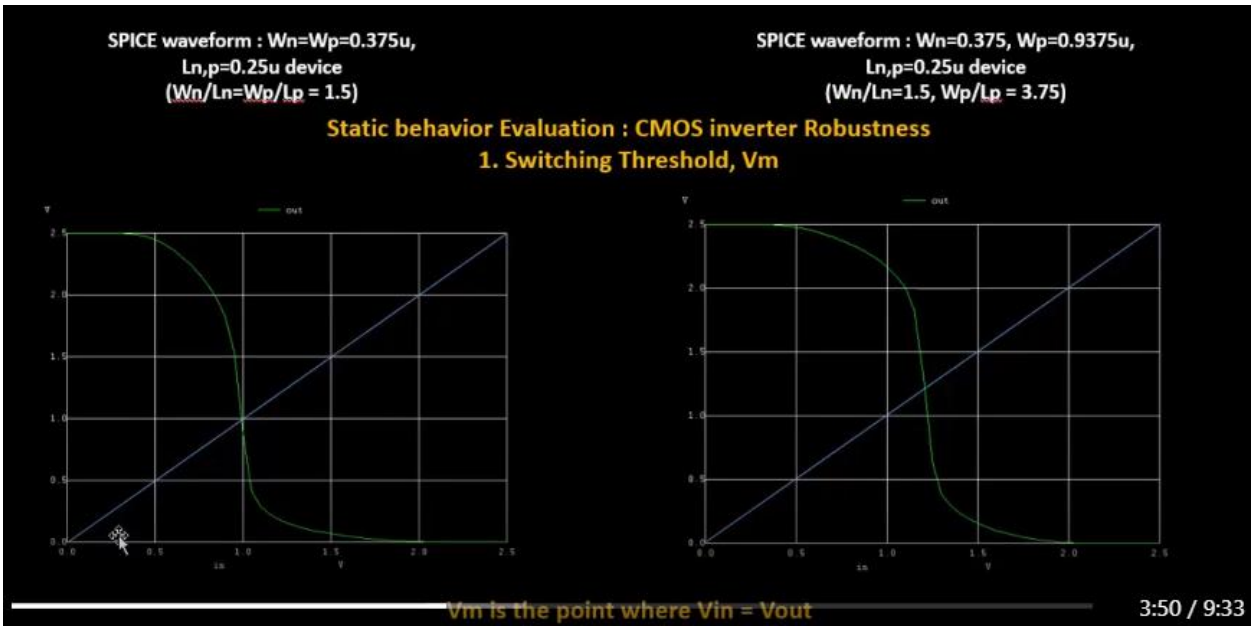

Nodes
M1
0.375u/0.25u
Vin
2.5V
Vdd
M2
0.375u/0.25u
cload
10fF
2.5V
Vss

4) Name ‘Nodes’


*** MODEL Descriptions ***
*** NETLIST Description ***
M1 out in vdd vdd pmos W=0.375u L=0.25u
M2 out in 0 0 nmos W=0.375u L=0.25u
vdd
M1
0.375u/0.25u
in
Vin
out
2.5V
Vdd
M2
0.375u/0.25u
cload
10fF
2.5V
0
Vss

Spice waveform

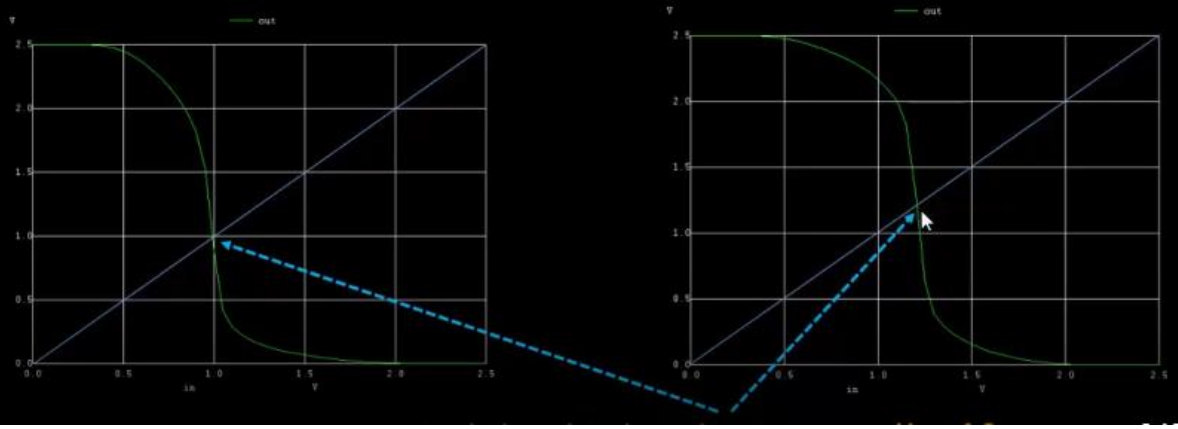




SPICE waveform : Wn=Wp=0.375u,
Ln,p=0.25u device
(Wn/Ln=Wp/Lp = 1.5)

SPICE waveform : Wn=0.375, Wp=0.9375u,
Ln,p=0.25u device
(Wn/Ln=1.5, Wp/Lp = 3.75)

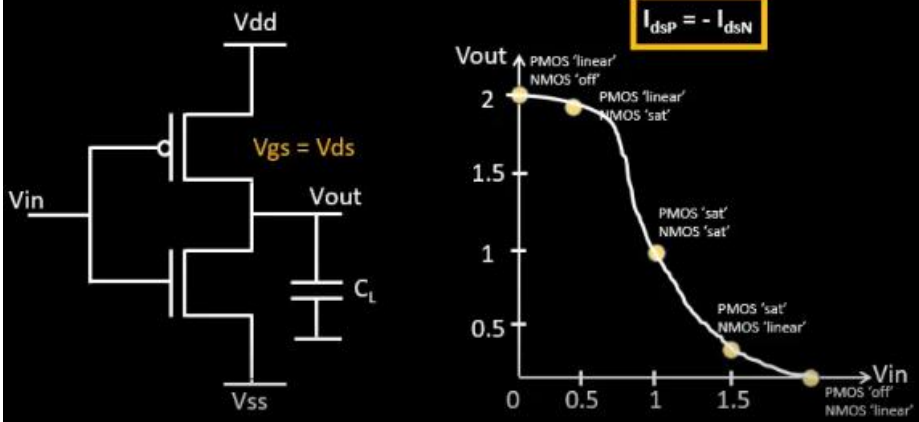
Static behavior Evaluation : CMOS inverter Robustness
1. Switching Threshold, Vm



SPICE waveform : Wn=Wp=0.375u,
Ln,p=0.25u device
(Wn/Ln=Wp/Lp = 1.5)

SPICE waveform : Wn=0.375, Wp=0.9375u,
Ln,p=0.25u device
(Wn/Ln=1.5, Wp/Lp = 3.75)

Static behavior Evaluation : CMOS inverter Robustness
1. Switching Threshold, Vm



Vm ~ 0.98v Vm is the point where Vin = Vout Vm ~ 1.2v

SPICE waveform : Wn=Wp=0.375u,
Ln,p=0.25u device
(Wn/Ln=Wp/Lp = 1.5)

SPICE waveform : Wn=0.375, Wp=0.9375u,
Ln,p=0.25u device
(Wn/Ln=1.5, Wp/Lp = 3.75)

Static behavior Evaluation : CMOS inverter Robustness

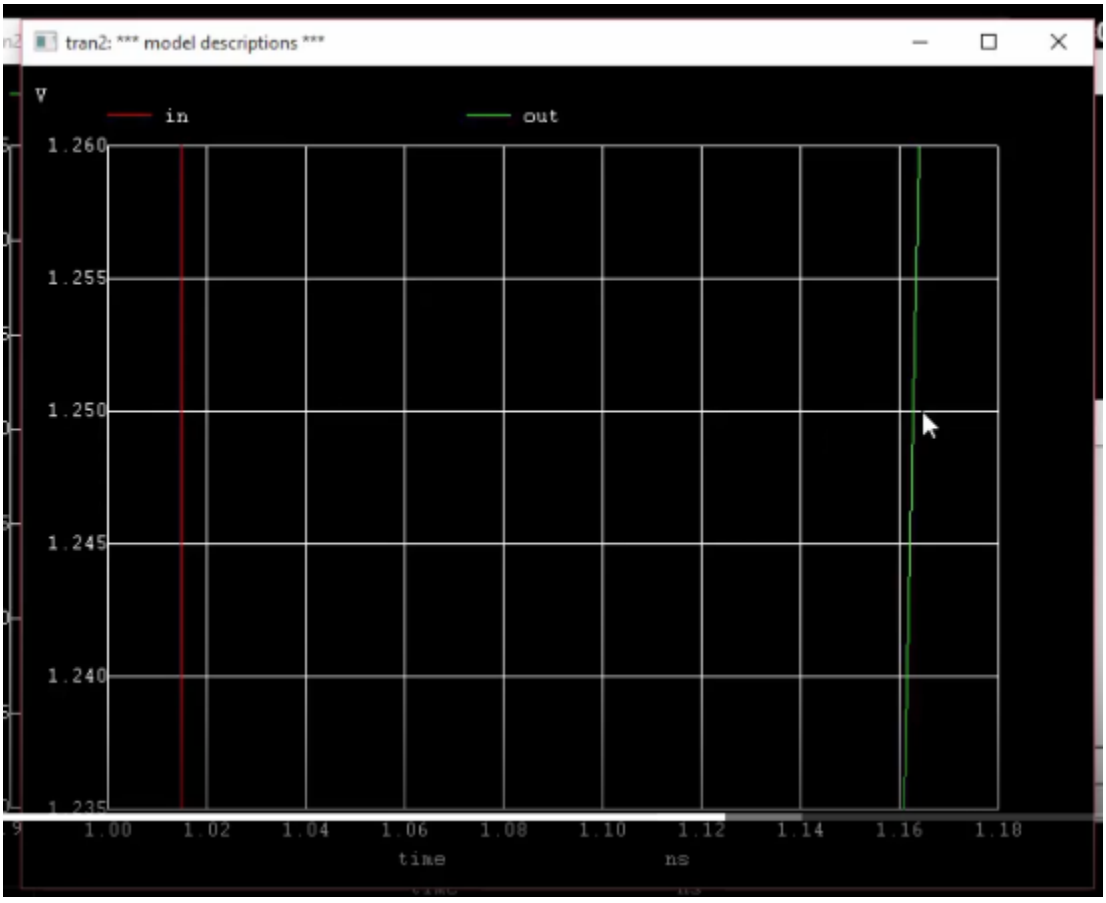
1. Switching Threshold, Vm

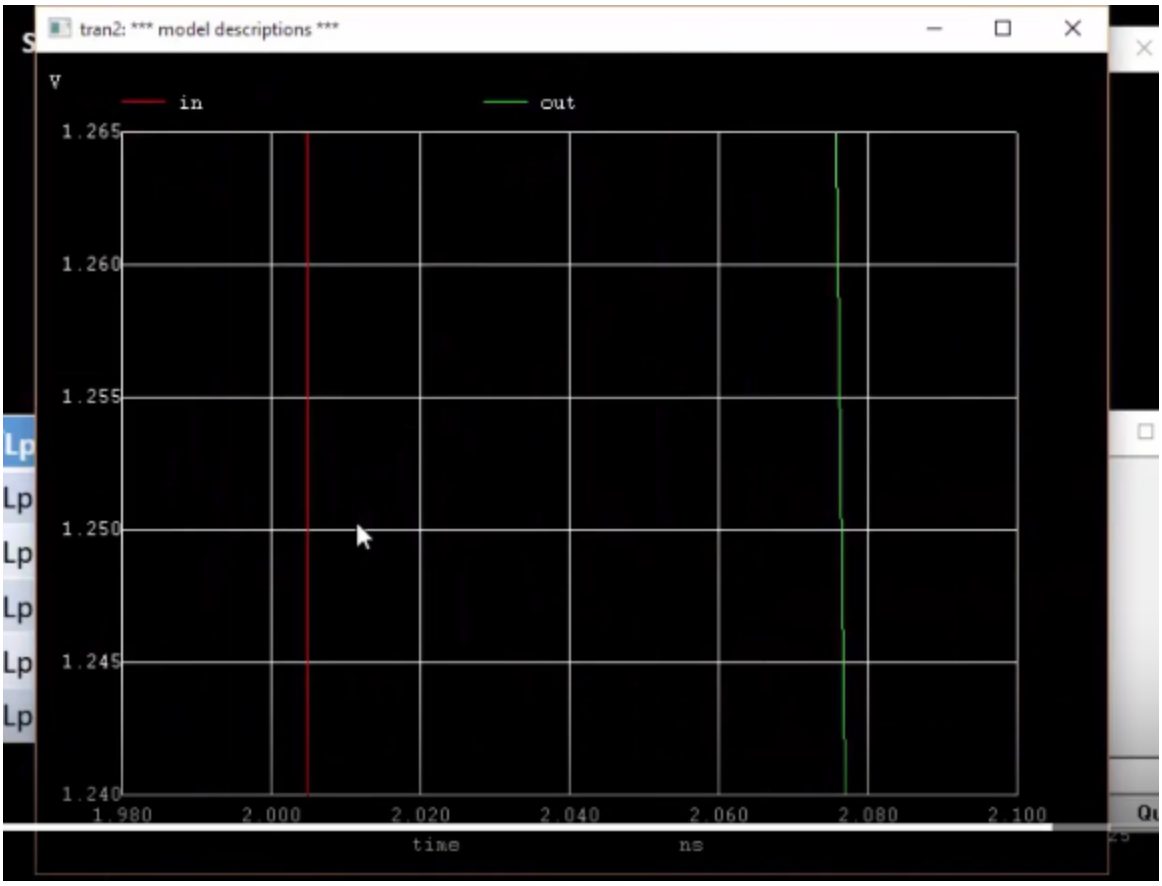
Wp/Lp	x.Wn/Ln
Wp/Lp	Wn/Ln
Wp/Lp	2Wn/Ln
Wp/Lp	3Wn/Ln
Wp/Lp	4Wn/Ln
Wp/Lp	5Wn/Ln

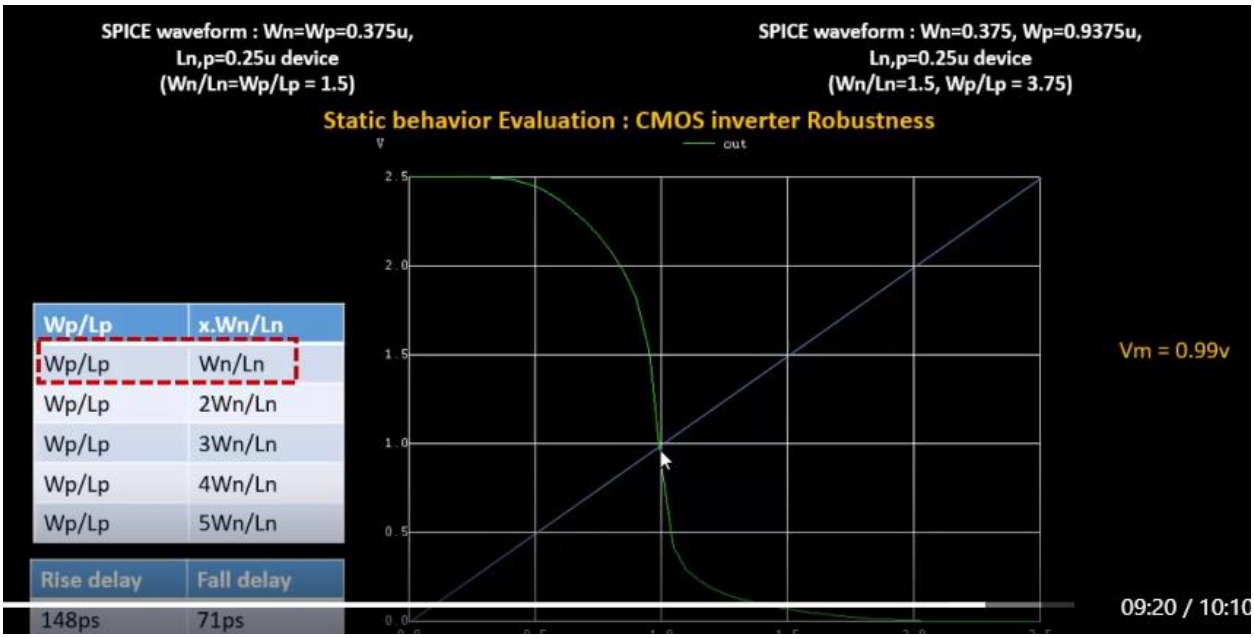
$$Vm = R \cdot Vdd / (1+R)$$

$$\text{Where } R = \frac{Kp \cdot Vdsatp}{Kn \cdot Vdsatn} = \frac{\left(\frac{Wp}{Lp}\right) Kp' \cdot Vdsatp}{\left(\frac{Wn}{Ln}\right) Kn' \cdot Vdsatn}$$

$$\frac{\left(\frac{Wp}{Lp}\right)}{\left(\frac{Wn}{Ln}\right)} = \frac{Kn' \cdot Vdsatn([Vm - Vt]) - \frac{Vdsatn}{2}}{Kp' \cdot Vdsatp([-Vm + Vdd + Vt]) + \frac{Vdsatp}{2}}$$




tran2: *** model descriptions ***
V
in
out
1.265
1.260
1.255
1.250
1.245
1.240
1.980
2.000
2.020
2.040
2.060
2.080
2.100
time
ns

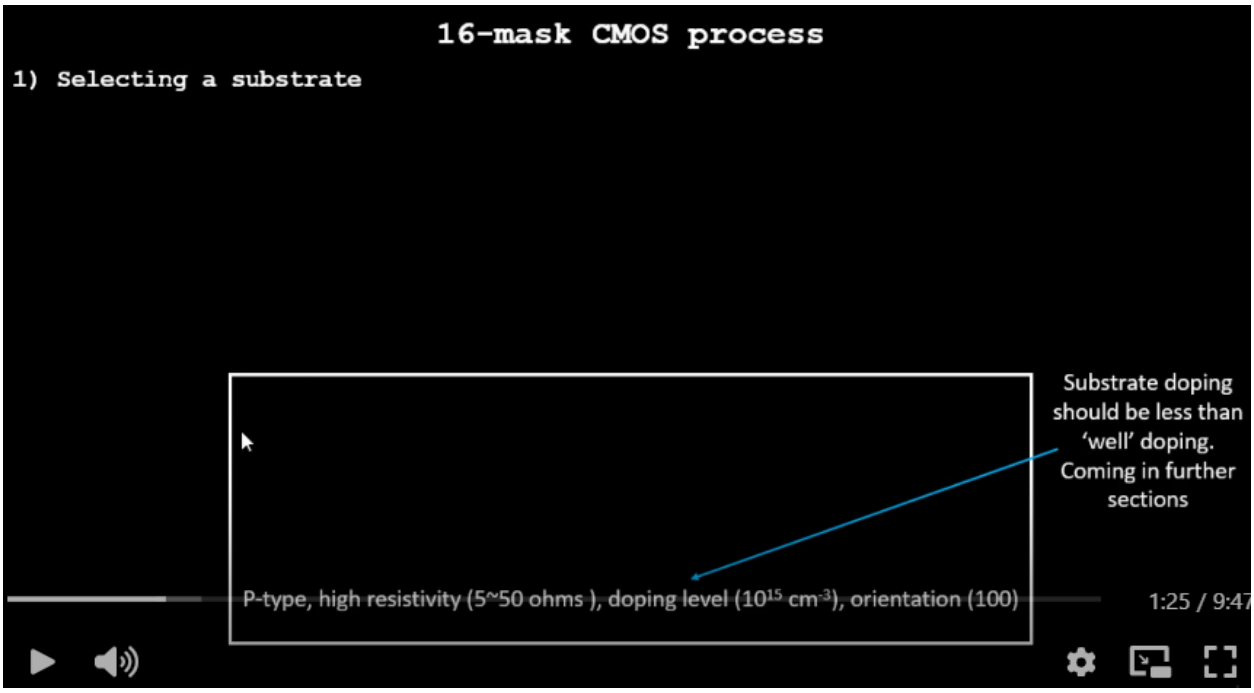

SPICE waveform : Wn=Wp=0.375u,
Ln,p=0.25u device
(Wn/Ln=Wp/Lp = 1.5)
SPICE waveform : Wn=0.375, Wp=0.9375u,
Ln,p=0.25u device
(Wn/Ln=1.5, Wp/Lp = 3.75)
Static behavior Evaluation : CMOS inverter Robustness
V
out
2.5
2.0
1.5
1.0
0.5
0.0
Wp/Lp
x.Wn/Ln
Wp/Lp
Wn/Ln
Wp/Lp
2Wn/Ln
Wp/Lp
3Wn/Ln
Wp/Lp
4Wn/Ln
Wp/Lp
5Wn/Ln
Rise delay
Fall delay
148ps
71ps
Vm = 0.99v
09:20 / 10:10

16-mask CMOS process.

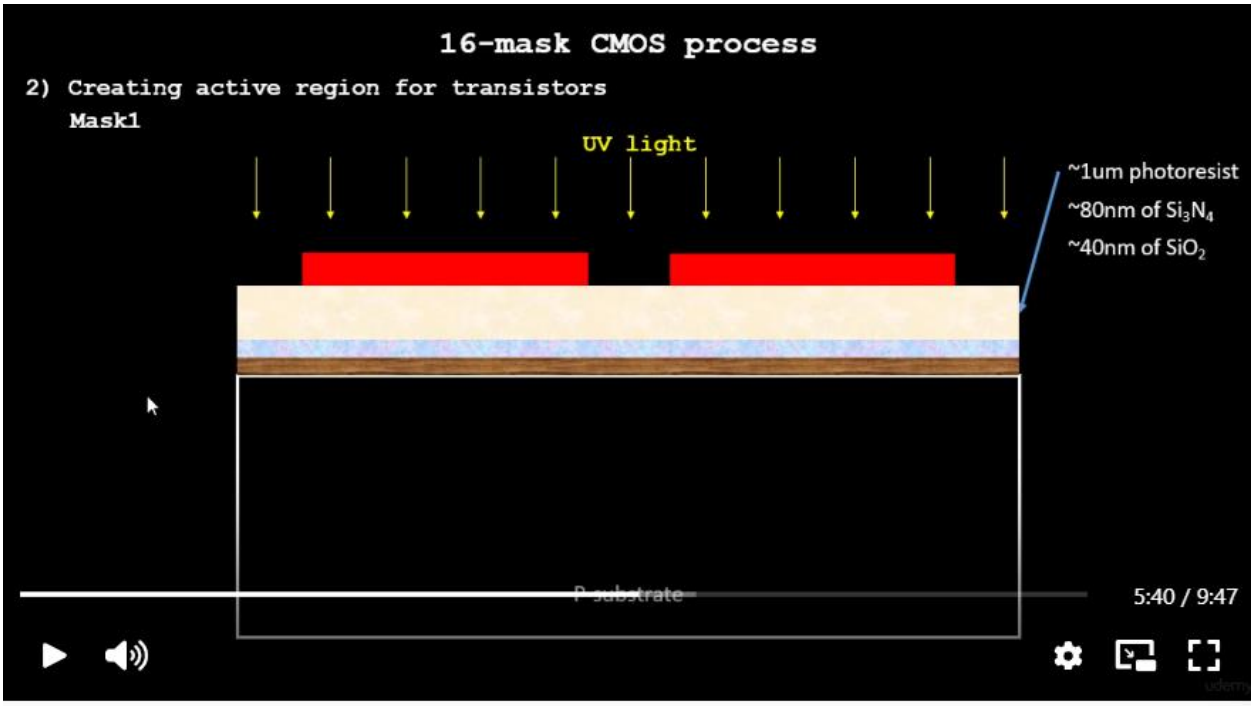
1) Selecting a substrate

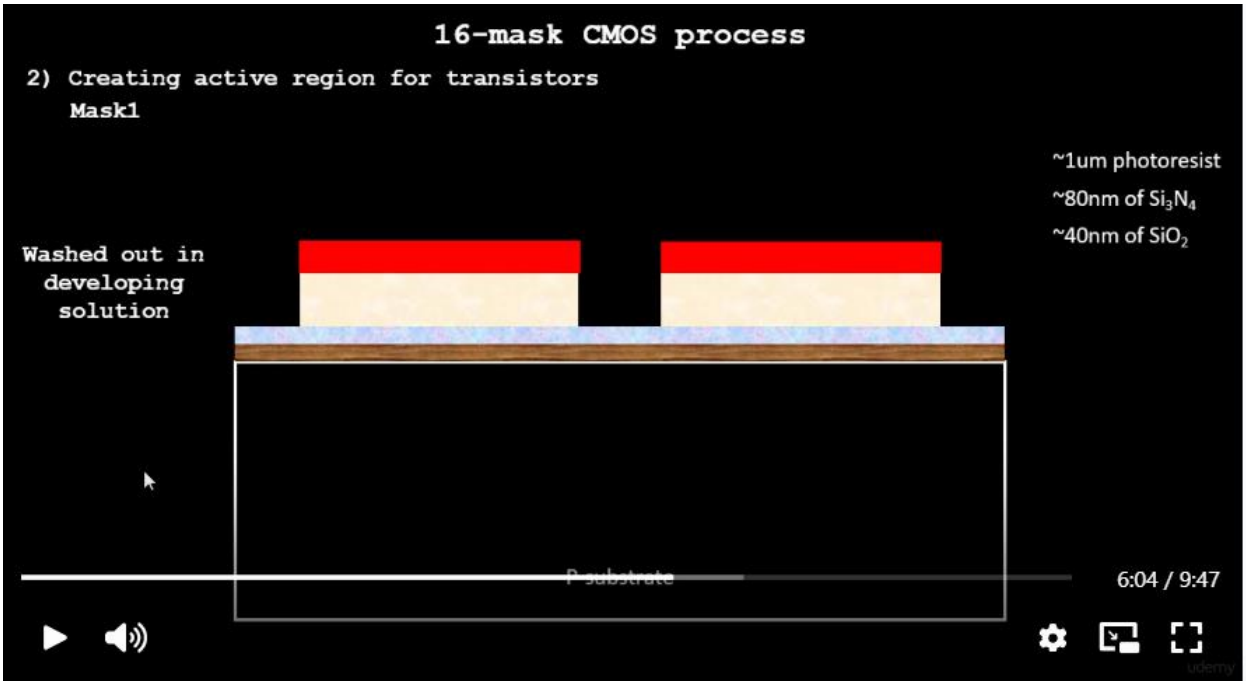
i) Doping level

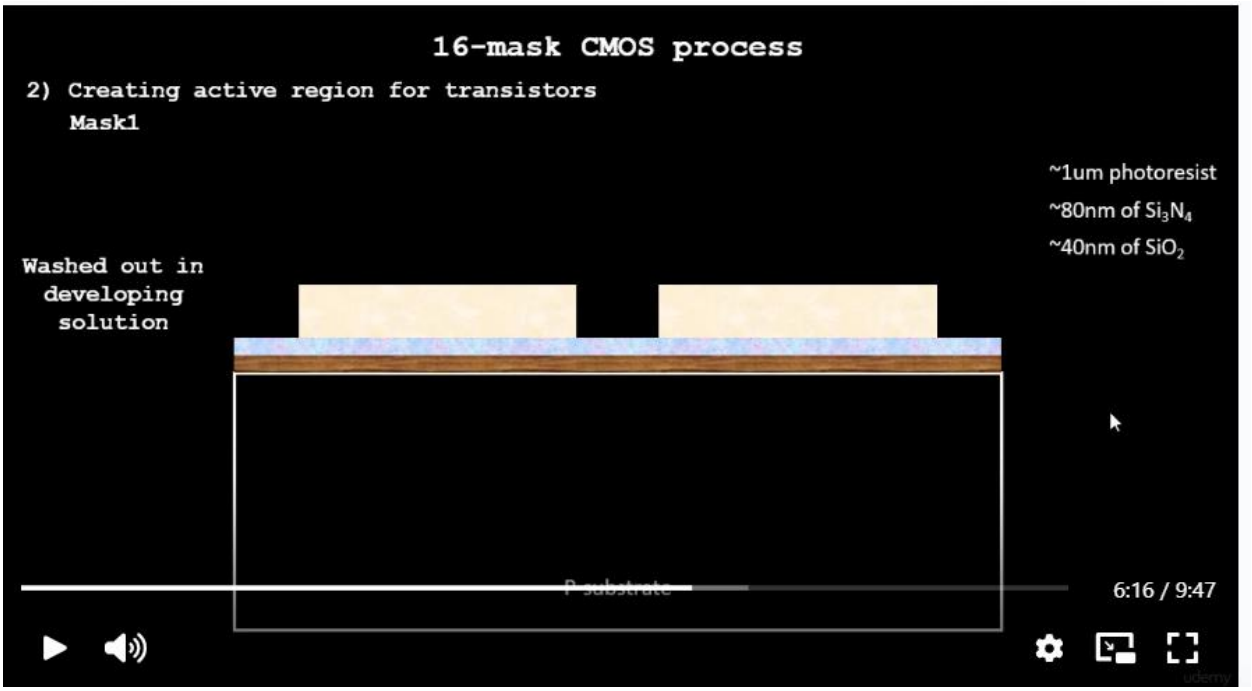
Substrate doping should be less than ‘well’ doping. Coming in further sections.

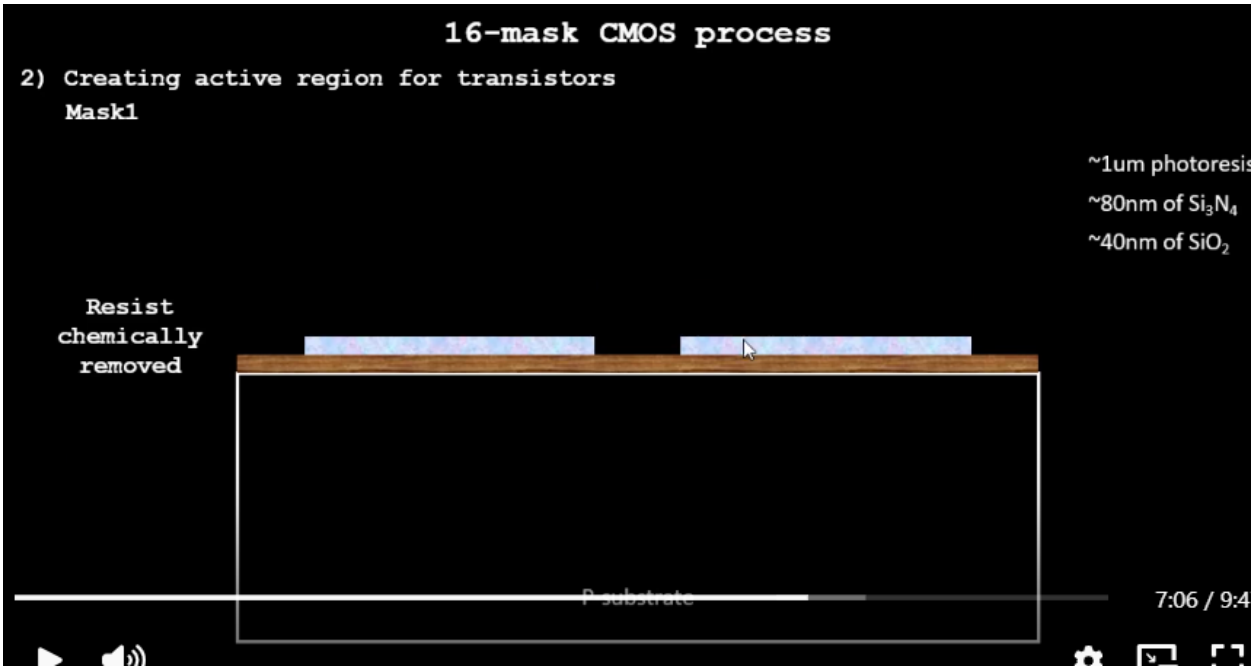


2)

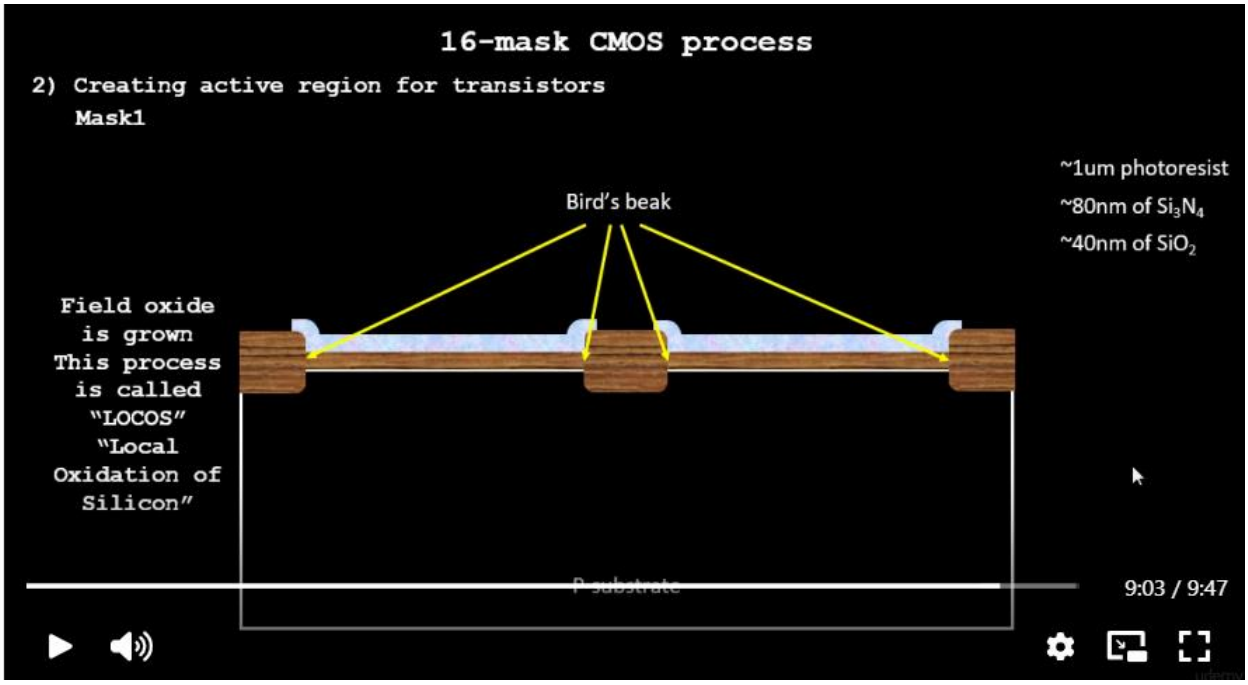

16-mask CMOS process
2) Creating active region for transistors
Mask1
UV light
~1um photoresist
~80nm of Si_3N_4
~40nm of SiO_2
P-substrate
5:40 / 9:47


16-mask CMOS process
2) Creating active region for transistors
Mask1
~1um photoresist
~80nm of Si_3N_4
~40nm of SiO_2
Washed out in developing solution
P-substrate
6:04 / 9:47


16-mask CMOS process
2) Creating active region for transistors
Mask1
~1um photoresist
~80nm of Si_3N_4
~40nm of SiO_2
Washed out in developing solution
P substrate
6:16 / 9:47

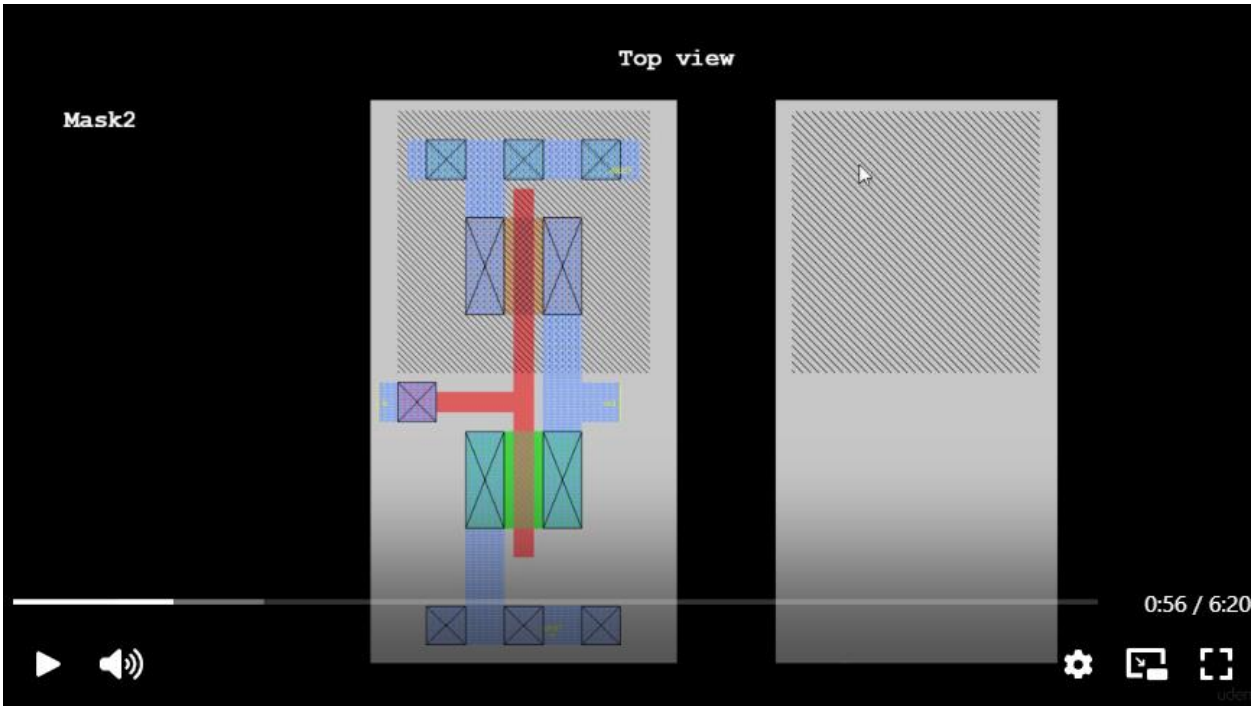

16-mask CMOS process
2) Creating active region for transistors
Mask1
~1um photoresis
~80nm of Si_3N_4
~40nm of SiO_2
Resist chemically removed
P substrate
7:06 / 9:4

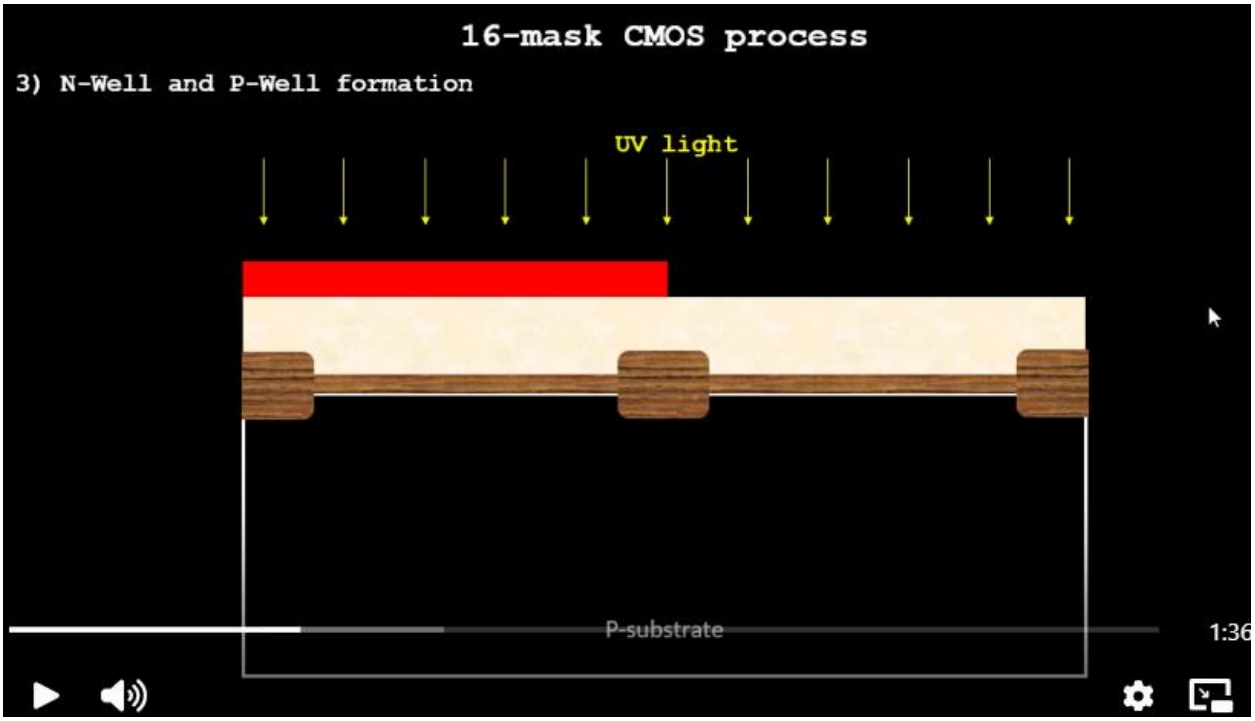

16-mask CMOS process
2) Creating active region for transistors
Mask1
~1um photoresist
~80nm of Si_3N_4
~40nm of SiO_2
Placed in oxidation furnace
P-substrate
8:49 / 9:47


16-mask CMOS process
2) Creating active region for transistors
Mask1
~1um photoresist
~80nm of Si_3N_4
~40nm of SiO_2
Bird's beak
Field oxide is grown This process is called "LOCOS" "Local Oxidation of Silicon"
P-substrate
9:03 / 9:47

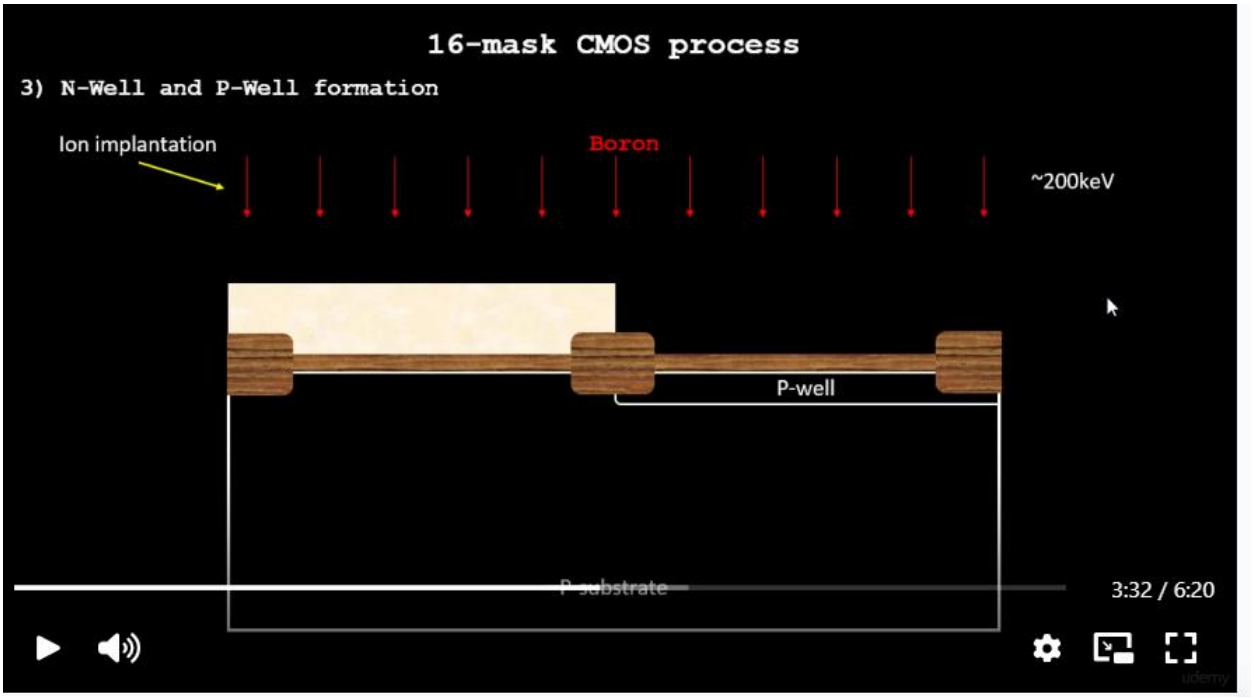

16-mask CMOS process
2) Creating active region for transistors
Mask1
~1um photoresist
~80nm of Si_3N_4
~40nm of SiO_2
Si3N4 stripped using hot phosphoric acid
P-substrate
9:28 / 9:47


16-mask CMOS process
3) N-Well and P-Well formation
Mask2
P-substrate
0:34 / 6:20

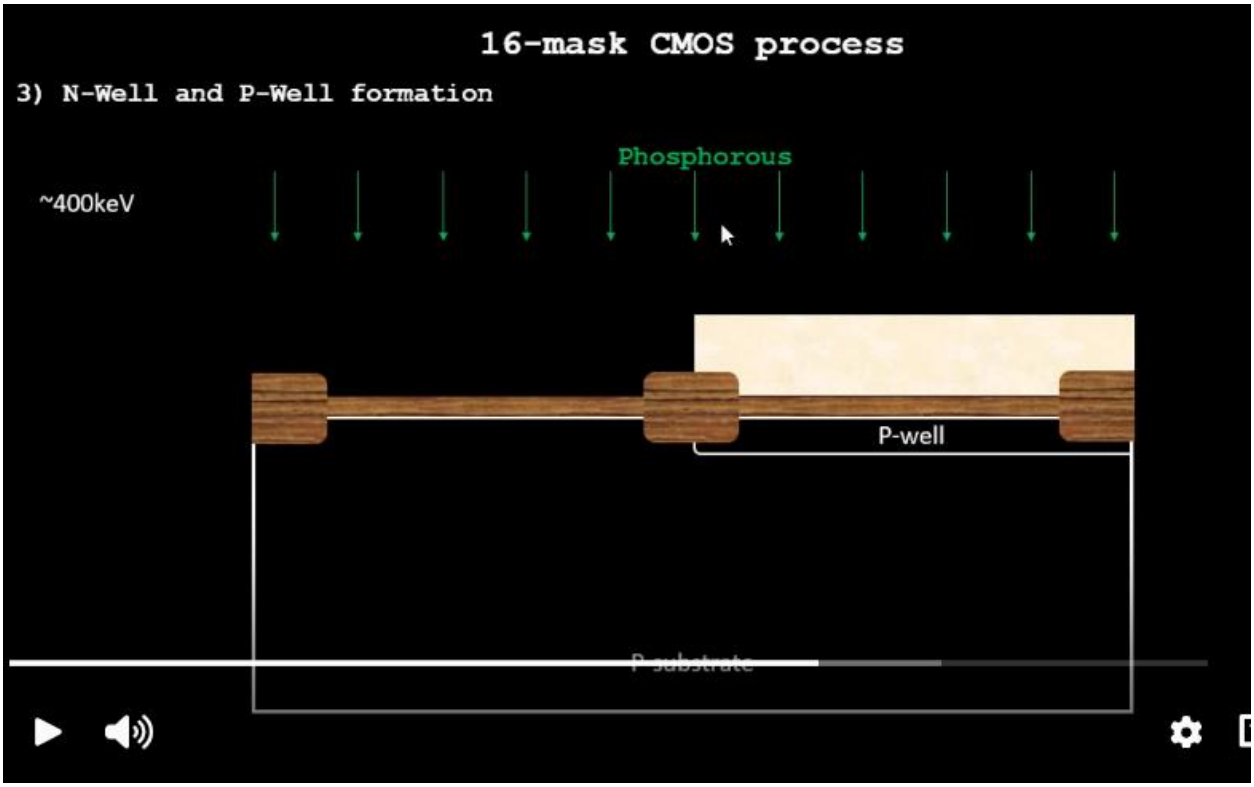

Top view
Mask2
0:56 / 6:20


16-mask CMOS process
3) N-Well and P-Well formation
UV light
P-substrate
1:36

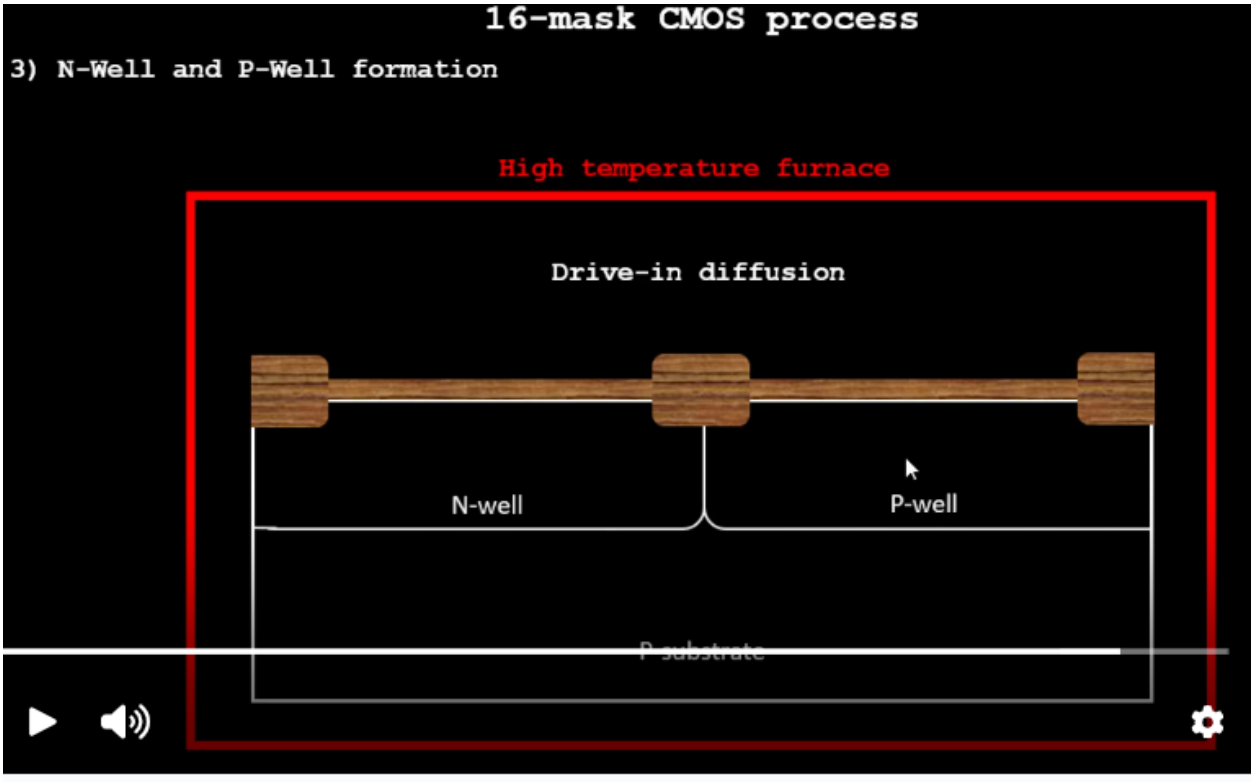

16-mask CMOS process
3) N-Well and P-Well formation
P-substrate
1:48 / 6:20


16-mask CMOS process
3) N-Well and P-Well formation
Ion implantation
Boron
~200keV
P-well
P-substrate
3:32 / 6:20

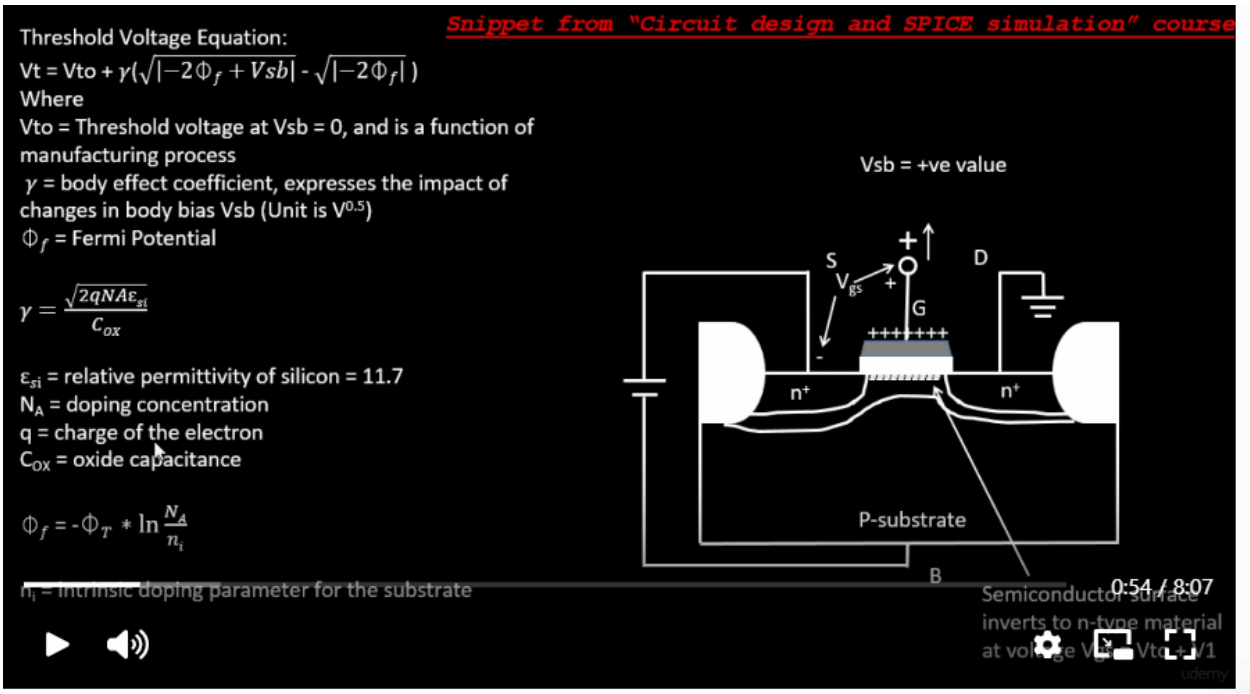

16-mask CMOS process
3) N-Well and P-Well formation
Mask3
Photo resist
P-well
P-substrate
4:01 / 6:20

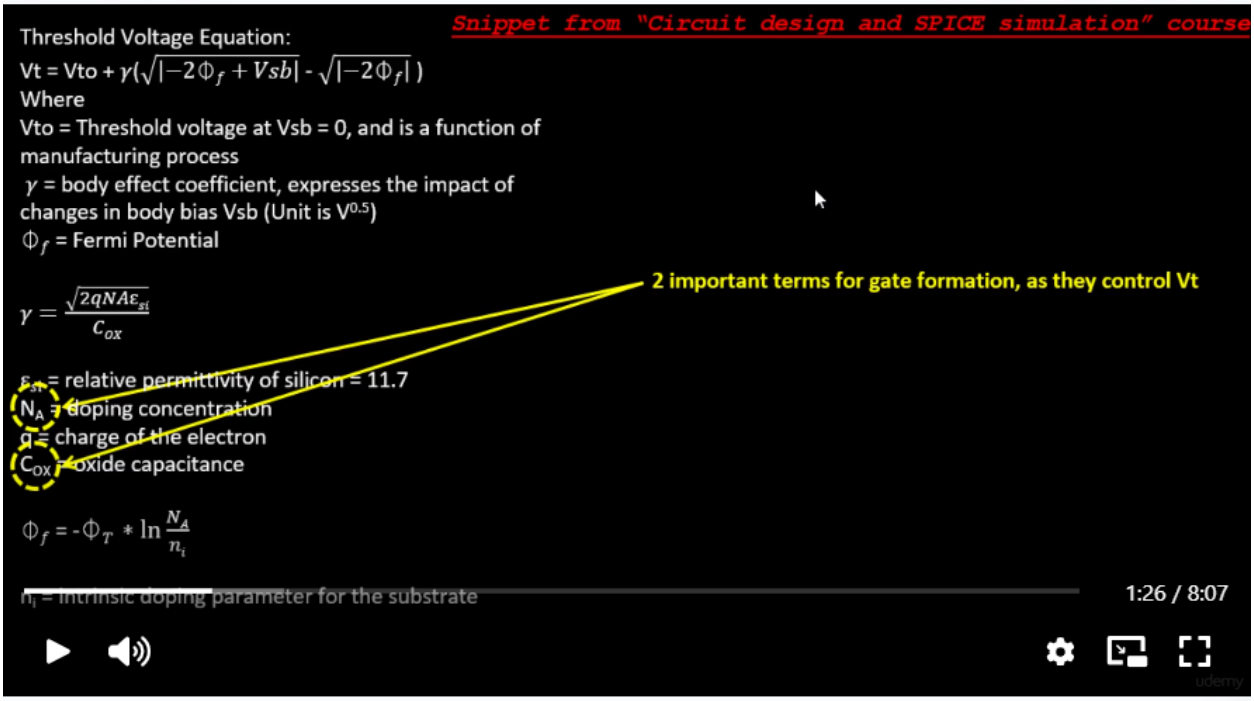

16-mask CMOS process
3) N-Well and P-Well formation
Phosphorous
~400keV
P-well
P-substrate

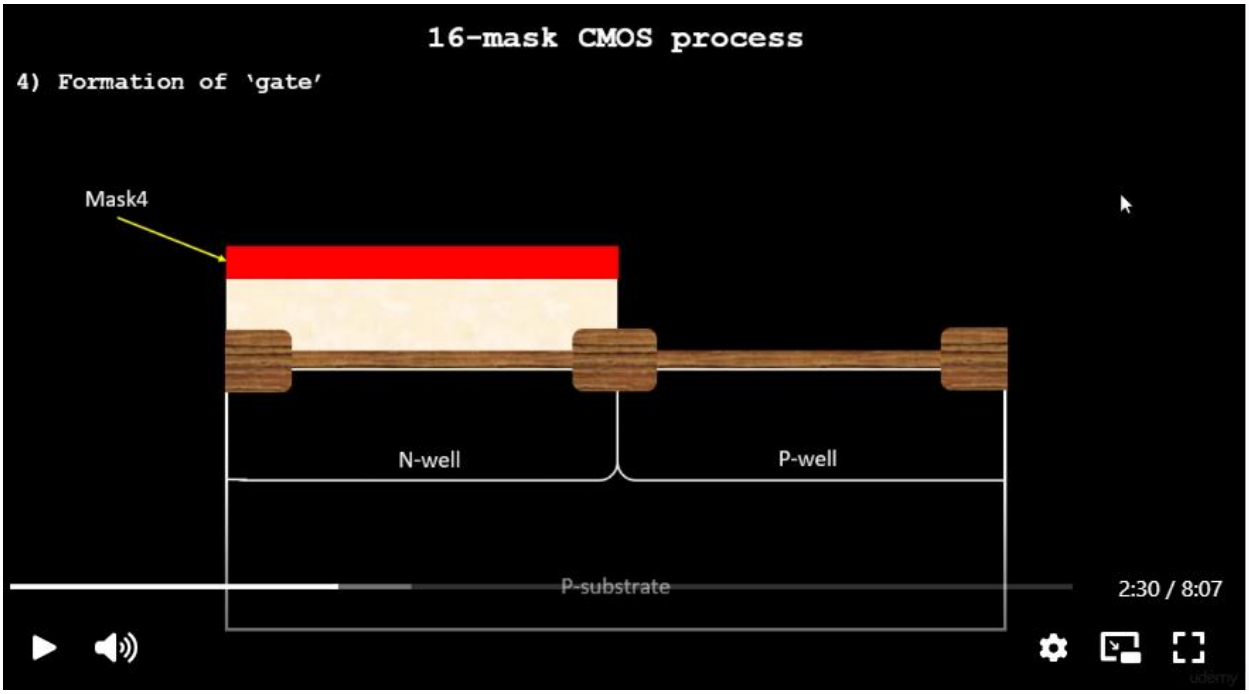

16-mask CMOS process
-Well and P-Well formation
N-well
P-well
P-substrate

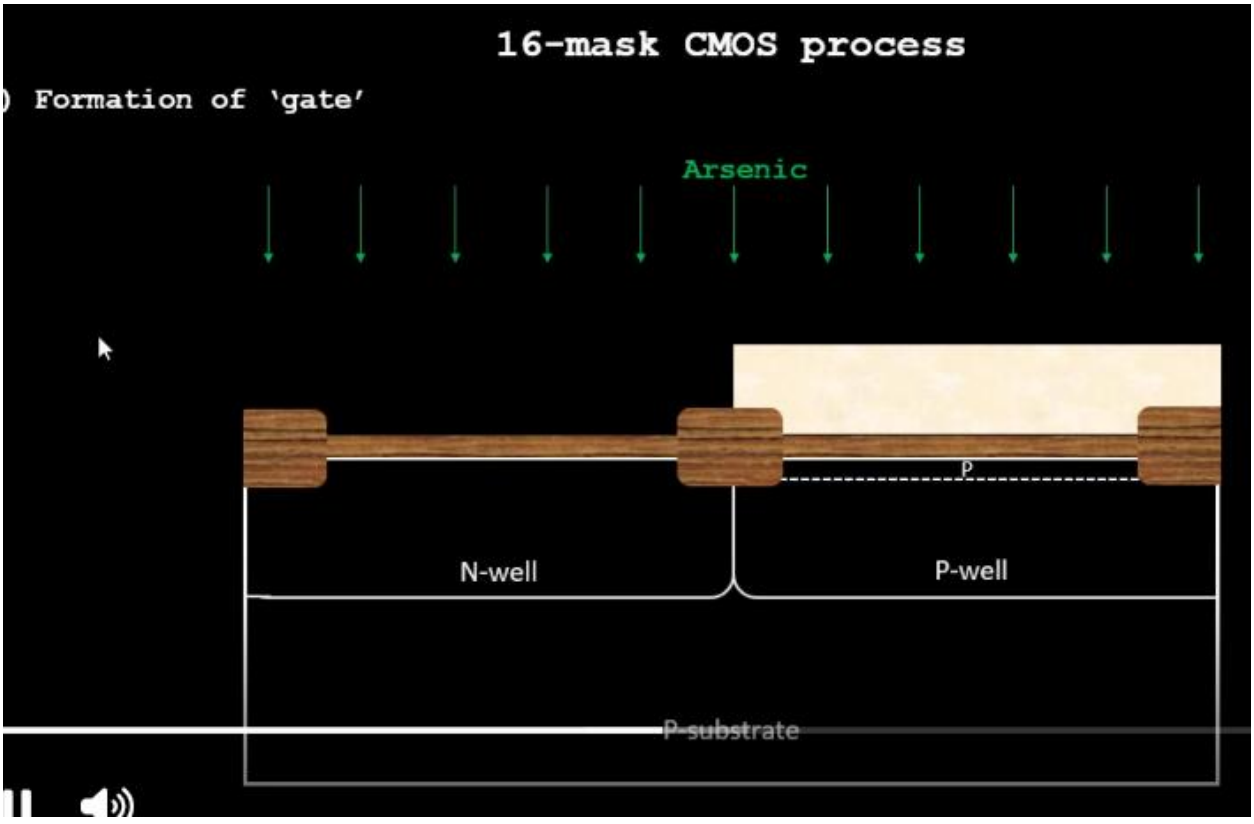

16-mask CMOS process
3) N-Well and P-Well formation
High temperature furnace
Drive-in diffusion
N-well
P-well
P-substrate

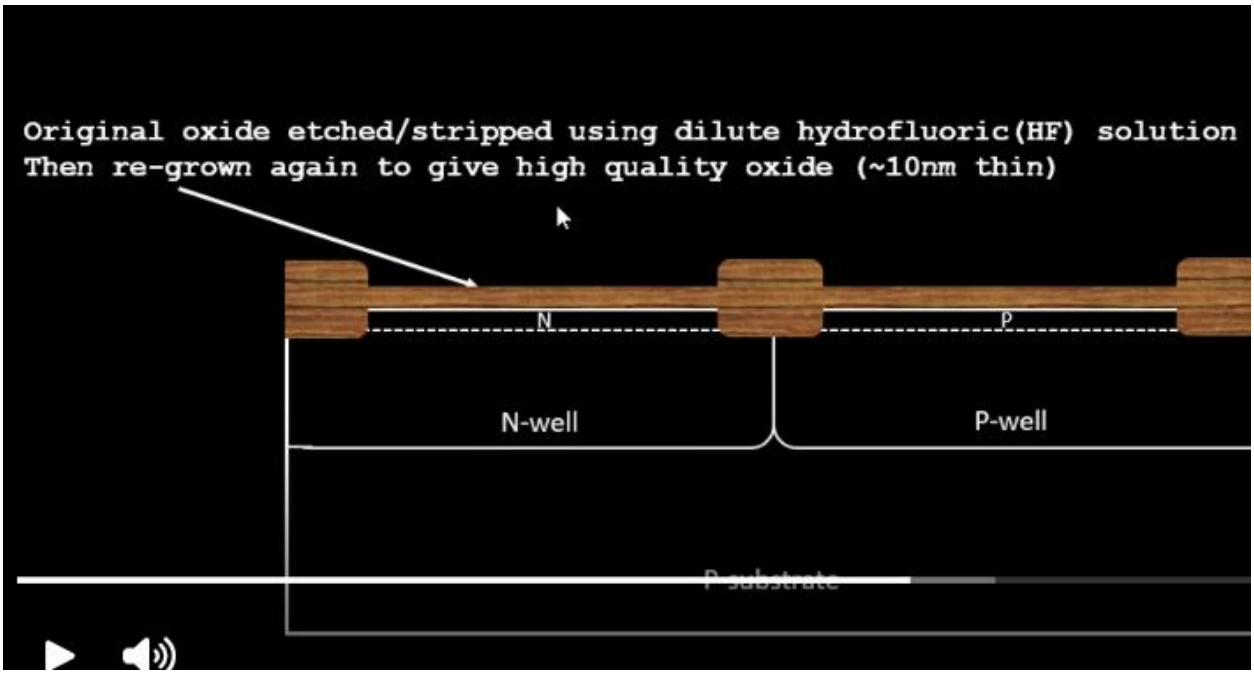
4) Formation of a gate.

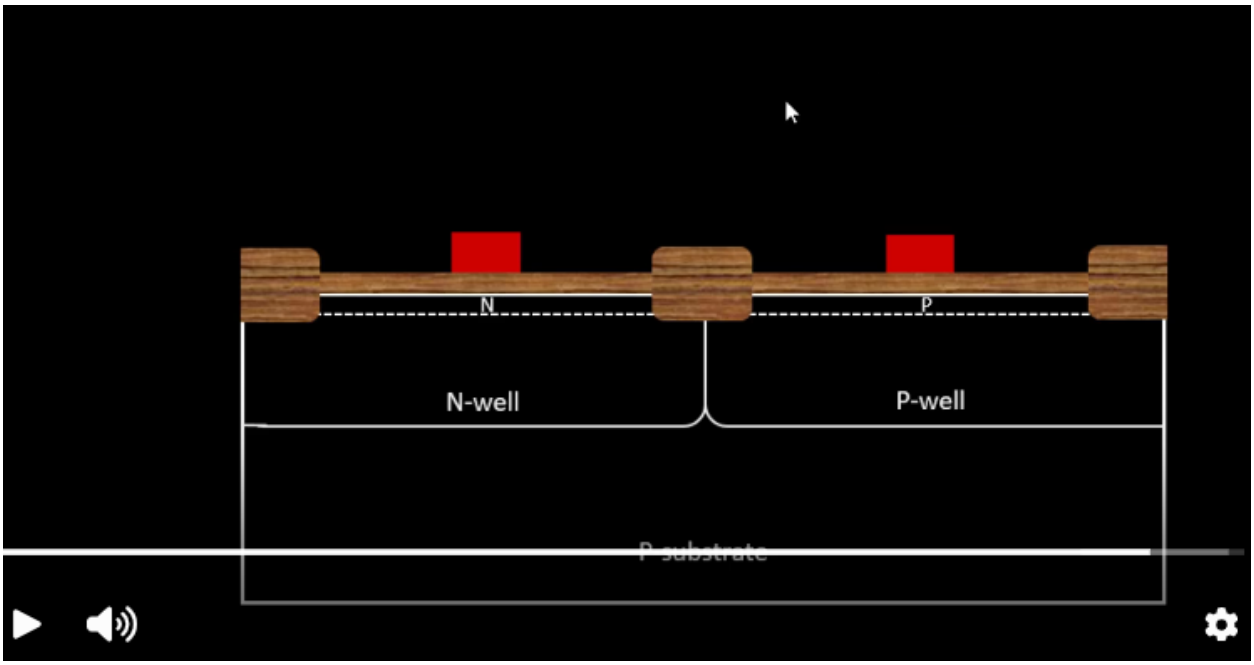




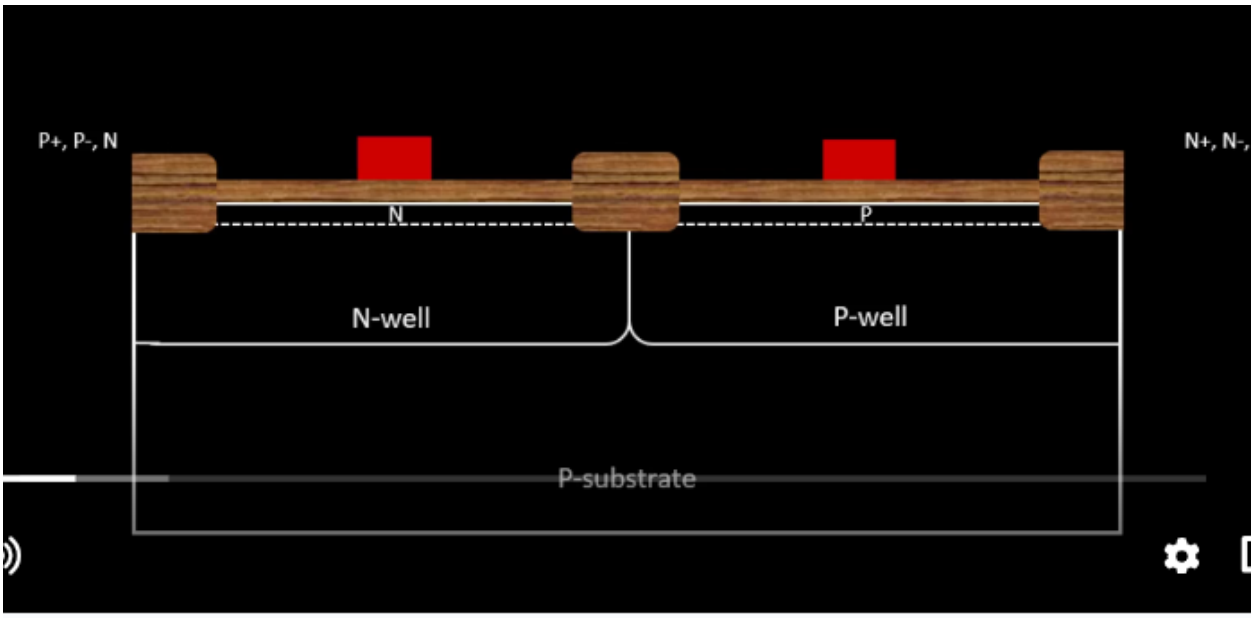

16-mask CMOS process
4) Formation of 'gate'
Mask4
N-well
P-well
P-substrate
2:30 / 8:07


16-mask CMOS process
) Formation of 'gate'
Arsenic
P
N-well
P-well
P-substrate





5)Lightly doped drain

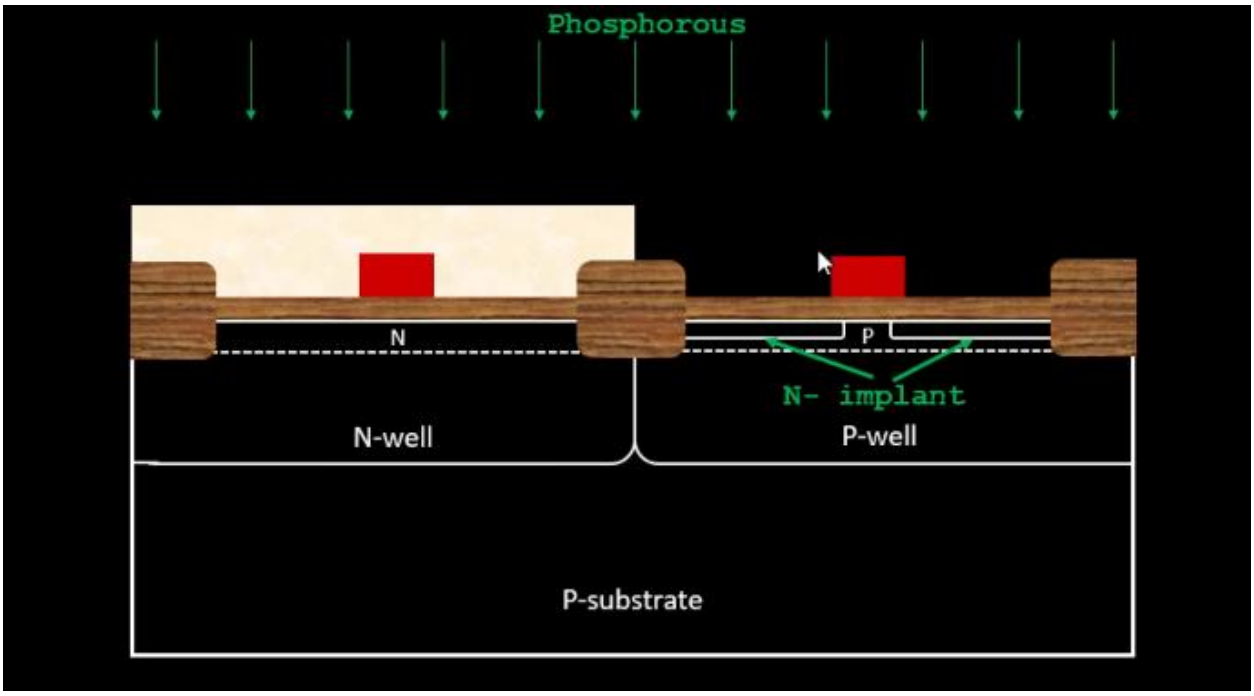


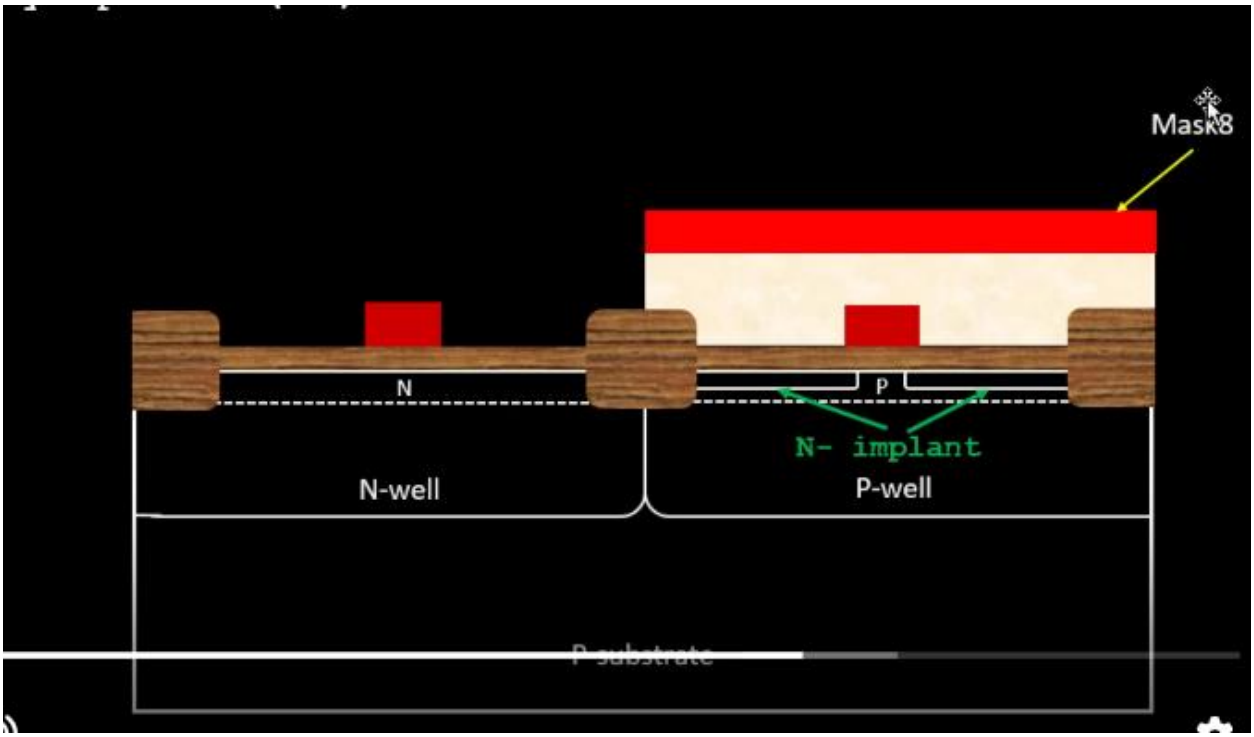
16-mask CMOS process

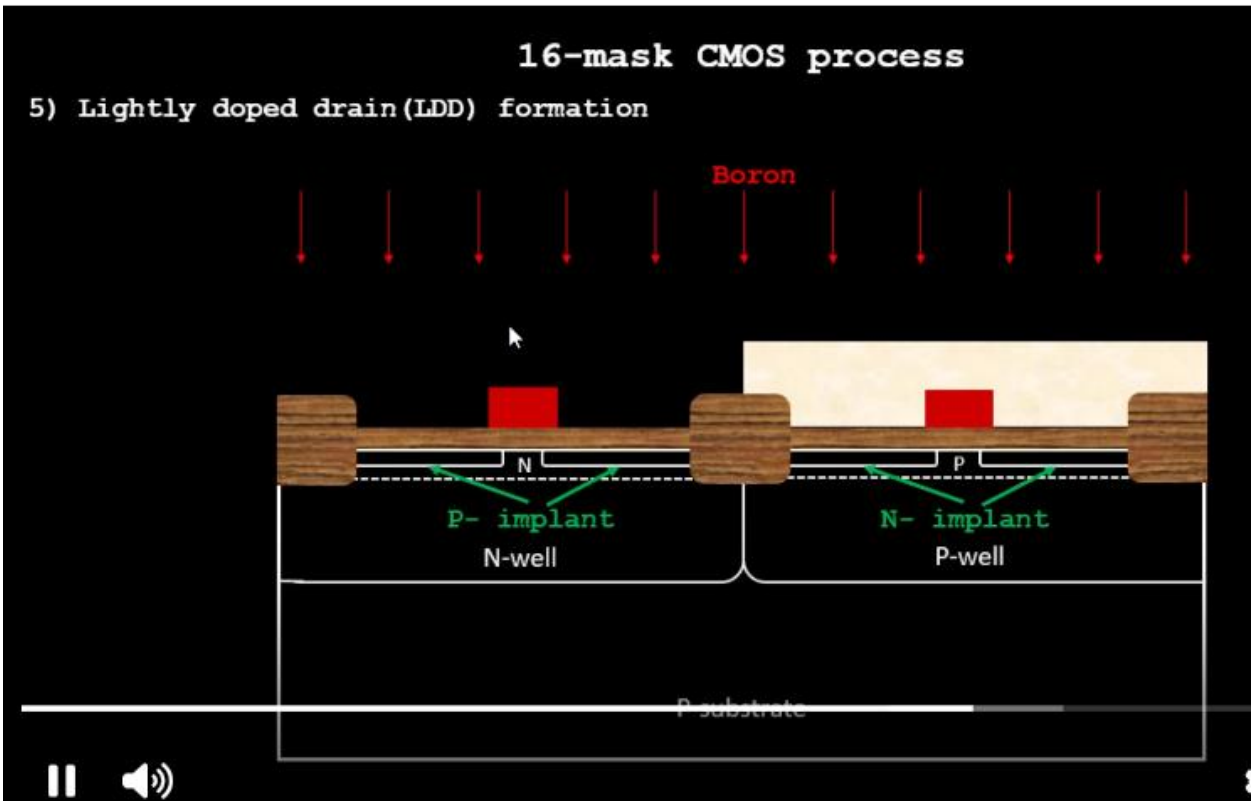
5) Lightly doped drain(LDD) formation

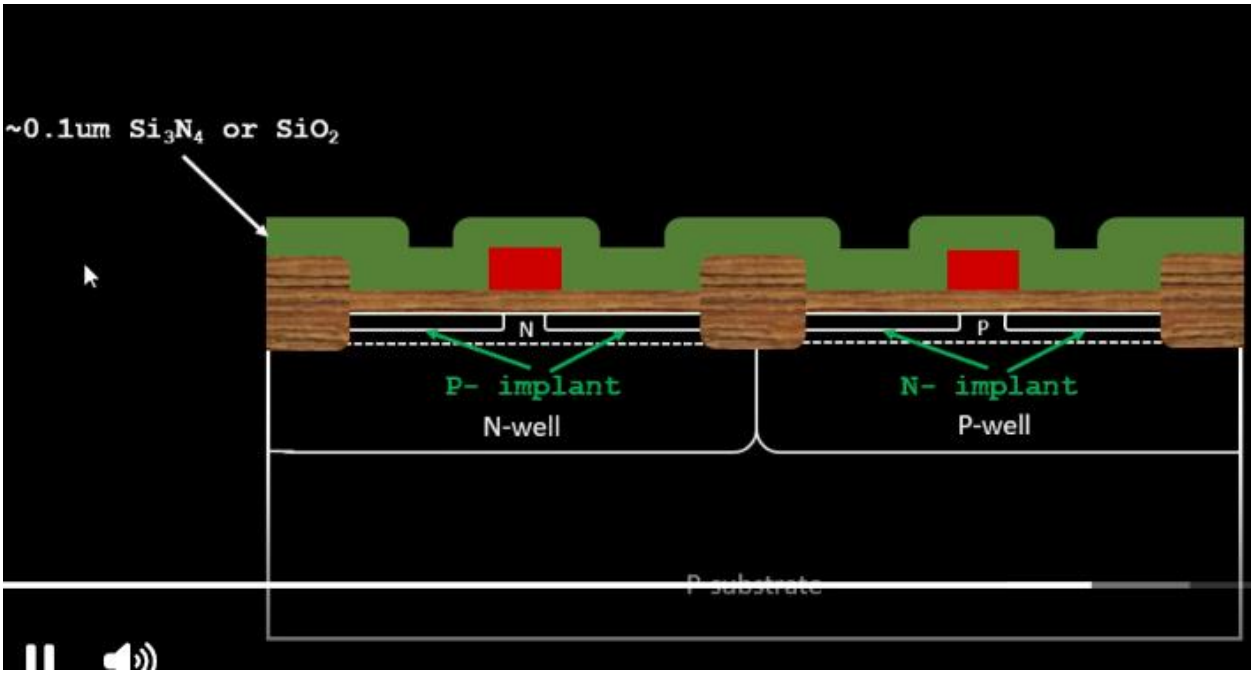
2 reasons for this
- Hot electron effect
- Short channel effect

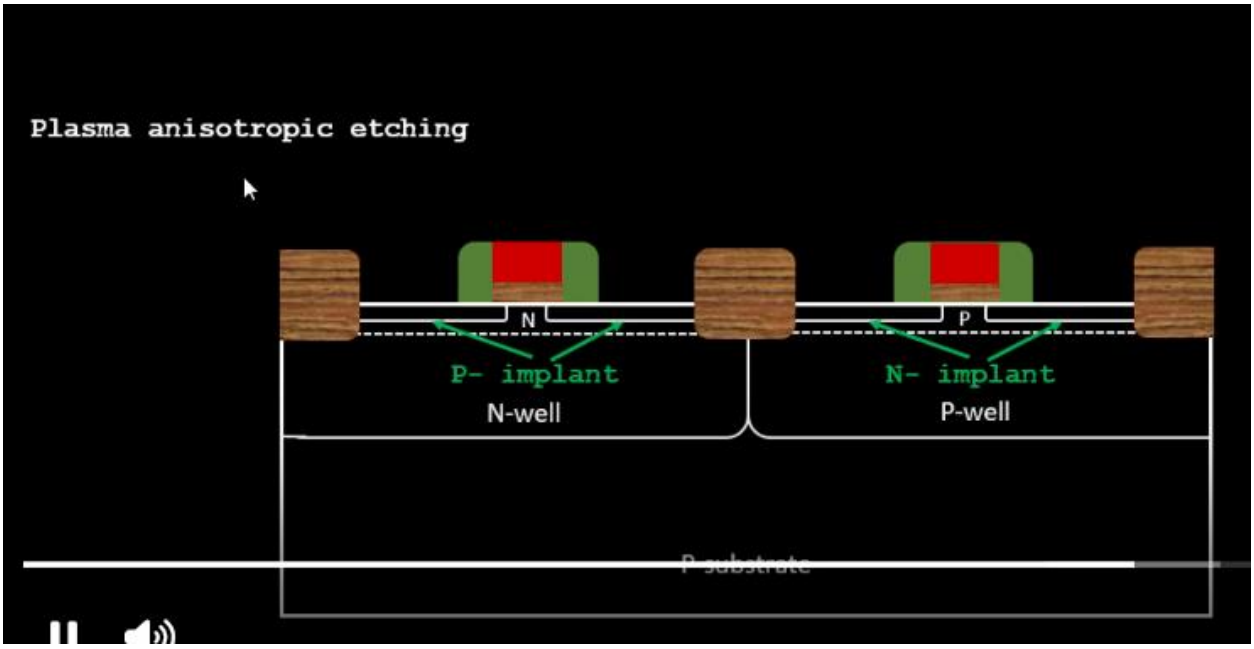
Electric field E=V/d
High energy carriers break Si-Si bonds
3.2eV barrier b/w Si conduction band
SiO2 conduction band

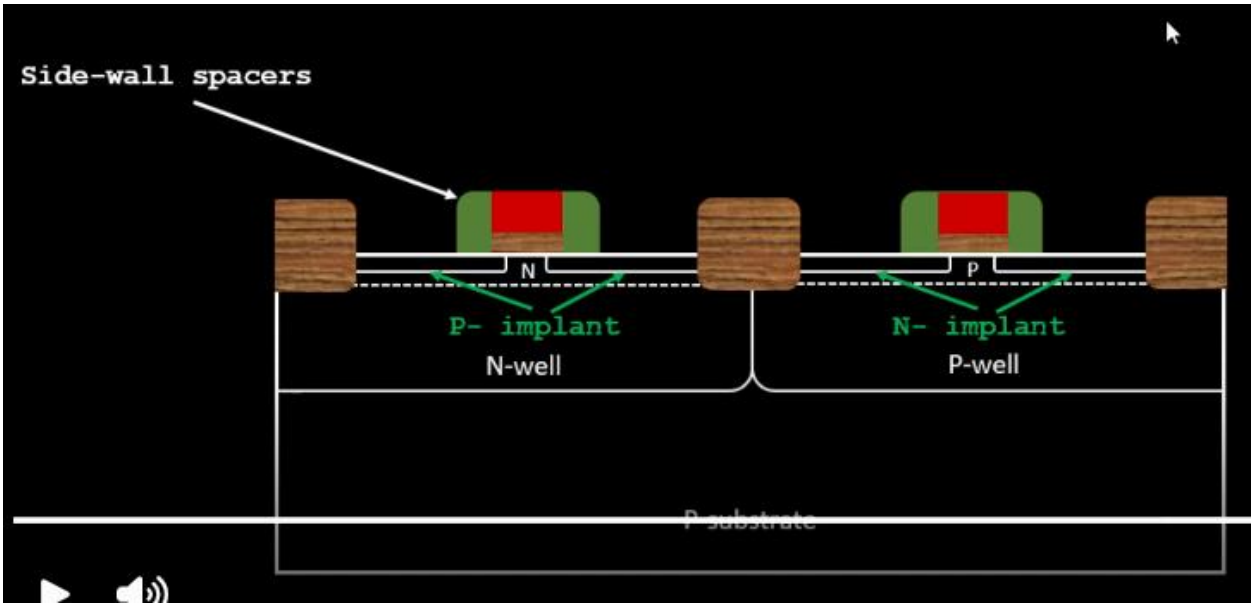

Phosphorous
N
P
N- implant
N-well
P-well
P-substrate


Mask8
N
P
N- implant
N-well
P-well
P-substrate

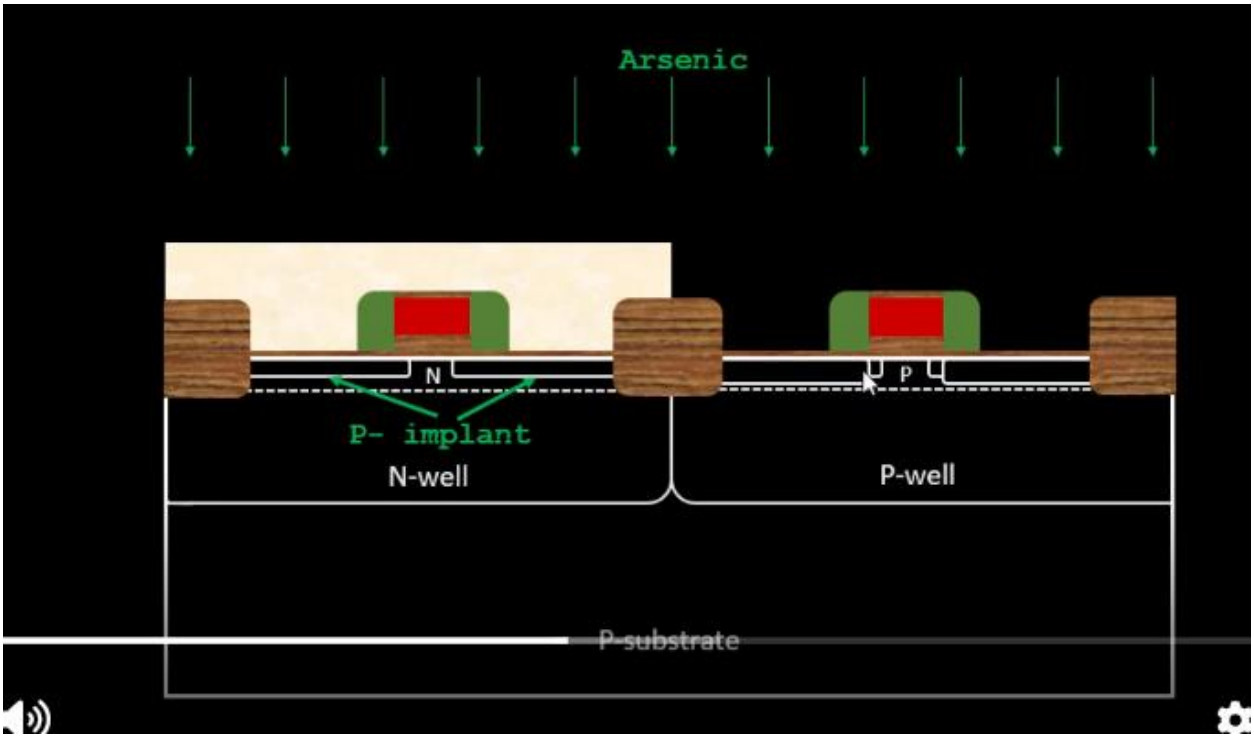

16-mask CMOS process
5) Lightly doped drain(LDD) formation
Boron
N
P
P- implant
N-well
N- implant
P-well
P substrate

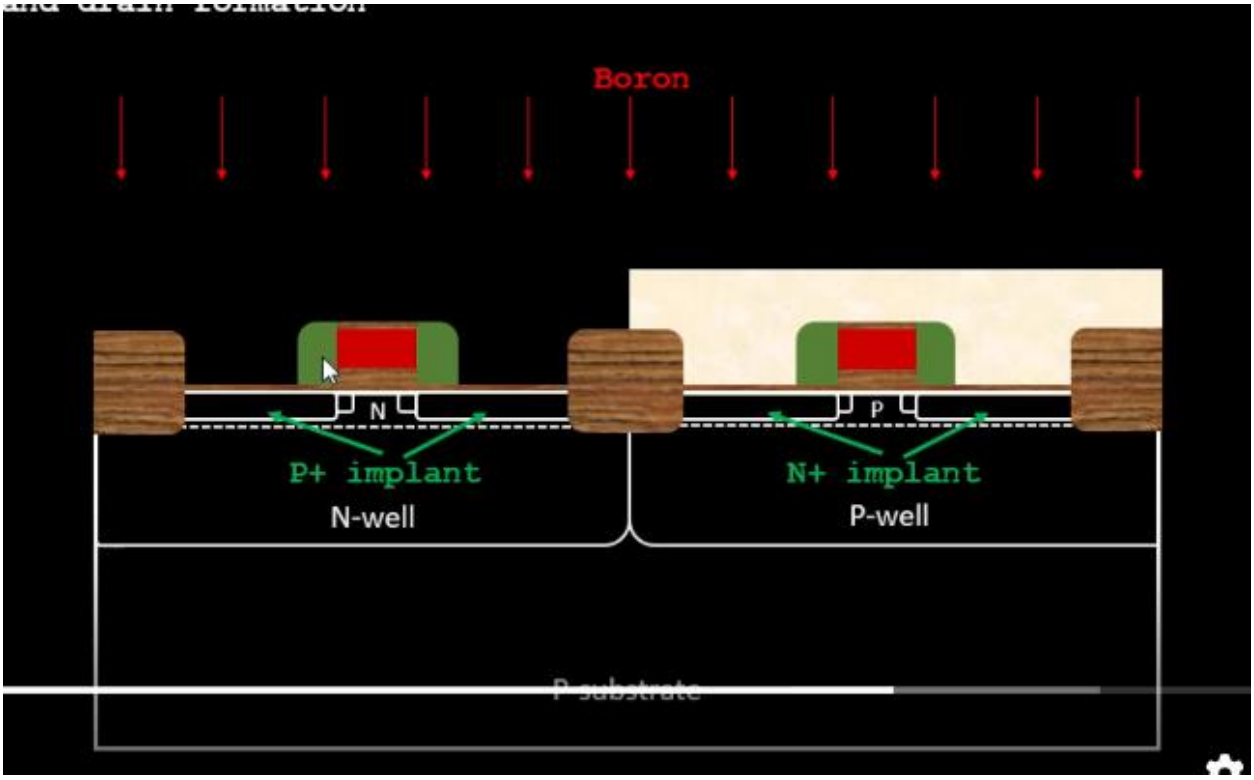

~0.1um Si_3N_4 or SiO_2
N
P
P- implant
N-well
N- implant
P-well
P substrate

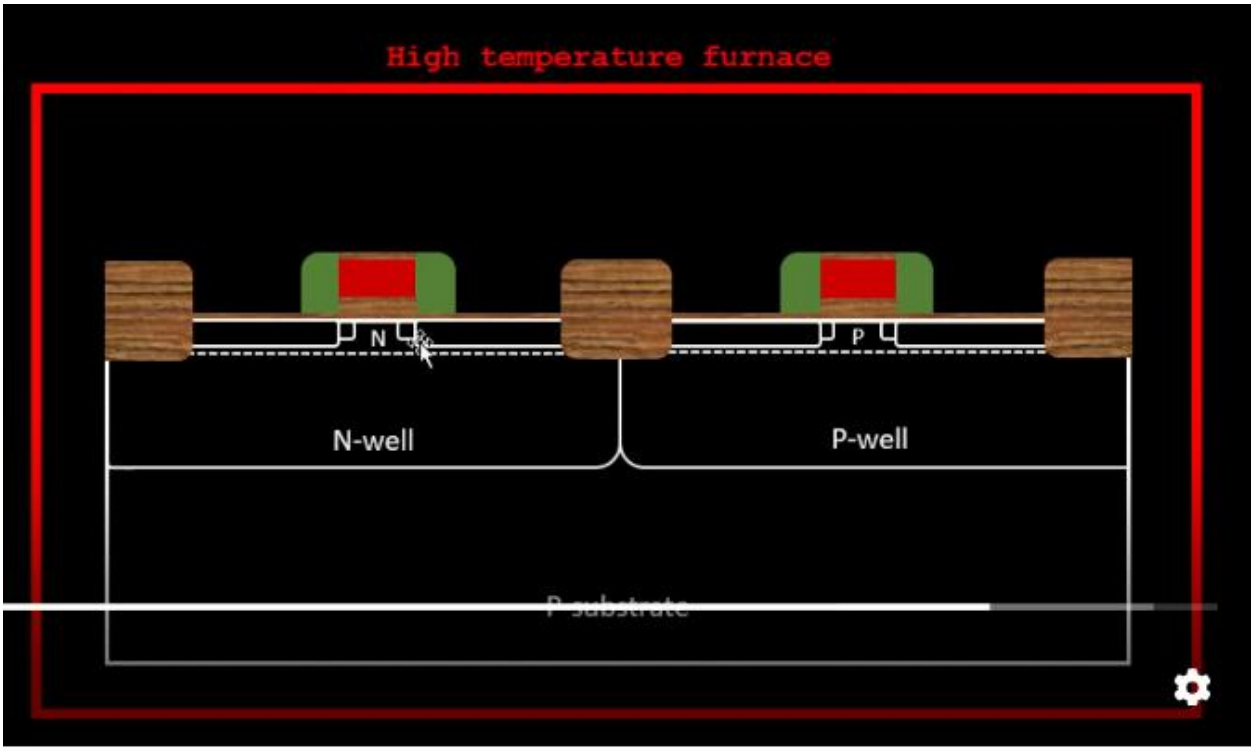


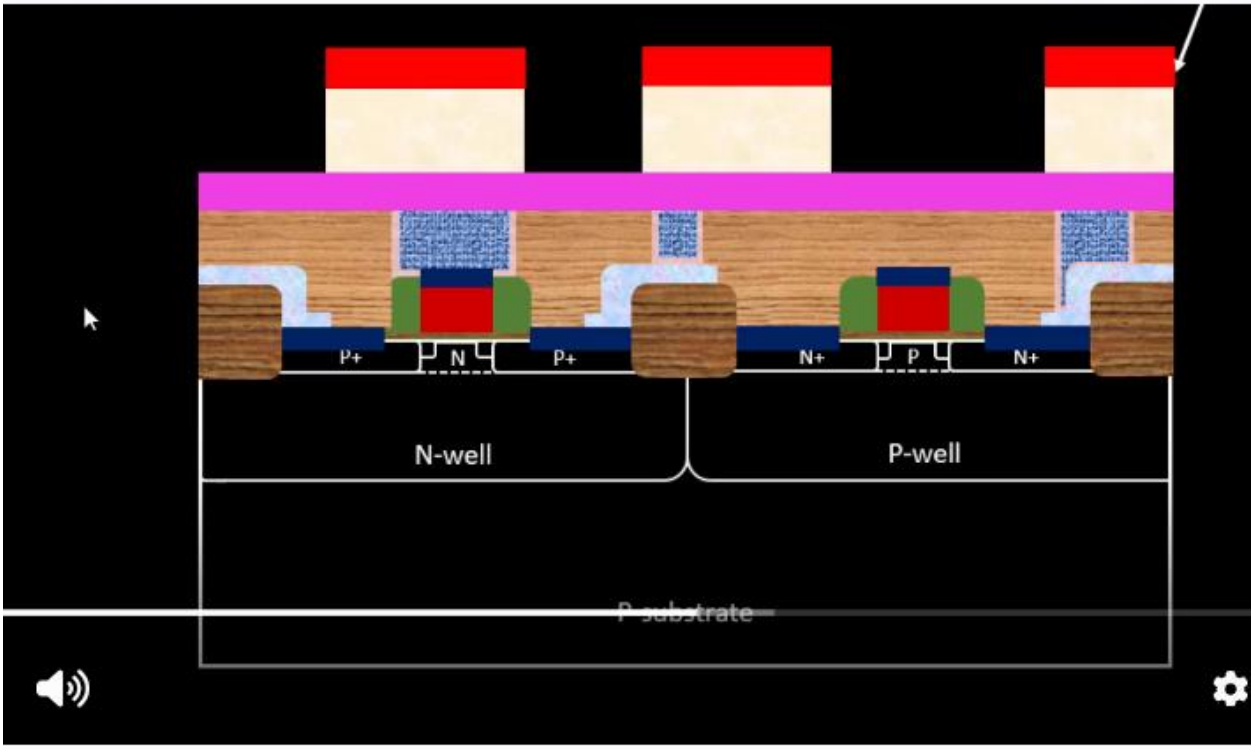


6)Source and the drain formation:


Arsenic
N
P
P- implant
N-well
P-well
P-substrate


Boron
N
P
P+ implant
N+ implant
N-well
P-well
P-substrate


High temperature furnace
N
P
N-well
P-well
P-substrate


P+
N
P+
N+
P
N+
N-well
P-well
P-substrate