## SEMESTER: MONSOON, SESSION: 2022-23

Examination & Semester: End Semester Exam- 1st Sem, B. Tech (Common) [Modular] Subject: Basics of Electronics Engineeric Subject Code: ECI 101 Max Marks: 100 Subject: Basics of Electronics Engineering Time: 3 Hours

## Instructions: Attempt all the questions in sequence as they are written.

(The right-side numbers indicate marks.)

Q1. (a) Show the Transfer Characteristics (Vo vs Vin) of a parallel negative clipping circuit by pn junction diode and clearly made. [5] junction diode and clearly marking the on and off conditions of the non-ideal diode

(b) Sketch in (current through 10 kΩ resistor) and V<sub>0</sub> (output voltage) for the network shown in Fig.1 below. The input signal V. [10]Fig.1 below. The input signal V<sub>1</sub> is a triangular waveform with 10 V as its peak value. The Si diodes used have 0.7 V<sub>1</sub> at 1.2 diodes used have 0.7 V as the forward bias voltage (cut-in voltage).

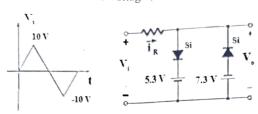


Fig.1

Obtain the output voltage  $v_o$  for the rightmost 4.4 k $\Omega$  resistor in the circuit shown in Fig.2 below. The input voltage vi is a sinusoid with 100 V as its peak amplitude. The diodes are considered to be ideal.

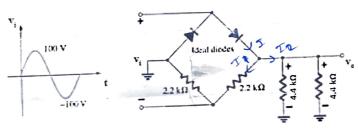


Fig.2

Q3. (a)  $I_{CBO}$  and  $I_{CEO}$ . How are they different? How are they related? Are they typically close in

magnitude? The current gain of the transistor is  $\beta = 120$ . Determine  $I_C$  and  $V_{CE}$  for the circuit given in [5]

(e) For the circuit in Fig.4 in which  $|V_{BE}| = 0.7 \text{ V}$  and  $\beta = 20$ , find the collector, base and emitter [5] voltages and currents.

(a) Draw the basic construction of a p-channel JFET. Draw the circuit to show the proper [5] biasing of the JFET and sketch the depletion region.

For the circuit in Fig.5, the transistor parameters are  $I_{DSS} = 4$  mA and  $V_P = -3$  V. Find  $R_D$ such that  $V_{DS} = |V_P|$ . What is the value of  $I_D$ ?

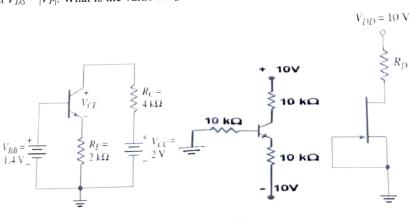
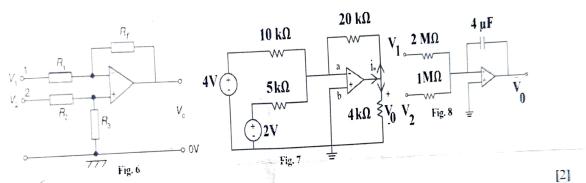


Fig.3

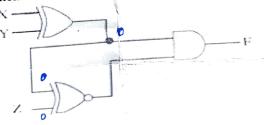
Fig.4

Fig.5

- Describe in brief the important characteristics of an ideal op-amp which are necessary to [5] understand the fundament concepts of op-amp operation.
  - Draw the schematic of a voltage follower using an ideal op-amp and derive its voltage gain. [5] Mention one important characteristic of a voltage follower.
- Q6. (a) In the differential amplifier shown in Fig.6,  $R_1 = 10 \text{ K}\Omega$ ,  $R_2 = 10 \text{ K}\Omega$ ,  $R_3 = 100 \text{ K}\Omega$ , and [5]  $R_f = 100 K\Omega$ . Determine the output voltage  $V_0$  if
  - (i)  $V_1=5~mV$  and  $V_2=0~mV$ , (ii)  $V_1=0~mV$  and  $V_2=5~mV$ , (iii)  $V_1=50~mV$  and  $V_2=5~mV$ , (iv)  $V_1=25~mV$  and  $V_2=50~mV$
  - [5] (b) Find  $v_0$  and  $i_0$  in the op-amp circuit shown in Fig.7.
  - (c) If  $v_1(t) = 20\cos(3t) \, mV$  and  $v_2(t) = 2t \, mV$  in Fig.8, find  $v_0(t)$  for t > 0. Assume that [5] the voltage across the capacitor is zero at t = 0.



Q7. (2) Express output F in canonical SOP form?



[2] (b) Convert (57)8 into a number system whose radix is 6.

[2] (C) Convert (46)10 into octal system.

[4] Perform (-7)10-(13)10 in binary using 1's complement method.

[5]

(c) Simplify  $F = \overline{(A + \overline{BC})} (A\overline{B} + ABC)$ [5]

Q8. (a) Prove the following using Boolean algebraic theorem  $\overline{ABC} + A\overline{BC} + AB\overline{C} + ABC = AB + BC + CA$ 

(b) Consider the Boolean function  $f(A,B,C,D) = \Sigma m(1,3,7,11,15) + \Sigma d(0,2,5)$  where m stands for Simplify the above function using K-Map and implement the simplified function using minimum number of 2-input NAND gates only.