# Shashank Sharma

## Electronics and Communication Engineer


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*Portfolio*

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I'm a driven B.Tech student at PES University in Bangalore. My project experience spans VLSI, IoT, Web Design, and Image Processing. I excel in Verilog, Python, C/C++, Web Development, MATLAB, Problem-Solving, and Photography. I'm a fast learner who thrives in collaborative settings. I'm eager to contribute as an intern and learn new tech and languages.

## Experience

### Research Intern

**CHIPS**

Research Intern May - September 2023

- Co-authored a research paper on optimizing sub-VT standard cells for energy-efficient designs under the guidance of Dr. Madhura Purnaprajna.
- Presented the research at a leading industry conference.
- Worked on physical design in VLSI under Prof. Kunal Ghosh

### ISRO Internship

AI/ML on FPGA 2023

- Working on hardware accelerator on deep neural network images processing
- Time period :- January 15th to may 15th 2024.

## Education

### Deeksha Jnana Sweekar

- 12th PU college
- Nov 2017 - Sep 2019

### PES University

- Bachelor of Technology - B.Tech in Electronics and Communications Engineering
- Nov 2020 - 2024

## Skills

- Programming Languages: Python, Verilog, C, C++
- Software Tools: Cadence Virtuoso, Quartus Prime Lite, Codasip, RIPES, MATLAB
- Web Development: React-Js , Tailwind CSS, MongoDb, JavaScript, HTML, CSS
- Other Skills: Problem-Solving, Photography, Teamwork

## Projects

- **Final Year Project in VLSI:** Developing a new routing algorithm that uses machine learning to optimize for power and area. Research paper comparing the performance of the new algorithm to existing routing algorithms is in progress.

- **Physical Design:** In this project, I've gained expertise in the entire synthesis process, encompassing work from the High-Level Language (HLL) and Assembly level language down to the generation of the GDS (Graphic Design System), all within the framework of OpenLane 2 and the Sky130 technology. Also in my previous internship I have created a library of UMC 55nm technology using Genus Legacy UI tool , TCL scripting , cadence and innovus

- **FPGA Programming Experience:** Used FPGA programming software (Quartus Prime Lite) and simulation tools (Codasip and RIPES) to design and optimize digital circuits. Compared the speed and number of cycles used by different circuits. Gaining my hands-on experience in using Vivado and Vitis at ISRO.

- **Website Design:** I possess practical expertise in Full Stack web development, having worked with foundational technologies such as HTML, CSS, and JavaScript, as well as modern tools like React.js and Tailwind CSS. Additionally, I have personally designed my own portfolio using React.js.

## Certificates

- **Cybersecurity**
  - PESU I/O
  - Dec 2020 - March 2021
- **Matlab**
  - PES University , Workshop
  - Jan 2021

## Awards and Honors

- State-level basketball and swimming champion