**Vending Machine using Verilog**

A Project Report

Submitted in the partial fulfillment of the requirements for the award of the degree of

Bachelor of Technology

in

Department of Electronics and Communication Engineering

By

B. Uday Kumar Reddy 2000040020

P. Shashikanth Reddy 2000040108

B. Likith Vishvendra 2000040199

under the supervision of

**Dr. I. GOVARDHINI**



Department of Electronics and Communication Engineering

K L E F, Green Fields,

Vaddeswaram-522302, Guntur (Dist.), Andhra Pradesh, India.

April, 2023

**KONERU LAKSHMAIAH EDUCATION FOUNDATION DEPARTMENT**

**OF ELECTRONICS AND COMMUNICATION ENGINEERING**

****

**DECLARATION**

The Project Report entitled **“Vending Machine using Verilog”** is a record of bonafide work of **B Uday kumar Reddy (20000400020), P Shashikanth Reddy (2000040108) and B Likith Vishvendra (2000040199)** submitted in partial fulfilment for the award of **B.Tech in Electronics and Communication Engineering to the K L University.** The results embodied in this report have not been copied from any other departments/University/Institute.

B Uday Kumar Reddy (2000040020)

P Shashikanth Reddy (2000040108)

B Likith Vishvendra (2000040199)

**KONERU LAKSHMAIAH EDUCATION FOUNDATION DEPARTMENT**

**OF ELECTRONICS AND COMMUNICATION ENGINEERING**



**CERTIFICATE**

This is to certify that the Project Report entitled “**Vending Machine using verilog”** is being submitted byB Uday kumar Reddy (20000400020), P Shashikanth Reddy (2000040108) and B Likith Vishvendra (2000040199)submitted in partial fulfilment for the award of B-Tech in Electronics and Communication Engineering to the K L University is a record of bonafide work carried out under our guidance and supervision.

The results embodied in this report have not been copied from any other departments/University/ Institute.

**Signature of the Supervisors Signature of the HOD**

**ACKNOWLEDGMENT**

Apart from the efforts by us, the success of any work depends largely on the encouragement and guidelines of many others. We take this opportunity to express our gratitude to the people who have been instrumental in the successful completion of this project.

We would like to show my greatest appreciation to my internal guide **Dr. I. GOVARDHINI** **Dept.** of electronics and communication engineering. We feel motivated and encouraged every time we attend her meetings. Without his encouragement and guidance this project would not have materialized and implemented.

We deeply in debted to my Head of the Department **Dr. SUMAN MALOJI** Dept. of electronics and communication engineering who modelled us both technically and normally for achieving greater success in life.

Finally, we owe a lot to the teaching and non-teaching staff of the Dept. of Electronics and communication engineering for their director indirect support in the entire course of our project work

**CONTENT**

**1.ABSTRACT**………………………………………………………………………………………2

**2.INTRODUCTION**…………………………………………………………………………….….2

1.1 Problem Statement……………………………………………………………….……...2

1.2 Aim………………………………………………………………………………...…….2

1.3 Objective………………………………………………………………………….….….2

**3.LITERATURE SURVEY** ………………………………………………………………………..3

**4**.**THEORETICAL ANALYSIS**... …………………………………………………………………3

3.1Verilog ……………………………………………………………………………………...….3

3.2Vivado………………………………...……………………………………………………….4

**5**.**METHODOLOGY** ………………………………………………………………………..……..4

**6**.**EXPERIMENT RESULTS** …………………………………………………………….………**..**7

**7**.**CONCLUSION** …………………………………………………………………………………..7

**8**.**REFERENCES**…………………………………………………………………………………...7

**ABSTRACT**

The vending machine is an automated machine that dispenses various products such as snacks, beverages, newspapers, tickets etc to customers when money or credit card is inserted. Vending machines are more accessible and practical than the convention purchasing method Now, vending machine market is a big business with huge annual revenue for leading nations. The machines usually work when a product is selected and some money (usually coins or paper money) is put in a slot.

Then, a button needs to be pushed, or a lever pulled. If there is enough money, the selected item will be dropped to a tray, where it can be taken out by the person making the purchase. The project aims to design a vending machine that can dispense soft drinks of different prices, it accepts all the coins i.e.: 5 Rupees,10 Rupees, 20 Rupees and 50 Rupees. Till it receives 10 Rupees it will not dispense anything. After it has received 10 Rupees it will dispense a soft drink. Any amount above that will be given back as a change.

The finite state machine (FSM) approach is adopted for the design of vending machine. The design is achieved by formulating the Verilog code for the FSM-based machine using behavioural modelling and simulating the testbench for the products.We used the software VIVADO(XILINX) Tool for the execution of project.

**INTRODUCTION**

* 1. Problem Statement:
* As day-by-day technology is boosting rapidly so automation is playing a major role.
* So, we can buy the things automatedly by using vending machines.
* So, for this automation we are doing this project.
  1. Aim:

To Design Vending Machine using Verilog. Optimize the power consumption and efficiency of the better than present Vending Machines.

* 1. Objectives:
* The main objective of a vending machine implemented using Verilog is to provide a user-friendly, efficient, and reliable means of purchasing products, while also ensuring the security and integrity of the system.
* The vending machine should be able to accept input from the user, such as the selection of a product and the amount of money to be paid.
* The vending machine should be able to dispense the selected product once the correct amount of money has been paid.
* The vending machine should be able to keep track of the inventory of products and alert the operator when the stock of a particular product is running low.
* The vending machine should be designed to operate reliably and efficiently under a range of conditions. It should be able to handle a high volume of transactions without breaking down or malfunctioning.

**LITERATURE SURVEY**

1. "Design and Implementation of a Vending Machine Controller Using Verilog HDL" by Faris A. Al-Sharaeh and Rana M. Fayyad: This study presents the design and implementation of a vending machine controller using Verilog HDL. The authors describe the design process and the Verilog code for the controller, which includes modules for input/output, state machines, and the dispensing mechanism.
2. "Design of Vending Machine Using Verilog HDL" by Gaurav Saxena and Pooja Saxena: This study describes the design of a vending machine using Verilog HDL. The authors present the Verilog code for the various modules of the vending machine, including the display module, coin input module, product selection module, and dispensing module.
3. "Vending Machine Design with Verilog HDL" by Asma Khalid and Muhammad Rizwan: This study presents the design and implementation of a vending machine using Verilog HDL. The authors describe the design process and the Verilog code for the various modules of the vending machine, including the input/output module, control module, and dispensing module.
4. "Design and Implementation of Vending Machine Controller Using Verilog HDL" by K. Deepthi, K. Chandra Sekhar, and B. Veerendra: This study presents the design and implementation of a vending machine controller using Verilog HDL. The authors describe the design process and the Verilog code for the various modules of the controller, including the input/output module, state machine module, and dispensing module.

**THEORITICAL ANALYSIS**

**3.1 Verilog:**

Verilog, standardized as IEEE 1364, is a hardware description language (HDL) used to model electronic systems. It is most commonly used in the design and verification of digital circuits at the register-transfer level of abstraction. It is also used in the verification of analog circuits and mixed-signal circuits, as well as in the design of genetic circuits.[1] In 2009, the Verilog standard (IEEE 1364-2005) was merged into the System Verilog standard, creating IEEE Standard 1800-2009. Since then, Verilog is officially part of the System Verilog language. The current version is IEEE standard 1800-2017.

A Verilog design consists of a hierarchy of modules. Modules encapsulate design hierarchy, and communicate with other modules through a set of declared input, output, and bidirectional ports. Internally, a module can contain any combination of the following: net/variable declarations (wire, reg, integer, etc.), concurrent and sequential statement blocks, and instances of other modules (sub-hierarchies). Sequential statements are placed inside a begin/end block and executed in sequential order within the block. However, the blocks themselves are executed concurrently, making Verilog a dataflow language.

Verilog's concept of 'wire' consists of both signal values (4-state: "1, 0, floating, undefined") and signal strengths (strong, weak, etc.). This system allows abstract modelling of shared signal lines, where multiple sources drive a common net. When a wire has multiple drivers, the wire's (readable) value is resolved by a function of the source drivers and their strengths.

One of the key benefits of using Vivado is its ability to optimize the design for performance, area, and power consumption. It achieves this through a combination of technology mapping, logic synthesis, and place-and-route algorithms. The tool can also generate timing reports and perform static timing analysis to ensure that the design meets the required timing constraints.

**3.2 Vivado:**

Vivado is a software suite developed by Xilinx that is used for designing and implementing digital circuits on programmable logic devices (PLDs) such as field-programmable gate arrays (FPGAs) and system-on-chip (SoC) devices. Vivado provides a comprehensive set of tools for designing, simulating, synthesizing, and implementing digital circuits, as well as debugging and verifying the functionality of the designs.

One of the key features of Vivado is its high-level synthesis (HLS) capability, which allows designers to describe their designs using high-level programming languages such as C, C++, and SystemC. This greatly simplifies the design process and reduces the time-to-market for new products.

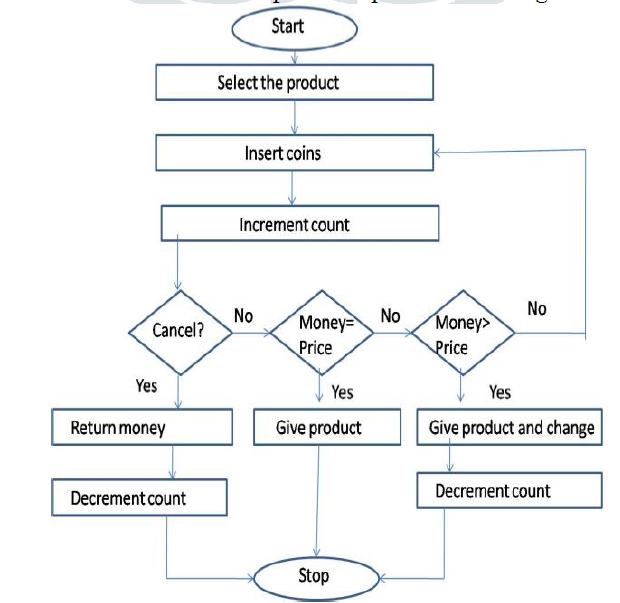
In addition to HLS, Vivado also includes a range of other tools such as a logic simulator, a timing analyzer, a power analyzer, and a debug environment. These tools enable designers to fully explore the design space, optimize their designs for performance and power consumption, and quickly identify and fix any issues that arise during the design process.

Vivado is also highly scalable and supports a wide range of PLDs, from small low-power FPGAs to high-performance SoCs with multiple processing cores and programmable logic fabric. This makes it an ideal choice for a wide range of applications, from low-power embedded systems to high-performance data center infrastructure.

Overall, Vivado is a powerful and versatile tool for designing and implementing digital circuits on programmable logic devices. Its high-level synthesis capability, comprehensive set of tools, and support for a wide range of PLDs make it an essential tool for modern digital design.

**METHODOLOGY**

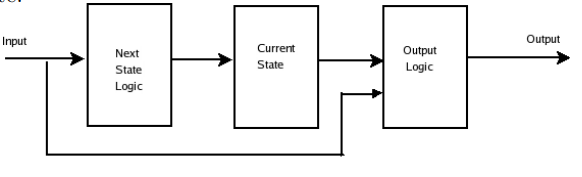
The project aims to design a vending machine that can dispense soft drinks of different prices, it accepts all the coins i.e.: 5 Rupees,10 Rupees, 20 Rupees and 50 Rupees. Till it receives 10 Rupees it will not dispense anything. After it has received 10 Rupees it will dispense a soft drink. Any amount above that will be given back as a change. The finite state machine (FSM) approach is adopted for the design of vending machine. The design is achieved by formulating the Verilog code for the FSM-based machine using behavioral and simulated in the XILINX (VIVADO).

****

**Flow Chart**

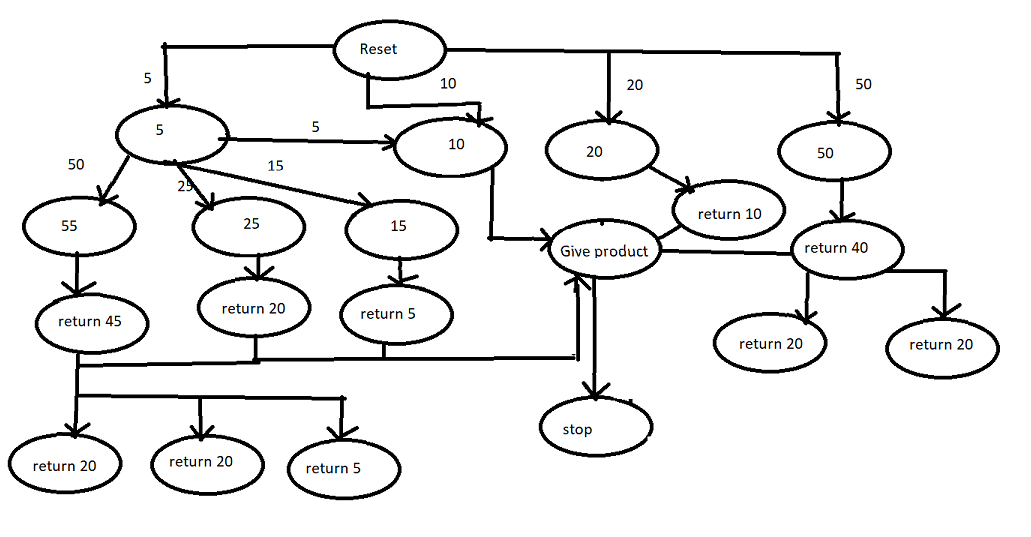
For this Project we are using the State Machines Concept in that state machines we are using Mealy State Machine.

If the next state of the system depends on both the present state and the present input, then it is called a Mealy Finite State Machine.



**Mealy Finite State Machine**

**State Diagram of Vending Machine**

****

* Here we have the first state that is reset state, if less amount is provided or non acceptable amount is provided then it will come back to reset state.
* Also if we provide amount 5,10,20 and 50 based on that it moves into further state ,gives product and return extra amount.
* The amount that will return also same 5,10,20 and 50 rupees as it want to return 45 rupees then it will return as 20,20 and 5 rupees.

**Code Explanation:**

* Here for code we are taking only 3 states so that code complexity get decreases and well understandable.

State 0🡪Represent the reset state(rupees 0)

State 1🡪Represents the State 1(rupees 5)

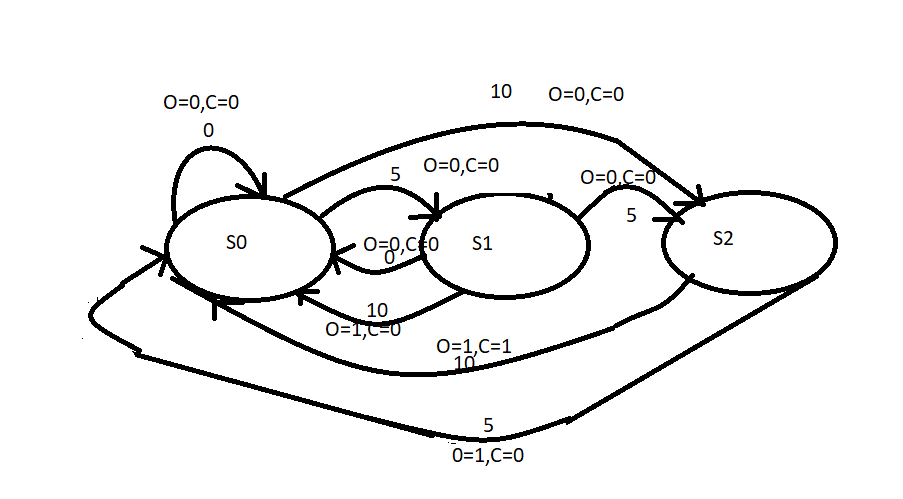
State 2->Represents the state 2(rupees 10)

Out->to show whether we get product or not

In->based on this input we move from 1 state to other(amount)

Change->amount left after providing the product

* Here we are providing product when it reaches 15 rupees
* Firstly reset is 1 and clock is zero then both out and Change are 0
* When reset is 0 and clock is On then it starts taking the input(in)



* When we are at State 0 :

If given input 0->it will be in the same state, out is 0, change is 0

If given input 1->it will move to state 1, out is 0, change is 0

If given input 2->it will move to state 2, out is 0, change is 0

* When we are at State 1:

If given input 0->it will be in the same state, out is 0, change is 0

If given input 1->it will move to state 2, out is 0, change is 0

If given input 2->it will move to state 0, out is 1, change is 0

* When we are at State 2:

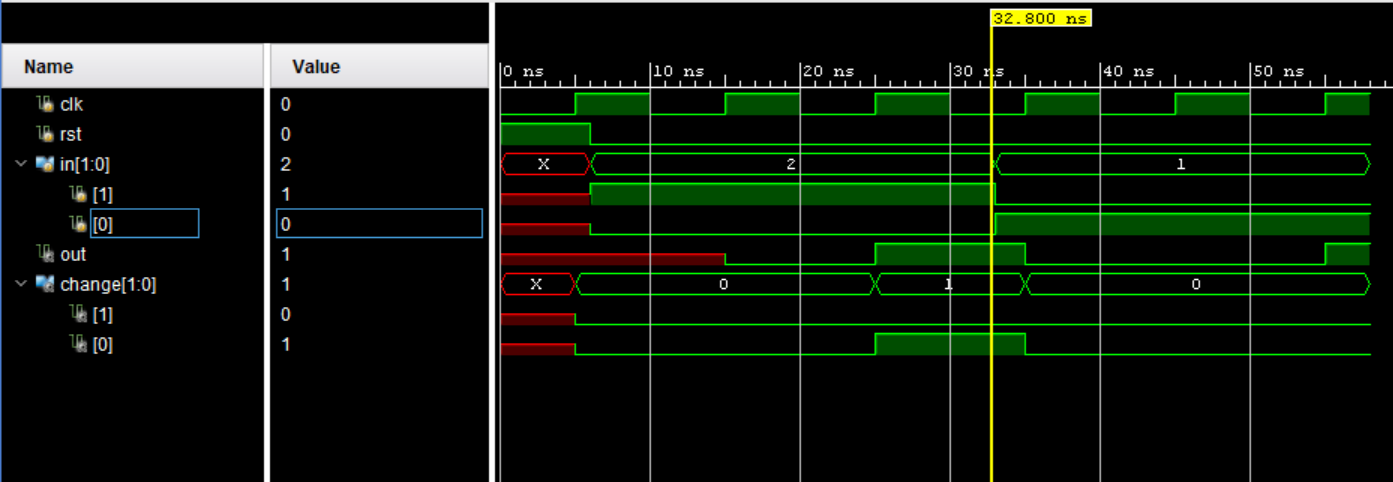
If given input 0->it will be in the same state, out is 0, change is 0

If given input 1->it will move to state 0, out is 1, change is 0

If given input 2->it will move to state 0, out is 1, change is 1

**Experimental Results:**

**Waveform:**

****

**Conclusion:**

The vending machine was successful in dispensing products when required amount is inserted into it. Also, with the additional features of dispensing product along with returning change when amount is inserted and returning total money when request is cancelled. The vending machine is successful in meeting the specifications laid out prior to the design. Our further plan of action is to implement this project on fpga boards and make vending Machine use everywhere.

**References:**

[1] R. Kiran Kumar, “FSM Based Design on the Replication of one-hot code using Verilog HDL,” Global Jouranl of Advanced Engineering Technologies, Vol.2, Issue-3, 2013.

[2] Abishek Luthra, “Design and Implementation of Vending Machine using Verilog HDL on FPGA,” International Journal of Innovative Research in Science, Engineering and Technology, Vol.4, Issue-11, November, 2015.

[3] Ana Monga, Balwinder Singh, Academic and Consultancy-Services Division, Centre for Development of Advanced Computing (C-DAC), Mohali, India, “Finite State Machine based Vending Machine Controller with Auto-Billing Features,” International Journal of VLSI design and Communication Systems (VLSICS), Vol.3, No.2, April 2012.

[4] P. Pradeepa, T. Sudhalavanya, K. Suganthi, N. Suganthi, M.Menagadevi, Suganthi, et. al., “Design and Implementation of Vending Machine using Verilog HDL,” International Journal of Advanced Engineering Technology.

[5] Muhammad Ali Qureshi, Abdul Aziz, Hafiz Faiz Rasool, Muhammad Ibrahim, Usman Ghani, Hasnain Abbas, “Design and Implementation of Vending Machine using Verilog HDL,” 2nd International Conference on Networking and Information Technology, IPCSIT, Vol.7, 2011.

[6] Ana Monga, Balwinder Singh, “Finite State Machine based Vending Machine Controller with Auto-billing Features,” International Journal of VLSI Design and Communication Systems, Vol.3, No.2, April, 2012.

[7] Ashwag Alrehily, Ruquiah Fallatah, Vijey Thayananthan, “Design of Vending Machine using Finite State Machine and Visual Automata Simulator,” International Journal of Computer Applications, Vol.115, No.18, April, 2015.