

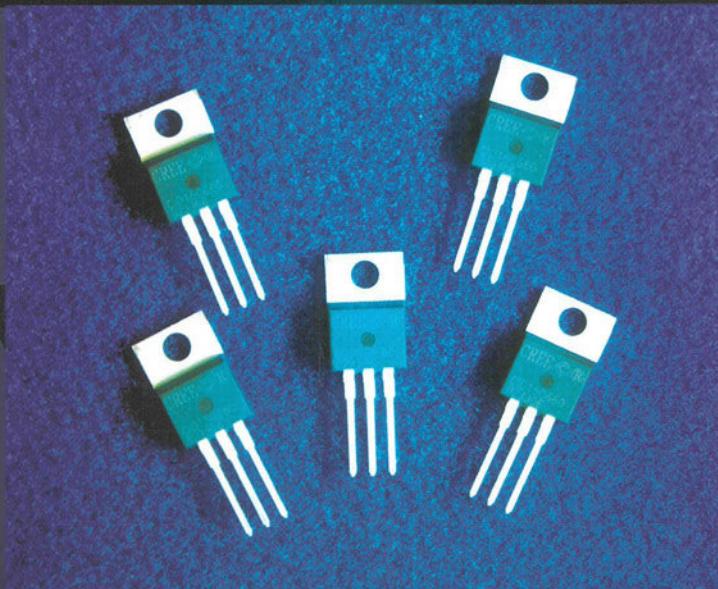
# SiC MATERIALS AND DEVICES

Volume 2

Michael Shur

Sergey Romyantsev

Michael Levenshtein



World Scientific

# **SiC MATERIALS AND DEVICES**

**Volume 2**

## **SELECTED TOPICS IN ELECTRONICS AND SYSTEMS**

*Editor-in-Chief: M. S. Shur*

---

### *Published*

- Vol. 27: Intersubband Infrared Photodetectors  
ed. *V. Ryzhii*
- Vol. 28: Advanced Semiconductor Heterostructures: Novel Devices, Potential Device Applications and Basic Properties  
eds. *M. Dutta and M. A. Stroscio*
- Vol. 29: Compound Semiconductor Integrated Circuits  
ed. *Tho T. Vu*
- Vol. 30: Terahertz Sensing Technology — Vol. 1  
Electronic Devices and Advanced Systems Technology  
eds. *D. L. Woolard, W. R. Loerop and M. S. Shur*
- Vol. 31: Advanced Device Modeling and Simulation  
ed. *T. Grasser*
- Vol. 32: Terahertz Sensing Technology — Vol. 2  
Emerging Scientific Applications and Novel Device Concepts  
eds. *D. L. Woolard, W. R. Loerop and M. S. Shur*
- Vol. 33: GaN-Based Materials and Devices  
eds. *M. S. Shur and R. F. Davis*
- Vol. 34: Radiation Effects and Soft Errors in Integrated Circuits and Electronic Devices  
eds. *R. D. Schrimpf and D. M. Fleetwood*
- Vol. 35: Proceedings of the 2004 IEEE Lester Eastman Conference on High Performance Devices  
ed. *Robert E. Leoni III*
- Vol. 36: Breakdown Phenomena in Semiconductors and Semiconductor Devices  
*M. Levinshtein, J. Kostamovaara and S. Vainshtein*
- Vol. 37: Radiation Defect Engineering  
*Kozlovski V. and Abrosimova V.*
- Vol. 38: Design of High-Speed Communication Circuits  
ed. *R. Harjani*
- Vol. 39: High-Speed Optical Transceivers  
eds. *Y. Liu and H. Yang*
- Vol. 40: SiC Materials and Devices — Vol. 1  
eds. *M. S. Shur, S. Rumyantsev and M. Levinshtein*
- Vol. 41: Frontiers in Electronics  
Proceedings of the WOFE-04  
eds. *H Iwai, Y. Nishi, M. S. Shur and H. Wong*
- Vol. 42: Transformational Science and Technology for the Current and Future Force  
eds. *J. A. Parmentola, A. M. Rajendran, W. Bryzik, B. J. Walker, J. W. McCauley, J. Reifman, and N. M. Nasrabadi*

*Published by*

World Scientific Publishing Co. Pte. Ltd.

5 Toh Tuck Link, Singapore 596224

*USA office:* 27 Warren Street, Suite 401-402, Hackensack, NJ 07601

*UK office:* 57 Shelton Street, Covent Garden, London WC2H 9HE

**British Library Cataloguing-in-Publication Data**

A catalogue record for this book is available from the British Library.

**SiC MATERIALS AND DEVICES**

**Volume 2**

Copyright © 2007 by World Scientific Publishing Co. Pte. Ltd.

*All rights reserved. This book, or parts thereof, may not be reproduced in any form or by any means, electronic or mechanical, including photocopying, recording or any information storage and retrieval system now known or to be invented, without written permission from the Publisher.*

For photocopying of material in this volume, please pay a copying fee through the Copyright Clearance Center, Inc., 222 Rosewood Drive, Danvers, MA 01923, USA. In this case permission to photocopy is not required from the publisher.

ISBN-13 978-981-270-383-5

ISBN-10 981-270-383-7

Editor: Tjan Kwang Wei

*Printed by Mainland Press Pte Ltd*

## PREFACE

This volume is the continuation of our recently published book on silicon carbide materials and devices.

As we stated in our Preface to Volume I, silicon carbide has been known investigated since 1907 when Captain H. J. Round demonstrated yellow and blue emission by applying bias between a metal needle and a SiC crystal. In 1923, a Russian scientist, Oleg Losev, discovered two types of light emission from SiC – the emission that we would now call "pre-breakdown" light and the electroluminescent emission. The potential of using SiC in semiconductor electronics was already recognized about a half of century ago. The most remarkable SiC properties are:

- Wide band gap (3 to 3.3 eV for different polytypes)
- Very large avalanche breakdown field (2.5 – 5 MV/cm)
- High thermal conductivity (3 – 4.9 W/cm K)
- High maximum operating temperature (up to 1,000 °C)
- Chemical inertness and radiation hardness

However, some of these potential advantages also cause exceptional technological difficulties in getting silicon carbide material to reach the device quality, and it has taken a few decades to travel the road from basic research to commercialization.

The breakthrough was reached in early 1990s, when nearly all basic semiconductor devices – p-n diodes, Schottky diodes, Metal Oxide Semiconductor Field Effect Transistor (MOSFETs), Metal Semiconductor Field Effect Transistor (MESFETs), bipolar junction transistors, thyristors, IMPATT diodes, and solar blind photodetectors – have been successfully demonstrated.

The first commercial SiC devices – power switching Schottky diodes and high temperature MESFETs – are now on the market.

For nitride based devices, silicon carbide has become a substrate of choice, because of its excellent thermal conductivity and decent lattice match. This includes both electronic and blue light emitting diodes and lasers, and, together with nitride based semiconductors, silicon carbide is now in the forefront of the semiconductor research.

The contributors to this two-volume book are recognized leaders in SiC technology and materials and device research. They provide complete and up-to-date review of the state-of-the-art.

The first volume has chapters on SiC materials properties (Chapter 1), SiC homo- and hetero-epitaxy (Chapter 2), Ohmic and Schottky contacts to SiC (Chapters 3 and 4), High

Power p-i-n rectifiers (Ch. 5), Microwave SiC diodes (Ch. 6), Thyristors (Ch. 7), and SiC static induction transistors (Ch. 8).

This second volume has additional four chapters. Chapter 1 on the growth of SiC substrates is authored by CREE, Inc. scientists who represent the company that has been a pioneer, innovator, and research and market leader in SiC technology. Chapter 2 (authored by Dr. Lebedev from famous A.F. Ioffe Institute) deals with deep defects in different SiC polytypes.

Deep defects define the properties of bulk SiC and, in many ways, the performance and reliability of SiC devices. In Chapter 3, Drs. Stephani and Friedrichs review recent work on SiC JFETs. Since demonstration of SiC JFETs by ONR-University of Minnesota-CREE, Inc. team<sup>1</sup> in 1980's, SiC JFETs demonstrated advantages related to bulk electron mobility in the channel (as opposed to much lower field effect mobility in SiC MOSFETs) and higher temperature performance. The last chapter by T. Paul Chow (Rensselaer Polytechnic Institute) and Anant K. Agarwal (CREE, Inc.) deals with Bipolar Junction Transistors (BJTs). This chapter reviews the complicated device physics raising many interesting and controversial issues important for these devices, which are still to demonstrate their full potential.

Both volumes will be useful for technologists, scientists, engineers, and graduate students who are working on silicon carbide or other wide band gap materials and devices. These books can also be used as a supplementary textbook for graduate courses on silicon carbide and wide band gap semiconductor technology.

---

<sup>1</sup> G. Kelner, M. S. Shur, S. Binari, K. Sleger, and H. S. Kong, High-Transconductance  $\beta$ -SiC Buried-Gate JFET's, IEEE Trans. Electron Devices, ED-36, No. 6, pp. 1045-1049 (1989); G. Kelner, M. S. Shur, S. Binari, K. Sleger, and H. S. Kong, A High Transconductance  $\beta$ -SiC Buried-Gate Junction Field Effect Transistor, in Proceedings of 2nd International Conference on Amorphous and Crystalline Silicon Carbide and Related Materials (ICACSC'88), Santa Clara, pp. 184-190, December (1988)

## CONTENTS

Preface	v
Growth of SiC Substrates	1
<i>A. Powell, J. Jenny, S. Muller, H. McD. Hobgood, V. Tsvetkov,     R. Leonard and C. Carter, Jr.</i>	
Deep Level Defects in Silicon Carbide	29
<i>A. A. Lebedev</i>	
Silicon Carbide Junction Field Effect Transistors	75
<i>D. Stephani and P. Friedrichs</i>	
SiC BJTs	105
<i>T. P. Chow and A. K. Agarwal</i>	

# SiC MATERIALS AND DEVICES

Volume 2

edited by

**Michael Shur**

Rensselaer Polytechnic Institute, USA

**Sergey Rumyantsev**

Rensselaer Polytechnic Institute, USA

Ioffe Institute of the Russian Academy of Sciences, Russia

**Michael Levinshtein**

Ioffe Institute of the Russian Academy of Sciences, Russia



**This page intentionally left blank**

## GROWTH OF SiC SUBSTRATES

ADRIAN POWELL, JASON JENNY, STEPHAN MULLER, H.McD.HOBGOOD, VALERI TSVETKOV,  
ROBERT LENOARD and CALVIN CARTER, Jr.

*Cree, Inc. 4600 Silicon Drive, Durham NC 27703, USA*  
*Adrian\_powell@cree.com*

In recent years SiC has metamorphized from an R&D based materials system to emerge as a key substrate technology for a significant fraction of the world production of green, blue and ultraviolet LEDs. Emerging markets for SiC homoepitaxy include high-power switching devices and microwave devices. Applications for heteroepitaxial GaN-based structures on SiC substrates include lasers and microwave devices. In this paper we review the properties of SiC, assess the current status of substrate and epitaxial growth, and outline our expectations for SiC in the future.

**Keywords:** SiC substrates, blue LEDs, high power switching, physical vapor transport, vapor phase epitaxy, hot wall epitaxy.

### 1. Introduction

Following in the footsteps of Si and GaAs, wide bandgap semiconductors are currently transitioning from research and development into real world applications. The commercialization of SiC that started a decade ago with the release of SiC blue LEDs[1] has accelerated over the past few years. The improvements made in SiC semiconductor device technology for electronic and optoelectronic applications are due in part to the commercial availability of SiC substrates of ever-increasing diameter and quality. Examples of current state-of-the-art devices include: high brightness and ultra-bright blue and green InGaN-based LEDs which take full advantage of the electrical conductivity of the 6H-SiC substrate by employing a conductive AlGaN buffer layer; microwave MESFETs on semi-insulating 4H-SiC substrates with power densities as high as 4.6 W/mm at 3.5 GHz and total CW output power of 100 W at 2.0 GHz from a single chip; 20 kV and 25 A p-i-n diodes fabricated on high quality SiC epitaxial layers; 1 cm<sup>2</sup> thyristors conducting 300 A at 5.5 V with 1770 V blocking voltage; and GaN/AlGaN HEMTs fabricated on semi-insulating 4H-SiC substrates exhibiting power densities of 11.4 W/mm at 10 GHz. These exciting device results stem primarily from the exploitation of the unique electrical and thermophysical properties offered by SiC compared to Si and GaAs. Among these are: a large band gap for high temperature operation and radiation resistance, high critical breakdown field for high power output, high saturated electron velocity for high frequency operation, and significantly higher thermal conductivity for thermal management of high power devices.

## 2. SiC Bulk Growth

In general semiconductor boules are grown by crystal pulling or seeded solidification from melts consisting of elemental (e.g. Si and Ge) or compound semiconductors (such as III-Vs and some II-VIs). Unfortunately, thermodynamic considerations render these approaches impractical at present for the production of industrial quantities of monocrystalline SiC. The SiC phase diagram [2] exhibits a peritectic at 2830°C with a total pressure of  $\sim 10^5$  Pa. Calculations suggest that stoichiometric melting occurs only at pressures exceeding  $10^5$  atm and temperatures  $> 3200^\circ\text{C}$  [3]. It is possible to create this type of growth conditions; for example those used for growth of small diamond crystals. However, such a process is currently not feasible for commercial production of large diameter semiconductor grade SiC. As the melt growth regime is not available, several alternative approaches have been investigated. The most common approach is Physical Vapor Transport which accounts for >90% of the supply of SiC wafers. Also, of increasing importance is High Temperature Chemical Vapor deposition (CVD) that is able to grow boules with exceptionally low impurity levels. Two further techniques that are in less common usage are the Sublimation Sandwich approach and Liquid Phase Epitaxy.

### 2.1. The Physical Vapor Transport Process

Large diameter SiC crystal growth is based on a modification of the original SiC sublimation method first developed by Lely [4] and extended later as a seeded sublimation technique by Tairov and Tsvetkov [5]. This latter method, more generically termed PVT, was further refined by Carter [10], Stein [6], and Barrett [7] for producing large diameter SiC boules, and various modifications of these techniques are now used at many laboratories worldwide. In general the source material is SiC powder that is heated

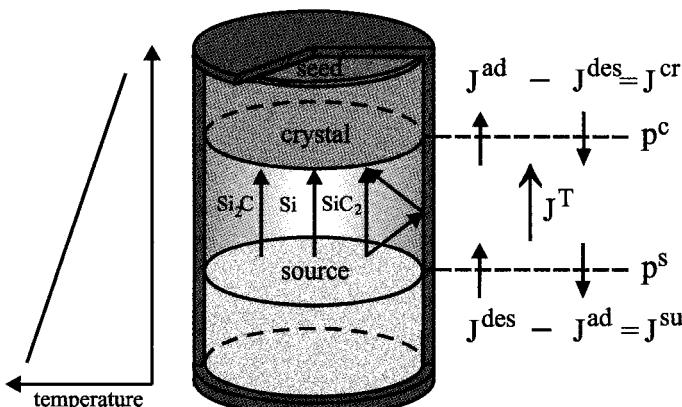


Fig. 1. Schematic of a SiC PVT growth crucible, and the mass transfer processes inside the crucible.  $J^{\text{ad}}$  and  $J^{\text{des}}$  are the adsorption and desorption fluxes.  $p^s$  and  $p^c$  are local partial pressures at the source and crystal, respectively [4].

to a temperature where significant sublimation can occur, Figure 1. As the region above the powder is kept at a lower temperature, the SiC gas species evolved (Si, SiC<sub>2</sub> and Si<sub>2</sub>C) will transport along the temperature gradient and condense on a seed SiC wafer placed at the cooler end of the crucible.

Although simple in concept the growth of SiC is complicated by the high temperature required (>2000°C) for significant sublimation to occur. This in turn limits the number of materials that will remain inert at these temperatures for the growth time required. The majority of groups utilize graphite to create the hot-zone of the furnace, though a limited number use components of Ta and TaC in the crucible. The SiC source is usually sublimed under partial vacuum conditions in the presence of a gas ambient (e. g. Ar, He, N<sub>2</sub>) which fills the growth chamber. The sublimation rate is to first order a function of the source temperature, the pressure of the ambient gas, and the thermal gradient in the system. Once a crystal has been grown, the crucible is typically dismantled and the crystal removed. It should be noted that one of the characteristics of the SiC boule is that compared to Si and GaAs crystals, for example, its aspect ratio tends to be low. One of the challenges facing the SiC industry is to grow substantially longer crystals. Figure 2 shows a sublimation grown boule produced by Dr. Nishizawa at ASIT in Tskuba, Japan. The boule is single crystal and at 100 mm this is the longest boule length published to date for SiC.

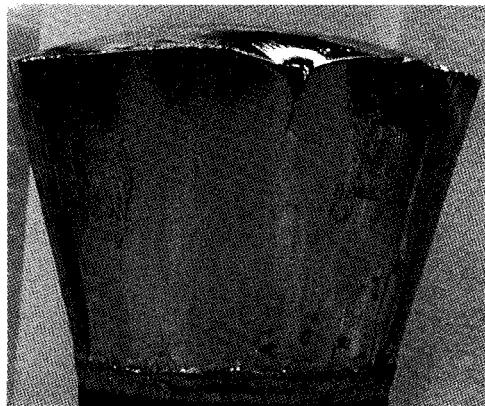


Fig. 2. 4-inch diameter SiC boule produced by the seeded sublimation technique. Photo courtesy Dr. Nishizawa of AIST.

## 2.2. Sublimation Epitaxy

Sublimation epitaxy involves the use of solid SiC as a source in a closed environment such as a graphite crucible. It is a very similar process to modified Lely boule growth except it typically takes place at lower temperatures (1800-2200°C), higher growth pressure (up to 1 atm), and with the source material close to or in intimate contact with the wafer. The greatest advantage of sublimation epitaxy over other epitaxial techniques

is the capability to grow at very high rates. There is of course an inherent limitation in that boules can not be grown to lengths longer than the seed-source distance, typically about 2 mm. Growth rates of up to 400  $\mu\text{m}/\text{hr}$  are achievable [8]. As with all viable boule growth techniques the grown material must be of higher quality than the seed. This improvement has been demonstrated for sublimation sandwich growth. A reduction in the dislocation density of sublimation epitaxial material over the density of the starting substrate has been demonstrated under certain conditions [9]. However, in the case of substrates with high micropipe or dislocation densities where domains of misoriented material are in close proximity, or in the case where there is a high degree of atomic plane curvature, this improvement does not occur as readily.

### **2.3. Liquid Phase Epitaxy**

Liquid phase epitaxy of SiC has been used for growth of epitaxial layers for devices for many years [66,10]. A wide range in doping level between  $10^{16}$  and  $10^{20} \text{ cm}^{-3}$  (both n- and p-type) has been obtained with growth rates as high as 150  $\mu\text{m}/\text{hr}$ . Difficulties in switching doping level and conductivity type during LPE have limited its usefulness. More recently, LPE has become of interest because of the ability of these layers to reduce the micropipe density in modified Lely substrates [11]. Initially, relatively thick layers were utilized with clear benefit in dislocation and micropipe reduction. More recent attempts involve much thinner layers but have still demonstrated improvement in crystalline quality over modified Lely substrate material [12]. The ability for LPE to fill micropipes is related to the fact that LPE is essentially an equilibrium growth technique and that any micropipes that are formed because of high supersaturation will no longer be energetically favorable.

### **2.4. High Temperature Chemical Vapor Deposition**

High temperature chemical vapor deposition (HTCVD) has been developed to obtain epitaxial quality material in a bulk growth process [13]. Potential advantages include the ability to directly control Si and C species concentrations, provide continuous source material, and grow with very high purity precursors. The main challenges for this approach are the delivery of the gas species to the hot zone of the reactor and the prevention of SiC deposits in the growth system. Figure 3 shows a schematic of a vertical growth system. Here the gas precursors are delivered at the base of the reactor in a carrier gas flow. Once in the system the gases react to create clusters of SiC in the central region of the hot zone. At the upper end of the reactor these SiC clusters sublime to provide the species needed for growth on the SiC seed crystal. The remaining gas then exits the growth system via holes in the upper region of the crucible. Typical growth temperatures are 1800-2300°C and growth rates can be as high as 1  $\text{mm}/\text{hr}$  [14], approaching that achievable by the modified Lely method. Both lightly doped and semi-insulating material [15] can be produced, with background impurity levels in the low  $10^{15} \text{ cm}^{-3}$  range [16]. This technique has the possibility of being utilized both for epitaxial layers for high-voltage devices as well as for substrate production.

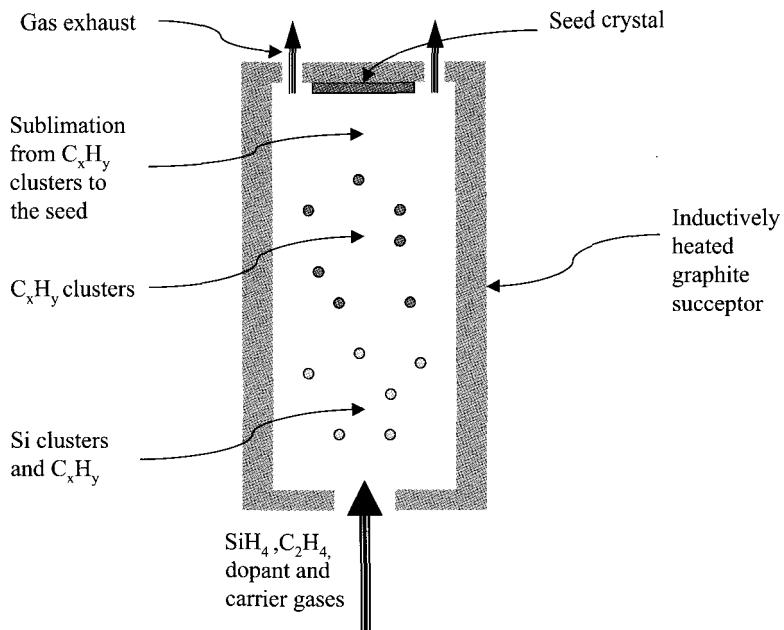


Fig. 3. Schematic showing the HTCVD process

### 3. Crystal Orientation

The majority of SiC produced today is utilized as a substrate for GaN epitaxy in the manufacture of blue and green LEDs and, as such, on-axis (0001) Si face material is desired. In addition there is also significant work with SiC homoepitaxy for which a slight offcut from the (0001) Si face is optimal. This offcut provides reduced surface terrace lengths, that in turn allow growth without the generation of 3C defects in the epitaxial layer, (typically either a 4° or 8° off cut is used). Typically this offcut is towards the <11-20> direction as this shows less roughening during the epitaxial growth [17]. As a consequence of this it is desirable to grow the crystals in a <0001> direction, or at an angle sufficiently close to the final wafer orientation so that the amount of material lost in the slicing operation is not a significant fraction of the boule.

There is also considerable interest in the fabrication of SiC devices on (11-20) surfaces where the channel mobility for MOSFET devices appears to be enhanced [18]. Substantial work by Ohtani [19] has shown that growth in the <11-20> direction is not only possible but may also be advantageous. In this growth direction there is no tendency for the SiC polytype to switch and the micropipe defect is not observed. There is a tendency for stacking faults to be created in this growth mode, but these can also be minimized through the use of a seed wafer that is orientated approximately 10° towards the <0001> direction from the <11-20> direction.

#### 4. Crystal Diameter Enlargement

Increasing substrate diameter is crucial for reducing the cost of SiC devices through economies of scale and the use of silicon or GaAs device fabrication equipment. However, growth of crack-free large diameter SiC crystals with high crystalline quality requires increased attention to system design and optimization of the thermal distribution in the growth environment to minimize excessive mechanical and thermoelastic stresses. Fig. 4 shows the progress in the growth of SiC crystals from less than 25 mm in the early 1990s up to current crystals, with diameters of 100 mm. This expansion has proceeded at a rate well in excess of that experienced in the silicon and GaAs industries, largely as a result of the crystal growth experience gained from these foregoing technologies.

Production volumes of 6H and 4H polytypes are now available at diameters up to 75-mm. Early prototype 75 mm diameter SiC wafers suffered from excessive low-angle grain boundaries near the wafer periphery. This problem has been circumvented in the intervening years allowing for the first time the extension of the PVT technique to the fabrication of fully single-crystal substrates with diameters up to 100 mm [20]. This represents a major step toward bringing SiC to parity with III-V compound semiconductors, such as GaAs, in available wafer area for device fabrication.

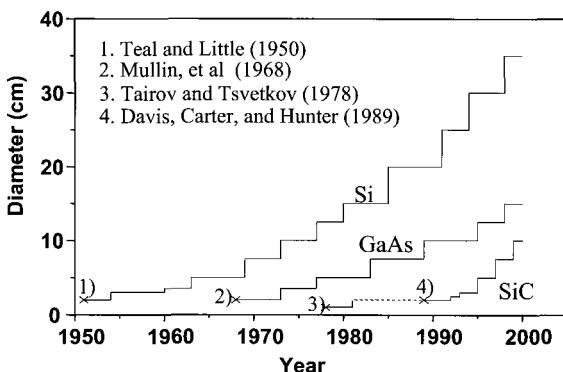


Fig. 4. Evolution of SiC diameter enlargement compared to silicon and GaAs technologies.

#### 5. Substrate Defects

Defects in nominally  $<0001>$  grown SiC include: polytype instabilities, open-core dislocations (called micropipes); low-angle boundaries; and conventional dislocations. Micropipe defects have historically prevented the commercialization of many types of SiC devices, especially high current power devices. However, recent improvements in growth techniques to reduce the micropipe density in substrates and epitaxial methods that cover these micropipes are enabling device production to be initiated. In the following section we will discuss the defects that occur in  $<0001>$  oriented growth.

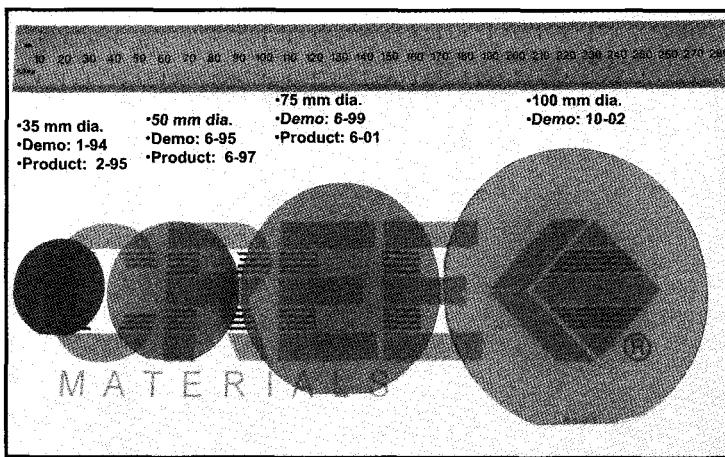


Fig. 5. Evolution of SiC diameter enlargement since 1994.

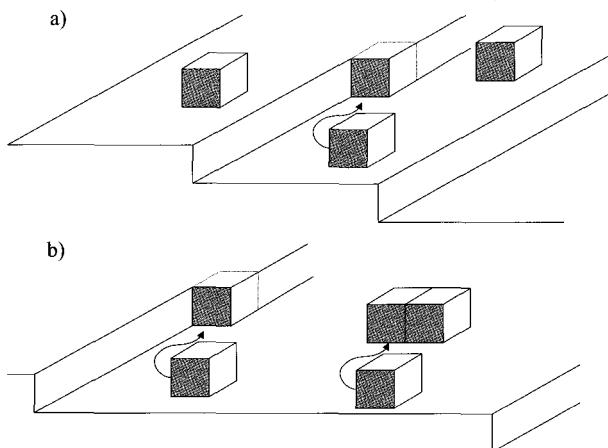


Fig. 6. Schematic of step modulated growth a) short terraces allow the diffusion of all arriving atoms to a step edge location for incorporation into the crystal, b) if the terrace size increases then arriving atoms may group into new growth nuclei without reaching the step edge.

### 5.1. Polytype stability

In SiC the difference between polytypes is essentially the stacking sequence of the Si-C bi-layers in the <0001> direction. Thus, to maintain a single polytype, the stacking sequence must remain involatile. This is relatively easy to achieve if growth is occurring by the propagation of steps across the SiC growth surface (Figure 6a). However, in SiC growth there is a tendency for step bunching which in turn leads to the formation of large terraces devoid of step edges. In this case, arriving Si and C atoms may not be able to diffuse to the step edges, and instead they may form new nuclei in the central regions of

the terrace (Figure 6b). These new nuclei may have differing bi-layer stacking sequences from the underlying material and thereby may initiate a change of polytype in the growing crystal.

There are a great many possible stacking sequences however, not all are commonly found. Figure 7 shows five of the more basic stacking sequences for SiC from the wurtzite structure, 2H (this polytype is not generally formed) through 4H, 15R, and 6H which each become less hexagonal in nature to the fully cubic 3C polytype.

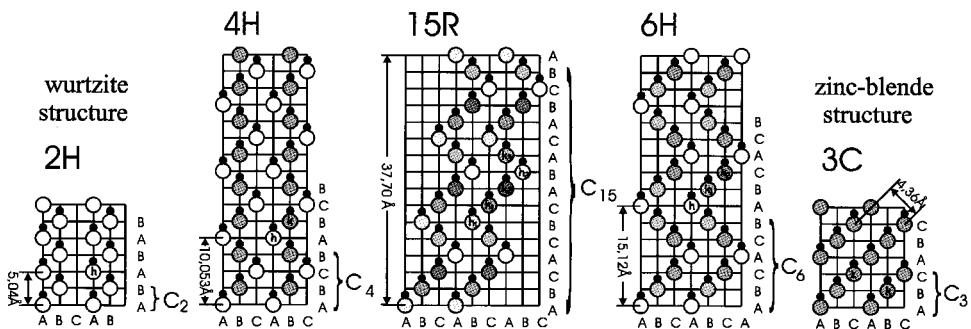


Fig. 7. Stacking sequences for five different SiC polytypes [21]



Fig. 8. Longitudinally sectioned SiC crystal exhibiting polytype switching.

In the manufacture of substrates it is clearly important to ensure that the entire wafer is of a single desired polytype. Owing to instabilities in growth conditions, spontaneous switching from one polytype to another may occur. In addition to altering the electrical properties of the material, this switching of polytype acts as a nucleation site for micropipes that then thread through the remainder of the boule material. Figure 8 shows a vertical slice of material from a boule where the polytype changes from 6H to 15R and

back several times. As a consequence of this, to produce low defect epitaxy it is key to ensure that the crystal polytype is maintained throughout the entirety of the growth process.

## 5.2. *Micropipes*

Most discussions about micropipe formation mechanisms revolve around Frank's theory [22] which associates the micropipe with a super screw dislocation that possesses a large Burgers vector, several times the unit cell dimension. The high strain energy density along the core of this super screw dislocation causes preferential sublimation during the growth process and consequentially the hollow core nature of the defect. Figure 9a shows a micropipe running vertically up through a slice of a SiC boule. The dark line is in fact a hollow tube in the material. In addition, the inside of the tube is often faceted indicating that growth and sublimation processes occur in the defect during the crystal growth process. The micropipe is in fact a super screw dislocation, and consequentially it acts as an extremely favorable growth site. This leads to the formation of growth spirals (Figure 9b) on the surface of the growing crystal. These growth spirals dominate growth on the basal facet of SiC boules and a single micropipe can generate a spiral pattern that is more than 1 cm across.

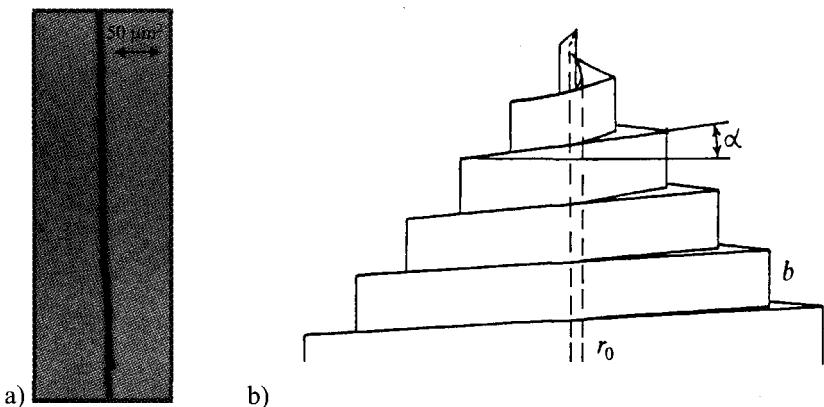


Fig. 9. a) a Cross-section of a SiC crystal showing a micropipe running in the  $<0001>$  growth direction b) Schematic of the super-screw dislocation intersecting the growth surface  $r_0$ = radius of pipe;  $b$  = Burgers vector;  $\alpha$  = spiral angle

The screw dislocation content of micropipes is indicated not only by the existence of growth spirals originating at micropipes, but also by the characteristic stress patterns around micropipes visible in stress birefringence [23], and by the results of synchrotron white beam X-ray topography (SWBXT) studies [24,25].

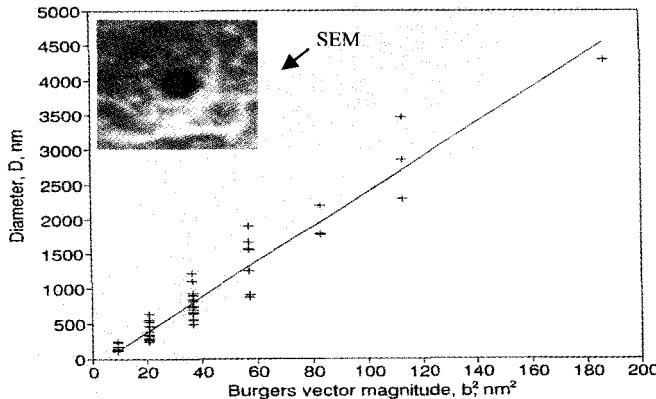


Fig. 10. Relationship between Burgers vectors measured using SWBXT, and hollow-core diameters measured using SEM [26].

Results from X-ray topography, Fig. 10, show a relationship between the magnitude of this Burgers dislocation and the diameter of the associated hollow core. Note, in 6H-SiC material, the critical Burgers vector magnitude above which micropipes tend to be generated is 3x the unit cell length [26]. Several mechanisms, or combinations of mechanisms, related to or specifically causing micropipes in SiC have been identified (Table I). In all these cases, one must consider the seed surface quality, the growth process stability and cleanliness, as well as the specific parameters controlling nucleation density and growth rate.

Table I. Mechanisms of micropipe formation.

Fundamental	
<u>Thermodynamic</u>	<u>Kinetic</u>
thermal field uniformity	nucleation processes
dislocation formation	inhomogeneous super-saturation
solid-state transformation	constitutional super-cooling
vapor phase composition	growth face morphology
vacancy super-saturation	
Technological	
process instabilities	seed preparation
contamination	

The characterization of micropipes can be achieved through a number of methods, but the most commonly utilized is to etch the SiC wafers in a bath of molten KOH at a temperature of 500°C. On the Si face (which has a relatively slow etch rate) the molten KOH can penetrate the hollow core of the micropipe, and then etch the available a-axis

face. The result of this preferential etching is shown in Figure 11 where on the Si face a large (100 micron diameter) pit has been etched out. If we consider the C face, this micropipe pit is much smaller in diameter and actually approximates to the true size of the micropipe. Typically the entire wafer can be characterized through examination of the Si face and etch maps such as Figures 12 and 14 provided.

Despite the different fundamental and technological reasons for micropipe formation, there has been a steady decrease in the micropipe density over the past several years. The analysis of defect-etched 4H-SiC wafers from low micropipe density boules has revealed areas up to 50 mm in diameter that are entirely free of micropipes. Fig. 12 corresponds to a digitized image of a 3-inch diameter 4H-SiC defect-etched wafer with a total of 10 micropipes corresponding to an overall density of  $0.22 \text{ pipes/cm}^2$ .

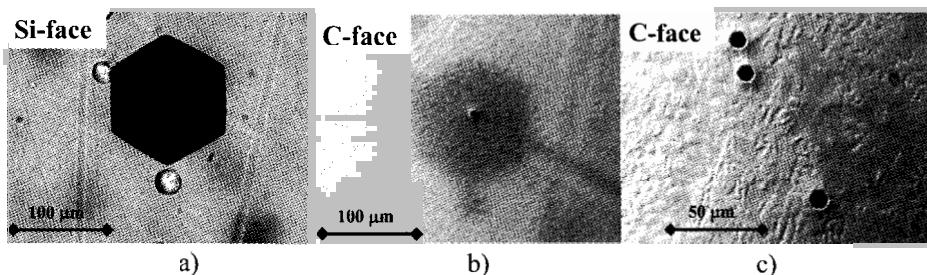


Fig. 11. Wafer surface after defect etching of a micropipe feature a) micropipe pit of the Si face, b) the same defect observed from the C face with through lighting, c) micropipe pits on the C face at a higher magnification.

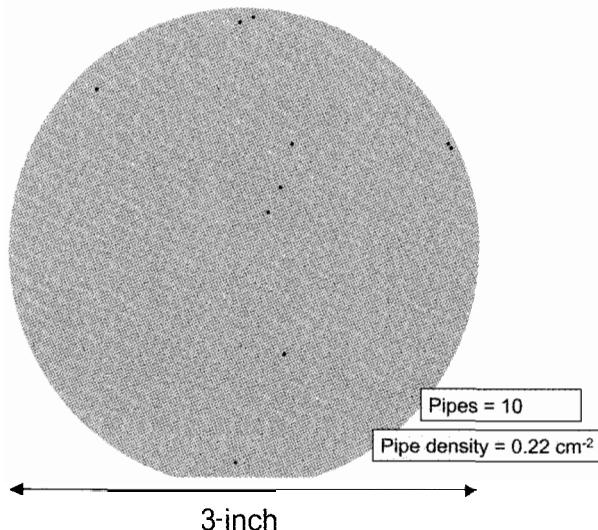


Fig. 12. 3-inch defect-etched 4H-SiC wafer with micropipe density of  $0.22 \text{ cm}^{-2}$

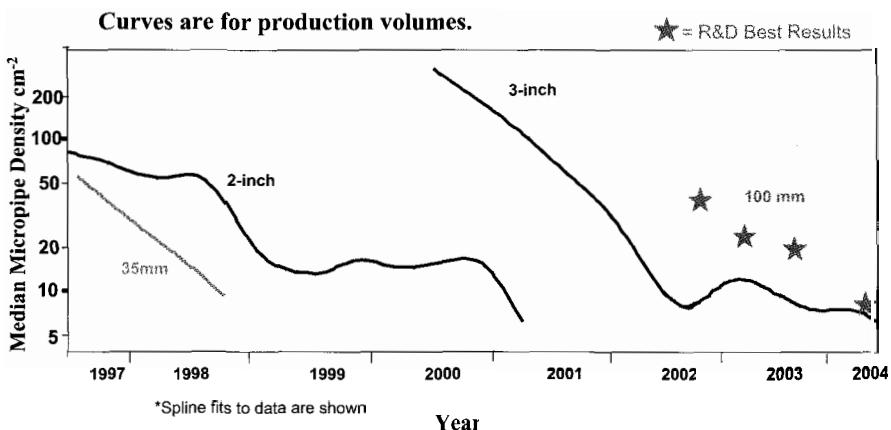


Fig. 13. Logarithmic plot of spline fits to the monthly median micropipe densities (MPD) for 35 mm, 2-inch, and 3-inch material. The four stars indicate the lowest MPDs obtained for 100 mm 4H material.

As the boule diameter is increased, it becomes more challenging to control all of the growth parameters in the system to the desired accuracy. As a consequence of this we transition from one diameter up to another we initially have an increased density of micropipe defects. This is shown in Figure 13 where the median micropipe density in production boules grown at Cree is shown. In addition this figure shows the present wafer quality level for 100 mm diameter wafers.

Of course the most pertinent measure of micropipe density is its effect on the yield of device structures. If we assume that a micropipe will cause a failure in a device grown over this defect [27], then we are able to create predictive yield maps for device structures grown on SiC wafers. Figure 14 shows such a map for 10 A Schottky diode structures

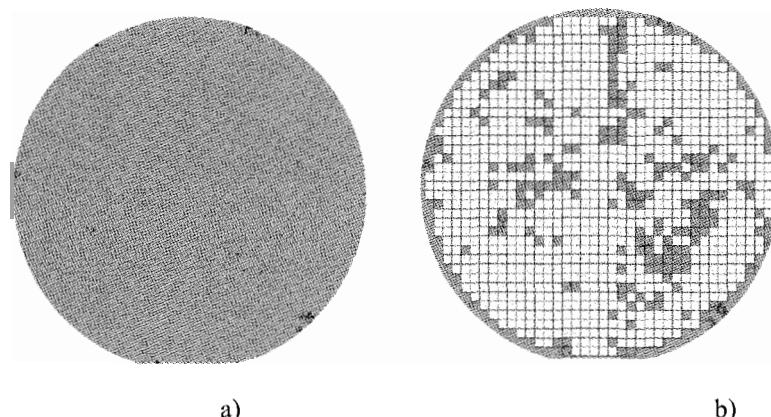


Fig 14. a) Micropipe etch map of 100 mm wafer showing a micropipe density of  $7 \text{ cm}^{-2}$ . b) Expected device yield map for the same 100 mm wafer showing a predicted yield of 83% for 10 A parts.

grown on one of our best 100 mm 4H SiC wafers. One should note that this assumes no failures due to epitaxial defects or device processing errors.

With the micropipe densities shown above, and additional work by Toyota Research Labs that has recently demonstrated 2-inch wafers free of micropipes[28], we do not believe that micropipe defects will be the limiting defects in the future for SiC devices.

### 5.3. Low Angle Grain Boundaries

Low-angle boundaries (LAGBs) near the crystal periphery tend to form with the growth of large diameter crystals grown under non-optimized process conditions. In SiC substrates, low angle boundaries are visible when the wafer is viewed through crossed polarizers (Figure 16a). These LAGBs represent the boundaries between regions of the SiC material that are slightly misaligned with respect to each other. This may be either a relative tilt of the (0001) planes or a rotation of the planes with respect to each other. Figure 15 illustrates three types of domain structure that can exist within any crystalline semiconductor wafer.

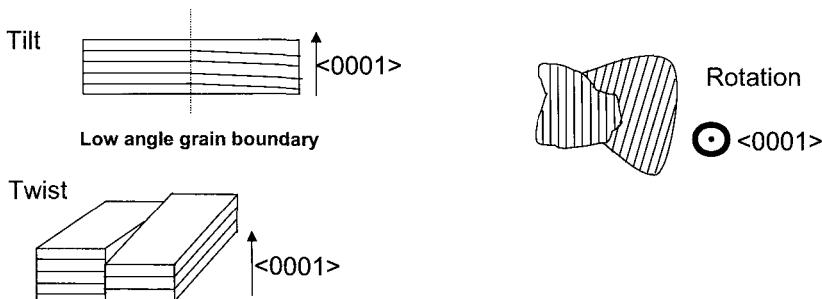


Fig. 15. Three types of mosaic structure that can be present in a semiconductor crystal. The Tilt and Twist types will be highlighted in a symmetric x-ray rocking curve, whereas an asymmetric x-ray rocking curve is required to show features due to rotation of the mosaic regions.

In addition to crossed polarizer images, double crystal X-ray diffraction can also be used to measure the LAGBs present in a wafer. If the more standard symmetrical reflection is used, then lattice tilts and twists will be observed. However, lattice plane rotations will not be observed. To see lattice plane rotations an asymmetrical reflection must be used that will reflect off a set of lattice planes that are not parallel with the wafer surface. In Figure 16c we show the asymmetric  $<2 -1 -1 9>$  X-ray rocking curve map (Tilt = 34 degrees). If one considers all three images, it can be seen that the contrast observable in the upper right section of the crossed polarizer image corresponds to a distortion in the asymmetric rocking curve map. This indicates that this feature is due to a rotated domain structure rather than a tilt or twist grain boundary.

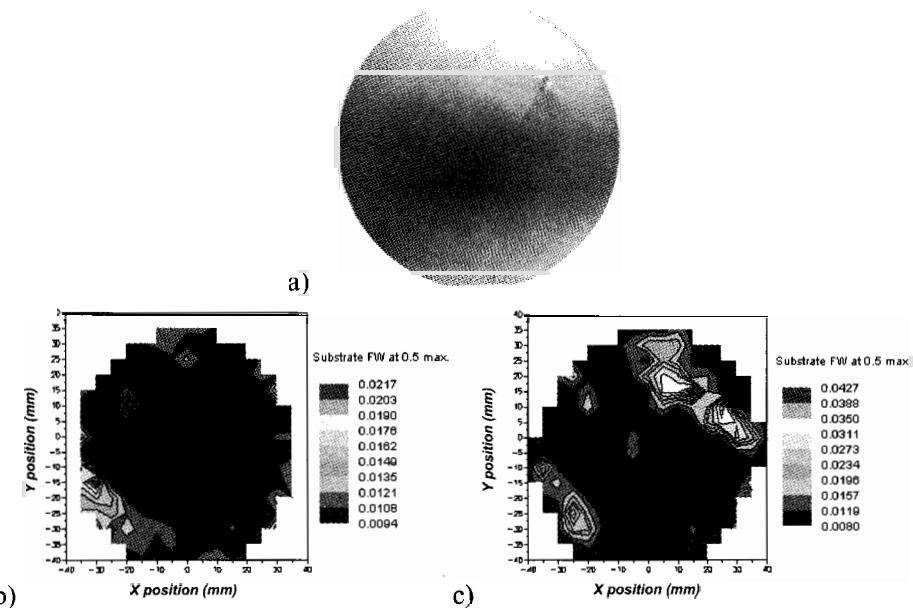


Fig. 16. Comparison of a) Cross polarizer image b) Symmetric  $<00012>$  X-ray rocking curve map and c) Asymmetric  $<2 -1 -1 9> >$  X-ray rocking curve map (Tilt = 34 degrees), of the same 3-inch diameter 4H wafer. In b and c the full width at half max values are plotted out for the wafer.

Grain boundaries generally consist of threading edge and screw dislocations, which will propagate throughout the entire boule and can be harmful to device structures. In addition, low angle grain boundaries can act as stress concentrators and increase the probability of wafer cracking at defect locations during the epitaxial growth process. For both these reasons it is desirable to reduce the density of low angle grain boundaries in the crystals. In Figs 17 and 18 we compare cross polarizer images of 75 and 100 mm wafers at early and later stages of development. In current commercial material the low

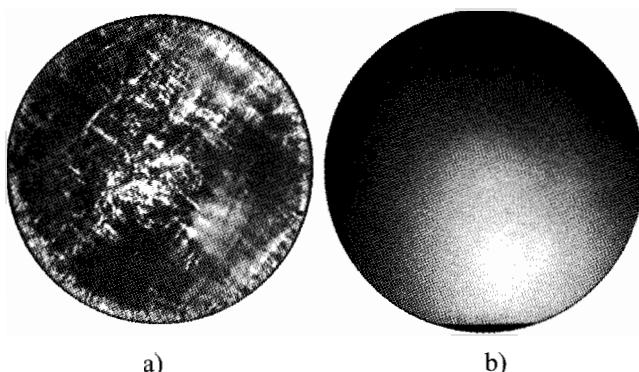


Fig. 17. Cross polarizer images of 3-inch 4H SiC wafers taken from a) November 1999 and b) September 2003.

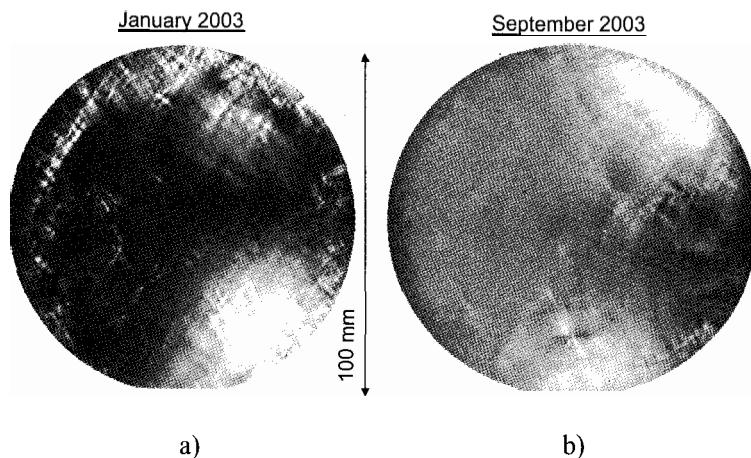


Fig 18. Cross polarizer images of 100 mm 4H SiC wafers taken from a) January 2003 and b) September 2003.

angle grain boundaries around the periphery of the wafer have been predominantly removed.

#### 5.4. Dislocations

The primary dislocations in commercial SiC substrates include micropipes (previously discussed), threading screw dislocations (TSDs), threading edge dislocations (TEDs) and basal plane dislocations (BPDs). Dislocations are considered to be problematic if they both propagate from the substrate into the epitaxial layer and then cause some measurable device degradation.

Dislocations originating in the substrate can change in character as they propagate into the epitaxial layer. Fig 19 shows the possibilities observed for differing dislocation types.

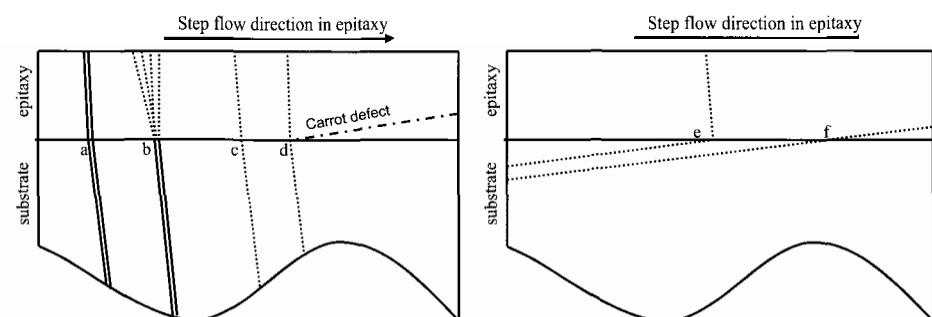


Fig. 19. Propagation of substrate defects into epilayers a) micropipe, b) micropipe to 11c dislocations, c) 1c dislocation, d) 1c dislocation to carrot defect and 1c dislocation, e) basal plane dislocation to threading edge dislocation, f) basal plane dislocation

As shown in Figure 19, micropipes can propagate directly into the epitaxial layer (a), or can dissociate at the substrate / epi interface into multiple closed core TSDs (b) [29].

Closed core TSDs, also depicted by c in Fig 19, are a concern for a number of device structures since they may contribute to premature breakdown [30]. Commercially available 3-inch SiC material typically has a TSD density of  $10^3$  to  $10^4 \text{ cm}^{-2}$ . In addition to simply propagating into an epilayer, TSDs may also spawn other epitaxial defects such as the carrot defect [31] shown as d in Fig. 19.

Threading edge dislocations (TEDs) are another class of defect in SiC substrates that may propagate into epilayers, in a manner similar to c in Fig. 19. TEDs are generally dispersed in SiC substrates at a density of about  $10^4 \text{ cm}^{-2}$ . In addition, TEDs also define low angle grain boundaries. Though clearly not desirable, these defects are considered to be less harmful to SiC devices than TSD and BPDs.

The last remaining class of defects that can propagate from substrates to epilayers are basal plane dislocations (BPDs). Typically the density of BPDs in commercial substrates ranges from  $10^3$  to  $10^4 \text{ cm}^{-2}$ . To take advantage of step-flow growth, SiC epilayers are usually grown on substrates cut off-axis by  $4\text{--}8^\circ$  so the basal plane of the crystal is tilted in respect to the wafer surface. Consequently, BPDs can propagate directly into the epitaxial layer from the substrate as shown by e in Fig 19. Most BPDs convert into the more benign TEDs during epilayer growth[32] (Figure 19f). However, any BPDs that do propagate into the epitaxy comprising the active area of the device can cause  $V_f$  drift in bipolar devices [33].

Characterization of these defects is again typically achieved through the use of a defect revealing molten KOH etch. These results can also be correlated with X-ray topography [34,35] to confirm the type of dislocation present. Figure 20 shows the type of pit observed for a 1c screw dislocation observed on the C face of a SiC wafer. Typically this is the only defect type that creates a significant pit on the C face.

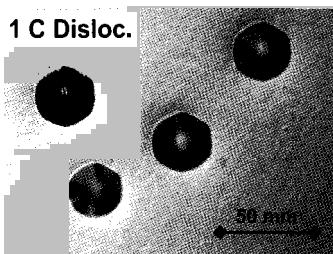


Fig. 20. Threading screw dislocations create relatively large pits on the C face of the wafers

Characterization of threading edge and basal plane dislocations is done on the Si face of the wafer. In Figure 21, a wafer with a 4-degree offcut is used so that the basal plane dislocations do intersect the surface. In this figure they produce elongated pits that run towards the top right of the image. 1c screw dislocations create a more circular and deeper pit that can be recognized by defect counting software.

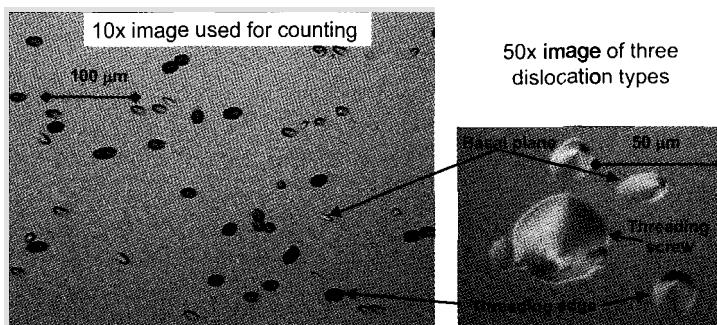


Fig. 21. Wafer surface after KOH etch to reveal dislocations. Three typical dislocation types are observed: threading screw, threading edge, and basal plane.

## 6. Doping in SiC

The main n- and p-type dopants in SiC are N and Al respectively. These are preferred because they create relatively shallow donor and acceptor levels in the SiC bandgap. Nitrogen incorporation is a function of the  $N_2$  partial pressure in the growth environment. For Al, the dependence is also roughly linear with Al concentration up to the  $10^{20} \text{ cm}^{-3}$  range. Nitrogen incorporation decreases with increasing growth temperature, [36] while Al incorporation increases. Further information may be found in a recent review by Rost [37].

The maximum attainable resistivity in undoped SiC crystals is limited principally by residual nitrogen and boron in the growth environment. Reduction of boron content in SiC is particularly difficult since it exhibits a transfer coefficient of near unity [38]. The extent to which these impurities dominate the electrical behavior of the undoped SiC crystals grown by PVT is largely a function of the purity of the source materials and the cleanliness of the growth system. Concentrations of nitrogen and boron in bulk crystals can be reduced to mid  $10^{15} \text{ cm}^{-3}$  level. In material of the highest purity, elemental metallic impurities typically exhibit concentrations  $\leq 0.01 \text{ ppmwt}$  and transfer coefficients less than unity.

Table II. Thermal Conductivity of SiC (T=300K)

<u>Crystal</u>	<u>Direction</u>	<u>Carrier (cm<sup>-3</sup>)</u>	<u><math>\kappa_{th}</math> (W/cm·K)</u>
4H-n-type	a	$5.0 \times 10^{15}$	4.9
4H n-type	c	$5.0 \times 10^{15}$	3.9
4H n-type	c	$2.0 \times 10^{18}$	3.3
4H s. i.	a	--	4.7
4H s. i.	c	--	3.7

For heat dissipation in high power density device structures, the thermal conductivity of the substrate is critical. Our data (Table II) indicates that at sufficiently low overall impurity content where isotope scattering can be neglected, the thermal conductivity in

bulk SiC shows a significant dependence on the free carrier concentration (electron-phonon scattering [39]). Thus, in bulk crystals exhibiting low impurity content, e.g. showing semi-insulating ( $>10^7 \Omega\text{-cm}$ ) behavior, the thermal conductivity approaches 5 W/cmK for heat flow directions perpendicular to the c-axis. This value is close to that determined by Slack for Lely-grown samples [40]. However, an appreciable reduction in heat conduction parallel to the c-direction is also observed, consistent with previous results [41]. For n-type doped material at the  $2 \times 10^{18} \text{ cm}^{-3}$  (typical for power device structures) it can be seen that the thermal conductivity in the c direction has decreased slightly (by 20%) from the high purity case, but is still significantly higher than that for Si (1.3 W/cmK) or GaAs (0.5 W/cmK) at similar doping densities.

## 7. SiC Substrates for Microwave Devices

One of the challenges for microwave devices is the loss of signal due to capacitive interactions with the substrate material. An effective way to remove this loss is to use an insulating or semi-insulating substrate. Additionally, microwave devices, such as homoepitaxially grown SiC MESFETs, require a semi-insulating 4H-SiC substrate owing to the high carrier mobility of the 4H polytype. The creation of this semi-insulating 4H-SiC substrate requires two key components. First, a deep electronic level is necessary to trap either electrons or holes and to supply a large activation barrier to their subsequent release. Second, control of shallow level impurities is required to supply proper compensation to the intended deep electronic level to optimize the Fermi-level can be pinned to the deep electronic level. In practice residual dopant levels provide sufficient shallow levels to supply this compensation, and the challenge is to ensure that the net concentration of carriers from the shallow levels is lower than the available density of states from the mid bandgap states. Thus, to achieve semi-insulating 4H-SiC one must reduce the density of shallow levels, and simultaneously provide a density of deep levels in the bandgap, at a concentration greater than the net density of shallow levels.

### 7.1. Shallow Electronic Levels

Typically in semiconductor systems, the term shallow electronic level implies a level residing quite close to either the valence or conduction band edges (usually within 100 meV). As silicon carbide is a wide bandgap material, this definition is expanded to include not only nitrogen ( $E_C - 40 \text{ meV}$ ) but also boron, even though, in the 4H polytype, boron resides  $\sim 350 \text{ meV}$  above the valence band edge. Table III is a listing of impurities in typical high purity wafers that have been analyzed using a calibrated SIMS technique. Of the principal shallow level impurities, only boron and nitrogen are present in appreciable quantities, typically  $5 \times 10^{15} \text{ cm}^{-3}$  and  $3 \times 10^{15} \text{ cm}^{-3}$ , respectively. These concentrations have been reduced by almost two orders of magnitude during the past three years, as the process has been refined. This reduction has significantly expanded our ability to successfully grow semi-insulating material.

Table III. SIMS analysis of high purity semi-insulating (HPSI) 4H-SiC material.

Element	Concentration [cm-3]
B	3.00E+15
N	5.00E+15
Na*, Al*	<5.00E+13
Ti*	1.00E+14
V*, Cr*	5.00E+13
Fe*, P*	2.00E+14
Ni*, F*	5.00E+14
Cu*	3.00E+14
O#	4.00E+16
As*	7.00E+14
* value at SIMS detection limit	
# value at instrument background limit	

The detection limit for nitrogen in SiC in a SIMS chamber well conditioned for this specific purpose has typically been  $2\text{e}15 \text{ cm}^{-3}$ . As the typical nitrogen concentration has been reduced in SiC crystals, the nitrogen in our R&D best wafers has fallen below this SIMS detection limit, and a new method of nitrogen quantification was required. To solve this problem a technique borrowed from SiC epitaxy, low temperature photoluminescence (LTPL), has been employed. In LTPL, the ratio of the  $Q_0$  and the  $I_{75}$  intensities have been shown to be proportional to the nitrogen concentration [42]. Using LTPL, we have demonstrated a nitrogen concentration of  $3\text{E}14 \text{ cm}^{-3}$  [43]. This value is the lowest ever reported for nitrogen in bulk-grown SiC.

## 7.2. Deep electronic levels

Early work on producing semi-insulating SiC [44] concentrated on adding a deep level in the bandgap associated with a metallic impurity (Vanadium). Other metallic impurities were tried, but none provided acceptable mid-bandgap levels. More recent work [45] demonstrated that the vanadium related defect has a large capture cross-section. Thus vanadium is unsuitable as a provider of the deep level in semi-insulating SiC owing to deleterious trapping of charge in SiC MESFET devices. The solution to this dilemma has been to simultaneously reduce the net carrier concentration due to shallow levels and adjust growth conditions to enhance the creation of defects that produce deep levels in the 4H-SiC bandgap. This material is termed High Purity Semi Insulating (HPSI) SiC. One of the major challenges in this field has been to identify specific defects responsible for the electronic nature of HPSI SiC. We have utilized a number of techniques including temperature dependent resistivity (TDR)[46], optical admittance spectroscopy (OAS)[47], deep level transient spectroscopy (DLTS) [48], and electron paramagnetic resonance (EPR) [49] to help this characterization.

We have employed TDR in conjunction with OAS to identify the electronic levels present in HPSI material. Temperature dependent resistivity measurements of representative HPSI samples have shown activation energies of 0.9, 1.1, 1.2, 1.35, 1.5

and 1.6 eV. In addition, analysis of OAS data (Figure 22) reveals five separate activation energies in a single sample with significant similarity between the TDR data and the OAS spectrum.

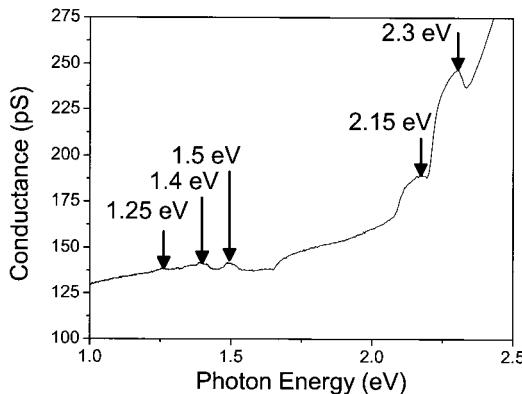


Fig. 22. Optical admittance versus photon energy revealing the presence of 5 distinct energy levels. Courtesy of W.C. Mitchell and S. Smith[50].

With the discovery of multiple activation energies in a large number of HPSI SiC samples, it is possible that multiple point defects are responsible for the semi-insulating character of the wafers. The types of point defects may not be as numerous as that of the electronic levels because deep levels may introduce multiple energy levels, as is the case of vanadium in SiC [51,52]. To resolve the specific trapping mechanism, the structure of the various defects responsible for the electronic levels must be determined. Magnetic resonance techniques were used on irradiated material and have identified several intrinsic point defects in SiC, including the carbon vacancy, the silicon antisite, and the carbon vacancy-carbon antisite pair [53, 54]. Subsequent analysis has shown that each of these defects is present in as-grown SiC [55], and point to the carbon vacancy as one of the principal deep level defects in HPSI.

In addition to the carbon vacancy, several other intrinsic point defects have been identified in as-grown HPSI material, including the carbon vacancy-carbon antisite pair, the silicon vacancy, and the silicon antisite. Other defects may be present, including ones that may be diamagnetic, and therefore not observable by EPR. After identifying several point defects, the next step in gaining improved control over the HPSI growth process is to identify the principal point defect or defects responsible for the deep electronic levels in HPSI material. This step involves the quantification of respective deep level concentrations, identification of capture cross-sections, and determination of the defect's electronic structure, each of which is underway.

### 7.3. Current status of HPSI material

Although challenging, the production of HPSI 4H-SiC substrates has been achieved, with 75-mm wafers being commercially available [56] and 100-mm HPSI wafers in development. Figure 23 is a high-resolution resistivity map of a typical 100-mm diameter HPSI wafer with a resistivity  $>2\times10^{11} \Omega\text{cm}$ . These very high resistivity levels can be achieved due to the breadth of the 4H-SiC bandgap.

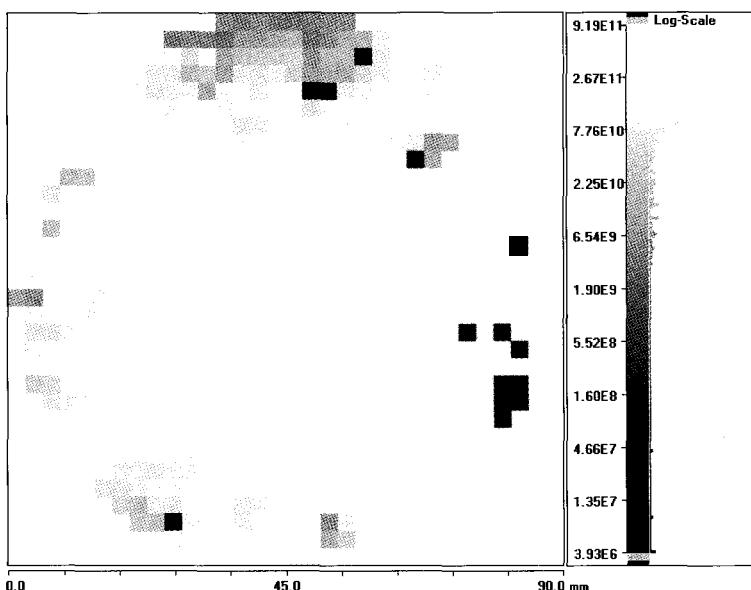


Fig. 23. High resolution resistivity map of a 100-mm diameter 4H-SiC HPSI wafer. The wafer is uniformly semi-insulating with a resistivity  $>2\times10^{11} \Omega\text{cm}$ .

## 8. Wafering and Polish

The fabrication of SiC boules into wafers is challenging due to the hardness (only diamond, boron nitride and boron carbide have higher Mohs values) and chemical stability of SiC (few effective etches are known for SiC, the most commonly utilized is molten KOH salt at 450°C). Typical processing steps are boule slicing, rough polish, and final chemical mechanical polish (CMP).

### 8.1. Boule Slicing

There are a multiplicity of options for slicing SiC boules into wafers, here we will discuss three approaches, inner diameter (ID) blade saws, fixed abrasive wire saws and slurry based wire saws.

ID slicing has been available for many years and provides a reliable method of producing SiC wafer blanks. The cutting surface is on the inner surface of a thin annular

blade. This blade is rotated at speeds up to 1500 rpm [57], the boule is positioned within the center region of the blade and slowly moved towards the circumference of the saw blade. This process enables only one wafer to be sliced at a time, however the system is typically automated thereby allowing entire boules to be sliced.

Over the past fifteen years the use of wire saws has become more popular. For wire saws, the abrasive can either be directly attached to the wire, or contained in a cutting slurry that coats the wire. For the former of these cases the diamond particles are bonded to the wire and this wire is drawn across the crystal allowing the diamond particles to cut at the exposed surface. Typically wires for this operation are 1 km or longer and this wire is drawn across the crystal many times in order to slice a wafer off the end of the boule. This type of fixed abrasive saw can be manufactured in both a single wire mode and a multiple wire modes [58]. Note that in the multiple wire modes only one wire is used, but it is wrapped around a set of spindles multiple times so that the entire boule can be sliced in one cutting operation. In a “multi wire saw” the wire is fed into one end of the mesh and collected on a spool after it has run through the entire mesh.

In the slurry saw case, a plain wire is used and this wire is again drawn over the crystal in order to slice [59]. In this case the cutting medium (either diamond or boron nitride particles in a slurry) is generally sprayed onto the wire immediately before it passes across the crystal. Typically these saws are configured in the “multi wire mode and the wires used on this type of saw are many kilometers long. The main advantage provided by the wire saw approach compared to the traditional ID saw is the low kerf loss achievable. This in turn allows a greater number of wafers to be sliced from each boule.

## 8.2. Polish

Following the slicing step, the wafers are polished using diamond slurries. As is typical for polishing operations the initial step utilizes larger diamond particle sizes. The degree of surface roughness and sub-surface damage present on the wafer is generally proportional to the size of the polishing particles used. Consequentially this dictates that polishing will progress through a series of steps each using a progressively smaller diamond grit size. This mechanical polishing will inevitably leave a thin layer of damaged material at the surface. The result of this damaged layer can be seen in Figure 25 where the homoepitaxial SiC film grown over a poorly polished wafer shows new defects originating from the substrate/film interface.

One method to remove this residual sub-surface damage is to remove the damaged layer with a reactive ion etch. However, although this provides a surface with minimized sub-surface damage, the surface roughness ( $R_a$ ) is in the 0.5 nm range [60]. In the last few years a CMP processes for SiC have been developed [61,62] that show a significant reduction in sub-surface damage levels. The current generation of CMP processes remove material at very slow rates and consequently are generally utilized as a final step after initial polishing with diamond slurries. However, these CMP processes are capable of providing smooth damage free surfaces. This is shown in Figure 26 a) where an AFM image of a CMP surface is shown to be atomically flat. In Figure 26 b) an optical image

of a CMP surface after a KOH defect etch is also shown. Here the only observable features are pits caused by dislocations in the substrate material. For comparison, the insert shows the surface of a defect etched wafer that did not receive the CMP polish. This CMP surface now provides an ideal surface for homoepitaxial SiC growth.

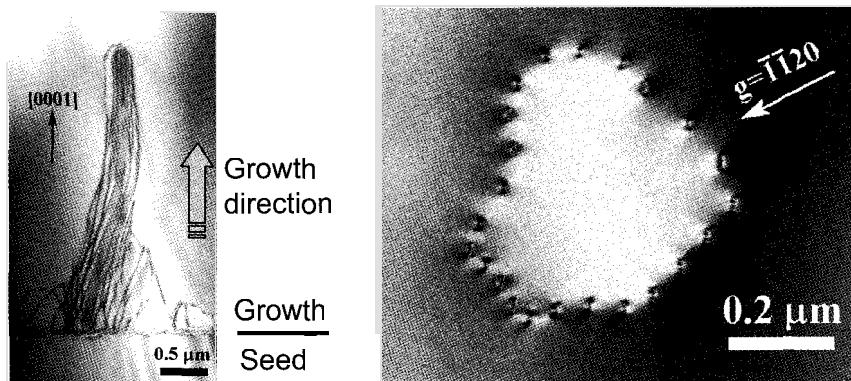


Fig. 25. a) Cross sectional and b) planar, TEM views of dislocation arrays in material deposited on a mechanically terminated SiC surface. Courtesy of Marek Skowronski of CMU

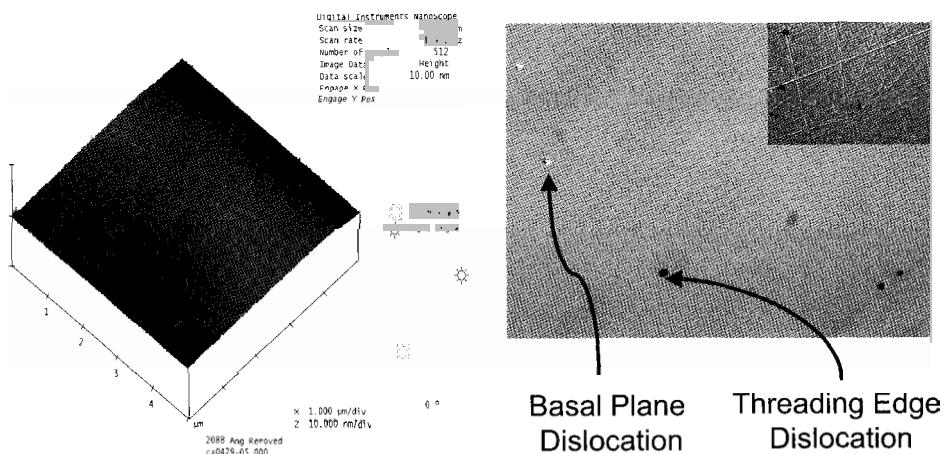


Fig. 26. Images of the surface of a wafer with CMP a) AFM image, b) optical image of sample following a defect etch; insert is for a non CMP wafer.

## 9. Substrate Cost

Historically one of the barriers to the development of SiC as a semiconductor has been the high cost of the substrates. Figure 27 shows that in 2001 n-type material sold for \$100 cm<sup>-2</sup>. However, over the last 5 years the price has reduced by 6x to a current

(Jan 2005) level of \$17 cm<sup>-2</sup> for volume purchases. Both yield improvements and the increasing diameter of the SiC wafers have driven this price reduction.

Although the substrate cost currently represents a relatively small fraction of the total device cost, it remains critical to further reduce the substrate price. To achieve this, the yield of the crystal growth process must be improved, along with cost reductions in the production line. Yield improvements will be driven by developments such as: increasing boule lengths; minimizing defective wafers, and minimizing losses in wafering and polish.

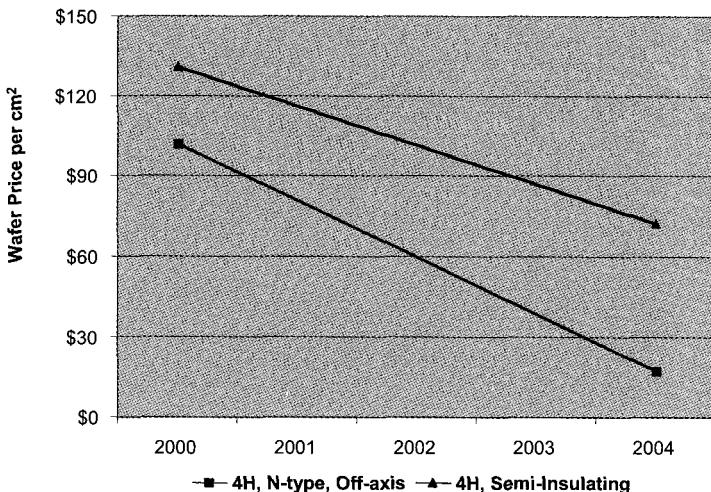


Fig. 27. Plot of the reducing price per cm<sup>2</sup> of n-type and semi-insulation 4H SiC material over the past 5 years

## 10. Conclusions

In recent years the quality and price of 3-inch 4H-SiC substrates and epitaxy have progressed to the point where power devices are a viable commercial product, the first of these being 600 V Schottky diodes, introduced in 2001. For these devices the key driver is now cost. Thus, reducing the cost of low micropipe 3-inch substrates and progressing to 100-mm wafer and epitaxial capability are critical milestones for the industry. For the development of high power PiN diodes and other bipolar devices the outlook is very promising. Recent work by J. Sumakaris [63] has demonstrated that SiC epitaxy can be grown on SiC substrates with an extremely low density of basal plane dislocations, thereby avoiding the V<sub>f</sub> drift problems previously observed in operating PiN diodes [64]. Consequentially, we currently see no further technical roadblocks in the development of a commercial bipolar product. SiC microwave devices are also currently available on HPSI 4H-SiC substrates. In addition to the progress observed for SiC epitaxial devices, GaN-based epitaxial structures such as LEDs are produced on SiC substrates. The size, quality, and cost of SiC wafers is now supporting a healthy and growing SiC industry.

## Acknowledgments

Much of the work reported here was supported by DARPA Contracts N00014-02-C-0306, N00014-02-C-0302, and Title III contract F33615-99-C-5316. We would like to recognize that this work represents the combined efforts of the crystal growth team at Cree Inc. which includes; this articles authors, M.F. Brady, D. Malta, and M. Calus. In addition the authors acknowledge to R. Trussell, for X-ray characterization, M. Laughner for CMP development and Prof. M. Skowronski and Prof. M. Dudley for defect characterization and discussions.

## References

- 1 R. F. Davis, G. Kelner, M. Shur, J. W. Palmour, and J. A. Edmond, "Thin film deposition and microelectronic and optoelectronic device fabrication and characterization in monocrystalline alpha and beta silicon carbide", Proc. IEEE, vol. 79, pp. 677-701, 1991.
- 2 R.I. Scace and G.A. Slack, "Solubility of carbon in silicon and germanium". J. Chem. Phys., 30, p. 1551, 1959.
- 3 V.F. Tsvetkov, S.T. Allen, H. S. Kong, C.H. Carter,Jr., "Recent progress in SiC crystal growth". Inst. Phys. Conf. Ser. No. 142, 1996.
- 4 J.A. Lely, "Darstellung von einkristallen von silizium carbid und beherrschung von art und menge der eingebauten verunreinigungen". Ber. Dt. Keram. Ges., 32, p. 299, 1955.
- 5 Yu. M. Tairov and V.F. Tsvetkov, J. Crystal Growth, 43, p. 209, 1978.
- 6 R.A. Stein et al, "Influence of surface-energy on the growth of 6H SiC and 4H SiC polytypes by sublimation". Mat. Sci. Eng. B, 11, p. 69 , 1992.
- 7 D.L.Barrett, et al."Growth of large SiC single crystals". J. Crystal Growth, 128, 1993.
- 8 M. Syväjärvi et al., "High growth rate of  $\alpha$ -SiC by sublimation epitax", Mater. Sci. Forum, vol. 264-268, pp. 143-146, 1998.
- 9 M. Syväjärvi, R. Yakimova, H. Jacobsson, and E. Janzén, "Structural improvement in sublimation epitaxy of 4H-SiC", J. Appl. Phys., vol. 88, pp. 1407-1410, 2000.
- 10 V. Dmitriev, "LPE of SiC and SiC-AlN", in *Properties of Silicon Carbide*, G.L. Harris, Ed., EMIS Data Review Series No. 13, London: INSPEC, 1995, pp. 214-227.
- 11 V.A. Dmitriev, S.V. Rendakova, V.A. Ivantsov, and C.H. Carter, Jr., "Method for reducing micropipe formation in the epitaxial growth of silicon carbide and resulting silicon carbide structures", United States Patent 5,679,153, October 21, 1997.
- 12 E. Kalinina, et al., "Material quality improvements for high voltage 4H-SiC diodes", Mater. Sci. Eng., vol. B180, pp. 337-341, 2001.
- 13 O. Kordina, et al, "High temperature chemical vapor deposition of SiC", Appl. Phys. Lett., vol. 69, pp.1456-1458, 1996.
- 14 A. Ellison, et al., "SiC crystal growth by HTCVD", Mater. Sci. Forum vol457-460, 2000, pp. 9-14.
- 15 A. Ellison, et al., "HTCVD growth of semi-insulating 4H-SiC crystals with low defect density", Mat. Res. Soc. Symp. Proc., vol. 640, 2001.
- 16 A. Ellison, et al., "Fast SiC epitaxial growth in a chimney CVD reactor and HTCVD crystal growth developments", Mater. Sci. Forum vol. 338-342, 2000, pp. 131-136.

- 17 H. S. Kong, J. T. Glass, and R.F. Davis, "Chemical vapor deposition and characterization of 6H-SiC thin films on off-axis 6H-SiC substrates", *J. Appl. Phys.*, vol. 64, pp. 2672-2679, 1988.
- 18 H.Yano, T.Hirao, T.Kimoto, H.Matsanami, K.Asano, and Y.Sugawawa, *Mater. Sci. Forum* **338** 1105 (2000).
- 19 N. Ohtani, M. Katsuno, T.Fujimoto, and H.Yashiro. p 137 "Silicon Carbide Recent Major Advances" Springer –Verlgag Berlin Heileburg 2004.
- 20 H. McD. Hobgood, et al., "Status of large diameter SiC crystal growth for electronic and optical applications". *Matls. Sci. Forum*, 338-342 (2000) 3.
- 21 St. G. Mueller, Herstellung von Siliziumkarbid im Sublimationsverfahren, Shaker Verlag, Aachen p. 90, 1998.
- 22 F.C. Frank, " Capillary equilibrium of dislocated crystals". *Acta Cryst.*, 4, p. 497, 1950.
- 23 St. G. Mueller, Herstellung von Siliziumkarbid im Sublimationsverfahren, Shaker Verlag, Aachen p. 90, 1998).
- 24 Si W, Dudley M, Glass R, et al. "Experimental studies of hollow-core screw dislocations in 6H-SiC and 4H-SiC single crystals". *Mater Sci Forum* 264-2: 429-432 Part 1-2 1998 .
- 25 X.R. Huang, M. Dudley, W.M. Vetter, W. Huang, W. Si, and C. H. Carter, Jr., "Superscrew dislocation contrast on synchrotron white-beam topographs: an accurate description of the direct dislocation image". *J. Appl. Crystallography*, 32, p. 516, 1999.
- 26 W.M. Vetter and M. Dudley, "Micropipes in silicon carbide crystals: Do all screw dislocations have open cores?". *J. Matl. Res.*, 15, p. 1649, 2000.
- 27 R.Rupp, M. Treu, P.Turkes, H.Beerman, T.Scherg, H.Preis, H.Cerva. *Mat Sci Forum* Vols 483-485 (2005) pp 925.
- 28 D. Nakamura, et al "Ultrahigh-quality silicon carbide single crystals. *Nature* 430 (2004) p 1009.
- 29 H.Tsuhida, I.Kamata, T.Jikimoto, T.Miyangi and K.Izumi., *Mat. Sci. Forum* 433-336, p131 2003.
- 30 P. G. Neudeck, "Electrical impact of SiC stuctural crystal defects on high electric field devices", *Matls. Sci. Forum*, 338-342 p.1161 2000.
- 31 X. Zhang, S. Ha, M. Benamarra, M. J. O'Loughlin, J. J. Sumakeris and M. Skowronski, *Applied Physics Letters*, submitted July, 2004.
- 32 U.S. patent application Serial No. 10/605,312 (2003).
- 33 H. Lendenmann, F. Dahlquist, N. Johansson, R. Söderholm, P.A. Nilsson, J.P. Bergman and P. Skytt, *Mater. Sci. Forum* Vol. 353-356 (2001) p. 727.
- 34 W. Si, M. Dudley, R. Glass, V. Tsvetkov C.H. Carter, Jr., *J. Elect. Matls.*, 26, p. 128, 1997.
- 35 CMU defect etch paper.
- 36 S. K. Lilov, Yu. M. Tariov, V. F. Tsvetkov, " Investigation of nitrogen solubility processes in Silicon carbide". *Krist. Tech.* 14, p. 111, 1979.
- 37 H.J.Rost, D.Schulz, and D.Siche. p 163 "Silicon Carbide Recent Major Advances" Springer –Verlgag Berlin Heileburg 2004.
- 38 R.C. Glass, et al., " The role of residual impurities in SiC grown by physical vapor transport". *Inst. Phys. Conf. Ser.* No. 142, p. 37, 1996.
- 39 D.T. Morelli, J.P. Heremans, C.P. Beetz, W.S. Yoo, and H. Matsunami, "Phonon-electron scattering in single crystal silicon carbide". *Appl. Phys. Lett.*, 63, p. 3145, 1993.
- 40 G.A. Slack, *J. Phys.* "Nonmetallic crystals with high thermal conductivity". *Chem. Solids* 34, p.321, 1973.

- 41 L.A. Burgemeister, W. von Muench, and E. Pettenpaul, "Thermal conductivity and electrical properties of 6H silicon carbide". *J. Appl. Phys.*, 50, p. 5790, 1979.
- 42 I. G. Ivanov , C. Hallin, A. Henry, O. Kordina and E. Janzen: *J. Appl. Phys.* **80** (1996) 3504.
- 43 Measurement courtesy of Jim Choyke, University of Pittsburgh, PA.
- 44 H.McD. Hobgood, R.C. Glass, G. Augustine, R.H. Hopkins, J. Jenny, M. Skowronski, W.C. Mitchell, M. Roth, *Appl. Phys. Lett.* **66** (1995) 1364.
- 45 E. Morvan, O. Norblanc, C. Dua, and C. Brylinski, *Mat. Sci. Forum* **353-6** (2001) 669.
- 46 J. R. Jenny, St. G. Müller, A. Powell, V. F. Tsvetkov, H. M. Hobgood, R. C. Glass, and C. H. Carter, Jr. , *J. Electronic Matls.*, **31** (2002) 366 Adrian, this is the TDR ref that talks about HPSI. Did you want a reference that discussed the technique? Ditto for the OAS, DLTS, and EPR references.
- 47 J. R. Jenny, D. P. Malta, M. R. Calus, St. G. Müller, A. R. Powell, V. F. Tsvetkov, H. McD. Hobgood, R. C. Glass and C. H. Carter, Jr., *Mater. Sci. Forum* **457-460** (2004) 35.
- 48 St. G. Mueller, M. F. Brady, W. H. Brixius, R. C. Glass, H. McD. Hobgood, J. R. Jenny, R. T. Leonard, D. P. Malta, A. R. Powell, V. F. Tsvetkov, S. T. Allen, J. W. Palmour and C. H. Carter, Jr., *Mater. Sci. Forum* **433-436** (2003) 39.
- 49 EPR ref (same as TDR ref).
- 50 Bill mitchel OAS reference this was something that they sent us and we published (in ref 48)
- 51 J. R. Jenny, M. Skowronski, W. C. Mitchel, H. M. Hobgood, R. C. Glass, G. Augustine, and R. H. Hopkins, *J. Appl. Phys.* 78 (1995) 3839-3842.
- 52 J. R. Jenny, M. Skowronski, W. C. Mitchel, H. M. Hobgood, R. C. Glass, G. Augustine, and R. H. Hopkins, *Appl. Phys. Lett.* 68 (1996) 1963-1965.
- 53 N.T. Son, P.N. Hai, and E. Jansen, *Phys. Rev. B* 63 (2001) 201201
- 54 Th. Lingner, S. Greulich-Weber, J.-M. Spaeth, U. Gerstmann, E. Rauls, Z. Hajnal, Th. Frauenheim, H. Ocerhof: *Phys. Rev. B* 64 (2001) 245212.
- 55 Private communication with B. Shanabrook, W. Carlos, and E. Glaser.
- 56 <http://www.cree.com>.
- 57 <http://www.orbitech.co.uk>
- 58 <http://www.diamondwiretech.com>
- 59 <http://www.hct.ch>
- 60 J. W. Palmour, H. Kong, J. Edmond, "Method of preparing silicon carbide surfaces for crystal growth". Patent # 4946547 1990.
- 61 L. Zhou, V. Audurier, P. Pirouz, and J. A. Powell, J. "Chemomechanical polishing of silicon carbide". *Electrochemical Soc.* **144** P.161 1997.
- 62 <http://www.novasic.com/>.
- 63 J.Sumakaris, *Matls. Sci. Forum*, 483-485 (2005) pp155-158.
- 64 J.P. Bergman, H. Lendermann, P.A. Nilsson, U.Lindefelt, P.Skytt, *Mat. Sci. Forum* 353-356 299 (2001).

**This page intentionally left blank**

## DEEP LEVEL DEFECTS IN SILICON CARBIDE

A. A. LEBEDEV

*Russian Academy of Science, A. F. Ioffe Physico-Technical Institute, Politehnicheskaja 26,  
Saint-Petersburg 194021, Russian Federation  
shura.lebe@mail.ioffe.ru*

Results obtained in recent studies of deep centers in 6H-, 4H-, and 3C-SiC are analyzed. The ionization energies and capture cross sections of centers formed by doping of SiC with different types of impurities or by irradiation, as well as the corresponding parameters of intrinsic defects, are presented. The involvement of these centers in radiative and nonradiative recombination is examined. Analysis of published data shows that a strong influence is exerted by intrinsic defects in the SiC crystal lattice both on the formation of deep centers and on the properties of the epitaxial layers themselves, such as their doping level and polytype homogeneity.

**Keywords:** Silicon carbide, deep levels, capacitance spectroscopy, electroluminescence.

### 1. Introduction

The considerable progress made in the development of SiC technology in the last 10–15 years has enabled creation of SiC semiconductor devices of almost all the basic types, including the first integrated circuits.

Deep centers determine many of the most important parameters of semiconductor devices. Deep centers in the bulk of a semiconductor affect the lifetime and diffusion length of minority charge carriers, efficiency of light-emitting diodes and photodetectors, gain of transistors, and magnitude of the temperature coefficient for the breakdown voltage of p-n junctions. As it is impossible now to predict theoretically the main parameters of impurity and defect centers in the new semiconductor material, the principal source of information on deep centers is experiment.

It is evident that further advance in the technology of SiC and design of new devices will, on the one hand, require studies of deep centers in epitaxial layers and p-n junctions fabricated by various techniques. On the other hand, analysis of parameters of devices that have already been created can yield additional information about the properties of deep centers in them. In addition, most of methods used to grow epitaxial layers and fabricate p-n junctions lead to formation of various deep centers in the bulk of the semiconductor and on its surface, which, in turn, affects the characteristics of devices created from them. Thus, it is possible to determine the optimum combination of techniques for creating a given type of devices with the best set of operating characteristics by studying the parameters and distributions of deep centers.

The purpose of this article is to summarize the currently available data on the parameters of deep centers in 6H-, 4H-, and 3C-SiC and to analyze the properties of these

centers from the standpoint of their possible influence on the characteristics of device structures based on silicon carbide.

## 2. Parameters of Deep Centers in SiC

### 2.1. Major dopant impurities in SiC

The allowed states in the band gap of semiconductors are traditionally divided into "shallow" and "deep." This division is extremely arbitrary and shallow states are usually assumed to be those with ionization energies  $E_i < 0.1$  eV and deep states, those with  $E_i > 0.1$  eV<sup>1</sup>. For silicon carbide, this division is even more arbitrary, since even the ground donor and acceptor levels have ionization energies  $E_i \geq 0.1$  eV. Thus, strictly speaking, all the levels that have been studied in silicon carbide are deep. However, we regard, in what follows, the levels that determine the resistance of the base regions as shallow, compared with the deeper levels that make no noticeable contribution to the concentration of the majority charge carriers.

#### 2.1.1. Nitrogen

Undoped SiC layers have *n*-type conductivity. This is accounted for by the uncontrolled doping of the growing layer by nitrogen; in addition, nitrogen has a rather high solubility in SiC ( $\approx 10^{21} \text{ cm}^{-3}$ )<sup>2</sup> and the lowest ionization energy among all the impurity donor levels. By implanting N ions, it is also possible to obtain thin, heavily doped layers of SiC in order to form ohmic contacts<sup>3,4</sup>.

The existence of nonequivalent sites in the SiC lattice shows up most clearly in the energy position of the deep centers associated with nitrogen atoms<sup>5-8</sup>. In all the main polytypes of SiC, nitrogen atoms have been observed in association both with cubic (c) and with hexagonal (h) lattice sites, with the ratio of the level concentrations ( $N_h/N_c$ ) equal to the ratio of the number of hexagonal and cubic sites in the crystal lattices of the different SiC polytypes.  $N_h/N_c$  is 1:1 for 4H, 1:2 for 6H, and 2:3 for 15R. According to the latest studies, the ionization energies of the nitrogen levels are as follows: [ $E_c = 0.081$ ,  $E_c = 0.138$ ,  $E_c = 0.142$  eV (6H)]<sup>9</sup>; [ $E_c = 0.052$ ,  $E_c = 0.092$  eV (4H)]<sup>10,11</sup>. Most investigators assume that nitrogen occupies a carbon site in the SiC lattice<sup>5, 12</sup>. However, data exist, at least for 3C-SiC and especially at concentrations  $\leq 10^{19} \text{ cm}^{-3}$ , which indicate that nitrogen also displaces silicon<sup>13</sup>. This contradiction may be accounted for by the fact that doping of SiC with nitrogen gives rise to various complexes formed in association with intrinsic defects of SiC or with background impurities, and the position of these complexes in the lattice differs from that of single nitrogen atoms. For example, Ti-N pairs, which give rise to a donor level  $E_c = 0.6$  eV, have been observed in 6H- and 4H-SiC<sup>14</sup>.

It has been reported<sup>15</sup> that no electron spin resonance (ESR), usually associated with nitrogen levels, is observed in the purest 4H-SiC layers. This was attributed to a significant contribution from intrinsic defects to the conductivity of lightly doped SiC layers. Another feature of SiC(N) samples is the formation of an exciton bound to a neutral donor level of nitrogen. The lines in the luminescence spectrum of 6H-SiC,

associated with the recombination of this exciton, have wavelengths of 4122, 4142, and 4144 Å<sup>16</sup>.

### 2.1.2. Aluminum

The *p*-type silicon carbide is customarily obtained using Al<sup>18-20</sup>, which forms the shallowest acceptor levels in the lower half of the band gap and has the highest solubility (~10<sup>21</sup> cm<sup>-3</sup>)<sup>21</sup>.

It was shown<sup>19</sup> that, when the concentration of Al is raised from 10<sup>18</sup> to 10<sup>21</sup> cm<sup>-3</sup>, its ionization energy decreases from 0.27 to 0.1 eV. Later, it was demonstrated<sup>22</sup> that the ionization energy of the levels of Al ( $E_v+0.24$  eV) is independent of its concentration up to 5 10<sup>20</sup> cm<sup>-3</sup> if the degree of compensation of the epitaxial layers is  $k < 0.01$ . For  $k > 0.01$ , the ionization energy falls to 0.1 eV ( $N_{Al} \sim 5 \cdot 10^{20}$  cm<sup>-3</sup>). These results were explained in terms of the percolation theory<sup>23</sup>: the interaction among all the forms of impurities in a compensated semiconductor gives rise to an additional potential, which reduces the ionization energy of the impurity. This explanation, however, does not rule out formation of several types of deep centers in silicon carbide doped with aluminum.

For example, deep level current spectroscopy of 6H-SiC *p-n* structures, with an n-base doped with Al during the growth process, has been used<sup>24</sup> to observe two deep acceptor levels which are absent in undoped samples produced by the same techniques:  $HK_1$  ( $E_v+0.22$  eV,  $\sigma_p=3.6 \cdot 10^{-12}$  cm<sup>2</sup>) and  $HK_2$  ( $E_v+0.28$  eV,  $\sigma_p=1.3 \cdot 10^{-15}$  cm<sup>2</sup>). The ratio of the ionization energies of the  $HK_1$  and  $HK_2$  centers,  $E_{i2}/E_{i1}=1.27$ , which substantially exceeds the energy ratio for acceptor impurity atoms lying in different non-equivalent sites of the SiC crystal lattice<sup>6</sup>. The concentration of the  $HK_1$  center ( $N_1$ ) remained essentially constant (~3·10<sup>15</sup> cm<sup>-3</sup>) in all the samples studied. At the same time, the concentration of  $HK_2$  centers ( $N_2$ ) decreased sharply upon a slight change in the overall degree of compensation. As a result, the  $N_2/N_1$  ratio changed from 7–12 to 2, although the ratio between the amounts of cubic and hexagonal sites in the 6H-SiC crystal lattice is 2:1. Thus, it is more probable that the  $HK_1$  and  $HK_2$  levels correspond to different types of deep centers in 6H-SiC (Al, N), rather than to a single type of center formed at different nonequivalent sites of the SiC crystal lattice.

A photocapacitance method has been used to observe in *p<sup>+</sup>-n* structures obtained by Al ion implantation<sup>25</sup> a band of levels in the upper half of the band gap, at energies of 0.15–0.5 eV, with a capture cross section  $\sigma_n \sim 10^{-22}$  cm<sup>2</sup>.

Thus far, the ionization energies of Al at different nonequivalent sites of the SiC lattice have not been clearly determined, although an energy separation was reported in a number of papers<sup>26</sup>. In any case, the observed difference in the ionization energies was ~0.03 eV, which, as a rule, is less than the spread in energies obtained by the different authors. Based on a number of optical and electrical measurements, we may assume that at least one center with an ionization energy  $E_v+0.23 \pm 0.01$  eV is associated with the Al impurity in SiC. For 4H-SiC(Al), deep level capacitance spectroscopy (DLTS) has revealed the presence of a level with  $E_v + 0.23$  eV<sup>26</sup>.

In ref.<sup>27</sup>, an Al acceptor with  $\sim 200$  meV and an unknown defect with  $\sim 370$  meV were found from the temperature dependence of the hole concentration  $p(T)$  in lightly Al-doped  $4H$ -SiC epilayers. Upon irradiation with 4.6 MeV electrons, the density of the Al acceptor decreases, whereas that of the unknown defect remains almost unchanged. In the authors' opinion, this indicates that the substitutional Al atoms in  $4H$ -SiC are displaced by irradiation or that the bond between the substitutional Al atom and the nearest neighbor atom is ruptured by irradiation.

Implantation of aluminum ions has been used to create heavily doped spacers for fabricating ohmic contacts to  $p$ -SiC. It is also possible to obtain  $p-n$  structures by ion implantation of Al in epitaxial  $n$ -type SiC layers<sup>28-29</sup>. Attempts have been made, although not very successfully, to obtain SiC/AlN solid solutions by implantation of large doses of Al and N<sup>30</sup>.

The doping of SiC with aluminum had been the only method (before GaN light-emitting diodes were produced) for creating light-emitting diodes with peak emission in the blue spectral range. Introduction of aluminum also leads to the formation of a bound exciton whose presence can be traced in all the main polytypes of SiC<sup>31</sup>.

### 2.1.3. Boron

A large number of papers have been concerned with the diffusion of boron in SiC<sup>32-42</sup>. This impurity is of interest because boron forms acceptor levels in SiC and can be used to make  $p-n$  junctions. In addition, boron has a high solubility,  $10^{20} \text{ cm}^{-3}$ , and is one of the most rapidly diffusing impurities in SiC. One feature of the diffusion distribution of boron in SiC is the existence of surface regions (high concentration, low effective diffusion coefficients) and bulk regions (conversely, low concentrations, high diffusion coefficients)<sup>32</sup>. This sort of boron distribution means that smooth  $p-n$  junctions are obtained with rather extended compensated regions as a result of its diffusion into n-SiC. This may result in S-shaped current-voltage characteristics for a diode produced in this manner<sup>33</sup>. Another shortcoming of boron, as a shallow acceptor impurity, is its high ionization energy,  $E_v + 0.35$  eV, according to Hall measurements<sup>34, 35</sup>. Therefore, the degree of ionization of the impurity at room temperature is negligible and, despite the high concentration of uncompensated acceptors, the concentration of ionized holes is still low. Thus, effective injection of holes from a boron-doped emitter can be observed only at high temperatures. All these facts mean that Al serves as the main acceptor impurity for doping of SiC. However, the diffusion of boron has not lost its importance for certain special applications in the technology of silicon carbide. One of these is fabrication of light-emitting diodes with peak emission in the yellow spectral range ( $6H$ -SiC). It has been found that boron doping yields luminescence with  $h\nu = 2.14$  eV<sup>36</sup>. Diffusion of boron into epitaxial  $p-n$  structures makes it possible to obtain  $p-i-n$  diodes<sup>37</sup>. It has been shown that presence of B enhances the nitrogen diffusion by a factor of  $\sim 60$ <sup>38</sup>. It was demonstrated in ref.<sup>39</sup> that boron doping of SiC gives, in addition to a shallow boron center, a deep D-center ( $E_v + 0.58$  eV). Later, an analog of the D-center was observed in  $4H$ -SiC<sup>41, 42</sup>. The fact that two types of levels, which are not related to different charge

states of a single center, are formed upon diffusion of boron into SiC is apparently associated with the complexity of the diffusion distribution of B in SiC. For example, it was assumed in ref.<sup>43</sup> that boron atoms diffuse in the form of associates with the intrinsic defects of the SiC lattice. Later, an investigation of boron diffusion from an implanted layer confirmed this point of view<sup>40, 44-46</sup>. According to<sup>44, 45</sup>, B diffuses in SiC by the kick-out mechanism with the assistance of silicon interstitials, similarly to the boron diffusion in Si. This assumption is in agreement with the results obtained in a study<sup>35</sup> of the concentrations of the shallow boron center and the D-center in SiC samples doped with boron by various techniques. It was shown that mostly D-centers are formed during diffusion, and mainly shallow boron centers are produced with boron doping in the course of growth of epitaxial layers. On the whole, we believe that it is quite probable that the surface branch of the diffusion distribution is associated with shallow boron centers, i.e., with boron atoms occupying sites in the SiC crystal lattice. At the same time, the bulk branch is formed by boron + intrinsic defect complexes.

According to the most recent ESR data, the structure of the shallow boron center corresponds to a boron atom that displaced Si ( $B_{Si}$ ), whereas the deep boron center is a complex of boron atoms with a carbon vacancy<sup>47-50</sup>. Note that the D-center is responsible for a characteristic level in SiC and it has been observed in SiC samples grown by various techniques<sup>51-52</sup>.

#### 2.1.4. Gallium

Gallium is another acceptor impurity in silicon carbide, but with a lower solubility than Al ( $\sim 1.2 \cdot 10^{19} \text{ cm}^{-3}$ )<sup>53, 21</sup> and a higher ionization energy [ $E_v + 0.29 \text{ eV}$  ( $6H$ ) and  $E_v + 0.3 \text{ eV}$  ( $4H$ )]<sup>53, 54</sup>, which is commonly not used for fabrication of  $p-n$  structures. Some authors have observed two acceptor levels ( $E_v + 0.31$  and  $E_v + 0.37 \text{ eV}$ ) related to Ga in  $6H$ -SiC<sup>55</sup>. The ionization energy of the gallium impurity has also been found to be independent of its concentration. Ga has close ionization energies in different SiC polytypes: ( $E_v + 0.34 \text{ eV}$ ) for  $3C$  and ( $E_v + 0.3 \text{ eV}$ ) for  $15R$ <sup>6</sup>. Just as aluminum, gallium is a substitution impurity in the silicon sublattice<sup>9</sup> and it can bind an exciton<sup>6</sup>.

#### 2.1.5. Indium

Very little is known about the properties of indium in silicon carbide. It appears to have a low solubility ( $\sim 10^{17} \text{ cm}^{-3}$ )<sup>21</sup>, and it has not been possible to obtain  $p$ -type SiC layers by implantation of indium during growth.

### 2.2. Other types of impurity centers in SiC

#### 2.2.1. Beryllium

It has been found in studies of SiC (Be) that Be is an amphoteric impurity in SiC<sup>56-58</sup>. It was found by Hall measurements, that Be is a double-charged acceptor ( $E_v + 0.42$  and  $E_v + 0.6 \text{ eV}$ ), but when introduced into a heavily doped  $p$ -type SiC, Be acts as a donor. Photoluminescence has been observed in  $n$ - and  $p$ -type  $6H$ -SiC(Be) crystals, with the

maximum intensity in the red spectral range, at 1.85–2.1 eV (293 K)<sup>59</sup>. As the temperature is lowered, a band peaked at ~2.4eV appears in the photoluminescence spectrum of *p*-type samples. Beryllium has not been used to fabricate device structures based on SiC. Only recently, it has been shown that Be ion implantation can be used to fabricate epitaxial *p*-type 6H-SiC layers and produce *p*–*n* structures based on them<sup>60</sup>. According to new DLTS data<sup>61</sup>, beryllium gives rise to three types of deep centers ( $E_c$ –0.34;  $E_c$ –0.44 and  $E_v$ +0.66 eV) in *n*-6H-SiC and one center ( $E_v$ +0.41) in *p*-6H-SiC<sup>62</sup>. ESR spectra of the Be acceptor centre have been studied<sup>63</sup>. The similarity of the structure of this center to that of the shallow boron level was noted.

### 2.2.2. Magnesium

The formation of two new levels has been observed (DLTS) in *n*-6H-SiC upon implantation of Mg ions ( $E_c$ –0.49 and  $E_c$ –0.45 eV)<sup>64</sup>. Annealing at of ~ 1600 °C leads to a rise in the concentration of these deep centers.

### 2.2.3. Scandium

A deep center with an energy  $E_v$  +(0.52–0.55) eV has been observed in DLTS studies of SiC (Sc)<sup>65</sup>; the position of its DLTS peak strongly depends on the electric field strength  $E$  in the space charge region [ $E$ =(1–2.6)  $10^5$ V/cm]. This was explained<sup>65</sup> in terms of the Poole-Frenkel effect, and the observed deep center was attributed to Sc. It is also known that SiC(Sc) samples have a photoluminescence peak in the yellow-green spectral range (6H polytype)<sup>66</sup>. When SiC is doped with scandium, it is possible to obtain *p*–*i*–*n* structures with a highly resistive  $\pi$ -region<sup>67</sup>. The EPR spectra of Si<Sc> in ref.<sup>68</sup> are explained as being due to an isolated Sc<sup>0</sup>(S=1/2) acceptor at carbon sites, but with a different microscopic configuration.

### 2.2.4. Titanium

Among the transition metals, Ti and V have been studied in greatest detail as impurities in SiC. On the one hand, this is accounted for by the fact that these metals are characteristic background impurities in SiC and, on the other, by their strong effect on the electrical properties of doped samples. Some time ago<sup>69</sup>, it was found that introduction of Ti gives rise to narrow lines at 2.79–2.86 eV in the photoluminescence spectrum of 6H-SiC. These lines were observed in 6H-, 4H-, 15R-, and 33R-SiC and the number of lines corresponded to the number of non-equivalent sites in the crystal lattice of a given polytype. At the same time, this sort of spectrum was not observed in the 21R and 3C polytypes of SiC(Ti). The relationship between Ti atoms and the observed photoluminescence spectrum was confirmed by a study of optically detectable magnetic resonance (ODMR) in 6H-, 4H-, 15R, and 15R-SiC(Ti)<sup>70</sup>. However, studies of the electron spin resonance<sup>71, 72</sup> demonstrated that centers associated with Ti exist only in 4H-SiC. Similar results were obtained in DLTS studies of SiC samples ion-doped with titanium<sup>73–76</sup>: two deep centers associated with titanium were observed in 4H-SiC(Ti) at

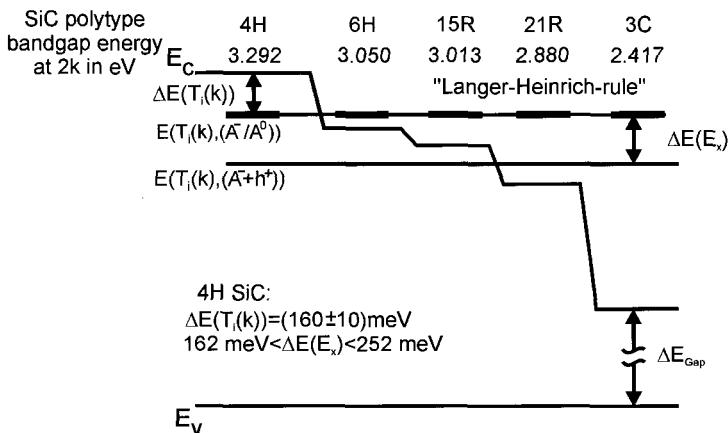


Fig. 1. A diagram illustrating the application of the Langer-Heinrich rule to a Ti center in SiC<sup>73</sup>.

$E_c=0.12$  and  $E_c=0.16$  eV, which correspond to the hexagonal and cubic positions of the impurity in the lattice. In 6H-SiC(Ti), no centers of this kind were revealed. A general analysis of the data for SiC(Ti) has been made by Dalibor *et al.*<sup>73</sup>. They assumed that the empirical Langer-Heinrich (LH) rule, which had been suggested earlier for the III-V and II-VI compounds<sup>77</sup>, applies to the SiC polytypes. According to the LH rule, the energy position of the levels related to the transition metals in a series of isovalent semiconducting compounds is unchanged with respect to some common energy level; in other words, the mutual position of the Ti levels in the SiC polytypes remains fixed and independent of the polytype parameters. At the same time, the possibility of observing these levels by various methods is determined by the band gap width of a given polytype. Thus, the ground state of titanium, observed by DLTS in 4H-SiC, will not be observed by this method in the other (narrower-gap) SiC polytypes, since it lies outside the gap (see Fig. 1). However, the energy of an exciton bound to a Ti atom is lower. Thus, photoluminescence owing, which is attributable to recombination of this exciton, has been observed in SiC polytypes with a narrower band gap. Based on the observation of excitons bound to Ti in 4H-, 6H-, and 15R-SiC and their absence in the narrower-gap 21R and 3C polytypes, the binding energy [ $\Delta E(Ex)$ ] of this exciton was estimated to be  $162 \text{ meV} < \Delta E(Ex) < 252 \text{ meV}$ <sup>73</sup>.

### 2.2.5. Vanadium

Studies of the behavior of vanadium in SiC became especially relevant after it was found that doping with V leads to formation of semi-insulating layers of silicon carbide<sup>85, 86</sup>. Introduction of vanadium during CVD growth yielded epitaxial layers of 6H-SiC with a resistivity of  $3000 \Omega \text{ cm}$ . These results were accounted for by the formation of a deep donor in SiC(V) near the midgap ( $E_c \sim 1.59$  eV), which was overcompensated by a background acceptor impurity (boron). According to data from various sources,

vanadium is an amphoteric impurity in SiC; i.e. it leads to formation of both donor and acceptor levels<sup>71–81</sup>. DLTS studies of SiC(V) revealed yet another level with ionization energies  $E_i$ –(0.65–0.75) eV and  $E_c$ –0.97eV for the 6H and 4H polytypes, respectively<sup>73, 75, 76, 82</sup>. It has been suggested that the LH rule holds for vanadium impurities in silicon carbide<sup>82</sup>.

#### 2.2.6. *Tantalum*

Investigation of parameters of this impurity is important, because Ta is used as material of growth cells in sublimation epitaxy of SiC<sup>85</sup>. The DLTS spectra of 4H-SiC samples implanted with Ta exhibit one dominating peak representing a trap energy of about  $E_i=E_c$ –0.67 eV<sup>86</sup>. The time constant of electron emission from the Ta-related trap strongly depends on the electric field strength. This indicates a donor like character of this deep level.

#### 2.2.7. *Chromium*

As for the levels formed during doping of SiC with chromium, there is no established viewpoint as yet. In a study of 6H-SiC ion-doped with Cr, two levels with  $E_c$ –0.38 and  $E_c$ –0.34eV were observed; the signals from these levels completely disappeared after the samples were annealed at  $T \geq 1600^\circ\text{C}$ <sup>64</sup>. At the same time, studies of SiC(Cr) obtained by a similar technique have revealed three levels in 4H-SiC ( $E_c$ –0.15,  $E_c$ –0.18, and  $E_c$ –0.74) and one in 6H-SiC ( $E_c$ –0.54eV)<sup>82,87,75,76</sup>. These results were interpreted in terms of the HL rule. The narrowing of the band gap ( $\Delta E \sim 0.22\text{eV}$ ) on going from 4H to 6H means that the two shallower levels lie outside the band gap and the ionization energy of the deeper level decreases by  $\Delta E$ . The IR photoluminescence associated with Cr in 4H and 6H SiC was studied in ref.<sup>88</sup>.

#### 2.2.8. *Molybdenum*

A center associated with a background Mo impurity has been found in commercial (CREE) SiC epitaxial layers<sup>90</sup>. It was found that Mo in 6H- SiC occupies a silicon site in the lattice and can simultaneously exist in two charge states, one of which forms an acceptor level in the *n*-type material near the midgap. In this regard, it was concluded that use of ohmic contacts based on Mo at high temperatures may lead to diffusion of Mo into the bulk of the semiconductor, with the resulting compensation of the *n*-type material and device degradation.

#### 2.2.9. *Manganese*

An ESR spectrum has been observed<sup>91</sup> and attributed to a doubly charged donor state of an impurity Mn atom occupying a hexagonal site of the 6H-SiC lattice. More detailed information about the properties of transition metals in SiC can be found in a review<sup>92</sup> and paper<sup>93</sup>.

### 2.2.10. Zinc

To identify Zn-related deep bandgap state in SiC, the radioactive isotope  $^{67}\text{Ga}$  (decay to  $^{67}\text{Zn}$ , half-life = 3.25 days) was used for radiotracer experiments<sup>94,95</sup>. This technique was described in detail in ref.<sup>96</sup>. DLTS identified one Zn-related level at  $E_t=1.16$  eV above the valence band edge in  $6H$ -SiC. The hole emission from this center is not affected by the electric field strength, which means that the center has a donor-like character.

### 2.2.11. Cadmium

In ref.<sup>95</sup>, similar radiotracer experiments were carried out for identification of the parameters of the Cd center in  $4H$ -SiC. Two states of Cd with roughly equal concentrations at  $E_v+0.9$  and  $E_v+1.19$  eV were identified. For both the states, the influence of the electric field strength on the hole emission is weaker than that expected for the (double) acceptor level.

### 2.2.12. Phosphorus

Being a Group-V element, phosphorus should form donor centers in SiC. However, a shallow donor impurity with a good solubility in SiC is available (nitrogen), and, therefore, the interest in other donor impurities for SiC has been limited. Phosphorus forms two donor levels in  $6H$ -SiC ( $E_c-0.085$  eV,  $E_c-0.135$ eV)<sup>97</sup> and  $4H$  SiC ( $E_c-0.053$  eV,  $E_c-0.093$  eV)<sup>98</sup> for the hexagonal and cubic lattice positions, respectively. With phosphorus ion implantation used, it was possible to obtain  $n^+$ -layers of  $6H$ -SiC with electrically active donor concentrations  $\geq 3 \cdot 10^{18} \text{ cm}^{-3}$ <sup>97,99,100</sup>. In ref.<sup>98</sup> it was also concluded that, for low-dose applications (i.e. overcompensation of semi-insulating substrates to produce channel layers in FETs), nitrogen appears to be a better choice for implantation into  $4H$ -SiC, because P is not activated to the same extent as nitrogen. Another method for doping of SiC with phosphorus is nuclear transmutation doping (NTD)<sup>101,102</sup>. NTD has been widely utilized in fabrication of power Si devices to obtain an extremely homogeneous donor concentration in the n-drift layers. This technology is based on the capture of thermal neutrons  $^{30}\text{Si}$  through the reaction [ $^{30}\text{Si}(n,\gamma)^{31}\text{Si}$ ] and the subsequent  $\beta$ -decay to form  $^{31}\text{P}$ (phosphorus) donors. In PL spectra of P-doped  $6H$ -SiC, new lines were observed, which can be attributed to recombination at neutral phosphorus donor of four particle exciton complexes<sup>103</sup>. In ref.<sup>104</sup>, the electron spin resonance in  $4H$ - and  $6H$ -SiC samples doped with P during CVD growth was studied.

### 2.2.13. Oxygen

By analogy with Si, it can be assumed that there will be a high concentration of background oxygen in SiC, which can have a significant effect on the parameters of fabricated devices. However, the number of studies devoted to this topic is small, and, therefore, it difficult to verify this assumption as yet. The effect of oxygen doping on the intensity of blue and yellow (boron-related) photoluminescence in  $6H$ -SiC has been studied<sup>105</sup>. No correlation was observed between the oxygen concentration and the

intensity of the blue luminescence, whereas it was found that oxygen is a co-activator of the yellow luminescence. A study of 4H-SiC samples ion-doped with oxygen has been carried out<sup>106</sup>. Two shallower ( $E_c$ -0.3 and  $E_c$ -0.44 eV) and three deeper ( $E_c$ -0.74,  $E_c$ -0.9, and  $E_c$ -0.95 eV) centers were found. These centers were identified as complexes containing oxygen atoms.

#### 2.2.14. Erbium

Erbium doping gives rise to a narrow line at  $\sim 1.54 \mu\text{m}$  in the photoluminescence spectra of various semiconductors<sup>107</sup>. A source of light for this optical band is of great interest from the practical standpoint, since it coincides with the absorption minimum of quartz optical fibers. It is assumed that this photoluminescence is associated with an intracenter transition in Er atoms, which are rarer weakly bound to the surrounding semiconducting matrix. Single-crystal samples of 4H-, 6H-, 15R-, and 3C-SiC ion-doped with erbium have been studied<sup>108</sup>. In the above-mentioned portion of the spectra of these samples, a narrow photoluminescence line was detected, whose intensity is virtually unchanged in the temperature range 2–400 K. At  $T > 400\text{K}$ , a rapid quenching of the photoluminescence was observed. No significant differences were revealed in the photoluminescence spectra of 4H, 6H, and 15R polytype samples, including the fine structure of the lines associated with the existence of non-equivalent sites in the SiC lattice. Apparently, the structure of the Er center in SiC and its properties are similar to those of erbium in other semiconductor materials. New DLTS measurements with a stable  $^{167}\text{Er}$  isotope revealed donor-like levels at  $E_t = E_v + 0.75$  in 6H-SiC<sup>109</sup>.

The parameters of the most extensively studied impurities in SiC are listed in Table 1.

Table 1. Parameters and properties of several impurities in 6H and 4H SiC

Impurity	Energy location, eV		Lattice site	Participation in recombination	Other properties	Donor or acceptor
	6H SiC	4H SiC				
N	$E_c - 0.081$	$E_c - 0.052$	C <sup>[5,12]</sup> Si <sup>[13]</sup>	Bound exciton	Heteropolytype	
	$E_c - 0.138$	$E_c - 0.092$		<sup>[17]</sup> , (cf Al, Ga, B)	epitaxy $6H \Rightarrow 3C$ <sup>[182-184]</sup>	D
	$E_c - 0.142$ <sup>[9]</sup> , $E_v + 0.23$ <sup>[22,23]</sup>	$E_c - 0.142$ <sup>[10]</sup> , $E_v + 0.23$ <sup>[22,23]</sup>				
Al	$E_v + (0.1 - 0.27)$ <sup>[19]</sup>	$E_v + 0.23$ <sup>[26]</sup>	Si <sup>[31]</sup>	Bound exciton	Heteropolytype	A
				<sup>[31]</sup> , Al-N DAR, CA recomb. <sup>[6]</sup>	epitaxy $6H \Rightarrow 4H$ <sup>[182-184]</sup>	
B	$E_v + 0.35$ <sup>[34,35]</sup>	$E_v + 0.29$ <sup>[134]</sup>	Si <sup>[47,48]</sup>	DAR B-N <sup>[199]</sup>	Heteropolytype epitaxy $6H \Rightarrow 4H$ <sup>[182-184]</sup>	A

Table 1 (Continued)

				Bound	
Ga	$E_v + 0.29$ [53,54]	$E_v + 0.3$ [53,54]	Si [53]	exciton <sup>[55]</sup> , DAR Ga-N, CA recomb* [6]	A
		$E_c - 0.34; E_c -$ 0.44			
Be	$E_v + 0.64$ [61]				Amphoteric impurity
	$E_v + 0, 41$ [62]				
Mg	$E_c - 0.45$ [64]				
Sc	$E_v + (0.52 - 0.55)$ [65]	C [68]	Yellow-green PL ( $6H\text{-SiC}$ ) <sup>[66]</sup>	Heteropolytype epitaxy $6H \Rightarrow 4H$ [182- 184]	A
Ti	$E_c - 0.6 \pm B,$ (pairs Ti-N) [14]	$E_c - 0.12$ $E_c - 0.16$ [73,74]	Si [68,70]	Bound exiton [68,69]	A [73,75- 76]
V	$E_c - 0.7$ [82,84] $E_v + 1.6$ [72-134]	$E_c - 0.97$ [71-81]	Si [81]	Radiative intracenter transition. <sup>[83]</sup>	Semi-insulating layers [78,79]; recombination center [83]
Ta		$E_c - 0.68$ [86]			D [86]
		$E_c - 0.15$			
Cr	$E_c - 0.54$ [82]	$E_c - 0.18$ $E_c - 0.74$ [82]			A [82]
Zn	$E_v + 1.16$ [94,95]				D [94,95]
Cd		$E_v + 0.9$			
P	$E_c - 0.085$ $E_c - 0.135$ [97]	$E_c - 0.053$ $E_c - 0.093$ [98]			D [97,98]
Er	$E_v + 0.78$	$E_v + 0.75$ [108]			D [108]

\*A conduction band-neutral acceptor radiative transition

It can be seen that there is a similarity between the parameters and properties of centers formed in different SiC polytypes doped by a given impurity if the related deep levels lie in the lower half of the band gap. If a given impurity forms centers with levels in the upper half of the band gap, then the parameters (and even the number) of these centers varies between different polytypes. This property of silicon carbide shows up even more clearly for intrinsic and radiation defects in SiC. Thus, for describing the properties of these latter, we thought it more appropriate to use the order of discussion of the material used in Sec. 1.3.

### **2.3. Intrinsic defects in silicon carbide**

#### *2.3.1. Centers in the lower half of the band gap*

##### *L-center*

Studies of 6H-SiC *p-n* structures fabricated by ion implantation of Al (ID structures) have revealed deep centers with ionization energies  $E_v+0.24\text{eV}$  and  $\sigma_p \sim 10^{-15} \text{ cm}^2$  (*L*-centers)<sup>39</sup>. L-centers have also been observed in *p-n* structures fabricated by sublimation epitaxy (SE structures) and in several *p-n* structures produced by containerless liquid epitaxy (CLE structures). In the implantation structures, the concentration of these centers increased near the metallurgical boundary of the *p-n* junction, whereas in other types of samples, no noticeable profile in the distribution of *L*-centers was observed.

The ionization energy of the L-centers was close to that obtained by other methods for the impurity Al level<sup>19</sup>. However, the presence of Al atoms in the base region and the drop in their concentration far from the *p*-region can be explained in the case of the ID *p-n* structures, whereas the presence of Al in the n-base at concentrations  $\sim 10^{16} \text{ cm}^{-3}$  appears improbable for the sharp CLE and SE structures. To clarify the relationship between the observed L-center and impurity Al atoms, CLE and SE *p-n* structures with an n-base doped with aluminum during growth of SiC(Al) have been studied<sup>24</sup>. Studies of these samples led to a conclusion<sup>10,111</sup> that the *L*-center is a defect complex that does not include directly an Al atom and is formed upon diffusion and implantation of Al, and for other reasons as well. Later, analogues of the *L*-center were observed in 4H-SiC samples obtained by sublimation<sup>112</sup> and in CVD-grown 4H- and 6H-SiC samples<sup>26,113</sup>.

##### *i-center*

In addition to L-centers, DLTS spectra of 6H-SiC ID structures have revealed a deep level in the lower half of the band gap (*i*-center). Various analytical techniques have shown that the DLTS peak of the *i*-center is broadened and cannot be described by the classical equation for the DLTS spectrum<sup>39</sup>. The observed broadening of the DLTS spectra may be caused by the overlap of capacitance signals from two (or more) deep centers with ionization energies  $E_1$  and  $E_2$ . The ionization energy of the *i*-center was found to fall within the interval  $E_v+(0.52-0.58) \text{ eV}$ .

Analogous ID structures have been obtained on the basis of 4H-SiC epitaxial films. Their DLTS spectrum was similar to the spectra of ID samples of 6H-SiC, and an analogue of the *i*-center with  $E_v+0.53\text{eV}$  was observed in them<sup>114,115</sup>. The closeness of the parameters of the *i*-centers in 6H and 4H indicates that the structures of these centers are similar for these polytypes. The distribution of *i*-centers in the base region of a diode has been measured in ID structures based on 6H- and 4H-SiC<sup>113</sup>. When the distribution profile of *i*-centers in structures based on 4H-SiC was extrapolated, a good agreement with the beginning of the profile in structures based on 6H-SiC was observed; this suggests that the character of the distribution of *i*-centers in structures based on 4H-SiC and 6H-SiC is the same. A comparison of the distribution of the *i*-centers and the  $N_d-N_a$  profile obtained from capacitance-voltage characteristics showed that the distributions of the compensating defects in the base are the same as the distribution of the *i*-centers. Thus, compensation of the base region in ID structures is caused by an increased concentration of deep acceptor levels (*i*-centers) near the metallurgical boundary of the *p-n* junction. The acceptor nature of the *i*-center is also confirmed by the ratio of the carrier capture cross sections ( $\sigma_p >> \sigma_n$ ) for this deep center. It has also been found<sup>45</sup> that implantation of Al in the purest epitaxial layers of 4H-SiC gives rise to an S-shaped current-voltage characteristic, which has been attributed to a high concentration of *i*-centers.

It has been found<sup>117,118</sup> that both 3C-SiC inclusions in epitaxial 6H-SiC layers and activator-centers for defect electroluminescence (DEL) are formed by the same mechanisms, which must be accompanied by relaxation of stresses in the epitaxial layer. In other words, in addition to a realignment of the 6H-SiC lattice to give inclusions of a cubic phase, stress relaxation may occur through merging of intrinsic defects into the more stable and more energetically favorable complex, which are activators for the defect electroluminescence. Since the *i*-center is activator for the defect electroluminescence, this suggests that it is a complex consisting principally of intrinsic defects of the SiC crystal lattice, whose concentration increases upon irradiation or implantation. This assumption is in a good agreement with the results obtained in ref.<sup>43</sup>, where, based on experiments on the thermal stability of the defect electroluminescence in SiC crystals with different concentrations of intrinsic structural defects, it was found that a carbon vacancy is included in the composition of the luminescence-activating center.

#### *D*-center

Although a *D*-center is not a purely structural defect (it obviously includes a boron atom), it is a characteristic background center in 6H- and 4H-SiC grown by various techniques<sup>39-48,52</sup>. These centers were first observed in a study of DLTS spectra in SiC(B) structures and, along with *i*-centers, in SE samples<sup>39,40</sup>. The closeness of  $E_T$ - and  $\sigma_p$  for *i*- and *D*-centers led to overlapping of their DLTS peaks in SE and ID structures. Thus, the ionization energy of the deep centers ( $E_i$ ), determined for structures of these types, varied in the range  $0.52 \leq E_i \leq 0.58\text{eV}$ . A study of the parameters of *i*- and *D*-centers for electric fields of  $(1-7) \cdot 10^5\text{ V/cm}$  yielded no noticeable dependence of the ionization energy of these deep centers on the electric field strength<sup>119</sup>.

Although the ionization energy of a *D*-center exceeds by more than 10% that of a *i*-center, the reverse is true for the hole capture cross sections of these centers, so that the charge-exchange time constants for these centers are very close at T~300 K. Here the deeper *D*-center is involved in charge exchange at lower temperatures, so that the total DLTS peak looks like a peak from a single center (Fig. 2).

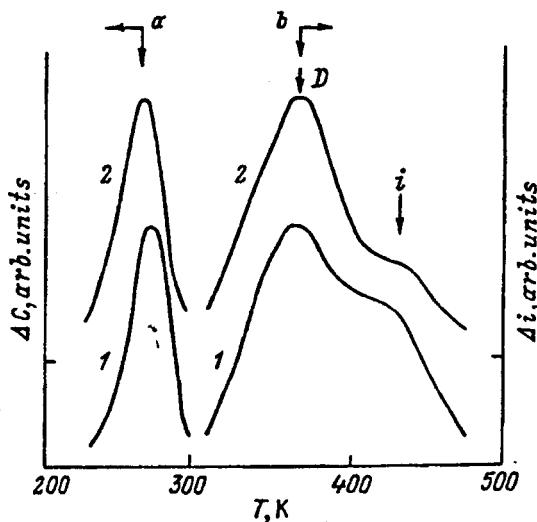


Fig. 2. DLTS (a) and *i*-DLTS (b) spectra of a sublimation-grown p-n structure with large (1) and small (2) ratios of the concentrations of *i*- and *D*-centers. Parameters of the spectra:  $t_1 = 10$ ,  $t_2 = 30$  ms (a) and  $t_1 = 0.1$ ,  $t_2 = 0.5$  ms (b)<sup>119</sup>.

In order to resolve the signal from these deep centers, the current-relaxation *i*-DLTS method has been used<sup>120</sup>. This method has a high resolving power, since it, in fact, yields the first derivative of the DLTS spectrum. In addition, the use of other temporal windows made it possible to enter a temperature region where the charge-exchange time constants for the observed deep centers differ more strongly. Fig. 2 shows an *i*-DLTS spectrum of an SE structure, in which the signals from the initial centers can be seen clearly<sup>119</sup>.

Thus, in SE structure both *i*- and *D*-centers exist. The ionization energies of these centers are independent of the electric field strength in the space charge region at the concentrations and reverse voltages that have been studied<sup>39,119</sup>. Methods for resolving the DLTS signals in these structures showed that *D*-centers predominate in SiC(B), and *i*-centers predominate in ID structures. Additional diffusion of boron into epitaxial SE layers prior to formation of the *p-n* junction also leads to predominance of the *D*-centers. In epitaxial 4*H*-SiC layers doped with boron during growth, an analogue of the *D*-center ( $E_v + 0.54$  eV) has been observed<sup>42, 73</sup>.

## Other defects

A center has been observed near the midgap ( $E_v +1.41\text{eV}$ ) in  $p$ - $6H$ -SiC and attributed to an intrinsic defect<sup>113</sup>. SiC samples doped with Mn and V and irradiated with neutrons have been studied<sup>121</sup>. A comparison of photoluminescence (PL) spectra and ESR data revealed the existence of a deep acceptor related to the appearance of red photoluminescence. Three traps ( $E_v+0.5$ ,  $E_v+0.56$ , and  $E_v+0.69\text{ eV}$ ) were found in a study of  $p$ - $6H$ -SiC (commercial photodetectors from CREE, Inc.)<sup>112</sup>. The first two of these have parameters close to those of the  $i$ - and  $D$ -centers, respectively.

### 2.3.2. Defects in the upper half of the band gap

#### $6H$ -SiC

##### R- and S-centers

In studies of  $6H$ -SiC Schottky diodes, two deep centers have been observed:  $S$  ( $E_c-0.35\text{eV}$ ,  $\sigma_p \sim 10^{-15}\text{cm}^2$ ) and  $R$  ( $E_c-1.27\text{ eV}$ )<sup>123-124</sup>. The concentrations of these levels,  $N_R$  and  $N_S$ , were the same within 10–20% in all the surface-barrier structures studied.  $N_R$  and  $N_S$  of  $\sim 10^{15}\text{ cm}^{-3}$  were close to the values of  $N_R$  and  $N_S$  in ID and SE  $p$ - $n$  structures based on these epitaxial layers. Thus, we may conclude that during the creation of a  $p$ - $n$  junction, there was no significant change in the concentration of the  $R$ - and  $S$ -centers.

In CLE structures, the concentrations of these deep centers were also the same and, on the average, an order of magnitude lower than those in SE structures. It has been shown that these centers are formed upon irradiation and ion implantation of  $6H$ -SiC<sup>73</sup>. Since these levels are annealed-out at different temperatures, it appears that they belong to two different centers, rather than to a single doubly charged center. A metastable defect in  $6H$ -SiC have been characterized using various junction space-charge techniques, annealing and simulation<sup>125</sup>. A double center ( $E_1/E_2$ ) ( $E_c-0.34$ ,  $E_c-0.41$ ) with parameters close to those of the  $S$ -center were observed first in substrates grown by the Lely method<sup>126</sup> and then in epitaxial layers grown by CVD<sup>127</sup>.  $R$ - and  $S$ -centers have been examined as the main centers of nonradiative recombination<sup>124</sup>. According to ref.<sup>128</sup>,  $E_1$  and  $E_2$  are acceptor levels of two negative  $U$ -centers. Donor levels of these centers lie at  $E_c-0.28\text{ eV}$  and  $E_c-0.2\text{ eV}$ , respectively. On the basis of ESR data, the structure of these centers was identified as a complex of Si-vacancies<sup>129</sup>.

#### $Z_1/Z_2$

Yet another double peak  $Z_1/Z_2$  ( $E_c-0.6-0.7\text{eV}$ ) was observed<sup>126</sup> and, later, also found in CVD epitaxial layers<sup>122</sup>. The ESR technique has been used previously to study several deep centers in  $6H$ -SiC substrates grown by the Lely method<sup>130</sup>. One of the centers observed, having the energy of  $\sim 600\text{ meV}$ , was related to a  $V_C-V_{Si}$  divacancy. It has been suggested that this center corresponds to the  $Z_1/Z_2$  center observed by DLTS<sup>73</sup>.

## 4H-SiC

A shallower intrinsic defect was found in sublimation-grown 4H-SiC epilayers at  $E_c$ –(0.16–0.18) eV<sup>131</sup>. The parameters of this center were very close to those of the radiation defects  $P_1/P_2$  from ref.<sup>73</sup>. More common for 4H-SiC is the background level  $Z_1$  with an energy  $E_c$ –(0.63–0.68) eV, which was identified in materials grown by different technological procedures<sup>73,127,131,132</sup>. According to ref.<sup>131</sup>, the concentration of  $Z_1$  falls with decreasing  $N_d/N_a$  value in the epilayer. However, it is still present in very-low-doped ( $N_{d,a} \sim 10^{14}$  cm<sup>-3</sup>) CVD epilayers<sup>116</sup>. For the same  $N_d/N_a$ , it is lower in layers with a high dislocation density. The  $Z_{1/2}$  defect concentration was observed to increase with the concentration of incorporated nitrogen<sup>133</sup>. In semi-insulating bulk 4H-SiC, a deep center was found at  $E_c$ –1.1 eV, which is not related to vanadium impurities<sup>134,135</sup>.

## 3C-SiC

Studies of background defects in 3C-SiC have been conducted on epitaxial layers grown on silicon substrates<sup>136, 137</sup>. Two centers were observed in ref.<sup>136</sup>, SC1 ( $E_c$ –0.34 eV) and SC2 ( $E_c$ –0.58 eV), with DLTS peaks that could be hardly observed on the background of a continuous relaxation band. These bands might be associated with a high density of volume defects (dislocations, etc.). After eight years, the quality of the epitaxial films was improved greatly and this was reflected in the DLTS spectrum shown in ref.<sup>137</sup>, in which the signals from the separate levels are now fully resolvable. Three deep centers were observed in ref.<sup>137</sup>: T<sub>1</sub> ( $E_c$ –0.32 eV), T<sub>2</sub> ( $E_c$ –0.52 eV), and T<sub>3</sub> ( $E_c$ –0.56 eV), the shallowest of which was identified with the previously observed SC1. In 3C-epilayers grown by sublimation epitaxy on 6H-SiC substrates, only one DC ( $E_c$ –0.62 eV) was found, close in parameters to T<sub>3</sub> and SC3<sup>117</sup>.

## 2.4. Radiation doping of SiC

### 2.4.1. Electrons

In a study of *n*-6H-SiC bombarded with 3.5–4 MeV electrons, centers were observed in the upper half of the band gap, with energies of 0.35, 0.6, and 1.1 eV<sup>138</sup>. All these defects were annealed-out at temperatures of up to ~1300K. According to their ionization energies, these defects can be associated with intrinsic defects: an S center,  $Z_1/Z_2$  and a center at  $E_c$ –1.06eV. In addition to an increase in the concentration of the background defects  $E_1/E_2$  and  $Z_1/Z_2$ , a new center  $E_3/E_4$  ( $E_c$ –0.57eV) was observed<sup>139–141</sup>. A similar increase in the concentration of the S center ( $E_1/E_2$ ) has been observed for CVD epitaxial layers bombarded with 2-MeV electrons<sup>120</sup>. In addition, a center ( $E_c$ –0.51 eV), which was annealed-out at temperatures ~800°C, has been observed. The most stable center with respect to annealing was the S-center, which was preserved up to temperatures of ~1000°C.

A bombardment of 4H-SiC CVD structures with 2–2.5-MeV electrons<sup>127,145–147</sup> led, in addition to an increase in the concentration of the background level  $Z_1$ , to formation of a set of defects:  $EH_1$  ( $E_c$ –0.45 eV),  $EH_2$  ( $E_c$ –0.68 eV),  $EH_4$  ( $E_c$ –0.72 eV),  $EH_5$  ( $E_c$ –1.15 eV),

and  $EH_6/EH_7$  ( $E_c - 1.65$  eV) and  $HH_1$  ( $E_v + 0.35$  eV). Most of these centers also appeared after implantation of He and some other ions<sup>73</sup>. In two, most recent of the above noted, publications<sup>142, 143</sup>, several new DC were found:  $E_c - 0.2$  eV;  $E_c - 0.32$  eV;  $E_c - 1.34$  eV. In ref.<sup>142</sup>, the deep level found at  $E_c - 0.5$  eV was identified as a vacancy-impurity complex, because it was found to have a lower saturation concentration and weak thermal stability. In *p*-type 6*H*-SiC, two deep centers have been identified at  $E_v + 0.55$  eV and  $E_v + 0.78$  eV after irradiation with 1.7-MeV electrons<sup>144</sup>. Both deep were centers annealed-out at 200–500°C. In ref.<sup>148</sup> photoexcitation-electron-paramagnetic-resonance (photo-EPR) studies were performed on *p*-type 4*H*-SiC irradiated with 2.5-MeV electrons. The photo-EPR results obtained for a positively charged carbon vacancy ( $V_{C+}$ ) can be explained in terms of the deep-donor model with a (+/0) level lying at  $(1.47 \pm 0.06)$ eV above the valence band edge.

#### 2.4.2. Neutrons

A number of deep centers have also been observed after neutron bombardment of SiC: ( $E_c - 0.5$ ,  $E_c - 0.24$ , and  $E_c - 0.13$  eV)<sup>149,150</sup>. It was shown that *p*-type SiC subjected to neutron irradiation has a weak electron conductivity before annealing<sup>148,152</sup>. After a high doze of neutron irradiation ( $\sim 10^{21} \text{ cm}^{-2}$ ), amorphization of 6*H* and 15*R* SiC samples takes place. Annealing of amorphized layers leads to formation of inclusions of 3*C*-SiC polytypes<sup>153</sup>. There are several more recent papers concerned with the effect of neutron irradiation on the properties of SiC<sup>154,155</sup>. Mostly the effect of this type of irradiation on the current-voltage characteristics of devices was studied. It has been reported that the rate of carrier removal for SiC is about 4.5 (carriers/cm<sup>3</sup> neutrons/cm<sup>2</sup>), which is roughly a factor of 3 lower than that for silicon<sup>156</sup>. In neutron-irradiated 3*C*-SiC, a deep centre  $E_c - 0.49$  eV, annealed-out at 350°C was found<sup>157</sup>. The measured value of free-carrier removal was  $7.2 \text{ cm}^{-1}$ , which is comparable with  $7.8 \text{ cm}^{-1}$  for Si irradiated with the same neutron spectrum.

According to an EPR study of neutron-irradiated and annealed 6*H*-SiC<sup>158</sup>, only the defect model of the carbon antisite–carbon vacancy pair ( $C_{Si} - V_C$ ) in the double positive charge state can explain all the experimental results. It was suggested in ref.<sup>158</sup> that this defect is formed from an isolated silicon vacancy produced by annealing, through movement of a carbon neighbor into the vacancy.

In ref.<sup>159</sup>, a conclusion was made that a high-temperature stable defect complex arises in 6*H*-SiC heavily neutron-irradiated and annealed at 1500°C. It was suggested that this complex may comprise a four-vacancy complex  $V_{Si} - 3VC$  and a split-interstitial antisite ( $C_2$ )<sub>Si</sub> or a pair of two antisites ( $C_2$ )<sub>Si</sub> –  $Si_C$ .

#### 2.4.3. Alpha-particles

It has been reported<sup>122</sup> that irradiation of *n*-and *p*-6*H*-SiC with alpha particles leads only to an increase in the concentration of the already existing background defects. These studies demonstrated that, in terms of radiation resistance, SiC is as good as InP, another radiation-resistant semiconductor.

#### 2.4.4. Protons

Several studies have been concerned with the possibility of proton (hydrogen) passivation of silicon carbide<sup>160–165</sup>. Irradiation with protons with the energy of 350 keV at a dose of  $1 \cdot 10^{14} \text{ cm}^{-2}$  resulted in a resistivity of *n*-4*H*-SiC as high as  $8 \cdot 10^6 \Omega \text{ cm}$  at room temperature<sup>165</sup>. At higher temperatures, the resistivity steeply decreased. The influence exerted by low-energy proton irradiation and subsequent annealing on the properties of SiC samples was studied in ref.<sup>164</sup>. It was demonstrated that whether or not proton irradiation of SiC can be used in various technological processes depends on the irradiation dose. The "boundary" dose for 100-keV protons is  $\sim 3 \cdot 10^{17} \text{ cm}^{-2}$ . Doses of  $\leq 3 \cdot 10^{17} \text{ cm}^{-2}$  lead to development of blistering in the course of annealing and can be used in the "Smart Cut" technology. At doses of  $\geq 3 \cdot 10^{17} \text{ cm}^{-2}$ , blistering is suppressed, in all probability, through amorphization of the irradiated layer.

The parameters and structure of deep centers in *n*-type 4*H*-SiC and 6*H*-SiC irradiated with 8 MeV protons were studied in ref.<sup>166–168</sup>. An analysis of irradiated samples demonstrated that  $N_d \cdot N_a$  decreases at room temperature and markedly increases on heating a structure to 650 K. For 6*H*-SiC, the  $N_d \cdot N_a$  value measured at 650 K was even higher than that in the initial structures prior to irradiation. As the irradiation dose increases, this difference becomes more pronounced (Fig. 3 and 4). Irradiation also leads to an increase in the resistance of forward-biased structures (Rb) at room temperature. On heating, the Rb value decreases exponentially with an activation energy  $\varepsilon_A$ . As the irradiation dose is raised, the  $\varepsilon_A$  value becomes higher, asymptotically approaching the value of  $\sim 1.1 \text{ eV}$  for 6*H*-SiC and  $1.25 \text{ eV}$  for 4*H*-SiC<sup>168</sup>. The parameters of these centers are close to those previously observed in electron-irradiated SiC (Table 1 and 2).

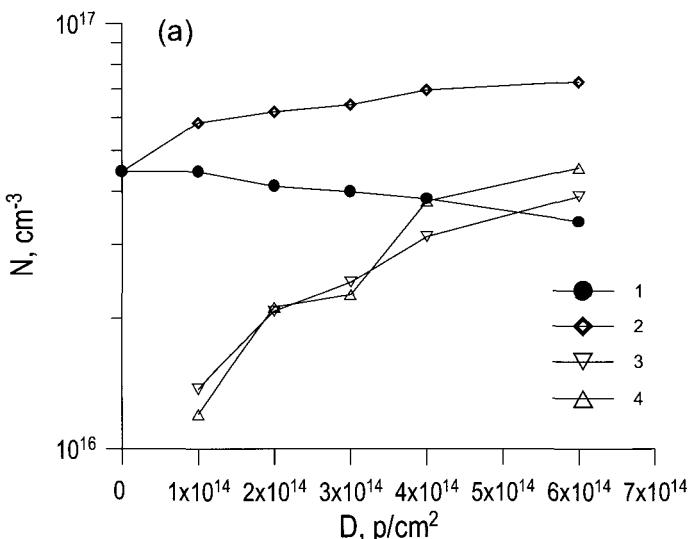


Fig. 3. 6*H*-SiC.  $N_d \cdot N_a$  at  $T = 300 \text{ K}$  (1) and  $T = 650 \text{ K}$  (2), difference of these (3), and concentration of the center at  $E_c - 1.1 - 1.22 \text{ eV}$  (4) vs. the irradiation dose. From ref.<sup>168</sup>

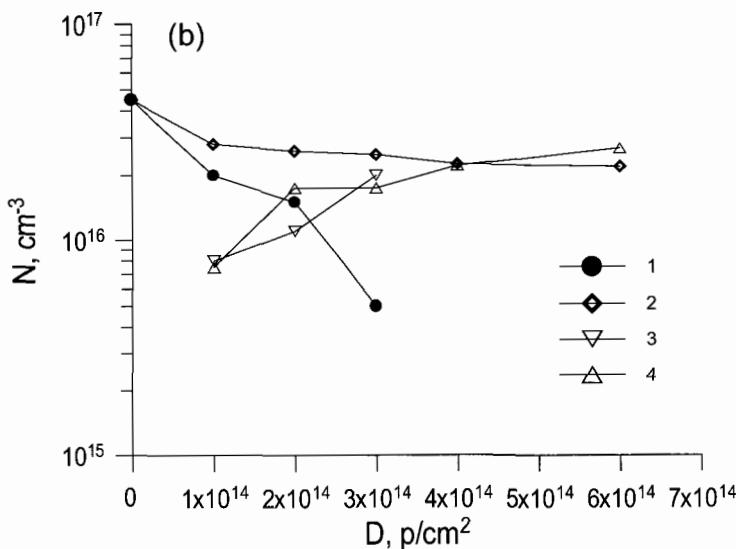


Fig. 4. 4H-SiC.  $N_d - N_a$  at  $T=300$  K (1) and  $T=650$  K (2), difference of these (3), and total concentration of the centers (RD1/2 + RD3 + RD4) (4) vs. the irradiation dose. From ref.<sup>[168]</sup>

Table 2. Parameters and properties of RDs observed in 6H-SiC

Parameters of observed RDs in proton irradiated SiC <sup>168</sup>			Correspondence to published data			Possible structure
$E_c - E_0$ , eV	$\sigma_n$ , cm <sup>2</sup>	T (ann.), K	Neutron irradiation <sup>[198]</sup>	Electron irradiation <sup>[143]</sup>	Structural defects	
0.16–0.2	$6 \cdot 10^{-17}$	800–950	$E_c - 0.13 E_c - 0.24$	$L_1/L_2$		Primary defects <sup>[168]</sup>
0.36/0.4	$2 \cdot 10^{-15}$	1100<..<1800	$E_c - 0.36/0.44$	$L_3/L_4$	$E_1/E_2^{[73]}, S^{[124]}$	Vsi-complex <sup>[129]</sup>
0.5	$5 \cdot 10^{-15}$	800–950	$E_c - 0.5$	$L_6$		Vc <sup>[143,168]</sup>
0.7	$4 \cdot 10^{-15}$	1100<..<1800	$E_c - 0.62/0.68$	$L_7/L_8$	$Z_1/Z_2^{[73]}$	Vc + Vsi <sup>[73,168]</sup>
0.8	$4 \cdot 10^{-15}$	1100<..<1800		$L_9$		
1.1 – 1.22	$2 \cdot 10^{-15}$	1100<..<1800		$L_{10}$	$R^{[124]}$	Vc + Vsi <sup>[168,181]</sup>

Table 3. Parameters and properties of RDs observed in 4H-SiC

Parameters of observed RDs in proton irradiated SiC <sup>168</sup>			Correspondence to published data			Possible structure
E <sub>c</sub> – E <sub>0</sub> , eV	σ <sub>n</sub> , cm <sup>2</sup>	T (ann.), K	Electron Irradiation [120,142,143,145–146]	Implantation of He <sup>+</sup> <sup>[73]</sup>	Structural defects	
0.18	6·10 <sup>-15</sup>	800–950	E <sub>c</sub> –0.2	P <sub>1</sub> /P <sub>2</sub>	E <sub>c</sub> –0.18±0.2 [131]	Primary defects <sup>[168]</sup>
			EH <sub>1</sub> (E <sub>c</sub> –0.45)			Vacancy+impurity <sup>[142]</sup>
0.63–0.75·10 <sup>-15</sup>	1100<..<1800		EH <sub>2</sub> ,EH <sub>4</sub>	Z <sub>1</sub>	Z <sub>1</sub> <sup>[73]</sup>	Vc <sup>[168]</sup>
0.96	5·10 <sup>-15</sup>	1100<..<1800		RD <sub>1/2</sub>		Vc+Vsi <sup>[168]</sup>
1.0	1·10 <sup>-16</sup>	1100<..<1800	EH <sub>5</sub>	RD <sub>3</sub>		Vc+Vsi <sup>[168]</sup>
1.5	2·10 <sup>-13</sup>	1100<..<1800	EH <sub>6</sub> /EH <sub>7</sub>	RD <sub>4</sub>	E <sub>c</sub> –1.1 eV [135]	Vc+Vsi <sup>[168]</sup>

#### 2.4.5. "Defect" luminescence

A short-wavelength luminescence at 2.6–2.3 eV was observed in 1966 by Makarov<sup>169</sup> in *n*-6H-SiC crystals bombarded with K and Li ions and then annealed. The luminescence spectrum consisted of two triplets of narrow lines (*H*- and *L*-lines) at 2.6 eV and a broad structureless band peaked at 2.35 eV. It was later established<sup>170,171</sup> that the broad band is not an extension of the fine structure and it was suggested that this band is due to radiative recombination involving a nitrogen donor level and an acceptor center that arises during implantation. The structure of the *H*- and *L*-lines has been studied in detail with their temperature dependences<sup>172</sup> and the spectrum itself is designated as D<sub>1</sub>. The D<sub>1</sub> spectrum has been recorded in SiC after irradiation with electrons<sup>173</sup>, neutrons<sup>151</sup>, and various types of ions<sup>171</sup>. It has therefore been possible to fabricate efficient light-emitting diodes operating in the green spectral range from 6H-SiC ion-doped with Al and Ga<sup>174</sup>. The irradiation has yielded luminescence with similar properties in other polytypes of SiC<sup>170</sup>. Since this sort of luminescence appears as a result of irradiation or implantation of various kinds of ions into SiC, it was suggested that the luminescence-activating center is either a purely defect or defect complex with a background impurity atom<sup>176–178</sup>. It was shown in ref.<sup>179</sup> shown that *H*- and *L*-lines can be accounted for by recombination of a bound exciton. No deep centers coupled to this defect have been observed. It was only suggested that the D<sub>1</sub> spectrum can be associated with the Z<sub>1</sub> center (in 4H-SiC)<sup>73</sup> or *i*-centre (in 6H-SiC)<sup>180</sup>.

#### 2.4.6. In summary

In summary of this section we can conclude that the spectrum of RDs introduced into each silicon carbide polytype is virtually independent of the material growth technology and charged particles used for irradiation (protons, alpha-particles, electrons).

Irradiation generates in both the polytypes deep acceptor centers to which electrons from shallower donor levels pass. This shifts downwards the Fermi level to give *n*-type 6*H*- and 4*H*-SiC layers that are semi-insulating at room temperature.

The number and properties of RDs appearing in two different SiC polytypes under irradiation are not totally identical. The  $N_d \cdot N_a$  concentration increases in irradiated 6*H*-SiC samples. By contrast, the total concentration of uncompensated donors in proton-irradiated 4*H*-SiC decreases. This indicates that acceptor centers are formed in 4*H*-SiC in the lower half of the band gap or donor centers are destroyed in its upper half. At the same time, the concentration of donor RDs formed in 6*H*-SiC exceeds that of the acceptor centers. The results obtained may be applicable in the SiC device fabrication technology for creating local high-resistance regions in the semiconductor. This result is particularly important for devices not intended to operate at high temperatures — e.g., photodetectors or various radiation detectors.

### 3. Influence of Impurities on the Growth of Epitaxial SiC Layers

#### 3.1. Heteropolytype SiC epitaxy

It has been found<sup>182–184</sup> that, when certain impurities are added to the growth zone of SiC layers, it is possible to obtain epitaxial films of a polytype other than that of the substrate. For example, introduction of the rare-earth elements Sc and Tb, as well as Al and B, yielded epitaxial 4*H*-SiC films on 6*H*-SiC substrates. The most efficient transformation of the polytype of the growing layer, 6*H*=>4*H*, has been observed upon introduction of Group-IV impurities: Sn, Pb, and Ge. Group-V impurities (nitrogen and phosphorus) facilitated the growth of the 3*C* polytype.

It was also found that changing the ratio of the Si and C concentrations in the growth zone had a significant effect on heteropolytype epitaxy. An increase in the Si concentration, for example, leads to a rise in the probability of formation of 3*C*-SiC or other polytypes with a low hexagonal percentage. At the same time, the introduction of an excess carbon made it possible to grow epitaxial layers of 4*H*-SiC from melts of Gd and Dy also on 6*H* substrates<sup>19</sup>. It has also been noted<sup>182</sup> that the transformation of the substrate polytype takes place especially easily during growth in the (0001)*C* direction. In this case, the temperature and growth rate had little effect on the process of heteropolytype epitaxy.

Thick epitaxial layers of 4*H*-SiC on 15*R*- and 6*H*-SiC substrates have been produced and then used as seeds to grow single-crystal ingots<sup>185,186</sup>. This was done on the (0001)*C* face, with Sc added to the vapor phase. The method made it possible to obtain epitaxial layers of both *n*- and *p*-types. It was noted<sup>186</sup> that a high concentration of Sc ( $\geq 10^{17} \text{ cm}^{-3}$ ) in the epitaxial films produced mechanical stresses in them. On the whole, the epitaxial

layers obtained in this way had a fairly high structural perfection, so that they could be used to fabricate field-effect transistors with a gate in the form of a *p-n*-junction (JFET transistors)<sup>187</sup>.

3C-SiC layers on 6H-SiC substrates can also be produced by sublimation growth with an excess of silicon and no additional doping<sup>188</sup>. In this case, 3C films grow with twinning, and the area of a single twin is, at most, 4–6 mm<sup>2</sup><sup>138,189</sup>. An *n*-6H-SiC/*p*-3C-SiC heterojunction has been fabricated by a similar technology and its electrical characteristics were reported in ref.<sup>190</sup>.

Since the nature of polytypism is still unclear, it is also rather difficult to understand the nature of the heteropolytype epitaxy. The probability of heteropolytype epitaxy can be affected not only by the impurity composition of the growth zone, but also by various other factors, ranging from thermodynamic (pressure, temperature) to crystallographic (orientation and the degree of imperfection of the substrate). It has been found<sup>191</sup>, for example, that if substrates of 6H-SiC produced by the Lely method with a high density of dislocations ( $\sim 10^5$  cm<sup>-2</sup>) are used in the standard (commonly employed to grow 6H layers) sublimation epitaxy process, epitaxial 3C layers will be grown.

Heteropolytype epitaxy processes have been related to the stoichiometric composition of various SiC polytypes<sup>182,192</sup>. It had been observed earlier that the ratio of the Si and C concentrations varies between different SiC polytypes, and that it decreases as the hexagonal percentage is increased. It was shown that the ratio of the Si and C concentrations was 1.046, 1.022, and 1.001 for 3C, 6H, and 15R, respectively<sup>193</sup>. An examination<sup>182</sup> of data on diffusion and solubility in various SiC polytypes indicated that the vacancy concentrations  $V_c$  are also different.

The observed dependence was accounted for ref.<sup>182</sup> by the fact that, when the stresses in the lattice rise as the concentration of carbon vacancies increases, bonds between atoms in cubic sites become more energetically favorable. This also leads to a realignment of the crystal and a polytype transformation. It was also assumed<sup>182</sup> that most of  $V_c$  are in an electrically inactive state. The formation of 3C inclusions in 6H-SiC *p-n*-structures under the action of a forward current has also been reported<sup>194</sup>.

### 3.2. Site-competition epitaxy of SiC

Larkin *et al.*<sup>195</sup> have found that the concentration of electrically active impurities depends on the ratio of the concentrations of C and Si in the gaseous phase during CVD growth of epitaxial SiC layers. They referred to this effect as site-competition epitaxy (SCE)<sup>195</sup>. The n-SiC epitaxial layers with uncompensated donor concentrations  $N_d \cdot N_a \sim 10^{14}$  cm<sup>-3</sup> has been obtained using SCE<sup>156,196</sup>. The observed dependence was accounted for the work<sup>195</sup> by a high concentration of C atoms on the crystal growth surface, which inhibits the implantation of N atoms that occupy carbon sites in the lattice. This dependence was observed only in the case of growth on the Si-face of the substrate. During growth on the C-face, changing the ratio of the C and Si concentrations had little effect on the concentration of the electrically active impurity. This model has been confirmed by secondary ion mass spectrometry (SIMS) measurements of the concentration of N atoms

in SiC epitaxial layers grown with different ratios of the C and Si concentrations in the gaseous phase. However, a change in the concentration of N atoms by a factor of 2.5–3.5 corresponded, in the SIMS data, to a decrease in  $N_d - N_a$  by a factor of 4 or 5. In our opinion, this indicates that some other factor may also affect the magnitude of  $N_d - N_a$ . This may be a dependence of the concentration of background acceptor defect centers in epitaxial layers on the ratio of the C and Si concentrations in the gaseous phase, which means that it might be assumed that the total concentration of background acceptor levels increases as the ratio of the C and Si concentrations is lowered. This assumption is consistent with a report<sup>196</sup> that lightly doped *p*-layers were obtained at the highest ratio of the C and Si concentrations in the gaseous phase.

Such an effect, i.e., the overcompensation of lightly doped *n*-layers by deep background acceptors (*i*- and *D*-centers), has also been observed during growth of 6H-SiC by sublimation epitaxy<sup>117</sup>. It has also been found in studies of epitaxial layers grown by sublimation epitaxy that raising the pressure of silicon ( $P_{Si}$ ) in the growth cell (increasing the ratio of the C and Si concentrations) leads to overcompensation of the growing layer and, then, with  $P_{Si}$  raised further, even more heavily doped *p*-SiC layers are obtained<sup>197</sup>.

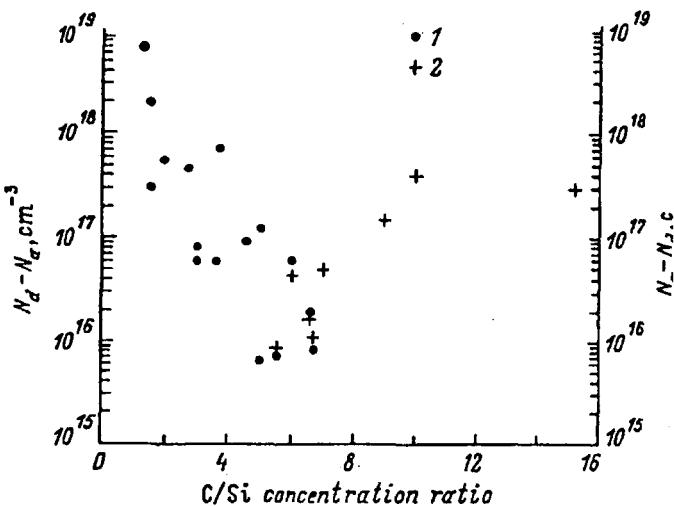


Fig. 5. The type of conductivity and  $N_d - N_a$  ( $N_a - N_d$ ) in 6H-SiC CVD epitaxial layers as a function of the concentrations of C and Si in the gaseous phase during growth: (1) *n*-type, (2) *p*-type<sup>198</sup>.

In studies of 6H-SiC layers grown by CVD (in methane+silane+ $H_2$ ) in our laboratory, it has also been found that, as the ratio of the concentrations of C and Si in the gaseous phase is raised, there is an initial inversion of the conductivity type, followed by the growth of progressively more heavily doped *p*-layers (Fig. 5). DLTS studies of these *p*-layers demonstrated that the main contribution to  $N_a - N_d$  is from deep acceptor centers ( $E_c + 0.2 \pm 0.02$  eV), whose parameters are close to those of the L-center, the usual

background center in layers grown by sublimation. The concentration of these centers increased as  $N_a-N_d$  became higher (i.e., as the ratio of the concentrations of C and Si, which was maintained in the gas mixture during growth of the given layer, was raised).

Thus, we believe that a change in the ratio of the C and Si concentrations during growth of epitaxial SiC layers not only affects the trapping of nitrogen atoms in the SiC lattice, but also influences the concentration of the background deep acceptor levels formed in the process.

#### 4. Deep Centers and Recombination Processes in SiC

##### 4.1. Deep centers and radiative recombination in 6H- and 4H-SiC p-n structures.

The wide band gap in SiC has made it possible to fabricate light-emitting devices for the essentially entire visible spectrum. The same mechanism of radiative recombination (the same technique for fabrication of a light-emitting diode) corresponding to different energies for the emission peak in different polytypes; i.e., compared to 6H-SiC, the position of the electroluminescence peak shifts to shorter wavelengths (in the case of a wider gap polytype) or to longer wavelengths (in the case of a narrower gap polytype) by an amount roughly equal to the difference between the band gaps of the given polytype and 6H-SiC (Fig. 6). As can be seen from this figure, the energy of the emission peaks depends linearly on the width of the band gap. The intercept formed by extrapolating these curves to zero  $h\nu_{max}$  can be used to roughly estimate the ionization energy of the recombination center [the sum of the energies of two centers, in the case of a donor-acceptor recombination (DAR)]

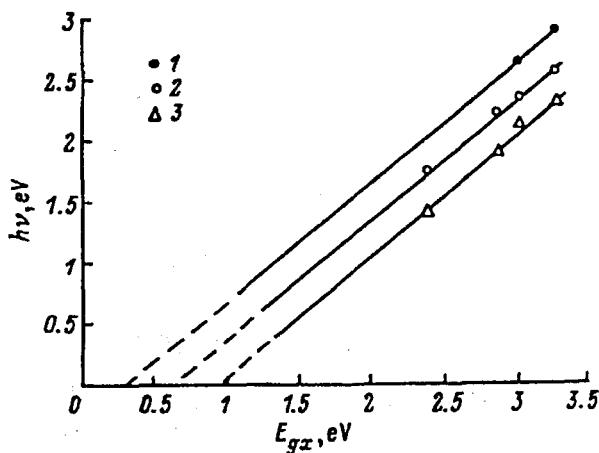


Fig. 6. The position of the peaks of several electroluminescence bands in SiC polytypes as a function of the excitonic band gap: (1) "aluminum" electroluminescence<sup>26</sup>, (2) "defect" electroluminescence<sup>175</sup>, and "boron" electroluminescence<sup>225</sup>.

The EL spectra of 4H and 6H p-n structures doped with various impurities were analyzed in detail in ref.<sup>198</sup>. It was concluded that, in 6H and 4H SiC, the *i*-center is the activating center for the "Defect" EL, D-center for the "boron" EL, and HK<sub>1</sub> and HK<sub>2</sub> centers for the "aluminum" EL.

Already, in Losev's papers, it was noted that, when the forward current density is raised, the emission spectrum of SiC *p*-*n* structures shifts to shorter wavelengths. An explanation for this effect, which is based on the tunnel mechanism of current transport in SiC *p*-*n* structures, was suggested<sup>199</sup>. This explanation<sup>199</sup> is evidently not relevant to modern SiC *p*-*n* structures, in which the thermal injection mechanism of current transport dominates. The position of the electroluminescence peak in 4H-SiC ID and SE *p*-*n* structures with different concentrations of the uncompensated donor impurity in the base and different concentrations of background deep acceptors has been studied<sup>118,200</sup>.

It was found that, as the forward current density is raised in SE structures of 4H- and 6H-SiC, there is a smooth shift of the electroluminescence peak over the approximate interval 2.14–2.35 eV (6H) and 2.4–2.52 (4H). The capacitance and current spectroscopy made it possible to detect *i*- and *D*-centers in SE. These deep centers are involved in various mechanisms of radiative recombination and the intensity of the electroluminescence they produce depends in different ways on the excitation level. For example, the electroluminescence spectrum in *p*-*n* structures obtained by sublimation epitaxy is a superposition of two electroluminescence bands, whose intensity ratio (the position of the peak ( $h\nu_m$ ) of the resulting band) depends on the forward current density, i.e.,  $h\nu_m=f(J)$ . Calculations<sup>118–200</sup> of  $h\nu_m=f(J)$ , based on the parameters and concentrations of *i*- and *D*-centers, produced results that are in a good agreement with the experiment.

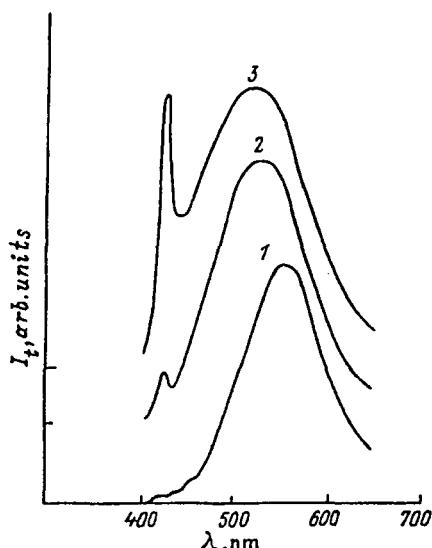


Fig. 7. Electroluminescence spectra of SE 6H-SiC samples with low concentrations of deep acceptor levels for different forward current densities  $J$  at room temperature (A/cm<sup>2</sup>): (1) 4, (2) 40, (3) 120<sup>201</sup>.

It has been shown<sup>201,202</sup> that, if the concentration of deep acceptor impurities in the base of a diode is low, then a peak associated with the recombination of a free exciton (Fig. 7) will appear at high forward current densities. The intensity of this band ( $I_{Ex}$ ) increases with  $J$  as  $I_{Ex} = (J)^n$ , where  $n$  is in the interval 2.2–2.7 for different samples. Such a rapid rise in the intensity of the exciton line may be associated with (1) temperature quenching of all the electroluminescence lines except the exciton line, or (2) an increase in the diffusion mean free path for holes as higher temperatures.

Therefore, the dependence  $hv_m = f(J)$  observed in several SiC  $p-n$  structures may be attributed to superposition of several independent electroluminescence lines which saturate at different forward current densities (different concentrations of the injected holes). The agreement<sup>118,200</sup> between the experimental and theoretical  $hv_m = f(J)$  dependences confirms the correctness of our determination of the activator centers and the validity of the recombination models of the defect electroluminescence and boron electroluminescence in SiC.

#### **4.2. Influence of deep centers on the diffusion length and lifetime in 6H-SiC $p-n$ structures**

It has been found previously<sup>203–205</sup> that the hole lifetime in sublimation-grown  $n$ -SiC lies in the range  $10^{-7}$ – $10^{-9}$  s, and that the diffusion mean free path of holes is in the range 0.01–1  $\mu\text{m}$ . It is clear that the recombination in SiC, which is an indirect band semiconductor, involves mostly deep centers. However, no centers that could be responsible for such a short lifetime have been found.

The temperature dependence of the hole diffusion length in epitaxial  $n$ -6H- and 4H-SiC obtained by different techniques has been studied<sup>206,207</sup>. It was found that the diffusion length ( $L_p$ ) increases with temperature. This sort of variation  $L_p = f(T)$  can be accounted for either by the involvement of rather shallow levels in the recombination or by a negative temperature dependence of the carrier capture cross section of a deep recombination center.

It has been found<sup>208</sup> by analysis of current-voltage characteristics and the magnitude of  $L_p$  in 6H-SiC  $p-n$  structures that nonradiative recombination mostly involves multiply charged centers whose parameters vary between structures obtained by different techniques. These centers, however, have not been observed experimentally.

It has been predicted<sup>83</sup> that the major center involved in nonradiative recombination in SiC is vanadium. This conclusion was based on the observed inverse proportionality between the intensity of donor-acceptor recombination in Al-N and the intensity of the luminescence associated with an intracenter transition at a vanadium center, i.e., the intensity of donor-acceptor recombination was quenched as the concentration of V increased. In our opinion, the evidence used to confirm this conclusion is not exhaustive, since a large number of different factors, in addition to the carrier lifetime, can affect the intensity of donor-acceptor recombination. These include the concentration of the centers, which was not determined in ref.<sup>83</sup>.

The recombination characteristics of minority carriers and the deep center characteristics in 6H-SiC *p-n* structures produced by different methods were studied comprehensively in ref.<sup>124</sup>. An analysis of the experimental data showed that the relaxation lifetime of minority carriers ( $\tau_{\text{rel}}$ ) is approximately 2 ns in SE structures and  $\tau_{\text{rel}}=20\text{--}30$  ns in CLE structures. The diffusion lengths of minority carriers in CLE and SE *p-n* structures with different levels of background doping were found to lie in the intervals 0.4–1.5 and 0.05–0.4  $\mu\text{m}$ , respectively.

The proposed lifetime was calculated using the parameters of the deep centers observed. The calculations showed that the only level whose parameters could account for the observed lifetime is the *S*-level. A calculation using the parameters of the *R*-center yielded a value of  $\tau_{\text{rel}}$  roughly an order of magnitude longer. Here, the concentrations of *R*- and *S*-centers in structures of both types were the same. The previously noted long lifetime of minority carriers in CLE structures, compared with that in SE structures, was attributed to a lower concentration of *S* and *R* deep centers in the CLE structures. A study of the dependence of  $\tau_{\text{rel}}$  and  $L_p^2$  at room temperature on the *S* and *R* concentrations showed that these quantities are inversely proportional.

The observed temperature dependence of  $L_p$  could be explained only using the parameters of a shallower *S*-center. A doubly charged *R-S* center has been suggested as a center determining the recombination parameters for the two types of 6H-SiC *p-n* structures that have been studied. However, the results of a later study cast doubt on the idea that these two levels belong to a single center<sup>82</sup>.

After CVD technology for growing SiC epitaxial layers was developed, the recombination characteristics of samples of this type were also studied<sup>209,210</sup>. The carrier lifetime was estimated by analyzing the kinetics of low-temperature photoluminescence to be 0.45  $\mu\text{s}$ , which is substantially longer than that in epitaxial SiC layers grown by other technologies. *S*- and *R*-centers were also found in CVD 6H-SiC layers, but their concentrations were one or two orders of magnitude lower than in SE structures<sup>73</sup>.

Fig. 8 shows a plot of  $L_p$  as a function of the concentration of *S*- and *R*-centers, which we have supplemented with data obtained for CVD samples in this study, along with data for the purest ( $\sim 10^{15}\text{cm}^{-3}$ ) SE layers. The figure shows that an inversely proportional dependence of  $L_p$  on the concentration of these levels is observed for all the three types of samples.

Therefore, these centers are currently the most likely candidates for the role of lifetime "killers" in 6H-SiC. Centers of this sort have not yet been observed in 4H-SiC.

In a recent study, it was found that  $L_p$  and  $\tau_p$  in 4H-SiC strongly depend on injection levels and change from 2  $\mu\text{m}$  and 15 ns (low injection level) up to 6–10  $\mu\text{m}$  and 140–400 ns (high injection level)<sup>211</sup>. Later it was shown, that the value of  $\tau_p$ , obtained from different measurement methods may strongly differ. The possible reason for this fact may be thin layer at the interface between the low-doped n-base of a diode and the high-doped p+ emitter. This layer can accumulate structural defects arising because of the lattice mismatch in the low- and high-doped SiC layers. This leads to a considerably shorter  $\tau_p$  in this layer in comparison with the rest of the base. Depending on the measurement

technology, you can get a value of  $\tau_p$ , corresponding to this layer or to the bulk of the base<sup>212</sup>. It was shown that a  $\tau_p$  better correlated with the switching characteristics of a device can be obtained by the method suggested by B. Gossik<sup>213</sup>. The  $\tau_p$  values recently obtained by this method for CVD-grown SiC epilayers are above  $10^{-6}$  s<sup>214</sup>.

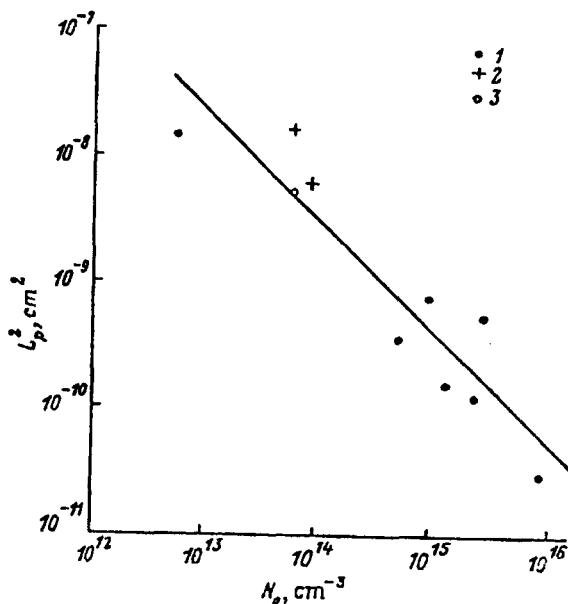


Fig. 8. Squared hole diffusion length in 6H-SiC epitaxial layers grown by different technologies as a function of the R-center concentration in  $p-n$  structures grown by (1) sublimation, (2) liquid phase epitaxy, and (3) CVD<sup>198</sup>

#### 4.3. Deep centers and the negative temperature coefficient for the breakdown voltage in SiC $p-n$ -structures

In 6H-SiC  $p-n$  structures where the electric field is parallel to the direction of the C crystal axis, the breakdown voltage generally has a negative temperature coefficient<sup>215</sup>. In a number of papers, this has been attributed to the crystalline structure of hexagonal SiC polytypes and to the existence of a natural superlattice<sup>216,217</sup>. Others<sup>218,219</sup> have suggested that the negative temperature coefficient for the breakdown voltage may be related to charge exchange between deep centers, as it has been shown for silicon<sup>220,221</sup>, or to the low structural perfection of SiC crystals<sup>222</sup>.

6H-SiC  $p-n$  structures obtained by sublimation epitaxy with boron diffusion carried out prior to formation of the mesa structures have been studied<sup>223</sup>. The test structures had a negative temperature coefficient for the breakdown voltage, equal to  $-2 \cdot 10^{-3} \text{ K}^{-1}$ . The magnitude of this temperature coefficient also depends on the temperature and falls by roughly an order of magnitude when the structures are heated to 600 K. In an analysis<sup>223</sup>

of the experimental data by the method used by the authors of refs.<sup>219-221</sup>, the effect of deep centers was taken into account. The model suggested in ref.<sup>223</sup> takes into account the charge exchange between deep acceptor levels by the pre-breakdown current in a lightly doped *p*-spacer near the metallurgical boundary of the *p-n* junction.

Two assumptions were made: 1) the avalanche region lies in a lightly *p*-doped region near the metallurgical boundary of the *p-n* junction and 2) the concentration of deep acceptor levels in this region is comparable with that of shallow acceptors. A region of this sort may develop because of the overcompensation of the *n*-type material, caused by diffusion of acceptor impurities (such as boron). The existence of a region of this type in the epitaxial-diffusion diodes tested has been demonstrated experimentally<sup>38</sup>. There is a well-known expression for the breakdown voltage of an abrupt *p-n* junction:

$$U_{br} = \frac{\varepsilon_a \cdot E_{cr}^2}{2qN_i}, \quad (1)$$

where  $E_{cr}$  is the critical electric field strength;  $N_i$ , the impurity concentration in the base; and  $q$ , elementary charge.

When  $U \ll U_{br}$ , there is essentially no current through the *p-n* junction and all the deep acceptors in the *p*-type region are filled with electrons ( $K=1$ ). Note to authors: please define  $K$ . When  $U \sim U_{br}$ , avalanche multiplication begins in the space charge region and deep acceptors capture the resulting holes. Since the acceptors that captured holes are neutral,  $K$  decreases and, accordingly, the electric field strength decreases. This leads to an increase in the observed value of  $U_{br}$ . It should be noted that the degree of filling of the levels depends on the temperature and decreases upon heating. For this reason,  $U_{br}$  decreases with temperature and we observe a negative temperature coefficient for the breakdown voltage.

On base of this equipment in ref.<sup>223</sup>, an expression was derived for  $U_{br}$  in the case when the influence on deep centers is important (note to authors: this sentence needs to be re-written):

$$U_{br} = U_{bro} \cdot \left( 1 + \frac{M\beta_i}{N_S \cdot (\Delta_p + \beta_i)} \right), \quad (2)$$

where  $M$  is the total concentration of deep acceptors;  $U_{bro}$ , the breakdown value of the *p-n* junction in the absence of deep acceptors;  $\Delta_p$ , the concentration of holes;

$$\beta_i = N_v \cdot V_t \cdot \sigma_p \cdot \exp(-E_t/kT); \quad (3)$$

$N_v$ , the density of states in the valence band;  $V_t$ , the thermal velocity of electrons;  $k$ , Boltzmann's constant;  $E_t$ , the ionization energy of deep centre; and  $\sigma_p$ , the hole capture cross section of deep centers.

At  $T \rightarrow 0$ ,  $\beta_i \rightarrow 0$  and  $U_{br}(T_{min}) \sim U_{bro}$ . In the case when  $T \rightarrow \infty$ ,  $\beta_i \rightarrow 1$  and, because  $N_v >> \Delta_p$ , we obtain

$$\frac{U_{br}(T_{\max})}{U_{bro} - 1} = \frac{M}{N_S}. \quad (4)$$

For the case examined in refs.<sup>205,206</sup>,  $U_{bro}$  and  $M/N_S$  were 800V and 0.65, respectively. Taking these values, together with the published values of  $N_v$ , we calculated the function

$$F = \left\{ \frac{U_{bro}}{U_{br} - 1} \right\}. \quad (5)$$

The calculated and experimental values of  $F$  are shown in Fig. 9. The figure shows that the best agreement between the theory and experiment is obtained for  $\Delta_p$  on the order of  $10^{11}-10^{12}\text{cm}^{-3}$ . However, the value of  $\Delta_p$ , determined from the pre-breakdown current by

$$\Delta_p = J/qV_S \quad (6)$$

(where  $J$  is the current density through the  $p-n$  junction, and  $V_S$  is the saturation rate), was  $10^{10}-10^{11}\text{cm}^{-3}$ . This discrepancy may be accounted for ref.<sup>223</sup> by the fact that breakdown in SiC usually occurs in local regions (microplasma breakdown) whose areas are more than an order of magnitude smaller than the total area of the  $p-n$  junction. However, in calculating the current density through the  $p-n$  junction, the area of the entire structure was used; in other words, in the regions where microplasma breakdown takes place there will be a substantially higher current density and value of  $\Delta_p$ , as required by this model.

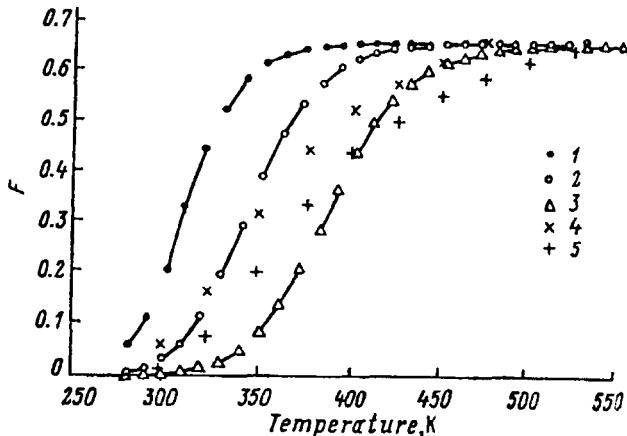


Fig. 9. Temperature variation of the calculated (1-3) and experimental (4-5) values of  $F$ . The calculations were done for  $\Delta P = (1) 10^{10}, (2) 10^{11}, (3) 10^{12} \text{ cm}^{-3}$ . The experimental values of  $U_{br}$  correspond to pre-breakdown currents of (4) 100 mA and (5) 500 mA<sup>223</sup>.

Therefore, the negative temperature coefficient for the breakdown voltage may be caused by charge exchange between D-centers ( $E_v + 0.58\text{eV}$ ), the deepest levels that exist in boron-doped SiC. The calculations of the temperature dependence of the negative temperature coefficient, based on this assumption and these parameters for the D-centers, are in a good agreement with the experiment.

It should be noted that natural superlattice can affect the electrical characteristics of SiC devices only in the case when the electric field ( $E$ ) is strictly parallel to crystal axis C. When the angle between  $E$  and C<sup>is</sup> greater than 5–10°, no superlattice effects will arise. For 4H-SiC, epilayers with better crystal perfection are grown on substrates with a misorientation of about 8°. Possibly, this is the reason why the breakdown temperature coefficient in 4H-SiC diodes is usually positive<sup>224</sup>

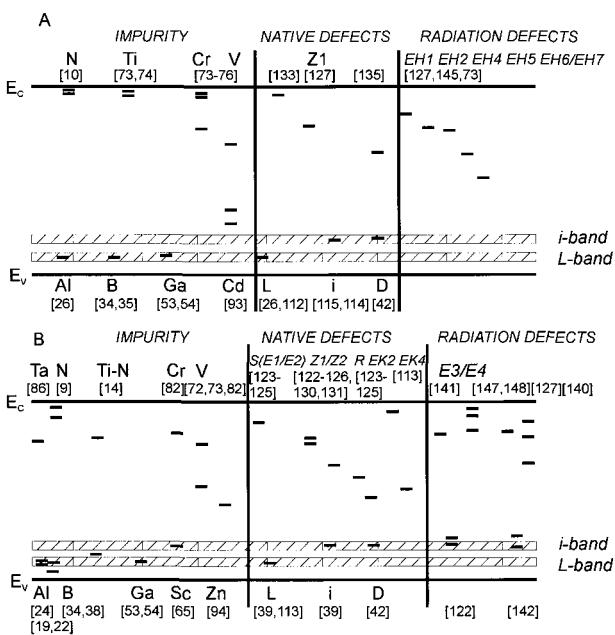


Fig. 10. Diagram of the positions of the known deep centers in the band gap of silicon carbide: (A) 4H-SiC, (B) 6H-SiC. Only those deep centers are indicated which have not been identified as previously observed structural defects<sup>198</sup>.

## 5. Conclusion

If the energies of the levels in the lower half of the band gap of 4H- and 6H-SiC (Table II and III) are compared, it will be noticed that most of the levels lie within two rather narrow bands in the band gap:  $E_v + (0.5\text{--}0.6)\text{eV}$  (*i*-band) and  $E_v + 0.2\text{--}0.3\text{eV}$  (*L*-band) (Fig. 10). The first band contains the levels related to the *D*-and *i*-centers and a scandium level. A deep aluminum level, a gallium level, and a level related to the *L*-center lie within the second band. The boron level also lies inside (4H) or near the edge (6H) of the

*L*-band. As the figure shows, the *4H*- and *6H*-SiC levels are distributed rather uniformly in the upper half of the band gap and it is impossible to distinguish any bands that coincide for both polytypes. Since the parameters of centers of the same type formed in the lower half of the band gap of different SiC polytypes are similar, it may be assumed that such bands are also present in other polytypes of silicon carbide. This conclusion is supported by the similarity of the characteristics and the shift, proportional to the band gap width, of the peaks of the main electroluminescence bands in various SiC polytypes (Fig. 6).

The formation of such bands within the band gaps of different SiC polytypes indicates that centers characteristic of SiC, as such, are present and coupled to the valence band, and the structure of these centers is about the same in different polytypes. It may also be assumed that each band is coupled to some "base" center consisting of intrinsic defects (this is an *i*-center in the first case and an *L*-center in the second) which can interact with atoms of an impurity introduced to form other centers with similar parameters.

What sort of intrinsic defect might be the main element in the formation of the defect complexes that produce deep centers in SiC? Fig. 11 shows the average concentrations of three intrinsic defects (*i*-, *D*-, and *L*-centers) in *6H*- and *4H*-SiC epitaxial layers grown by sublimation epitaxy<sup>112</sup>. The figure shows that there is a fairly good correlation between the drop in the concentration of carbon vacancies ( $V_c$ ) and the increase in the percentage of the hexagonal polytype and the reduction in the concentration of these centers.

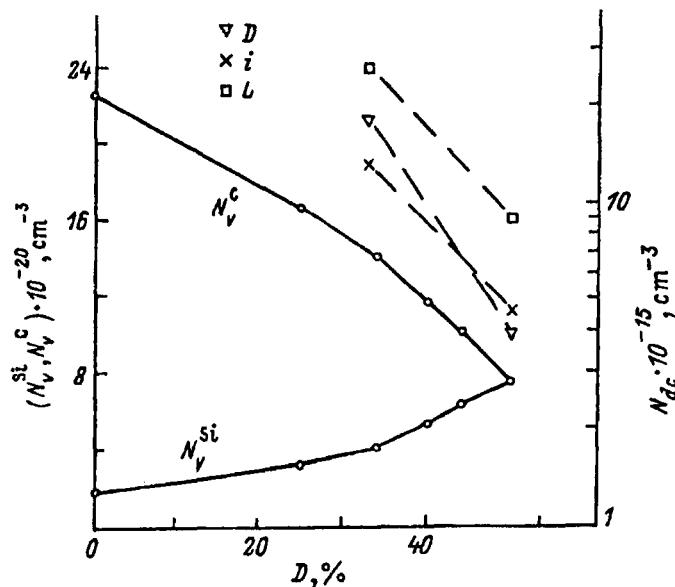


Fig. 11. Concentration of carbon ( $N_v^C$ ) and silicon ( $N_v^Si$ ) vacancies<sup>193</sup> and the average concentration of deep acceptor levels (*I*-, *L*-, *D*-centers) in sublimation-grown epitaxial layers as a function of the degree of hexagonality of the SiC polytype<sup>191</sup>.

The conclusion that the main complex-forming defects in SiC are carbon vacancies is supported by various publications in which it has been suggested that  $V_c$  is involved in the formation of different centers, while isolated vacancies merge into stable clusters<sup>149, 150</sup>. Note that the impurities (Sc, B, Al) used in heteroepitaxy of SiC<sup>182</sup> form deep centers whose levels lie within the above-mentioned  $L$ - and  $i$ -bands. The model of heteropolytype epitaxy, suggested in ref.<sup>182</sup>, can also be regarded as stating that each of the SiC polytypes corresponds to an equilibrium concentration of defects (carbon vacancies). When this concentration is changed by adding impurities that generate excess defects or bind vacancies into complexes, it becomes possible to produce by heteroepitaxy polytype films that have a lesser or greater degree of hexagonality, respectively, than the substrate.

Since an increase in the concentrations of  $L$ - and  $i$ -centers has been observed upon irradiation and implantation<sup>39,114,122</sup> (i.e., the equilibrium vacancy concentration was changed), it may be assumed<sup>112,198</sup> that irradiation or implantation (or other technological actions) can cause a transformation of the polytype of already-grown epitaxial structures. This assumption is consistent with the results of a study<sup>194</sup> concerned with degradation of blue 6H-SiC light-emitting diodes by a forward current, in which it was found that inclusions of the 3C polytype appeared in the degraded structures.

This analysis of published sources, therefore, demonstrates the considerable influence exerted by intrinsic defects in the SiC crystal lattice both on the formation of deep centers (and, accordingly, on radiative and nonradiative recombination processes) and on the properties of the epitaxial layers themselves (their doping level and polytype uniformity). A detailed study of the factors controlling the formation of defects and their interactions with one another and with impurity atoms will make it possible to greatly improve the parameters of SiC devices and allow SiC to occupy a central position, along with Si and GaAs, in modern semiconductor electronics.

## Acknowledgements

The author thanks V. V. Zelenin and N. S. Savkina for providing SiC samples for measurements, A. N. Kuznetsov and E.V.Bogdanova for preparing the ohmic contacts, A. M. Strel'chuk for providing data on measurements of diffusion lengths, and D. V. Davydov for help with the capacitance measurements.

## References

1. L. S. Berman and A. A. Lebedev, *Capacitance Spectroscopy of Deep Centers in Semiconductors* [in Russian], Nauka, Leningrad, 1981.
2. M.Bockstede, A.Mattausch, O.Pankratov, "Solubility of nitrogen and phosphorus in 4H-SiC: A theoretical study" *Appl.Phys.Lett.*, 85, 58–60 (2004).
3. M. V. Rao, J. B. Tucker, M.c. Ridgway, O. W. Holland, N. Papanicolau, J.Mittereder, "Ion-implantation in bulk semi-insulating 4H-SiC", *J. Appl. Phys.*, **86**, 752–758 (1999).
4. M. A. Capano, J. A. Cooper Jr., M. R. Melloch, A. Saxler, W. C. Mitchel, "Ionization energies and electron mobilities in phosphorus- and nitrogen implanted 4H-silicon carbide", *J. Appl. Phys.*, **87**, 8773–8777 (2000).

5. H. H. Woodbery and G. W. Ludwig, "Electron Spin Resonance studies in SiC", Phys. Rev. **124**, 1083–1089 (1961).
6. I. Ikeda, H. Matsunami, and T. Tanaka, "Site effect on the impurity levels in 4H, 6H, 15R SiC", Phys. Rev. B **22**, 2842–2854 (1980).
7. M. V. Alekseenko, A. G. Zabrodskii, and M. P. Timofeev, "Thermal ionization of nitrogen non equivalent states in 6H-SiC", Sov. Tech. Phys. Lett. **11**, 422–427 (1985).
8. E. N. Kolabukhova, S. N. Lukin, "ESR Spectrum of Nitrogen in 6H SiC in the ground and Exited States", Mat.Science Forum., **338–342**, 791–794 (2000).
9. W. Sutrop, G. Pensl, W. J. Choyke, R. Steine, and S. Leibenzeder, "Hall effect and infrared absorption measurements on nitrogen donors in 6H-silicon carbide", J. Appl. Phys. **72**, 3708–3713 (1992).
10. W. Gotz, A. Schoner, G. Pensl, W. Sutrop, W. J. Choyke, R. Steine, and S. Leibenzeder, "Nitrogen donors in 4H-silicon carbide", J. Appl. Phys. **73**, 3332–3338 (1993).
11. C. Q. Chen, J. Zeman, F. Engelbrecht, C. Peppermuller, R. Helbig, Z. H. Chen, G. Martinez, "Photothermal ionization spectroscopy of shallow nitrogen donor states in 4H-SiC" J.Appl.Phys., **87**, 3800–3805 (2000).
12. Th. Troffer, W. Gotz, A. Schoner, G. Pensl, R. P. Devaty, and W. J. Choyke, "Hall effect and infrared absorption measurements on nitrogen donors in 15 R", Inst. Phys. Conf. Ser. **137**, 173–176 (1994).
13. A. E. Nikolaev, I. P. Nikitina, and V. A. Dmitriev, "Highly nitrogen doped 3C-SiC grown by liquid phase epitaxy" Inst. Phys. Conf. Ser.**142**, 125–128 (1996).
14. V. S. Vainer, V. A. Il'in, V. A. Karachinov and Y. M. Tairov, "EPR of the impurity pairs (TiN)<sup>0</sup> in silicon carbide, polytype 6H", Sov. Phys. Solid State **28**, 201–204 (1986).
15. Yu. A. Vodakov, E. N. Kalabukhova, S. N. Lukin, A. A. Lepneva, E. N. Mokhov, and V. D. Shanina, "Berillium as donor impurity in Silicon Carbide", Sov. Phys.Solid State **20**, 258–263 (1978).
16. P. J. Dean and R. L. Hartman, "Magneto-Optical Properties of the Dominate Bound Exiton in undoped 6H-SiC", Phys. Rev. B **5**, 4911–4924 (1972).
17. A. O. Euwarage, S. R. Smith, and W. C. Mitchel, "Shallow and deep levels in n-type 4H-SiC" J. Appl. Phys. **79**, 7726–7730 (1996).
18. Van H. Daal, W. F. Knippenberg, and J. D. Wassher, "On the electronic conduction of a-SiC crystals between 300 and 1500 K", J. Phys. Chem.Solids **24**, 109–127 (1963).
19. G. A. Lamakina, Yu. A Vodakov, E. N. Mokhov, V. G. Oding and G. F. Kholuyanov, "Compared investigation of the electrical properties of the three silicon carbide polytypes", Sov. Phys. Solid Stale **12**, 2356–2360 (1970).
20. I. V. Kodrau and V. V. Makarov, "Investigation of the blue electroluminescence of the silicon carbide doped by aluminum and boron by ion implantation", Sov. Phys. Semicond. **11**, 809–811 (1977).
21. E. N. Mokhov, M. M. Usmanov, G. F. Yuldashev, and B. S. Makhmudov, "Doping of the silicon carbide by group III A elements during growth of the crystal from vapor phase", Izv. AN SSSR. Neorg. mater. **20**, 1383–1386 (1984).
22. A. Schoner, N. Nordell, K. Rottner, R. Helbig, G. Pensl, "Dependence of the aluminum ionization energy on doping concentration and compensation in 6H SiC", Inst. Phys. Conf.Ser. **142**, 493–496 (1996).
23. B. I. Shklovskii and A. L. Efros, Sov. Phys. Semicond. (Structure of the impurity zon in low doped semiconductors (A rewiev )", **14**, 351–383 (1980).
24. M. M. Anikin, N. I. Kuznetsov, A. A. Lebedev, N. S. Savkina, A. L.Syrkin, and V. E. Chelnokov, "Current spectroscopy of the deep centers in 6H-SiC pn structures with build in electric field", Semiconductors **28**, 278–281 (1994).

25. P. A. Ivanov, Ya. V. Morozenko, and A. V. Suvorov, "Investigation of the deep centers in ion implanted 6H-SiC pn junctions" Sov. Phys. Semicond. **19**, 879–881 (1985).
26. N. I. Kuznetsov and A. S. Zubrilov, "Deep centers and electroluminescence in 4H-SiC diodes with p-type base region", Mater. Sci. Eng., B **29**, 181–184 (1995).
27. H. Matsuura, K. Aso, S. Kagaminara, H. Iwata, T. Ishida, K. Nishikawa "Decrease in Al acceptor density in Al-doped 4H-SiC by irradiation with 4,6 MeV electrons" Appl.Phys.Lett. **83**, 4981–4983 (2003).
28. M. M. Anikin, A. A. Lebedev, I. V. Popov , V. E. Sevast'yanov, A. L. Syrkin, A. L. Suvorov, V. E. Chelnokov "Rectified diode based on silicon carbide", Sov.Tech.Phys.Lett., **10**, 444–445 (1984).
29. E. Kalinina, G. Kholujanov, V. Soloviev, A. Strel'chuk, A. Zubrilov, V. Kossov, R. Yafaev, A. P. Kovarski, A. Hallen, A. Konstantinov, S. Karlsson, C. Adas, S. Rendakova, V. Dmitriev., "High-doze Al – implanted 4H-SiC p+-n-n+ junctions",Appl.Phys.Lett., **77**, 3051–3053 (2000).
30. V. Heera, J. Pezold, X. Ning, and P. Pirouz," High dose co-implantation of aluminium and nitrogen in 6H –silicon carbide", Inst. Phys. Conf. Ser. **142**, 509–512 (1996).
31. L. L. Clemen, R. P. Devaty, W. J. Choyke, J. A. Powel, D. J. Larkin, J. A. Edmond, and A. A. Burk, "Recent developments in the characterization of the aluminum center in 3C, 4H, and 15R SiC", Inst Phys. Conf. Ser. **137**, 297–300 (1994).
32. Yu. A. Vodakov, G. A. Lomakina, and E. N. Mokhov, " Non-stekhiomrtry and polytypizm of the silicon carbide", Sov. Phys. Solid State **24**, 780–786 (1982).
33. A. N. Andreev, M. M. Anikin, A. A. Lebedev, N. K. Poletaev, A. M. Strel'chuk, A. L. Syrkin, and V. E. Chelnokov, " A relationship between defect electroluminescence and deep centers in 6H-SiC", Inst. Phys. Conf. Ser.**137**, 271–274 (1994).
34. A. I. Veinger, Yu. A. Vodakov, Yu. Kulev, G. A. Lomakina, E. N. Mokhov, V. G. Oding, and V. I. Sokolov, " Impurity position of the boron in silicon carbide", Sov. Tech. Phys. Lett. **6**, 566–570 (1980).
35. V. S. Balandovich and E. N. Mokhov, "Two deep boron levels in silicon carbide: dependence on growth conditions and nitrogen concentration", *Transactions Second Int. High Temp. Electron. Conf.* (Charlotte NC, 5–10 USA, 1994) v. **2**, p. 181–186.
36. E. E. Violin and G. F. Kholuyanov," Extraction of the charge carriers by electric field and mechanism of the electroluminescence in silicon carbide", Sov.Phys. Solid State **8**, 2716–2718 (1966).
37. S. Ortolland, C. Raynaud, J. P. Chante, M. L. Locatelli, A. N. Andreev, A. A. Lebedev, M. G. Rastegaeva, A. L. Syrkin, N. S. Savkina, and V. E.Chelnokov, "Effect of boron diffusion on high-voltage behavior of 6H-SiC p+nn+ structures", J. Appl. Phys. **80**, 5464–5468 (1996).
38. G.J.Phelps, N.G.Wrigth, E.G.Chester, C.M.Jonson, A.G.O'Neill, S.Ortolland, A.Horsfall, K.V.vassilevski, R.M.Gwilliam, P.G.Coleman and C.P.Burrows "Enhanced nitrogen diffusion in 4H-SiC" Appl.Phys.Lett. **80**, 228–230 (2002).
39. M. M. Anikin, A. A. Lebedev, A. L. Syrkin, and A. V. Suvorov, " Investigation of deep levels in SiC by capacitance spectroscopy methods", Sov. Phys. Semicond. **15**, 69–71 (1985).
40. Y.Gao, S.I.Soloviev and T.S.Sudarshan, "Investigation of boron diffusion in 6H-SiC" Appl.Phys.Lett. **83** 905–907 (2003).
41. M. M. Anikin, A. A. Lebedev, N. K. Poletaev, A. M. Strel'chuk, A. L. Syrkin, and V. E. Chelnokov, " Deep centers and blue-green electroluminescence in 4H-SiC" Inst. Phys. Conf. Ser. **137**, Chap. 6, 605–607, (1994).
42. A. A. Lebedev and N. K. Poletaev, "Deep centers and electroluminescence of the boron doped 4H-SiC p-n structures", Semiconductors **30**, 238–241 (1996).
43. A. O. Konstantinov, " About nature of the point defects, arising during diffusion of the acceptor impurity in silicon carbide", Sov.Phys. Semicond. **26**, 151–158 (1992).

44. M. S. Janson, M. K. Linnarson, A. Hallen, B. G. Svensson, N. Nordel and H. Bleichner, "Transient enhanced diffusion of implanted boron in 4H-silicon carbide", *Appl.Phys.Lett.* **76**, 1434–1436 (2000).
45. M. Laube, G. Pensl and H. Itoh, "Suppressed diffusion of implanted boron in 4H-SiC", *Appl.Phys.Lett.* **74**, 2292–2294 (1999).
46. H. Bracht, N. A. Stolwijk, M. Laube, G. Pensl, "Diffusion of boron in silicon carbide: Evidence for the kick-out mechanism" *Appl.Phys.Lett.* **77**, 3188–3190 (2000).
47. P. G. Baranov and E. N. Mokhov, "Electron paramagnetic resonance of deep boron in SiC", *Inst. Phys. Conf. Ser.* **142**, 293–296 (1996).
48. T. Frank, T. Troffer, G. Pensl, N. Nordell, S. Karlsson, and A. Schoner, "Incorporation of the D-centre in SiC Controlled either by Co- implantation of Si/B and C/B or by Site-Competition Epitaxy" *Material Science Forum* **264–268**, 681–684 (1998).
49. Yu. A. Vodakov, G. A. Lomakina, E. N. Mokhov, M. G. Rainm, and V. I. Sokolov, "Influence of the growth conditions on thermal stability of the defect electroluminescence with D1 spectrum in neutron irradiated 6H-SiC", *Sov. Phys.Semicond.* **20**, 1347–1352 (1986).
50. A. van Duijn-Arnold, J. Moi, R. Verberk, J. Schmidt, E. N. Mokhov, and P. G. Baranov, "Spatial distribution of the electronic wave function of the shallow boron acceptor in 4H- and 6H-SiC", *Phys.Rew. B.*, **60**, 15829–15847 (1999).
51. S. Jang, T. Kimoto, and H. Matsunami, "Deep levels in 6H-SiC wafers and step-controlled epitaxial layers", *Appl. Phys. Lett.* **65**, 581–583 (1994).
52. M. S. Mazzola, S. E. Sadow, P. G. Neudeck, V. K. Lakdawala, and S. We," Observation of the D-centre in 6H-SiC pn diodes grown by chemical vapor deposition" *Appl. Phys. Lett.* **64**, 2730–2733(1994).
53. Yu. A. Vodakov, G. A. Lomakina. E. N. Mokhov, E. I. Radovanova, V. I. Sokolov, M. M. Usmanova, G. F. Yuldashev, and B. S. Makhmudov, "Silicon Carbide Doped with Gallium", *Phys. Status Solidi A* **35**, 37–42 (1976).
54. T. Troffer, G. Pensl, A. Schoner, A. Henry, C. Hallin, O. Kordina, and E. Janzen, "Electrical Characterization of the Gallium Acceptor in 4H- and 6H-SiC" *Material Science Forum* **264–268**, 557–560 (1998).
55. M. Gong, S. Fung, C. D. Beling, G. Braner, H. Wirth, W. Skorupa "Gallium implantation induced deep levels in n-type 6H-SiC", *J.Appl.Phys.* **85**, 105–107 (1999).
56. A. Henry, C. Hallin, I. G. Ivanov, J. P. Beigman, O. Kordina, and E. Janzen, "Ga bound excitons in 3C, 4H and 6H-SiC Inst. Phys. Conf. Ser. **142**, 381–384 (1996).
57. Yu.A.Vodakov, G.A.Lomakina, E.N.Mokhov, V.G.Oding, "Berillium as a donor impurity in silicon carbide", *Sov.Phys.Sol.State* **20**, 258–261 (1978).
58. Yu. A. Vodakov, G. A. Lomakina, E. N. Mokhov, and V. G. Oding, " EPR in 2-mm diapason and optical adsorption of the intrinsic defect in epitaxial layers of 4H SiC", *Sov. Phys. Solid State* **33**, 1869–1873 (1991).
59. E. V. Violin, A. A. Kal'nin, V. V. Pasynkov, Yu. M. Tairov, and D. A.Yas'kov, "Luminescence of silicon carbide with different impurities", *Mater. Res. Bull.* **4**, S231-S241 (1969).
60. Y. Zheng, N. Ramungul, R. Patel, V. Khemka, and T. P. Chow, "Beryllium-Implanted 6H-SiC P+N Junctions", *Material Science Forum* **264–268**, 1049–1052 (1998).
61. X.D.Chen, S.Feng, C.D.Beling, M.Gong, T.Henkel, H.Tanoue, and N.Kobayashi, "A deep level transient spectroscopy study of beryllium implanted n-type 6H-SIC" *J.Appl.Phys.* **88**, 4558–4562 (2000).
62. X.D.Chen, C.C.Ling, S.Fung, C.D. Beling, M.Gong, T.Henkel, H.Tanoue and N.Kobayashi "Beryllium implantation induced deep level defects in p-type 6H-silicon carbide" *J. Appl.Phys* **93**, 3117–3119 (2003).

63. P. G. Baranov , "Radio-spectroscopy of wide band gap semiconductors: SiC and GaN", Phys. Solid State **41**, 798 (1999).
64. M. B. Scott, J. D. Scofield, Y. K. Yeo, and R. L. Hengehold " Deep Level defect Study of Ion Implanted (Ar,Mg,Cr) n-Type 6H-SiC by Deep Level Transient Spectroscopy" Material Science Forum **264–268**, 549–552 (1998).
65. V. S. Ballandovich, "Scandium acceptor in 6H SiC", Semiconductors, **25**, 152–157 (1991)
66. H. Vakhner and Yu. M. Tairov, "Luminescence of the silicon carbide, doped by scandium", Sov.Phys. Solid State **11**, 1972–1975 (1969).
67. D. P. Litvin, A. A. Mal'tsev, A. V. Naumov, A. D. Roenkov, and V. I.Sankin, " P+  $\pi$ -N+ structures with double injection based on silicon carbide", Sov. Tech. Phys. Lett. **13**, 523–526 (1987).
68. S.Greulich-Weber, M.Masz, J.-M. Spaeth, E.N.Mokhov, and E.N.Kolabukhova, Mat.Science Forum V 338–342 (2000) 809.
69. A. W. C. Kemenade and S. H. Hagen, "Proof of the involvement of Ti in the Low-temperature ABC Luminescence spectrum of 6H SiC" ,Solid State Common. **14**, 1331–1333 (1974).
70. K. M. Lee, Le. Si. Dang, G. B. Watkins, and W. J. Choyke, "Optically detected magnetic resonance study of SiC:Ti", Phys. Rev. **B32**, 2273–2284 (1985).
71. K. Maier, H. D. Muller, and J. Schneider, "Transition Metals in Silicon Carbide (SiC): Vanadium and Titanium", Mater. Sci. Forum **83–87**, 1183–1194 (1992).
72. K. Maier, J. Schneider, W. Wilkening, S. Leibenzeder, and R. Steine, "Electron spin resonance studies of transition metal deep level impurities in SiC", Mater. Sc. Eng., B **11**, 27–30 (1992).
73. T. Dalibor, G. Pensl, H. Matsunami, T. Kimoto, W. J. Choyke, A. Schoner, and N. Nordel, "Deep defect Centers in Silicon Carbide Monitored with deep Level Transient Spectroscopy" Phys. Status Solidi A **162**, 199–232 (1997).
74. T. Dalibor, G. Pensl, N. Nordel, A. Schoner, and W. J. Choyke, "Ground States of the Ionized Iso-electronic Ti Acceptor in SiC", Material Science Forum **264–268**, 537–540 (1998).
75. N. Achtziger, W. Witthuhn, "Band gap states of Ti,V and Cr in 4H-SiC silicon carbide", Appl.Phys.Lett. **71**, 110–112 (1997).
76. N.Achtziger, W.Witthuhn, "Band-gap states of Ti,V and Cr in 4H-SiC: Identification and characterization by elemental transmission of radioactive isotopes", Phys.Rev **57**, 12181–12196 (1998).
77. J. M. Langer and H. Heinrich, "Deep-level impurities: A possible guide to prediction of band-edge discontinuities in semiconductor heterojunctions", Phys. Rev. Lett. **55**, 1414–1417 (1985).
78. H. Mc D. Hobgood, R. C. Glass, A. Augustine, R. H. Hopkins, J. Jenny, M. Skowronski, W. C. Mitchel, and M. Roth, "Semi-insulating 6H-SiC grown by physical vapor transport", Appl. Phys. Lett. **66**, 1364–1366 (1995).
79. W. C. Mitchel, M. D. Roth, A. O. Evvaraye, P. W. Yu, S. R. Smith, J. Jenny, M. Skowronski, H. McD. Hodgood, R. C. Glass, G. Augustine, and R. H. Hopkins, "Electronic properties of semi-insulating vanadium- doped 6H-SiC", Inst. Phys. Conf. Ser. **142**, 313–316 (1996).
80. K. F. Dombrovskii, U. Kaufman, M. Kunzer, K. Maier, J. Schneider, V. B. Shields and M. G. Spencer, "Deep donor state of vanadium in cubic silicon carbide (3C-SiC)", Appl. Phys. Lett. **65**, 1811–1813 (1994).
81. J. Schneider, H. D. Muller, K. Maier, W. Wilkening, F. Fuchs, A. Doroen, S. Leibenzader, and S. Steine, "Infrared spectra and electron spin resonance of vanadium deep level impurities in silicon carbide", Appl. Phys. Lett. **56**, 1184–1186 (1990).
82. N. Achtziger, J. Grillenberg, and W. Witthuhn, " Radiotracer Identification of Ti,V and Cr band gap States in 4H and 6H-SiC" Material Science Forum **264–268**, 541–544 (1998).

83. St G. Muller, D. Hofmann, A. Winnacker, E. N. Mokhov, and Yu. A. Vodakov, "Vanadium as a recombination centre in 6H SiC", Inst. Phys. Conf. Ser. **142**, 361–364 (1996).
84. B. S. Balandovich and G. N. Violina, "an investigation of radiation defects in silicon carbide irradiated with fast electrons" Cryst.Latt.def and Amorph.Mat. **V13**, 189–193 (1987)
85. A. O. Konstantinov and P. A. Ivanov, "Sublimation growth of silicon carbide in the growth system free of carbon materials", Inst.Phys.Conf. Ser **N137**, 37–40 (1994).
86. J. Grillenberg, N. Atchitziger, R. Sielemann, and W. Witthunh, "Radiotracer identification of a Ta-related deep level in 4H-SiC", J.Appl.Phys. **88**, 3260–3265 (2000).
87. N. Achitziger and W. Witthunh, "Deep levels of chromium in 4H-SiC", Mater. Sci. Eng., B **46**, 333–335 (1997).
88. N. Achitziger, J.Grillenberg, and W. Witthunh, "Band gap states of V and Cr in 6H – silicon carbide", Appl.Phys A **65**, 329–331 (1997).
89. N.T.Son, A.Ellison, B B.Magnusson, M.F.MacMillan, W.M.Chen, B.Monemar, E.Janzen "Photoluminescence and Zeeman effect in chromium doped 4H and 6H SiC", J.Appl.Phys, **86**, 4348–4353 (1999).
90. M. Kuznser, K. F. Dombrovski, F. Fuchs, U. Kaufmann, J. Schneider, P. G. Baranov, and E. N. Mokhov, "Identification of optically and electrically active molybdenum trace impurities in 6H-SiC substrate", Inst. Phys. Conf. Ser. **142**, 385–388 (1996).
91. M. Feege, S. Grenlich-Weber, and J.-M. Spaeth, "Observation of an interstitial manganese impurity in 6H-SiC", Semicond. Sd. Technol. **8**, 1620–1625 (1993).
92. J.Baur, M.Kunzer, and J.Schneider "Transition Metals in SiC Polytypes, as Studied by Magnetic Resonance Technique", Phys.Stat.Sol.(a) **162**, 153 (1997).
93. W.V.M. Machado, J.F.Justo, and L.V.C. Assali "3d-Transition Matalts in Cubic and Hexagonal Silicon Carbide" Mater. Science Forum **483–485**, 531 (2005).
94. J. Grillenberg, N. Atchitziger, F. Gunter and W. Witthunh, "Radiotracer investigation of deep Ga and Zn related band gap states in 6H-SiC", Appl.Phys.Lett. **73**, 3698–3699 (1998).
95. J. Grillenberg, N. Atchitziger, and W. Witthunh, "On the Existance of deep Levels of the Acceptors Ga and In and of the Potential Double Acceptors Zn and Cd in SiC", Mat.Science Forum **338–342**, 749–752 (2000).
96. N. Achitziger, J. Grillenberg, and W. Witthunh, "Radioatracer spectroscopy of deep levels in the semiconductor band gap", Hyperfine Interaction, **120/121**, 69–79, (1999).
97. K. Abe, T. Ohsima, H. Iton, Y. Aoki, M. Yoshikawa, I. Nashiyama, and M. Iwami," Hot Implantation of Phosphorus Ions into 6H-SiC" Material Science Forum **264–268**, 721–724 (1999).
98. M. A. Capano, J. A. Cooper, Jr, M. R. Melloch, A. Saxler, W. C. Mitchel, "Ionization energies and electron mobility's in phosphorus and nitrogen implanted 4H –silicon carbide", J.Appl.Phys. **87**, 8773 –8777 (2000).
99. E. M. Handy, M. V. Rao, O. W. Holland, K. A. Jones, M. A. Derenge, N. Papanicolaou, "Variable-dose ( $10^{17}$ – $10^{20}$  cm $^{-3}$ ) phosphorus ion implantation into 4H SiC", J.Appl.Phys. **88**, 5630–5634 (2000).
100. A. Uedono, S. Tanigawa, T. Ohshima, H. Itoh, M.Yoshikawa, I. Nashiyama, T. Frank, G. Pensl, R. Suzuki, T. Ohdaira and T. Mikado, "Crystallization of an amorphous layer in P+ implanted 6H-SiC studied by monoenergetic beams", J.Appl.Phys. **87**, 4119–4125.
101. S. Tamura, T. Kimoto, H. Matsunami, M. Okada, S. Kanazawa, I. Kimoto, "Nuclear Transmutation Doping of Phosphorus into 6H-SiC", Mat.Science.Forum **338–342**, 849–852 (2000).
102. H. Heissenstein, H. Sadowskii, Ch. Pepermuller and R. Helbig, "Radiation Defects and Doping of SiC with Phosphorus by nuclear Transmutation Doping (NTD)", Mat.Science. Forum **338–342**, 853–856 (2000).

103. S. G. Sridhara, L. L. Clemen, D. G. Nizhner, R. P. Devaty, W. J. Choyke, D. J. Larkin "Phosphorus Four Particle Donor Bound Exiton Complex in 6H SiC" Mat.Science.Forum **264–268**, 465–468 (1998).
104. N.T.Son, A.Henry, J.Isoya, and E.Janzen, "Electron Paramagnetic Resonance of Shallow Phosphorous Centers in 4H- and 6H-SiC", Mater. Science Forum **483–485**, 515 (2005).
105. G. P. Kholuyanov, Yu. A. Vodakov, and E. V. Violin,"Role of the oxygen in blue and "boron" luminescence of silicon carbide", Sov. Phys. Semicond. **5**, 141–143 (1971).
106. T. Dalibor, G. Pensl, T. Yamamoto, T. Kimoto, H. Matsunami, S. Sridhara, D. C. Nizher, R. P- Devaty, and W. J. Choyke, "Oxyde –Related Defect Centers in 4H Silicon carbide", Material Science Forum **264–268**, 553–556 (1998).
107. H. Ennen, J. Schnider, G. Ponrenke, and A. Axmann, "1,54  $\mu\text{m}$  luminescence of erbium – implanted III-V semiconductors and silicon", Appl. Phys. Lett. **43**, 943–946 (1983).
108. W. J. Choyke, R. P. Devaty, L. L. Clemen, M. Yoganathan, G. Pensl, and Ch. Hassler, " Intense erbium –1,54m photoluminescence from 2 to 525K in ion-implanted 4H, 6H,15R and 3C SiC", Appl. Phys. Lett. **5**, 1668–1670 (1994).
109. G.Pasold, f.Albrecht, J.Grillenberger, U.Grossner, C.Hulsen, W.Witthuhn and R.Sieleman "Erbium-related band gap states in 4H- and 6H-silicon carbide" J.Appl.Phys. **93**, 2289–2291 (2003).
110. M. M. Anikin, A. A. Lebedev, I V. Popov, A. L. Syrkin, A. V. Suvorov, and G. P. Shpynev, " Investigation of the Al and B levels in SiC diodes by capacitance spectroscopy method" in *Technology of Semiconductor Power Devices* [in Russian], Valgus, Tallin 19–24 (1987).
111. N. I. Kuznetsov, A. P. Dmitriev, and A. S. Fuman, "Properties of a center associated with an Al impurity in 6H-SiC", Semiconductors **28**, 584–586 (1994).
112. A. A. Lebedev, "Irradiation as a possible method for producing SiC heterostructures", Semiconductors, **33**, 1004–1006 (1999).
113. N. I. Kuznetsov and J. A. Edmond, deep level s influence on current relation in 6H-SiC diodes", Sov. Phys. Semicond. **31**, 1481–1485 (1997).
114. M. M. Anikin, A. A. Lebedev, A. A. Lebedev, A. L. Syrkin, and A. V. Suvorov, " Capacitance spectroscopy of pn junction made of epitaxial 4H-SiC, doped by implantation of Al ions", Sov. Phys. Semicond. **20**, 1357–1359 (1986).
115. M. M. Anikin, A. A. Lebedev, I. V. Popov, A. M. Strel'chuk, A. L. Syrkin, A. V. Suvorov, and V. E. Chelnokov, " Structure with an ion-implanted pn junction in epitaxial 4H-SiC with an S-type current-voltage characteristic", Sov. Phys. Semicond. **20**, 1036 (1986).
116. K.Fujihira, T.Kimoto, and H.Matsunami, "High-purity and high quality 4H-SiC grown at high speed by chimney-type vertical hot-wall chemical vapor deposition" Appl.Phys.Lett. **80**, 1586 (2002).
117. D. V .Davydov, A. A .Lebedev, A. S. Tregubova, V. V. Kozlovskii, A. N. Kuznetsov, and E. V. Bogdanova " Investigation of 3C-SiC Epitaxial Layers Grown by Sublimation Etptaxy",Mater.Science Forum **338–342**, 221–224 (2000).
118. A. A. Lebedev, M. P. Scheglov, and T. V. Sokolova, " Is the green electroluminescence of pn structures in 6H SiC due to crystalline inclusion of the 3C polytype?", Tech. Phys. Lett. **21**, 654–655 (1995).
119. M. M. Anikin, N. I. Kuznetsov, A. A. Lebedev, N. K. Poletaev, A. M. Strel'chuk, A. L. Syrkin and V. E. Chelnokov, " Shift of the electroluminescence peak in 6H-SiC based diodes with the forward current density", Semiconductors **28**, 270–273 (1994).
120. J. P. Doyle, M. O. Adoelfotooh, B. G. Svensson, A. Schoner, and N. Nordel, "Characterization of electrically active deep level defects in 4H and 6H SiC", Diamond Relat. Mater. **6**, 1388–1391 (1997).

121. E. N. Kolabukova, S. N. Lukin, E. N. Mokhov, J. Reinke, S. Greulich-Weber, and J.-M. Spaeth, "New deep acceptor at  $E_v + 0.8$  eV in 6H silicon carbide", Inst. Phys. Conf. Ser. **142**, 333–335 (1996).
122. G. C. Rubicki, "Deep level defects in alpha particle irradiated 6H silicon carbide", J. Appl. Phys. **78**, 2996–3000 (1995).
123. M. M. Anikin, A. N. Andreev, A. A. Lebedev, S. N. Pyatko, M. G. Rasetsagaeva, N. S. Savkina, A. M. Strelchuk, A. L. Syrkin, and V. E. Chelnokov " High-temperature Au-SiC-6H Schottky diode", Sov. Phys. Semicond. **25**, 198–201 (1991).
124. M. M. Anikin, A. S. Zubrilov, A. A. Lebedev, A. M. Strel'chuk, and A. E. Cherenkov, "Recombination processes in 6H-SiC pn structures and the influence of deep centers", Sov. Phys. Semicond. **25**, 289–293 (1991).
125. C.G.Hemmigson, N.T.Son, O.Kordina and E.Janzen "Metastable defects in 6H-SiC: experiments and modeling" J.Appl.Phys **91**, 1324–1330 (2002).
126. H. Zhang, G. Pensl, A. Domer, and S. Leibenzeder, "Deep centers in n-type 6H-SiC", Ext. Abstr. Electrochem. Soc. Mtg., 699–700 (1989).
127. Y.nakakura, M.Kato, M.Ichimura, E.Arai, Y.Tokuda, and S,Nishino "Characterization of deep levels in 6H-SiC by optical-capacitance-transient spectroscopy", J. Appl.Phys. **94**, 3223 (2003).
128. C. G. Hemmingson, N. T. Son and E. Janzen, "Observation of negative – U centers in 6H silicon carbide", Appl.Phys.Lett. **74**, 839–841 (1999).
129. A. Kawasuso, F. Redmann, R. Krause-Rehberg, P. Sperr, Th. Frank, M. Weidner, G. Pensl and H. Itoh "Vacancies and deep levels in electron-irradiated 6H-SiC epilayers studied by positron annihilation and deep level transient spectroscopy" J.Appl.Phys, **90**, 3377–3382 (2001).
130. A. I. Vainer, V. A. Il'in, Yu. M. Tairov, and V. F. Tsvetkov, "Paramagnetic deep centers parameters investigation in 6H-SiC", Sov. Phys. Semicond. **15**, 902–906 (1981).
131. A. A. Lebedev, D. V. Davydov, N. S. Savkina, A. S. Tregubova, M. P. Scheglov, R. Yakimova, M. Suvajarvi and E.J anzen, "Structural Defects and Deep-Level Centers in 4H-SiC epilayers grown by sublimation epitaxy in vacuum" Semiconductors, **34**, 1183–1136 (2000).
132. T. Dalibor, G. Pensl, T. Kimoto, H. Matsunami, S. Shidhara, R. P. Devaty, and W. J. Choyke, " Radiation-induced defect centers in 4H silicon carbide", Diamond Relat. Mater. **6**, 1333–1337 (1997).
133. I.Pintilie, L.Pintilie, K.Irmscher and B.Thomas " Formation of the  $Z_{1,2}$  deep-level defects in 4H-SiC epitaxial layers: Evidence for nitrogen participation" Appl.Phys.Lett **81**, 4841–4843 (2002)
134. W. C. Mitchel, R. Perrin, J. Goldstein, A. Saxler, M. Roth, S. R. Smith, J. S. Solomon and A. O. Euwarage "Fermi level control and deep levels in semi-insulating 4H-SiC", J.Appl.Phys **86**, 5040–5044 (1999).
135. M.E.Zvanut and V.V.Konovalov "the level position of a deep intrinsic defects in 4H-SiC studied by photoinduced electron paramagnetic resonance " Appl. Phys.Lett. **80** 410–412 (2002)
136. P. Zhou, M. G. Spencer, G. L. Harris, and K. Fekade, "Observation of deep levels in cubic silicon carbide", Appl. Phys. Lett. **50**, 1384–1385 (1987).
137. K. Zankenes, M. Kayiambaki, and G. Constandnidis, "Electron traps in b-SiC grown by chemical vapor deposition on silicon (100) substrates", Appl. Phys. **66**, 3015–3017 (1995).
138. V. S. Balandovich and G. N. Violina, "An Investigation of radiation defects in silicon carbide irradiated with fast electrons", Cryst. Lattice Defects Amorphous Mater. **13**, 189–193 (1987).
139. A.Castaldini,A.Cavallini, L.Rigutti, and F.Nava "Low temperature annealing of electron irradiation induced defects in 4H-SiC" Appl.Phys.Lett. **85**, 3780 (2004).

140. L.Storasta, J.P.Bergman, E.Janzen, A.Henry, and J.Li "Deep levels created by low energy electron irradiated in 4H-SiC", *J.Appl.Phys.* **96**, 4909 (2004).
141. Z.Zolnai, N.T.Son, C.Hallin, and E.Janzen " Annealing behaviour of the carbon vacancy in electron-irradiated 4H-SiC", *J.Appl.Phys.* **96**, 2406 (2004).
142. M. Gong, S. Fung, C. D. Beiling, Zhipu You, "Electron – irradiation – induced deep levels in n-type 6H-SiC", *J.Appl.Phys* **85**, 7604–7608 (1999).
143. V. S. Ballandovich, " Relaxation spectroscopy of the irradiation induced defects in 6H-SiC", *Sov.Phys.Semicond.* **33**, 1188–1192 (1999).
144. M. Gong, S. Fung, C. D. Beiling, Zhipu You, " A deep level transient spectroscopy study of electron irradiation induced deep levels in p-type 6H-SiC", *J.Appl.Phys* **85**, 7120 –7122 (1999).
145. C. Hemmingson, N. T. Son, O. Kordina, E. Janzen, J. L. Lindstrom, S. Savarge, and N. Nordel, "Capacitance transient studies of electron irradiated 4H-SiC", *Mater. Sci. Eng. B* **46**, 336–339 (1997).
146. C. Hemmingson, N. T. Son, O. Kordina, E. Janzen, J. P. Bergman, J. L. Lindstrom, S. Savarge, and N. Nordel, "Deep level defects in electron-irradiated 4H SiC epitaxial layers", *J.Appl.Phys.* **81**, 6155–6159 (1997).
147. M.L.David, G.Alferi, E.M.Monakhov, A.Hallen, C.Blanchard, B.G.Svensson, J.F.Barbot "Electrically active defects in irradiated 4H-SiC" *J.Appl.Phys* **95** 4728–4733 (2004).
148. N.T.Son, B.Magnusson and E.Janzen "Photoexcitation-electron-paramagnetic-resonance studies of the carbon vacancy in 4H-SiC" *Appl.Phys.Lett.* **81** 3945–3947 (2002).
149. I. M. Pavlov, M. I. Iglytsin, M. G. Kosaganov, and V. N. Solomatin, "Centers with spin 1 in silicon carbide, irradiated by neutrons and a-participles", *Sov. Phys. Semicond.* **9**, 1320–1326 (1975).
150. A. I. Veinger, A. A. Lepeneva, G. A. Lomakina, E. N. Mokhov, and V. I.Sokolov, Sov., "Annealing of the radiation defects in n-SiC(6H), irradiated by neutrons", *Phys. Semicond.* **18**, 1932–1937 (1984).
151. V. V. Makarov, "Luminescence and optical properties of the neutron irradiated SiC", *Sov. Phys. Solid State* **13**. 1974–1979 (1971).
152. R. N. Kyutt, A. A. Lepeneva, G. A. Lomakina, E. N. Mokhov, A. S. Tregubova, M. P. Scheglov and G. F. Uldashev , "Formation of the defects during annealing of the neutron irradiated silicon carbide", *Sov.Phys. Solid State* **30**, 2606–2610 (1988).
153. A. A. Lepeneva, E. N. Mokhov, V. G. Odintsov and A. S. Tregubova, Silicon carbide, irradiated by high doses of neutrons", *Solid State Physics* **33**, 2217–2221 (1991).
154. X.D.Chen, S.Fung, C.C.Ling, C.D.Beling and M.Gong " Deep level transient spectroscopic study of neutron-irradiated n-type 6H-SiC" **94** 3004–3010, (2003).
155. M. Okada, T. Kimura, T. Nakata, M. Watanbe, S. Kanazawa, I. Kanno, K. Kamitani, K. Atobe, and M. N. Nakagawa, "Radiation-induced defects in neutron-irradiated 4H- and 6H-SiC single crystals", *Inst. Phys. Conf. Ser.* **142**,469–472 (1996).
156. H. Matsunami and T. Kimoto, "Step controlled epitaxial growth of SiC: high quality homoepitaxy", *Mater. Sci. Eng., R.* **20**, 125–166 (1997).
157. V.Nagesh,J.W.Farmer,R,F,Davis and H,S,Kong, "Defects in neutron irradiated SiC", *Appl.Phys.Lett.* **50**, 1138–1140 (1987).
158. Th.Lingner, S.Greulich-Weber, J.-M. Spaeth, U.Gerstmann, E.Rauls, Z.Hajnal, Th.Frauenheim, and H.Overhof, "Structure of silicon vacancy in 6H-SiC after annealing identified as the carbon vacancy-carbon antisite pair", *Phys.Rev. B* **64**, 245212 (2001).
159. I.V.Ilyin, M.V.Muzafarova, E.N.Mokhov, S.G.Konnikov and P.G.Baranov, "Multi-defect Clusters in Neutron Irradiated Silicon Carbide: Electron Paramagnetic Resonance Study" *Mater. Science Forum* **483–485**, 489 (2005).

160. H. J. von Bardeleben, J. L. Cantin, I. Vickridge and G. Battistini, "Proton-implantation defects in n-type 6H- and 4H-SiC: An electron paramagnetic resonance study". Phys.Rev. **62** 10126–10134 (2000).
161. A.Gali, P.Deak, N.T.Son and E.Janzen "Hydrogen passivation of nitrogen in SiC" Appl.Phys.Lett. **83** 1385–1387 (2003).
162. Ya.Koshka "Optically induced formation of the hydrogen complex responsible for  $4B_0$  luminescence in 4H-SiC" Appl.Phys Lett. **82** 3260–3262 (2003).
163. P.A. Ivanov, O.I. Kon'kov, V.N.Panteleev, T.P.Samsonova, "Influence of the plasma treatment of silicon carbide surface on characteristics of field effect transistors with latent gate", Sov.Phys.Semicond. **31**, 1404–1407 (1997).
164. N. Atchtziger, J. Grillenberger, W. Witthuhn, M. K. Linnarsson, J. Janson, B. G. Svensson "Hydrogen passivation of silicon carbide by low-energy ion implantation", Appl.Phys.Lett. **73**, 945–947 (1998).
165. R. K. Nadela and M. A. Capano, "High resistance layers in n-type 4H silicon carbide by hydrogen ion implantation", Appl.Phys.Lett. **70**, 886–888 (1996).
166. E.V.Bogdanova, V.V.Kozlovski, D.S.Rumyantsev, A.A.Volkova, A.A.Lebedev "Modification of the Silicon Carbide by proton irradiation" Material science forum **457–460** 817–820 (2004).
167. A. A. Lebedev, D. V. Davydov, A. M. Strel'chuk, V. V. Kozlovskii, A. N. Kuznetsov, and E. V. Bogdanova, "Deep centers appearing in 6H and 4H SiC after proton irradiation", Mat.Science **338–342**, 973–976 (2000).
168. A. A. Lebedev, A. I. Veinger, D. V. Davydov, A. M. Strel'chuk, V. V. Kozlovskii, N. S. Savkina "Doping of n-type 6H-SiC and 4H-SiC with defects created with a proton beam", J.Appl.Phys. **88**, 6265–6271 (2000).
169. V. V. Makarov and N. N. Petrov, "Influence of the ion bombarding on cathodoluminescence of Silicon Carbide", Sov.Phys. Solid State **8**, 1272–1276 (1966).
170. V. V. Makarov, "Cathodoluminescence of different modification of the SiC crystals, containing radiation defects", Sov. Phys. Solid State **9**, 457–461(1967).
171. N. V. Kodrau and V. V. Makarov, "Luminescence spectrum of defects in ion implanted SiC", Sov. Phys. Semicond. **15**, 813–815 (1981).
172. L. Patrick and W. J. Choyke, "Photoluminescence of Radiation Defects in Ion-Implanted 6H-SiC" Phys. Rev. B **5**, 3253–3259 (1972).
173. V. V. Makarov and N. N. Petrov, "Cathodoluminescence of the silicon carbide mono crystals, irradiated by fast electrons", Sov.Phys.-Solid State **8**, 2714–2715 (1966).
174. V. M. Gusev, K. D. Demakov, V. M. Efimov, V. I. Ionov, M. G. Kosagonova, N. K. Prokofeva, V. G. Stolyarova, and Yu. N. Chekushkin, "electro-luminescence properties of several SiC polytypes, ion doped by Al", Sov. Phys. Semicond. **15**, 1413–1416 (1981).
175. K. D. Demakov, V. S.Ivanov, V. G. Stolyarova, and V. M. Tarasov, "Transition electroluminescence characteristics of the lights emitted diodes, formed on a-SiC by ion implantation of  $Al^+$  ions", Sov. Phys. Semicond. **12**, 644–647 (1978).
176. Yu. A. Vodakov, G. A. Lomakina, E. N. Mokhov, M. G. Ramm, and V. I. Sokolov, "Influence of the growth condition on thermal stability of the defect electroluminescence with D1 spectrum in 6H SiC irradiated by neutrons", Sov. Phys.Semicond. **20**, 1347–1351 (1986).
177. Yu. M. Suleimanov, A. M. Grekhov, and V. M. Grekhov, "Electron- oscillation structure of the D1 spectrum in irradiated silicon carbide", Sov. Phys. Solid State **25**, 1060–1063 (1983).
178. Yu. A. Vodakov, A. I. Girka, A. O. Konstantinov, E. N. Mokhov, A. D.Roenkov, S. V. Svirida, V. V. Semenov, V. I. Sokolov, and A. V. Shishkin, "Ligh emitting diodes based on silicon carbide, irradiated by fast electrons", Semiconductors **26**, 1041–1044(1992).
179. W. J. Choyke, "Optical and electronic properties of SiC", in *NATO ASI Ser. Physics and Chemistry of Carbides, Nitrides and Borides*, ed by R. Freer (Manchester, 1989).

180. A. N. Andreev, M. M. Anikin, A. A. Lebedev, N. K. Poletaev, A. M. Strel'chuk, A. L. Syrkin, and V. E. Chelnokov, "Relationship between "defect" luminescence in 6H SiC and deep-level centres", *Semiconductors* **28**, 430–435 (1994).
181. A. I. Veinger, V. A. Il'in, Yu. M. Tairov and V. F. Tsvetkov, "Investigation parameters of the paramagnetic deep centers of the vacancies nature in 6H SiC", Sov.Phys.Semicond. **15**, 902–908 (1981).
182. Yu. A. Vodakov, G. A. Lomakina, and E. N. Mokhov, "Non-stekhiometry and polytypism of silicon carbide", Sov. Phys. Solid State **24**, 780–796 (1982).
183. Yu. Vakhner and Yu. M. Tairov, "About polytypism of SiC, growing from liquid phase" Sov.Phys. Solid State **12**, 1213–1214 (1970).
184. Yu. A. Vodakov, E. N. Mokhov, A. D. Roenkov, and M. M. Anikin, "Impurity influence on silicon carbide polytypism", Sov. Tech. Phys. Lett. **5**, 147–149(1979).
185. A. A. Maltsev, A. Yu. Maksimov, and N. K. Yushin, "4H-SiC single crystal ingots grown on 6H-SiC and 15R-SiC seeds", Inst. Phys. Conf. Ser. **142**, 41–44 (1996).
186. A. A. Maltsev, D. P. Litvin, M. P. Scheglov, and I. P. Nikitina, "High- resistively epitaxial films of 4H-SiC doped by scandium" Inst. Phys.Conf. Ser. **142**, 137–140 (1996).
187. P. A. Ivanov, A. A. Maltsev, V. N. Pantaleev, T. P. Samsonova, A. Yu. Maksimov, N. K. Yushin, and V. E. Chelnokov, "4H-SiC field-effect transistor hetero- epitaxially grown on 6H-SiC substrate by sublimation", Inst. Phys. Conf. Ser. **142**, 757–760 (1996).
188. Yu. A. Vodakov, G. A. Lomakina, E. N. Mokhov, and V. G. Oding, "Influence of the polytype structure on impurity diffusion in SiC", Sov. Phys. Solid State **18**, 1695–1698 (1977).
189. A. N. Andreev, A. S. Tregubova, M. P. Scheglov, A. L. Syrkin, and V. E. Chelnokov, "Influence of growth conditions on the structural perfection of b-SiC epitaxial layers fabricated on 6H-SiC substrates by vacuum sublimation", Mater. Sci. Eng., B **46**, 141–146 (1997).
190. A. M. Strel'chuk, N. S. Savkina. A. N. Kuznetsov, A. A. Lebedev, "Investigation characteristics of pn structures grown by sublimation heteroepitaxy of 3C-SiC on 6H-SiC" Abstr. ECSRM-2000 (Germany, Sept 3–7 2000, Kloster Banz). 200 (2000)
191. A. A. Lebedev and N.A.Sobolev "Capacitance spectroscopy of deep centers in SiC" Material Science Forum **258–263**, 715–720 (1997).
192. Yu. A. Vodakov and E. N. Mokhov, "Point defects in silicon carbide", Inst. Phys. Conf. Ser. **137**, 197–206(1994).
193. N. D. Sorokin, Yu. M. Tairov, V. F. Tsvetkov, and M. A. Chernov, "Investigation of the crystal-chemical properties of the silicon carbide polytypes", Kristallografiya **28**, 910–914 (1983).
194. G. Zeinther and D. Theeis, "A new degradation phenomena in blue light emitting silicon carbide diodes", IEEE Trans. Electron Devices **ED-28**, 425–427(1981) .
195. D. J. Larkin, P. G. Neudeck, J. A. Powell, and L. G. Matus, "Site-competition epitaxy for superior silicon carbide electronics", Appl. Phys.Lett. **65**, 1659–1661 (1994).
196. E. Janzen and O. Kordina, "Recent progress in epitaxial growth of SiC for power device application", Inst. Phys. Conf. Ser. **142**, 653–658 (1996).
197. A. N. Andreev, N. Yu. Smirnova, M. P. Scheglov, M. G. Rastegaeva, V. P. Restagaev, and V. E. Chelnokov, The influence of vapor phase composition in a growth cell on the doping level of silicon carbide epitaxial layers grown by vacuum sublimation", Semiconductors **30**, 1074–1082 (1996).
198. A.A.Lebedev " Deep level centers in silicon carbide: A review" Semiconductors **33**, 107–130 (1999).
199. H. Matsunami, M. Ikeda, and T. Tanaka, " Proton assisted tunneling in SiC LED's, prepared by overcompensation method", Jpn. J. Appl. Phys. **19**, 1323–1328 (1980).

200. M. M. Anikin, A. A. Lebedev, N. K. Poletaev, A; M. Strel'chuk, A. L.Syrkin, and V. E. Chelnokov, " Deep centers and blue-green electroluminescence of 4H-SiC", Semiconductors **28**, 288–291 (1994).
201. A. A. Lebedev, N. K. Poletaev, M. G. Rastegaeva, and N.S.Savkina, "Electroluminescence of aluminum-doped 6H-SiC p-n structures", Semiconductors **28**, 981–984 (1994).
202. A. A. Lebedev and M. C. do Carmo, "6H-SiC P-N structures with predominate exciton electroluminescence, obtained by sublimation epitaxy", Mater. Sci. Eng, B **46**, 275–277 (1997).
203. A. V. Naumov and V. I. Sankin, "Lifetime of the non-equilibrium holes in diodes, based on SiC", Sov. Phys. Semiconductors **23**, 630–634 (1989).
204. V. I. Sankin, R. G. Verenchikova, Yu. A. Vodakov, M. G. Ramm, and A. D. Roenkov, "Diffusion length of minority charge carriers in 6H and 4H", Sov. Phys.Semicond. **16**, 839–841 (1983).
205. V. S. Balandovich and G. N. Violina , "Photocapacitance effect in silicon carbide, doped by boron", Sov. Phys. Semicond. **15**, 959–961 (1981).
206. M. M. Anikin, A. A. Lebedev, S. N. Pyatko, V. A. Soloviev, and A. M. Strel'chuk, "Minority Carrier Diffusion Length in epitaxially grown SiC(6H) pn diodes" Springer Proc. Phys. **56**, 269–273 (1992).
207. A. M. Strel'chuk, "Lifetime and diffusion length of non-equilibrium carriers in SiC p-n structures", Sov. Phys.Semicond. **29**, 850–864 (1995).
208. A. M. Strel'chuk and V. V. Evstropov, "Dominant recombination centre in 6H SiC", Inst. Phys. Conf. Ser. **155**, 1009–1012 (1997).
209. O. Kordina, J. P. Bergman, A. Henry, and E. Janzen, "Long minority carrier lifetime in 6H-SiC grown by chemical vapor deposition", Appl. Phys. Lett. **66**, 189–191 (1995).
210. J. P. Bergman, E. Janzen, S.G.Sridhara and W.J.Choyke, " Time resolved PL Study of Multi Bound Exitons in 3C SiC", Material Science Forum, **264–268**,485–488 (1998).
211. N. V. Daykonovala, P. A. Ivanov, V. A. Kozlov, M. E. Levinshtein, J. W. Palmor, S. L. Rumyantsev and R. Singh, "Steady-State and Transient Forward Current-Voltage Characteristics of 4H-Silicon Carbide 5,5 kV Diodes at High and Superhigh Current density", IEEE transaction on Electron Devioces **46**, 2188–2194.
212. P.A.Ivanov, M.E.Levinshtein, T.T.Mnatskanov, J.W.Palmour, and A.K.Agarwal " "Power bipolar devices, based on Silicon Carbide. A review",Semiconductors, **39**, 897 (2005).
213. B.R.Gossik, J.Appl.Phys, **27**, 905 (1956).
214. S.A.Reshanov and G.Pensl "Comparasion of Electrically and Optically Determined Minority carrier Lifetimes in 6H-SiC" Mater. Science Forum **483–485**, 417 (2005).
215. A. O. Konstantinov, D. P. Litvin, and V. I. Sankin, "Abrupt silicon carbide pn junctions with high structural perfection", Sov. Tech. Phys. Lett. **7**, 572–576 (1981).
216. Yu. A. Vodakov, A. O. Konstantinov, D. P. Litvin, and V. I. Sankin, "Avalanche ionization in silicon carbide pn junctions", Sov. Tech. Phys. Lett. **7**, 3-6(1981).
217. A. P. Dmitriev, A. O. Konstantinov, D. P. Litvin, and V. I. Sankin, "stroking ionization and super lattice in 6H SiC" Sov. Phys. Semicond. **17**, 1093–1098 (1983).
218. M. M. Anikin, S. M. Vainshtein, A. M. Strel'chuk, and A. L. Syrkin, "Negative Temperature coefficient of the avalanche breakdown in silicon carbide pn junctions ",Sov. Tech. Phys. Lett,**14**, 545–547 (1988).
219. M. M. Anikin, M. E. Levinshtein, I. V. Popov. V. P. Rastegaev, A. M. Strel'chuk, and A. L. Syrkin," Temperature dependence of the avalanche breakdown in silicon carbide pn junctions " Sov. Phys. Semicond. **22**, 995–999 (1988).
220. A. S. Kyuregyan and P. N. Shilygin," Temperature dependence of the avalanche breakdown of the pn junctions with deep levels" Sov. Phys. Semicond **23**, 729–734 (1989).

221. E. V. Astrova, V. M. Volle. V. B. Voronkov, V. A. Kozlov. and A.A.Lebedev, "Influence of the deep levels on diodes breakdown voltage" Sov. Phys. Semicond **20**, 1326–1329 (1986).
222. P. G. Neudeck and Ch. Fazi, "Positive temperature coefficient of breakdown voltage in 4H-SiC PN junction rectifiers", IEEE Electron Device Lett **18**, 96–98 (1997)
223. A. A. Lebedev, S. Ortoland, C Raynaud, M. L. Locatelli, D. Planson, and J. P. Chante, "Deep centers and negative temperature coefficient of the breakdown voltage of SiC p-n structures", Sov. Phys. Semicond. **31**, 735–737 (1997).
224. C.Banc, E.Bano, T.Ouisse, K.Vassilevski and K.Zekentes "Photon Emission Analysis of Defect-Free 4H-SiC pn Diodes in Avalanche Regime" Mater. Science Forum **389–393**, 1293 (2002).
225. R. M. Potter, "Photoluminescence and electroluminescence in alpha silicon carbide", Mater.Res.Bull.**4**, S223-S230 (1969).

**This page intentionally left blank**

## SILICON CARBIDE JUNCTION FIELD EFFECT TRANSISTORS

DIETRICH STEPHANI

*SiCED Electronics Development GmbH & Co. KG, a Siemens Company*  
Günther-Scharowsky-Str.1, D-91052 Erlangen,  
Tel. ++49 9131 731718 Fax ++49 9131 723046  
Email : [dietrich.stepani@siemens.com](mailto:dietrich.stepani@siemens.com)  
[www.siced.de](http://www.siced.de)

PETER FRIEDRICHHS

*SiCED Electronics Development GmbH & Co. KG, a Siemens Company*  
Günther-Scharowsky-Str.1, D-91052 Erlangen,  
Tel. ++49 9131 734894 Fax ++49 9131 723046  
Email : [peter.friedrichs@siemens.com](mailto:peter.friedrichs@siemens.com)  
[www.siced.de](http://www.siced.de)

The chapter will give an overview about the theory of JFETs with special attention to the wide band gap issues related to SiC. After a comprehensive discussion of relevant structures and topologies experimental results are presented and discussed. Especially vertical structures are in the focus of this chapter. Characteristic I-V data will be shown as well as application specific solutions regarding the temperature behavior or the ruggedness of the devices. The status of the JFETs technology will be judged and compared to alternative solutions like MOSFETs or lateral JFETs. Finally, an outlook will be given regarding targeted applications for SiC VJFETs and the resulting requirements as targets for future improvements.

*Keywords:* SiC, JFETs, vertical JFETs, avalanche

## 1. Introduction

### 1.1 Historical review

A solid state electronic device, similar to a Metal Semiconductor Field-Effect Transistor (MESFET) was for the first time described by Julius Edgar Lilienfeld<sup>1</sup> as early as in 1926 while ten years later the first Field-Effect Transistor (FET) with an insulating gate (MISFET) was described by Oskar Heil<sup>2</sup> in 1936 – 12 years before the Transistor was announced.

The Junction (Gate) Field Effect Transistor (JFET, rarely named JUGFET) has been predicted by William Shockley<sup>3</sup> soon after the announcement of the point-contact Bipolar Junction Transistor (BJT) by J. Bardeen and W. Brattain<sup>4</sup>. The JFET possesses advantages over the bipolar junction transistor in so far as it does not require any input current to function as an electronically-controlled switch or as a voltage-controlled resistor, as long as we neglect any leakage currents, the current to charge the space charge regions, or prevent the JFET from a bipolar injection mode.

W. Shockley realized in his outstanding theoretical work, that the discovery of p-type and N-type semiconductors would make it possible to build a solid state analog of the vacuum tube triode by sandwiching a thin p-type semiconductor layer between two n-type pieces. This is schematically depicted in Fig.1, showing the two P-N junctions face to face, separated by the thin p-type layer. A current flowing through the p-type layer can be altered by the (common positive) potentials of the two n-type pieces with respect to the p-type semiconductor because of the voltage dependent space charge regions which limit the extension of the conducting channel. Therefore the JFET can be treated as a voltage controlled resistor (as long as the drain voltage is sufficiently small).

Based on Shockley's theoretical work, Dacey and Ross<sup>5</sup> reported the first working JFET. They also considered the effect of a field dependent mobility later<sup>6</sup>.

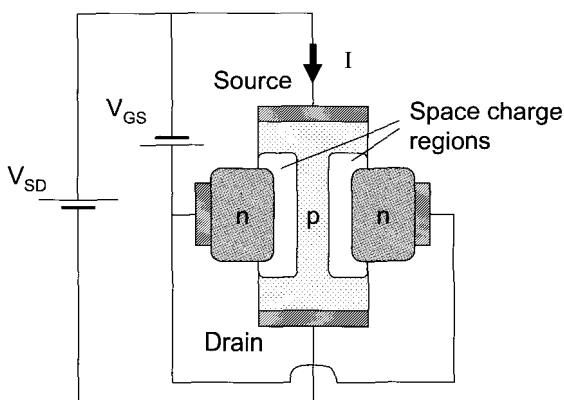


Fig. 1. Schematic representation of a P-channel JFET according to Shockley's fundamental theoretical work. The absence of a significant drain current is anticipated for the sketched space charge region . “The” semiconductor material at this time was Germanium.

Since the transconductance  $g_m$  and the channel conductance  $g_D$  of a JFET

$$g_m \equiv \frac{\partial I_D}{\partial V_G} \quad ; \quad g_D \equiv \frac{\partial I_D}{\partial V_D} \quad , \quad (1)$$

both depend linearly on the carrier mobility  $\mu^{7,8}$ , and in semiconductors electron mobility is in general significantly higher than hole mobility, the channel of a JFET is by far in most cases of the devices formed in N-type material. Silicon-based JFETs are still used typically in low-noise, low-signal level analogue applications, and as current limiters.

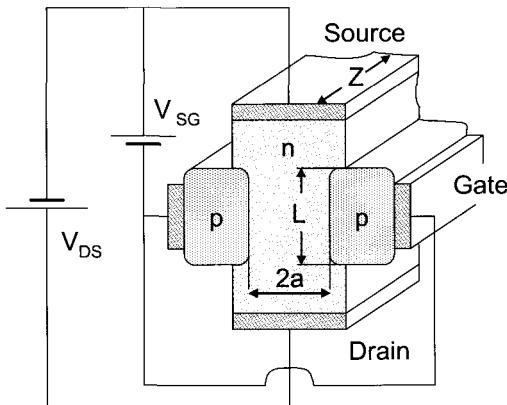


Fig. 2. N-channel JFET and geometrical definitions. Z denotes the gate width and L denotes the gate length, a equals the half channel width.

### 1.2 Some important basics of SiC-JFET semiconductor physics

With respect to Figure 2 we shall now, following Cze<sup>9</sup>, introduce some basic parameters of the channel region of a JFET. Neglecting at the moment any built in potential  $V_{bi}$  or space charge region due to the junction gate, the maximum conductance  $g_{max}$  of the channel for zero gate voltage and negligible drain voltage is simply derived by

$$g_{max} = \frac{Z}{L} \cdot q \cdot \mu \cdot N_D \cdot a \quad . \quad (2)$$

To deplete the channel a pinch off voltage  $V_p$  is required which is easily obtained from the depletion approximation by

$$V_p = \frac{q \cdot N_D \cdot a^2}{2 \cdot \epsilon} \quad , \quad (3)$$

and the pinch off current  $I_p$  (saturated drain current because of neglecting  $V_{bi}$ ) follows with Shockley's gradual channel approximation as

$$I_p = \frac{\mu \cdot q^2 \cdot N_D^2 \cdot a^3}{6 \cdot \epsilon} \cdot \frac{Z}{L} \quad (4)$$

Clearly it follows that the maximum conductance of the channel can't be higher than

$$g_{\max} = \frac{I_p}{3 \cdot V_p} \quad (5)$$

For any given pinch off voltage  $V_p$  we see that the maximum channel conductance is determined by (substituting the half channel height  $a$  by  $V_p$  in Eq. 2)

$$g_{\max} = \mu \cdot \sqrt{N_D} + \sqrt{2 \cdot \varepsilon \cdot q \cdot V_p} \cdot \frac{Z}{L} \quad , \quad (6)$$

and, with other words the maximum conductance of the channel scales linearly with the carrier mobility and with the square root of the channel doping density for a fixed pinch off voltage. The carrier mobility depends on doping density and temperature and decreases with increasing doping density and increasing temperature. However, the reduction of carrier mobility with growing channel doping density is weaker than the square root of doping density and therefore higher doping density of the channel leads to a higher channel conductance. An additional benefit of a higher channel doping density is a smaller channel height for a fixed pinch off voltage, which again allows to maintain the long channel condition ( $L/a \gg 1$ ) for a shorter gate length. Using an empirical expression for the relationship between electron mobility in 4H-SiC and doping density  $N_D$  given by Eq. (6) for room temperature<sup>10</sup> it can be shown that for a fixed pinch off voltage the channel conductivity increases with doping density within a wide range.

$$\mu(N_D) = \frac{900}{\left[ 1 + \left( \frac{N_D}{1.94 \cdot 10^{17}} \right)^{-0.61} \right]} \quad , \quad (7)$$

In Fig. 3 the half-channel height  $a$ , and the maximum conductance  $g_{\max}$  are displayed versus doping density for a pinch off voltage of 20V and  $Z/L = 1$ .

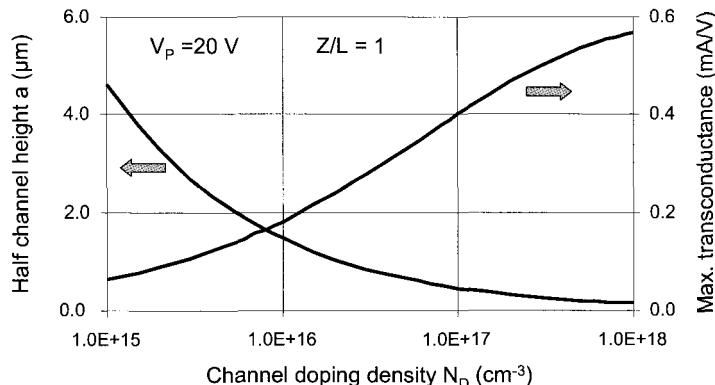


Fig. 3. Half-channel height  $a$ , and max. channel conductance  $g_{\max}$  versus doping density in the channel for a pinch off voltage of 20V and a ratio of gate width  $Z$  to gate length  $L$  of unity. Higher doping density results in higher channel conductivity.

Although the electron mobility in 4H-SiC is just moderately high, because of the about 10x higher breakdown electric field strength in 4H-SiC compared to silicon, the doping density can be almost a 100x higher than in silicon for a given blocking voltage. This makes SiC power JFETs very attractive because a high blocking voltage can be achieved with a low on-resistance.

### 1.2.1 Electron mobility in hexagonal SiC

4H-SiC is of hexagonal (Wurtzite) crystal symmetry and has three equivalent conduction band minima which are located at the M-point at very edge of the Brilloin zone in the k-space. Two principal axes of the ellipsoidal constant-energy surfaces are directed perpendicular to the c-axis giving rise to a transversal effective electron mass. The third axis of the ellipsoidal constant energy surfaces is directed parallel to the c-axis and in this direction we observe the longitudinal effective electron mass. The transversal relative effective electron mass  $m_{tr} \cong 0.42$  is slightly higher than the longitudinal relative effective electron mass<sup>11</sup>  $m_{lr} \cong 0.33$ . Therefore electron mobility in 4H-SiC is of anisotropic nature and highest in ⟨1000⟩ directions. For low-doped 4H-SiC the electron mobility perpendicular to the c-axis (transversal) reaches about 85% of the electron mobility parallel (longitudinal) to the c-axis<sup>12</sup>. This is in fortunate contrast to 6H-SiC, where the electron mobility is not only significantly lower but the anisotropy is also much more pronounced, as obvious from Table 1. Having both available, 4H-SiC and 6H-SiC, it does not make any sense to fabricate a JFET (or a MESFET) with 6H-SiC.

Table 1: Electron mobility in n-type low-doped ( $N_D \ll 10^{16} \text{ cm}^{-3}$ ) hexagonal SiC.

Modification	$\mu_l$ (parallel c-axis)	$\mu_t$ (perpendicular c-axis)
4H-SiC	$950 \text{ cm}^2/\text{Vs}$	$800 \text{ cm}^2/\text{Vs}$
6H-SiC	$100 \text{ cm}^2/\text{Vs}$	$400 \text{ cm}^2/\text{Vs}$

Electron mobility in 4H-SiC is affected by various scattering mechanism. Besides the well recognized ionized impurity scattering and acoustic phonon scattering mechanism, intervalley scattering and optical phonon scattering mechanism do also play a significant role<sup>13</sup>, leading to a rather complex behaviour of the electron mobility versus doping density and temperature. But, to make it as simple as possible, at low doping density ( $\sim 10^{15} \text{ cm}^{-3}$ ) there is a significant reduction in electron mobility with temperature which may be described for  $T > 300\text{K}$  by

$$\mu(T) \approx \mu(300K) \cdot \left( \frac{300K}{T} \right)^{\alpha} ; \quad \alpha \geq 2.8 \quad . \quad (8)$$

The higher the doping density, the less the electron mobility is influenced by temperature, leading to a situation, where the electron mobility is almost independent from doping density. However, because of the now enhanced ionized impurity scattering

the electron mobility is clearly reduced but less sensitive to temperature. A qualitative picture of this behaviour is shown in Fig. 4.

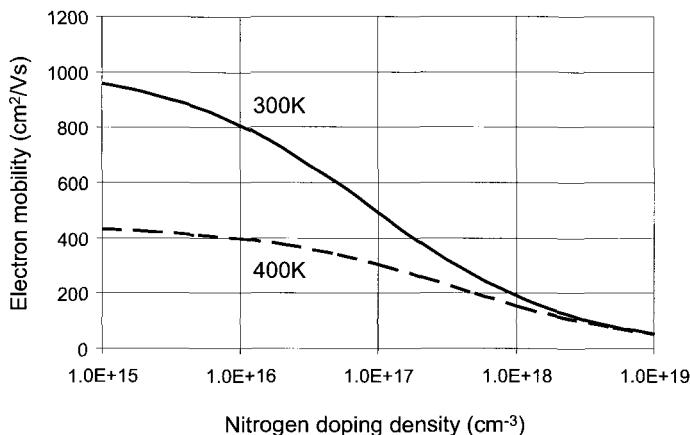


Fig. 4. 4H-SiC electron mobility versus doping density for  $T = 300\text{K}$  and  $T = 400\text{K}$ .

### 1.2.2 Incomplete ionization of dopants in 4H-SiC

4H-SiC exhibits two different donor lattice sites, a cubic one and a hexagonal one, the hexagonal one showing the lower ionization energy. For nitrogen as the donor the corresponding activation energies amount about 50 meV for the hexagonal lattice site and about 90 meV for the cubic lattice site. Depending on doping density and temperature the donors may not be fully ionized. This dependence is shown in Fig. 5a.

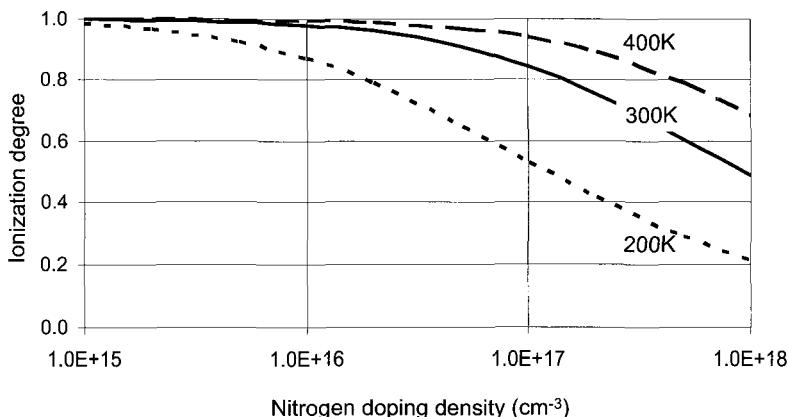


Fig. 5a. Ionization degree  $N_D^+/N_D$  versus Nitrogen doping density  $N_D$ ; parameter temperature. The average ionization energy of 75 meV was used in the approximate calculations<sup>14</sup>.

Fig. 5a shows that for a nitrogen doping density of  $5 \cdot 10^{17} \text{ cm}^{-3}$  at room temperature only about 60% of the dopants are ionized while at 400K about 80% are ionized. This in combination with the behaviour of the electron mobility leads to a lower reduction of channel conductivity with temperature for higher doping density.

Incomplete ionization, however, is much more pronounced for p-type doping as can be seen from Fig. 5b.

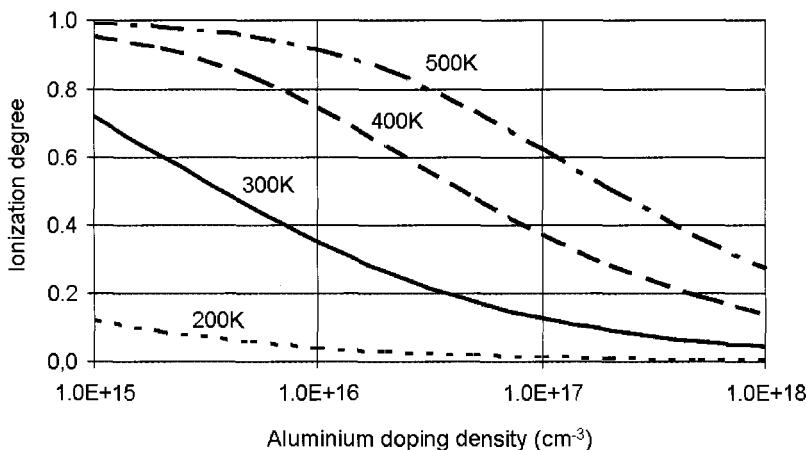


Fig. 5b. Ionization degree  $N_A^+ / N_A$  versus aluminium doping density  $N_A$ ; parameter is the absolute temperature. The ionization energy of 210 meV was used in the calculations<sup>14</sup>.

The low ionization degree of p-doped 4H-SiC in combination with the much lower hole mobility compared with the electron mobility (see Table 1) makes p-doped material not really suited to conduct a large current.

### 1.2.3 Consequence

The channel doping density of a normally-on SiC-JFET should be chosen as high as possible with respect to the reproducible manufacturability of the channel height, in order to get a high conductivity together with its low reduction when temperature increases. Operation significantly above room temperature because of self-heating is a unique characteristic for power semiconductor devices.

### 1.2.4 Built-in voltage

With no applied voltage every pn-junction has a built in voltage  $V_{bi}$  (in addition an accompanying space charge region  $w_{bi}$  see Eq. (10)) of

$$V_{bi} = \frac{k \cdot T}{q} \cdot \ln \left( \frac{N_A \cdot N_D}{n_i^2(T)} \right) \quad , \quad (9)$$

where the intrinsic carrier concentration  $n_i$  is negative exponentially dependent on the band-gap energy  $E_g$ . With the wide band-gap of 4H-SiC ( $E_g \approx 3.24$  eV at room temperature) the intrinsic carrier concentration is extremely small, leading to pronounced built-in voltage in the order of about 3 V at room temperature for practically relevant doping concentrations. This is about 3.5 times higher than for instance that in silicon. The intrinsic carrier concentration of 4H-SiC at room temperature is just about  $8 \cdot 10^{-9} \text{ cm}^{-3}$  while its counterpart in silicon amounts about  $1.4 \cdot 10^{10} \text{ cm}^{-3}$ , more than 18 orders of magnitude difference. The space charge region  $w_{bi}$  for an abrupt pn-junction because of the built-in voltage (the low doping at the n-side)

$$w_{bi} = \sqrt{\frac{2 \cdot \epsilon \cdot V_{bi}}{q \cdot N_D}} \quad (10)$$

is therefore not at all negligible in a 4H-SiC JFET. This can be seen from the

$$I_{DS} = \frac{3 \cdot I_p}{V_p} \cdot \left\{ V_{DS} - \frac{2}{3 \cdot V_p^{1/2}} \cdot \left[ (V_{DS} + V_{SG} + V_{bi})^{3/2} - (V_{SG} + V_{bi})^{3/2} \right] \right\} \quad (11)$$

current-voltage characteristics of a JFET in the gradual channel approximation.

Note that we have introduced the positive direction of the gate voltage from the source to the gate in Eq. 11.

If the half-channel height  $a$  and the channel doping density  $N_D$  are chosen such that

$$w_{bi} \geq a, \quad (12)$$

which is equivalent to

$$V_{bi} \geq V_p, \quad (13)$$

the channel is depleted and  $V_{SG}$  needs to become negative ( $V_{GS}$  positive) to conduct current in the channel. The device is normally-off. A large built-in voltage makes the design of a normally-off JFET certainly easier than a small one.

### 1.3. Normally-on or normally-off?

Because of the relatively high built-in voltage of 4H-SiC pn-junctions it may be much more advantageous to realize a normally-off JFET with SiC than with silicon, since to first order the gate voltage must be lower than the built-in voltage in order to omit bipolar injection at the gate. If the gate voltage exceeds the built-in voltage, the device is said to

operate in its bipolar operation mode and significant hole injection into the channel occurs.

However, it must be pointed out that process control in doping density and moreover in channel height definition, need to be very stringent in manufacturing of normally-off JFETs. This is illustrated in Fig. 6 where the normalized variation of the saturated drain current is shown versus the half-channel height. The nominal half channel-height  $a = 0.5 \mu\text{m}$  was varied by  $\pm 10\%$ , the nominal doping concentration is  $7 \cdot 10^{15} \text{ cm}^{-3}$  and its margins are  $6 \cdot 10^{15} \text{ cm}^{-3}$  and  $8 \cdot 10^{15} \text{ cm}^{-3}$  respectively.

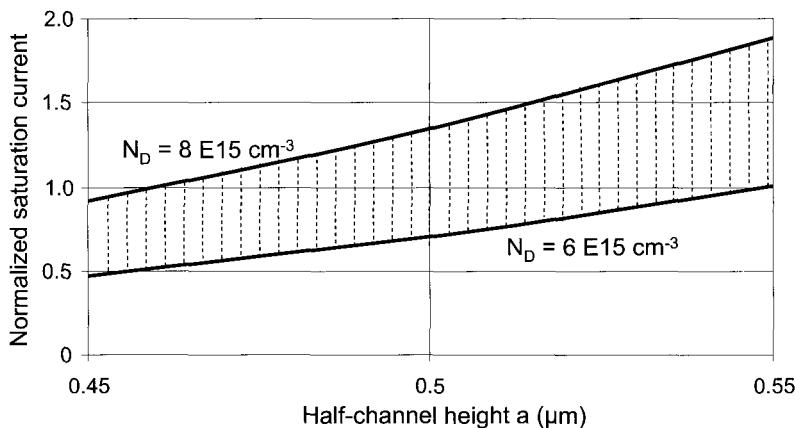


Fig. 6. Variation of the normalized saturated output current for a normally-off SiC JFET at 300K junction temperature. A 10% half-channel variation (nominal  $0.5 \mu\text{m}$ ) was assumed and the margins in doping density ( $\pm 1 \cdot 10^{15} \text{ cm}^{-3}$ ) around the nominal doping density of  $7 \cdot 10^{15} \text{ cm}^{-3}$  are depicted in the figure.

With the given variations of  $\pm 10\%$  in channel height delineation control and around  $\pm 14\%$  in doping density control the calculated variation in the saturated drain current is about +88% and -53% from its nominal value. Considering the built-in voltage now and denoting the achievable maximal channel conductance by  $g_m$  we obtain

$$g_m = g_{\max} \cdot \left( 1 - \sqrt{\frac{V_{SG} + V_{bi}}{V_p}} \right) \quad (14)$$

To fairly compare the channel conductance of normally-on and normally-off devices we allow  $V_{SG} = -V_{bi}$ . Then the normalized channel conductance scales simply with the ratio of the square root of the pinch-off voltage  $V_p$  over the built-in voltage  $V_{bi}$ .

$$g_{\max} = \frac{Z}{L} \cdot \mu \sqrt{2 \cdot \epsilon \cdot N_D \cdot V_{bi}} \cdot \sqrt{\frac{V_p}{V_{bi}}} \quad (15)$$

If this ratio is less-equals one, the device is normally-off. Normally-on devices will therefore always show a higher channel conductance than normally-off devices for

identical  $Z/L$ . The very critical issue in fabricating normally-off JFETs is to maintain their normally-off condition considering fabrication tolerances. If we assume  $\pm 10\%$  control in doping density  $N_D$  and  $\pm 10\%$  in the control of the half-channel height  $a$ , we end up by using Eq. 16 with

$$\pm \frac{\Delta V_p}{V_p} = \pm \left( \frac{\Delta N_D}{N_D} + \frac{2\Delta a}{a} \right) \quad (16)$$

and a variation of  $\pm 30\%$  for the pinch off voltage  $V_p$ . In this case we would have to design the device with a nominal pinch off voltage  $V_{pnom}$  of

$$1.3 \cdot V_{pnom} \leq V_{bi} \quad . \quad (17)$$

## 2. Lateral SiC-JFETs

Early lateral SiC JFETS<sup>15, 16, 17, 18</sup> as schematically shown in Fig. 7 should not be treated as power semiconductor devices but as demonstrators to show essential properties of the SiC technology. Among these, the high temperature operation capability ( $600^\circ\text{C}$ ) of an n-channel SiC JFET was demonstrated already in 1993<sup>15</sup>.  $550^\circ\text{C}$  operation was also shown for a normally-off p-channel JFET<sup>18</sup>.

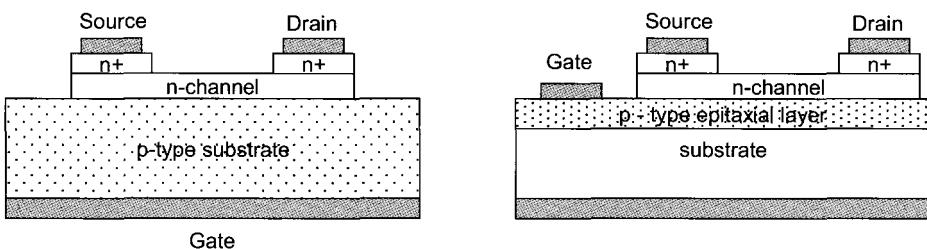


Fig. 7. Early lateral SiC JFETs utilizing a so called buried gate.

Lateral JFETs have recently gained more attention<sup>19,20</sup> by utilizing the Reduced-Surface-Field (RESURF) technique as schematically shown in Fig. 8.

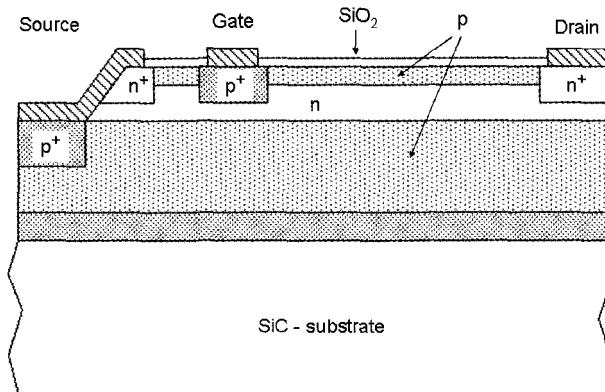


Fig. 8. Cross sectional schematic view of a RESURF JFET

Device processing starts with epitaxial growth of 4 layers in sequence. Firstly a highly p-doped buffer layer is grown onto the wafer, followed by a low-doped p-type layer of sufficient thickness to block the drain potential. The growth of an n-type channel layer follows which is covered by a p-type layer of adequate thickness and doping density to reduce efficiently the surface electric field between gate and drain. Masked ion implantation defines n<sup>+</sup>-source, n<sup>+</sup>-drain and the p<sup>+</sup>-gate. Masuda et al.<sup>20</sup> have achieved a normally-on device which blocks about 800 V at gate-to-source voltage of -10V, while a specific on-resistance of 6.3 mΩcm<sup>2</sup> has been reported, applying a gate-to-source voltage of +2V.

Although a lateral switching device is said have some advantages in a power module with respect to system integration<sup>19</sup> it must be pointed out, that because of the three electrodes owing different electrical potentials on the wafer surface, significant wiring problems and insulation problems have to be solved in the design of a 600V or higher blocking voltage device. And, the cell density of such a device or with other words the achievable ratio Z/L per unit area will always be smaller than in a vertical JFET. A further point to consider is the poor conductivity of p-type 4H-SiC material (low acceptor ionization in combination with a low mobility, see chapter 1.2). This and the generally poor quality of p-type 4H-SiC substrates impedes in the use of a sinker concept. The sinker concept uses a p-type wafer and allows contacting the source at the back of the wafer.

### 3. The Vertical JFET (VJFET)

#### 3.1 *The purely vertical JFET*

A purely vertical JFET is schematically depicted in Fig. 9.

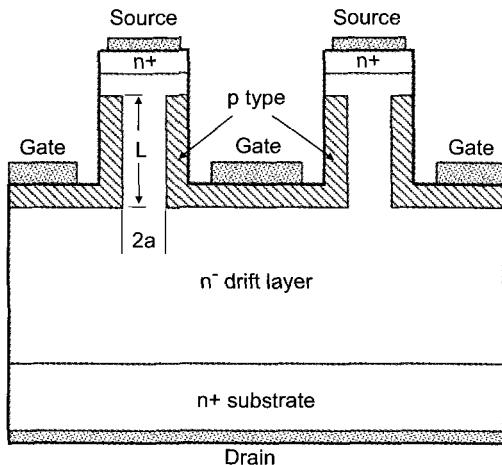


Fig. 9. Cross-sectional view of a purely vertical JFET

The question of whether a structure as shown in Fig.9 shall be named a SIT or a VJFET depends on whether the device shows a triode-like behaviour or a pentode-like one. In a SIT an increasing drain potential weakens the potential barrier in the channel such, that an increasing number of electrons from the source can overcome the barrier, leading to an exponentially growing drain current. This injection is similar to that at the emitter-base junction of a bipolar transistor. The “induction” of the drain potential onto the potential barrier in the channel gave the device its name. In a VJFET this induction is negligible and in the saturation regime the drain current is independent from the drain voltage. Long channel devices  $L/a \gg 1$  show pentode-like characteristics, short channel devices  $L/a < 3$  tend to triode-like characteristics. We shall in the following discuss only long channel devices.

For a JFET power switch there are three characteristics particularly important:

- the on-resistance (as low as possible)
- the blocking voltage (as high as possible)
- the saturated drain current (as high as possible)

### 3.1.1 Purely vertical power Junction Field-Effect Transistors – state of the art A.D. 2005

Diffusion of dopants in hexagonal SiC takes significantly place only at very high temperatures ( $T > 2200\text{K}$ ). Therefore pn-junctions can be formed either by epitaxial layer growth or by (masked) ion implantation and subsequent high temperature annealing.

Mizukami et al.<sup>21</sup> have tried to utilize high energy (several MeV) masked Al ion implantation to form deep p-gates within the epitaxially grown n- drift layer. The gate length achieved by this method was about  $2.5 \mu\text{m}$ . Subsequent masked phosphorous implantation defined the n<sup>+</sup> source. 600V class vertical JFETs were targeted. For  $V_{SG} = -$

2.5 V ( $V_{GS} = 2.5$  V) a specific on-resistance of  $16 \text{ m}\Omega\text{cm}^2$  was reported, while for  $V_{SG} = 46$  V the device blocked 900 V. However, as depicted in Fig. 10 the channel created by high energy ion implantation becomes (double) funnel-shaped because of ion scattering processes. This will cause a strong influence of the drain potential onto the potential barrier in the channel.

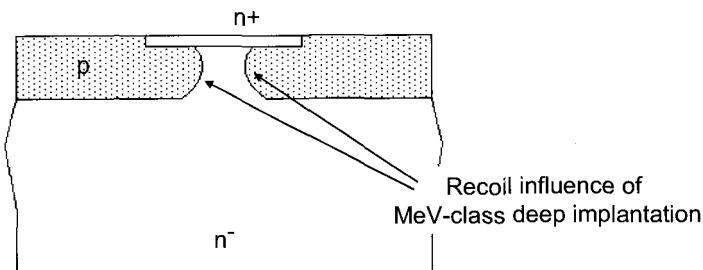


Fig. 10. Scheme of the channel shape produced by high energy ion implantation

Tanaka et al.<sup>22</sup> have epitaxially grown a p-type layer on an n-type drift layer. Trenches have subsequently been etched into the p-type layer down to the drift layer and this structure was overgrown again by an epitaxial n-type layer, in this way realizing a buried gate structure. Since diffusion of dopants in SiC is generally negligible, the p-type profile is conserved in the subsequent epitaxial overgrowth process. From the data reported this device should be treated as a SIT and was also named as a SIT by the authors, since the channel aspect ratio  $L/a$  was about 2.5 and the device was normally off. At -12V gate voltage the device is said to block 700 V while at +2.5 V gate voltage a specific on-resistance of  $1.01 \text{ m}\Omega\text{cm}^2$  was reported. This is certainly an outstanding demonstrator; however, process tolerances in doping density and in submicron pattern transfer by reactive ion etching may lead to a very wide scatter in on-resistance and blocking voltage (see chapter 1.3).

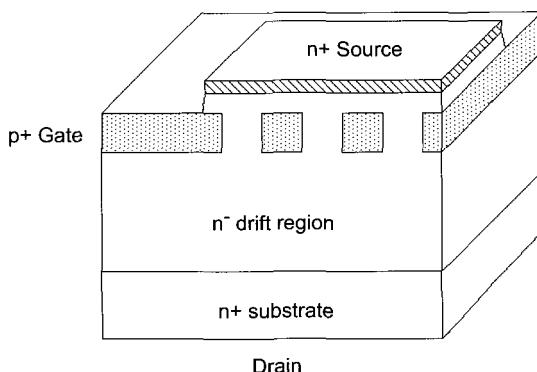


Fig. 11. Vertical JFET(SIT) fabricated by dry etching and epitaxial overgrowth (see text)

Zhao et al.<sup>23</sup> have solved the problem of a more adequate channel aspect ratio by firstly etching the strip-line masked n-type drift layer to a certain depth, resulting in vertically walled mesas of n-type material on top of the remaining drift layer. In order to realize the p-type doping at the bottom and the sidewalls (see Fig. 9) by ion implantation, the substrate was tilted against the direction of the ion beam and rotated. The devices are generally normally off and, require a positive gate-to-source voltage close to or above the built in voltage of the pn junction to be adequately turned on. This again leads to a significant gate leakage current and from a power semiconductor devices point of view the normally-off VJFET behaves more or less like a bipolar junction transistor with a decreasing current gain, the higher the gate voltage is chosen. For a (one) normally-off JFET a specific on-resistance of  $3.6 \text{ m}\Omega\text{cm}^2$  in combination with a blocking voltage of 1,726V were reported.

E. Hanna et al.<sup>24</sup> have reported a vertical JFET where a poly-silicon gate is separated from the vertical channel region by a thin insulating silicon-dioxide layer, while the poly-silicon gate is in contact with a p-type implanted SiC layer at the bottom of the gate. This is schematically illustrated in Fig. 12. The device was named MOS-enhanced JFET.

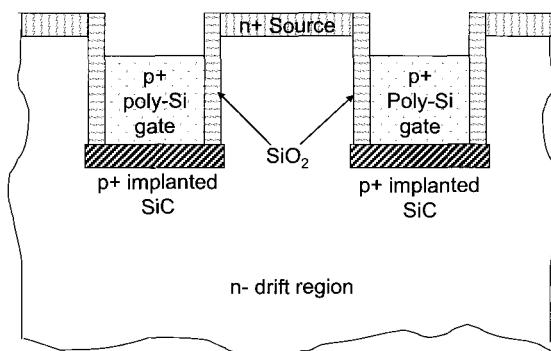


Fig. 12. Cross-sectional view of a MOS-enhanced JFET according to Hanna et al.<sup>24</sup>

The reported device is normally on, but does not suffer from an exaggerated gate leakage current if the gate voltage exceeds the built-in voltage of the pn-junction. This is because of the poly-silicon gate which forms a Schottky-barrier contact with the p-doped SiC. A positively increasing gate voltage leads to an accumulation of carriers in the channel by the sidewall oxide and thus to a strongly reduced on-resistance of the device, while at negative gate voltage electrons in the channel become more and more depleted. Therefore, the device could also have been named as depletion-mode trench MOSFET. A blocking voltage of 600 V combined with a specific on-resistance of  $2.86 \text{ m}\Omega\text{cm}^2$  were reported.

*One of the properties of all purely vertical JFETs to mention is their inherently high gate-to-drain capacitance (Miller-capacitance). A further inherent disadvantage for purely vertical JFETs is, that the bipolar diode formed between gate and drain can't be used as an integrated freewheeling diode (see Fig. 15 for reference).*

### 3.2 The vertical JFET with lateral channel

A simple schematic illustration of such a device is shown in Fig. 13.

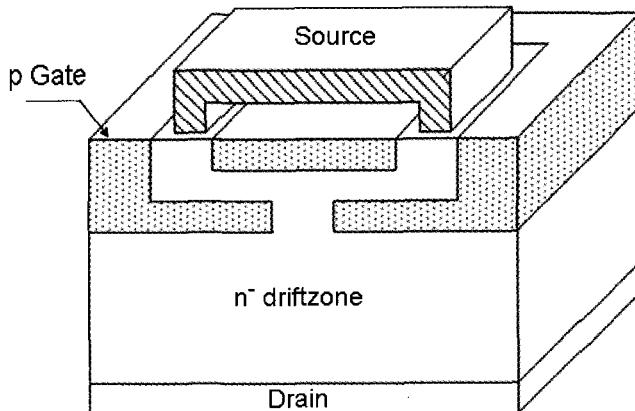


Fig. 13. Simplified cross-sectional view of a VJFET with lateral channel. In this art form illustration the insulation of the source contact from the gate is solved by a bridge-like structure.

As may be evident from Fig. 13 it will not be simple to realize such a structure with planar technology having available just epitaxial layer growth and ion implantation available for differently doped layers.

A more technical drawing as shown in Fig. 14 depicts that significant wiring and insulation problems need to be solved in order to realize a dense cell structure.

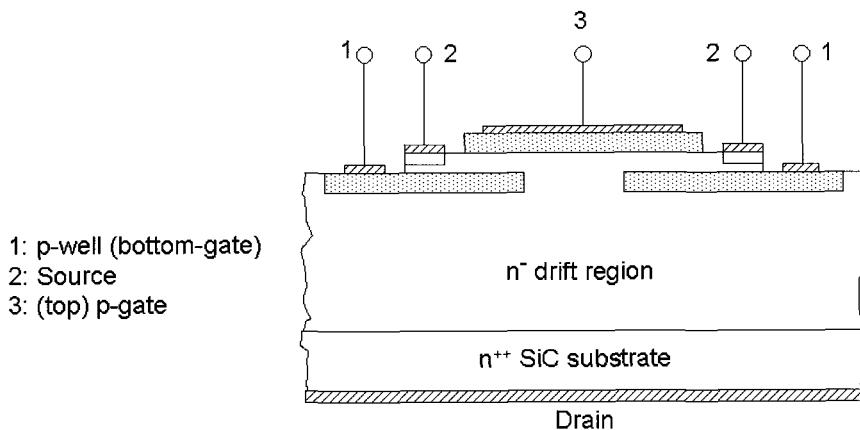


Fig. 14. Cross section of a vertical JFET with lateral channel and available electrodes.

The p-well can be realized by masked Al ion implantation into a first epitaxially grown layer. After growing a second n-doped layer – the channel layer - at typically 1600°C, the Al ion implanted regions are annealed and because of the lack of diffusion

the doping profile is conserved. The (top) p-gate layer can be formed also by masked ion implantation into the channel layer. Subsequent high temperature annealing activates the ion implanted Al dopants.

A structure as simplified shown in Fig. 14 can be packed more densely and fabricated easier, if the source is connected directly to the (top) p-gate (case A) or to the p-well (case B). However, if connecting the source to the p-well this results not only in a rugged body diode, but results also in a much smaller gate-to-drain capacitance. Furthermore, the integrated body diode in case A is connected between source and gate, while in case B it is connected between source and drain. This is schematically shown in Fig. 15.

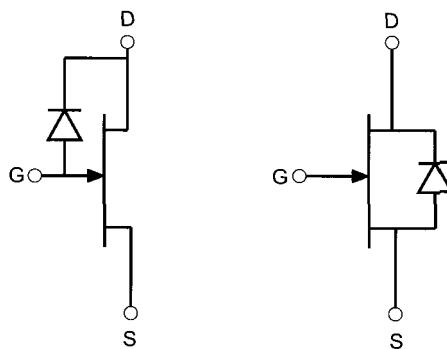


Fig. 15. Circuit diagrams showing the body diode if the source is connected to the top gate or in a purely vertical JFET (left) and if the source is connected to the p-well (right).

The resulting device structure when connecting the source to the p-well is shown in Figure 16.

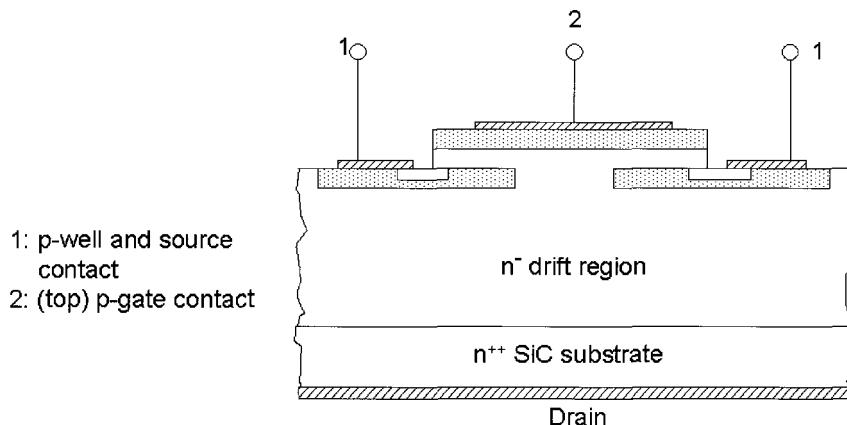


Fig. 16. Cross section of a vertical JFET with lateral channel. The n<sup>+</sup> source is embedded in the p-well and reaches below the p gate, in order to minimize the source resistance.

As long as  $V_{SG} = 0$ , the channel conductance is not changed with respect to a symmetrical gate like in a purely vertical JFET. However, while in a symmetrical normal-on JFET the gate voltage to deplete the channel  $V_{SGd}$  is simply given by

$$V_{SGd} = V_p - V_{bi} \quad (18)$$

(note that the pinch-off voltage is defined in the absence of a built-in voltage) in the asymmetrical case a voltage of

$$V_{SGd} = V_p \cdot \left( 2 - \sqrt{\frac{V_{bi}}{V_p}} \right)^2 - V_{bi} \equiv 4 \cdot \left( V_p - \sqrt{\frac{V_{bi}}{V_p}} \right) \quad (19)$$

is required, to fully deplete (pinch-off) the channel.

Since both, the channel height and the channel doping density as well as the p-gate can be formed by ion implantation into a low doped epitaxially grown planar layer, the achievable precision in the fabrication of vertical JFETs with lateral channel exceeds by far that achievable with purely vertical JFETs.

The idea to realize the described solution for a VJFET with a lateral channel and vertical current flow was predominantly triggered by experience gained from normally-off silicon carbide DMOSFETs. In SiC, in the mid nineties MOSFETs in 4H-SiC suffered from a poor channel mobility and thus, it was not possible to realize power MOSFETs with very low on-resistance. A pragmatic approach was to leave the surface inversion channel and to create a bulk channel where the full utilization of the bulk mobility will be possible. Such a structure evidently would be a JFET like, however, in order to maintain advantageous features like an integrated body diode e.g. or a high cell density, the uncommon way of connecting the second gate of a JFET to the source was chosen. Physical simulation revealed furthermore that this approach offered the opportunity to get rid of one important drawback of known power JFET structures namely, the poor blocking gain BG defined by the influence of the drain voltage  $V_D$  on the carrier repelling potential  $V_C$  in the depleted channel

$$BG = \frac{\partial V_D}{\partial V_C} \quad (20)$$

Especially high voltage vertical JFET structures suffered from a triode like behaviour and thus, in silicon JFETs are popular for low blocking voltages only (maximum 150V .. 200V).

Mandatory for a successful design was a precise definition of the buried p-layer where the distance of the p-wells in relation to the channel length and height is the most important design parameter. Like shown in figure 17, avalanche breakdown occurs at the edges of this buried layer and the layout must be chosen in a way that up to this condition the electric field can be effectively shielded from the channel region. By doing this, pentode like characteristics can be achieved.

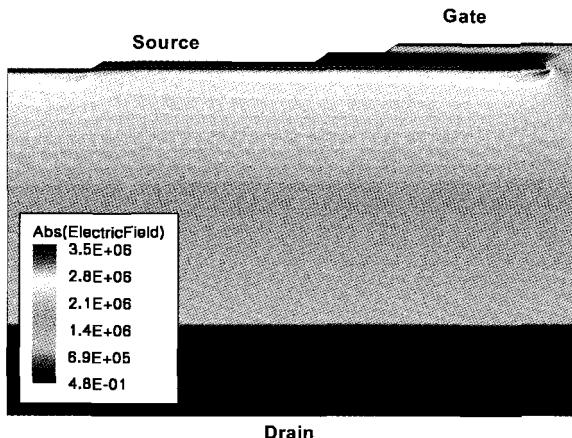


Fig. 17. Simulated electric field distribution in forward blocking mode for a VJFET with a lateral channel like sketched in Fig. 16 (performed using ISE TCAD), the unit for the numbers is V/cm.

The gate bias necessary to pinch off the channel and therefore to block the device becomes now independent of the drain bias and thus, the driver design is much more easier and more comparable to standard solutions like known for IGBT's e.g. (although with the opposite polarity and philosophy since the JFET is inherently normally on).

In the literature, several attempts where presented which targeted to normally off JFETs or even quasi normally off structures<sup>25</sup> (both, with lateral and vertical channels). In this case, the possibility to modulate the channel is limited to some volts of bias, decreasing with temperature (as long as a purely unipolar current flow is assumed). However, mainly the surge current capability will be limited in such structures and since this parameter was identified as crucial from an application point of view, the later described JFETs were designed “as on as possible”.

Initially, two types of such vertical JFET structures were investigated. Half cells of these structures with the potential drop (0.1V per line) under forward bias are shown in Fig 18.

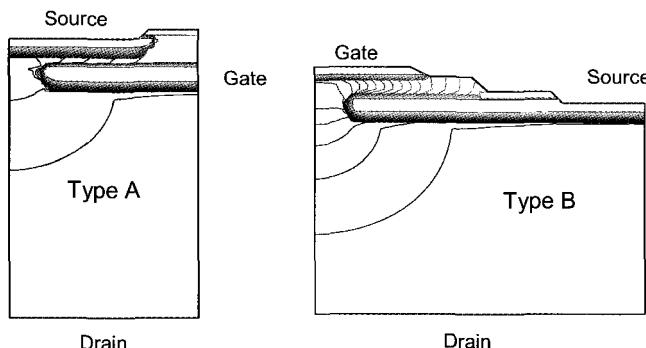


Fig. 18. VJFET structure A (left) with buried gate acting as the controlling (biased) electrode and VJFET structure B with the upper p-layer as gate electrode under forward bias for approx. 100A/cm<sup>2</sup>, type A exhibits a voltage drop of 0.8V, type B of 2 V.

The devices were fabricated in n-type 4H-SiC. Both structures exhibit a buried p-layer. Between this buried layer and a second p-layer at the top of the device, a lateral channel is formed for controlling the device current. From a designer's point of view, this solution allows for a design of the so-called head region independent of the desired blocking voltage for the case that the dimensions of the head region as well as the distance between the buried p-regions are carefully adjusted.

The head region of both types is formed by a second epitaxial layer after forming the buried p-layer via ion implantation into the drift zone. This layer determines important parameters like pinch-off bias, saturation current etc. (see the following sections).

In the blocking regime, the voltage drops between the buried p-layer and the substrate and is supported by the lower n<sup>-</sup>-epitaxial layer. In the case of silicon carbide, this layer can be designed much thinner and with a higher doping than for conventional silicon devices. This results in very low specific on-resistances. For a 1200V switch, e.g., in the classical planar silicon technology an approx. 80μm thick layer with a doping density of  $1 \times 10^{14} \text{ cm}^{-3}$  is necessary, resulting in a specific on-resistance of  $800 \text{ m}\Omega\text{cm}^2$ . The same blocking voltage can be obtained in SiC with a 12μm thick layer doped with  $1 \times 10^{16} \text{ cm}^{-3}$ , giving a specific on-resistance of less than  $10 \text{ m}\Omega\text{cm}^2$ .

The structure shown in Fig. 18 left shows extremely low on resistances since the current flows directly from the source region through the channel into the drift region. As shown in Fig. 18 the voltage drop in the channel region is small (see the number of potential lines in Fig. 18). Additionally, since the doping and height of the channel can be more precisely adjusted than for a vertical channel, a wide range of pinch-off voltages and saturation currents can be realized. However, in this structure, the Miller capacitance is quite large since the area of the gate-drain capacitance is large. Furthermore, in order to realize a high cell density, the gate resistivity is to a great extent determined by the p-type conductivity in the buried layer, which is – because of incomplete ionization and low hole mobility (see chapter 1.2) – very low in SiC. Thus, the switching speed of this type of device is rather limited. The second configuration in Fig. 18 right allows ohmic contacts to all p-regions. In combination with the low miller capacitance for such structures the switching speed can be increased. The disadvantage, however, is a pre-channel region between the source area and the channel necessary for blocking the Gate-Source pinch-off voltage. This pre-channel results in an increase of the on resistance of the device, simulation reveals that nearly 30% of the device resistance is caused by this pre-channel.

As a consequence of the upper presented results, a third topology was developed, combining the advantages of both topologies. Figure 16 shows a unit cell of this design. The controlling gate is again located on the top of the device, while the source region was completely shifted into the buried p-gate layer, very similar to the well known concept of vertical DMOS. Additionally, in this configuration the gate length can be adjusted very precisely and self aligned, while in the other concepts always alignment errors and pattern shifts caused by epitaxial overgrowth can occur. This concept was further improved over several generations addressing the following parameters

- surge current capability : JFETs inherently have lower surge currents capabilities compared to MOSFETs. Even if the current limiting feature is often

of advantage, e.g. in short circuit operation, the device should be able to handle at least five times the nominal current for the use in most of the targeted applications<sup>26</sup>

- further reduction in  $R_{on}$  and pinch-off voltage control : both,  $R_{on}$  and the pinch off voltage are largely influenced by the homogeneity of the second epitaxial layer. Technological means were developed which lead to both, a further reduction and homogenization of  $R_{on}$  and a well controlled, homogeneous pinch-off voltage. In addition by doping engineering in the channel, the increase of the on-resistance with temperature could be reduced, leading to lower static losses at operating temperature<sup>27</sup>
- Avalanche behavior: the device topology was improved in order to rule out electric field enhancements at corners, the edge or other localized spots in order to achieve a homogeneous and rugged avalanche. These techniques resulted also in a further reduction of the specific on-resistance since by removing these critical points, a better utilization of the maximum field in SiC was possible.
- Better device volume utilization was the target for the last optimization step, again the reduction in  $R_{on}$  and a higher surge current capability as well as an improved  $R_{on}$  vs. temperature characteristic were the primary targets.

Figure 19 shows I-V characteristics for a large area device based on the latest generation of vertical VJFETs at SiCED owing the structure shown in Figure 16. A specific on-resistance of about  $10\text{m}\Omega\text{cm}^2$  for 1200V blocking voltage was achieved.

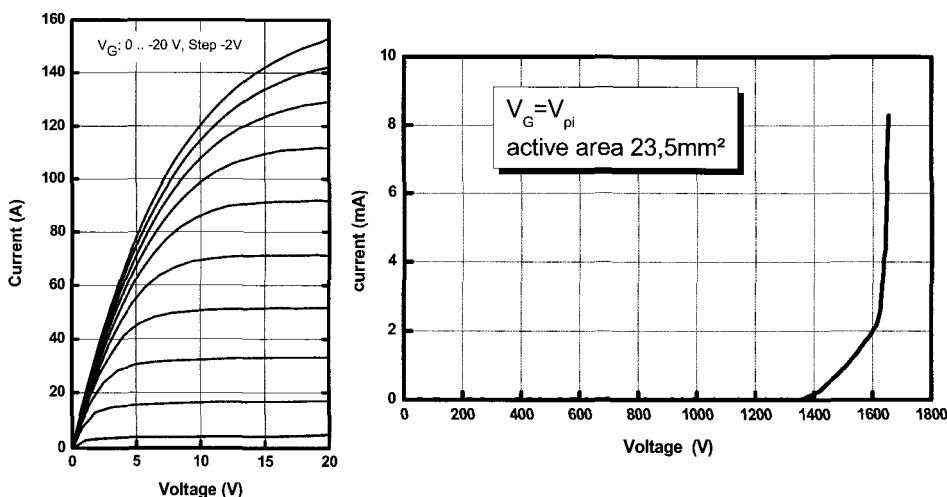


Fig. 19. I-V Characteristics of a large area single die 1200V SiC VJFET, the  $R_{on}$  was  $<50\text{m}\Omega$  at room temperature

### 3.2. Current limiters

The feature of limiting the current which is inherent to JFET structures created the wish of circuit engineers to have a two terminal devices acting as a solid state fuse without interrupting an electrical circuit, but ensuring operation by limiting the current flow even in case of a short circuit to a given value. Especially SiC components gained a specific interest due to the ability of SiC pn-junctions to operate properly even at elevated temperatures. During limiter operation, large losses will occur within the semiconductor and therefore, the chip will heat up. In silicon, quickly the physical limit will be achieved which restricts the use of Si in such applications. SiC, however, theoretically could work up to several hundreds °C, and thus, could be a potential candidate for a current limiter with the potential of not only limiting current, but also suppressing short circuit currents as was proven by the testing of first generations of VJFETs<sup>34</sup>. Several publications dealt with theoretical considerations, however, for most of the structures investigated or suggested up to now the contradictory demands on a low on-resistance in normal operation and a limiting behavior relatively close to the nominal current (see Fig. 20) were difficult or combine in only one device.

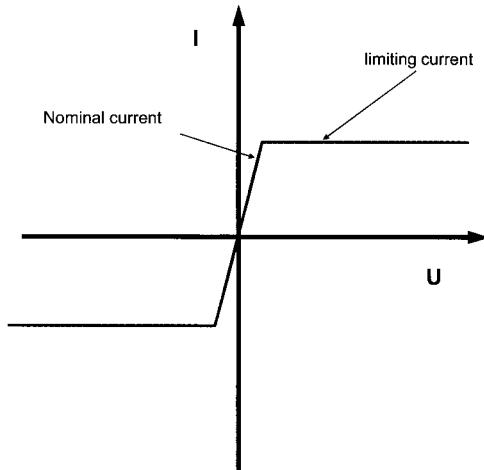


Fig. 20. Expected I-V behavior for a current limiting device, in the ideal case, the differential on-resistance in normal operation is close to zero, in fault operation (limiting case) infinite.

Thus, today the solid state current limiter especially for higher currents in the range of some amps or more is a challenge even by assuming JFET like structures in SiC. For protecting small signal inputs in telecommunication circuits solutions could be feasible, however, in these circuits the cost pressure is enormous and therefore, it will be questionable whether limiters will become commercial success.

Solutions where the limiting device is not a pure two terminal block or combined with a switch could offer intermediate solutions by actively turning off such a combination in the case of failure. Now, the short circuit ruggedness of JFET-like structures can be utilized. Since most of the known structures can be easily operated in short circuit for

more than  $100\mu\text{s}$  (what is more than a factor of ten higher than today's silicon capabilities), a detection circuitry based on simple comparator functions can be used and the limiting device itself can be smoothly turned off in such a case. Alternatively a switching device can be placed in series which can take over the turn off function in case of a failure.

### 3.3. Power switches based on SiC VJFETs

#### 3.3.1. The cascode approach

The aforementioned several optimization steps were implemented into different generations of VJFETs. Initially, the connection into cascode with a low voltage MOSFET<sup>28</sup> was chosen for offering a normally off device with a control characteristic virtually identical to silicon MOSFETs or IGBT's (see Figure 21). In cascode configuration, both devices operate as two resistors in series as long as the MOSFET is turned on. After turning off the MOSFET, its drain-source bias increases and provides the necessary pinch off voltage of the JFET. Thus, after reaching this value, the JFET will block and every further increase of the potential at the drain of the cascode will be supported by the JFET. The cascode itself represents the internal structure of a power MOSFET in a hybrid version.

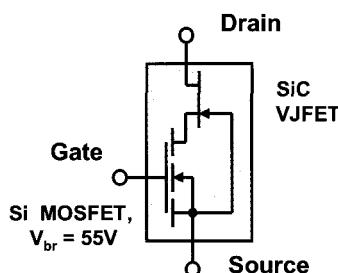


Fig. 21. Connection of a vertical JFET into cascode with a low voltage silicon power MOSFET. From a users point of view the device behaves basically like a well known three terminal MOSFET

The equivalent circuit of every power MOSFET<sup>29</sup> consists of a low voltage MOS switch and a high voltage VJFET connected to each other as shown in Fig. 22. Thus, for the user the device should act like a high voltage MOSFET. This was proven by analyzing the basic I-V characteristic as well as the dynamic behavior of the cascode<sup>30</sup>. Prominent features are low on-resistances combined with a high switching speed. For hard switched applications, more than 100kHz operating frequency even for blocking voltages far above 1000V becomes feasible. It was shown, that for reliable and fast cascode operation, the gate response of the JFET must be quick enough in order to avoid transient avalanche effects in the MOSFET<sup>35</sup>. Therefore, the concept with the control gate at the surface of the chip and the buried gate connected to the source (see Fig. 16) is preferred for fast switching processes.

A challenge represents the adjustment of the MOSFET and the JFET as well as the used packaging approach. Due to the hybrid concept, additional stray inductances appear in the internal structure, furthermore, the capacitances of the JFET and the MOSFET should be carefully fitted to each other in order to avoid steep changes with the applied drain source voltage as shown in Fig. 22.

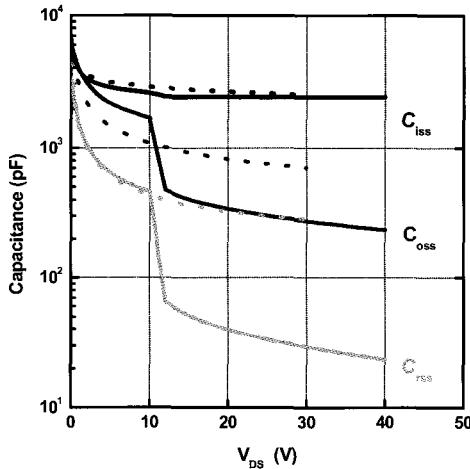


Fig. 22. Capacitance characteristic of a cascode (solid line) compared to the data for a low voltage MOSFET alone (dotted line)

Especially for the expected very fast switching behavior of unipolar SiC components, these parasitic parts can deteriorate the achievable performance. Occasionally uncontrollable oscillations occur, furthermore, on a first glance there seems to be no chance to influence the slope of the transients via gate resistors as usually done in Silicon (especially during the turn off transients in Fig. 23).

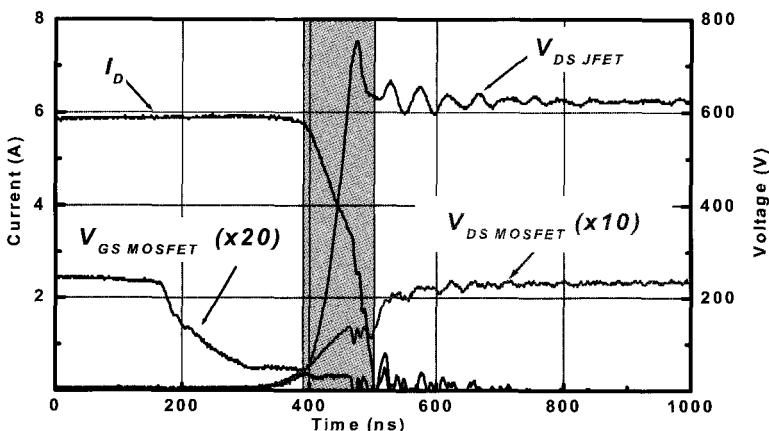


Fig. 23. Typical turn-off characteristics of a cascode (chopper circuit), the slopes of bias and current within the marked transient time interval are only slightly influenced by using gate resistors at the MOSFET gate in the typical range of some Ohm (see also Fig. 24)

It could be shown, that by far large resistors are necessary in order to achieve the required controllability (Fig. 24). In summary, for using the full dynamic potential of these high voltage switches, the packaging design as well as the PCB layout need to be carefully addressed in order to reduce parasitic inductances as far as possible.

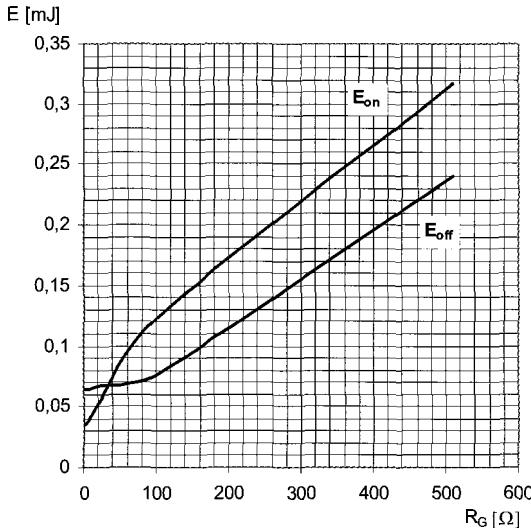


Fig. 24. Controllability of the turn-on/turn off energy losses for the cascode by increasing the gate resistor of the MOSFET gate. It can be seen that for small gate resistors ( $<100\Omega$ ) nearly no control of the transients (and thus the energy) is possible.

In reverse operation, the cascode behaves predominantly like the low voltage silicon MOSFET since the JFET acts only as a series resistor and the turn-on of the SiC JFET body diode is unlikely. In contrast to high voltage silicon MOSFETs, the internal body of a 30V...50V MOSFET exhibits only small reverse recovery charges and short recovery times. Thus, even for freewheeling operation the cascode offers considerable advantages compared to existing silicon solutions using MOSFETs or even IGBT's with freewheeling pin diodes (see Fig. 25).

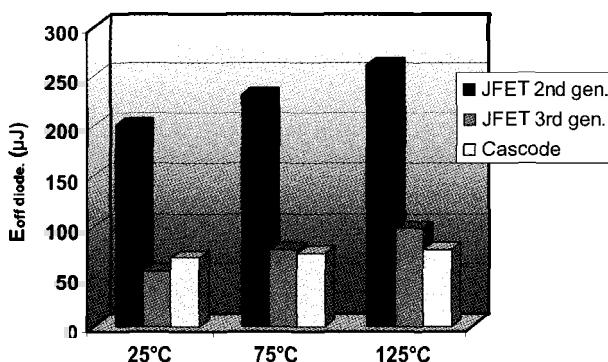


Fig. 25. Turn off energies for the internal body diode of the latest generation VJFETs and the cascode with a 40A/55V silicon power MOSFET at SiCED. Best available 1200V silicon pin diodes of comparable current ratings have already at room temperature turn off energy losses of  $> 1\text{mJ}$ .

### 3.3.2. Single die VJFET

Though most of the circuit designers required firstly the cascode configuration, the request to operate the single die VJFET appears more and more. Most of the circuit developers asking for the single die VJFET would like to utilize either the temperature capabilities offered by the JFET or would like to take advantage of the further improved speed after omitting the MOSFET in the switch<sup>30</sup>. The on a first glance critical issue of working now with a normally on device needs to be addressed, however, in normal operation there is no real problem, solutions need to be evaluated where in the case of faults or during turn on a safe operation is guaranteed. In addition, this is not completely new since the vacuum tube electronics as well as first semiconductor switches were basically normally on ones and thus, the phantasm of the circuit engineers is required to deal with this feature.

### 3.3.3. Applications for SiC VJFETs

Due to the similarity to well known unipolar switching devices based on silicon SiC VJFETs offer the potential to replace silicon switches and even to create new solutions based on solid state devices. In motor drives, e.g., today mostly IGBTs with freewheeling diodes are used. Replacing these diodes by SiC Schottky Barrier devices will be a first, already realized first step towards an improved performance in these systems. The next step will be the diode-less solution with only one device per switching function, since SiC switches offer a very fast body diode and thus, no external freewheeling path must be established. This offers reduced losses, simpler systems with a higher reliability and a higher power density due to the smaller footprint. Other potential applications can be found in switch mode power supplies. The trend towards higher frequencies for this type of applications is ongoing; therefore, SiC devices will have from a purely technical point of view of enormous advantage due to the ability of unipolar switching up even for blocking voltages above 1000V, combined with low capacitance for a given current rating. Simpler systems can be realized having available a fast switch with a high blocking voltage (e.g. the replacement of bridge topologies containing four switches with a simple single switch forward converter)<sup>36</sup>. The breakthrough of this attempt is still hindered by the new feature of high voltages within a system, however, also for these applications a mind change will help to promote a new technology. One precondition for the use of SiC VJFETs in these simple topologies is extraordinary avalanche ruggedness. Latest results prove that SiC VJFET prove their expected potential and show a very high single pulse avalanche energy which is considerably higher than silicon devices of comparable die size and in addition a rugged behavior under repetitive avalanche conditions<sup>37</sup>. Numerous other ideas how to utilize the advantageous features offered by SiC switching devices are under development and will offer a broad application base for the future.

### 3.3.4. High temperature operation

One particular topic of interest for the use of SiC VJFETs should be addressed in this in this chapter. Especially during the first years of the third millennium the request to have a high temperature semiconductor device available was more and more observed. However, besides a few exceptions<sup>31</sup> such devices have not appeared on the market up to now. The reason for this may be the rather limited market size of such devices, which were generally devoted to so called “geothermal” applications. This situation may change substantially in the near future because of two emerging fields of applications. On the one hand Hybrid Electric Vehicles (HEV) and on the other hand a more electric aircraft represent two distinct markets – presumably of growing size, which will require semiconductor power devices capable of reliable operation up to 300°C junction temperature.

In the course of this discussion the region of junction temperatures up to 300°C will be named just elevated temperature, with respect to the potential capabilities of silicon carbide. The required blocking voltage within these fields of applications will mostly be around and above 600V. It is obvious that there will be tremendous demands on packaging technologies especially for air-cooled applications in aircrafts. While in HEV applications silicon based MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) and IGBTs (Insulated Gate Bipolar Transistors) are feasible for reliable operation at rated blocking voltage of 600 V and maximum junction temperature of 200°C (175°C is already available), this does most probably not hold for higher junction temperature. While silicon based power electronic switches will be (and are) used for HEV drive inverters, for DC-DC converters this is an open question because of the much higher switching frequency necessary to achieve the required power density.

There is an ongoing discussion whether SiC MOSFETs will be capable of high reliability operation up to junction temperatures of 300°C. High reliability means at least a Mean Time to Failure (MTTF) of more than 10 million hours of operation. The corresponding Failure in Time (FIT) rate is correspondingly lower than 100 (1 FIT equals 1 failure in one billion hours of operation). Power MOSFETs generally have “thick” oxides e.g. 80 nm and are operated at “low” electric fields e.g. 2.5 MV/cm in comparison to silicon based ULSI – integrated circuits (some nm and around 5 MV/cm) suggesting that Time Dependent Dielectric Breakdown (TDDB) is not the major concern with planar silicon MOS-based power devices. “High-Temperature” Silicon on insulator based MOSFETs<sup>31</sup> are on the market and TDDB of oxides grown on plane silicon may not be the most severe killing factor for silicon based 600 V power MOSFETs, but the thermally generated leakage current of the body diode will allow only low voltage (e.g. <100 V) power MOSFETs to be candidates for elevated temperatures.

The utilization of SiC MOS-based devices will strongly depend on the reliability of the gate oxide. Contributions by M.K. Das<sup>32</sup> may suggest an estimated MTTF for TDDB of dry grown oxides on n-type 4H-SiC annealed in N<sub>2</sub>O at 1300°C in excess of 10 million hours for operating conditions of 3 MV/cm and 300°C. However, it is by far not clear whether this can be achieved for TDDB of SiC based power MOSFETs. Here are at least two regions of concern. The one – well known from silicon based power MOSFETs – is

the oxide between the overlap of the gate to the source which is stressed in the forward conduction mode. The other region of concern – not known from silicon based power MOSFETs – is the oxide between the gate and the center of the accumulation region which is stressed may be even more in the forward blocking condition, if the high breakdown electric field of SiC shall be utilized. Very recent work by S. Krishnaswami et al.<sup>33</sup> suggest that 4H-SiC double implanted MOSFETs (DIMOSFET's) have at least more than two orders of magnitude less MTTF than MOS capacitors on n-type 4H-SiC<sup>32</sup>, indicating that high reliability 4H-SiC DIMOSFETs operating up to 175°C are feasible, reliable operation up to 300°C will be very hard to achieve. Please notice that all members of the FET-family utilizing an oxide under high electric field stress will suffer from the aforementioned.

Therefore the VJFETs are the most promising candidates for high temperature switches. They take advantage of using only pn-junctions in the active device area where high electric field stress occurs and can therefore fully exploit the high temperature abilities of SiC in a gate controlled switching device.

In general, every unipolar power electronic device increase its on-resistance with increasing temperature because of decreasing electron mobility and therefore create increasing losses with increasing temperature at constant current. In 4H-SiC VJFETs was shown that due to the independent design of channel and drift regions a favorable tuning of the on-resistance increase can be achieved<sup>27</sup>. Fig. 26 presents a result obtained for 600V devices in comparison with state of the art Silicon super junction MOSFETs.

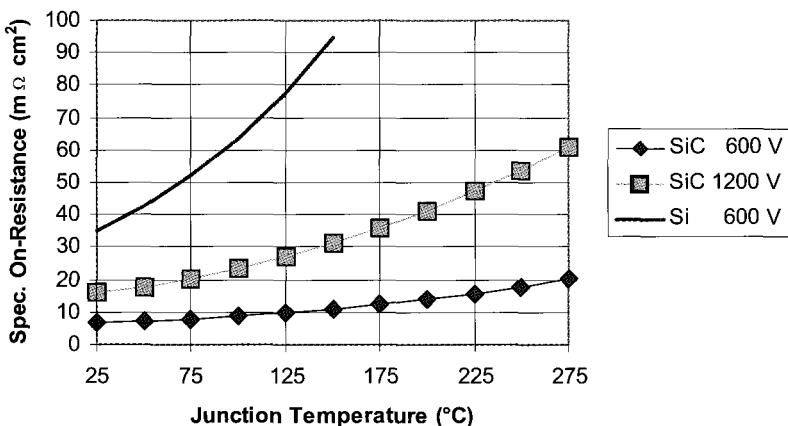


Fig. 26. Increase of the on-resistance of vertical VJFETs with the junction temperature compared to 600V charge compensated silicon devices. Taking into account an exponential increase, for the silicon device  $T^{2.7}$ , for a 1200V SiC VJFET  $T^2$  and for the 600V VJFET only  $T^{1.6}$  can be extracted

The very low exponent of 1.6 for the  $R_{on}$  increase with temperature allows for an attractive loss balance at temperatures above 200°C without loosing the ability to parallel devices in order to achieve higher current ratings in future systems.

Enormous advantages arise from the threshold voltage behavior of a JFET structure with increasing temperature. The threshold voltage is virtually independent of temperature, simply based on the fact that the pinch-off bias  $V_p$  in a JFET is defined by

the channel doping and its geometry (eq.21, the (small) change in the built in-voltage  $V_{bi}$  with temperature can be neglected in cases with  $V_p \gg V_{bi}$ ). In MOSFETs (and also IGBT's), several temperature dependent factors result in a decrease of the threshold voltage with temperature with the danger of unwanted turn on at  $T_j > 200^\circ\text{C}$  (eq.22).

$$\text{JFET} \quad V_p = \frac{q \cdot N_D \cdot a^2}{2 \cdot \epsilon_s} - V_{bi} \quad (21)$$

$$\text{MOSFET} \quad V_T = \sqrt{\frac{\frac{4 \cdot \epsilon_s \cdot k \cdot T \cdot N_A \ln \frac{N_A}{n_i}}{\epsilon_{ox}} + \frac{2 \cdot k \cdot T}{q} \ln \frac{N_A}{n_i} - \frac{Q_{ss}(T)}{C_{ox}}}{\frac{\epsilon_{ox}}{t_{ox}}}} \quad (22)$$

The experimental verification for the JFET was presented in<sup>27</sup> as well as the proof that even for  $300^\circ\text{C}$  junction temperature the leakage current increase less than one order of magnitude compared to the room temperature level. Finally, the reverse recovery behavior, usually known to deteriorate seriously with increasing temperatures for most silicon devices, is only slightly affected by the increase in temperature (see Fig. 25).

## References

1. J. E. Lilienfeld, US patent 1,745,175 (1926)
2. O. Heil, CH patent 184396 (1936)
3. J. Bardeen and W. H. Brattain, *The Transistor, A Semiconductor Triode*, Phys. Rev., **74**, 230 (1948)
4. W. Shockley, *A Unipolar Field-Effect Transistor*, Proc. IRE, **40**, 1365 (1952)
5. G.C. Dacey and I. M. Ross, *Unipolar Field-Effect Transistor*, Proc. IRE, **41**, 970 (1953)
6. G. C. Dacey and I. M. Ross, *The Field-Effect Transistor*, Bell Syst. Tech. J., **34**, 1149 (1955)
7. S. M. Sze, *Physics of Semiconductor Devices*, Second Edition, John Wiley & Sons, ISBN 0-471-05661-8
8. J. Baliga, *Modern Power Devices*, Krieger Publishing Company, Malabar, Florida, 1992
9. S. M. Sze, *Semiconductor Devices, Physics and Technology*, John Wiley & Sons
10. W. J. Shaffer, G. H. Negley, K. G. Irvine and J. W. Palmour, Conductivity anisotropy in epitaxial 6H and 4H-SiC, Mat. Res. Soc. Sym., vol. 339, 1994, pp. 595-600

11. D. Volm, B. K. Meyer, and D. M Hofmann, *Determination of the electron effective-mass tensor in 4H SiC*, Phys. Rev. B., **53**, 15409, (1996)
12. M. Schadt, G. Pensl, R. P. Devaty, W. J. Choyke, R. Stein, D. Stephani, *Anisotropy of the electron Hall mobility in 4H, 6H and 15R silicon carbide*, Appl. Phys. Lett., **65**, 3120, (1994)
13. H. Iwata and K. M. Itoh, G. Pensl, *Theory of the anisotropy of the electron Hall mobility in n-type 4H- and 6H- SiC*, J. Appl. Phys., **88**(4), (2000), pp. 1956-1961
14. M. Lades, *Modeling and Simulation of Wide Bandgap Semiconductor Devices: 4H/6H-SiC*, Shaker Verlag, Aachen 2002, ISBN 3-8265-9799-0
15. K. Dohnke, R. Rupp, D. Peters, J. Voelkl and D. Stephani, *6H-SiC junction field effect transistor for high-temperature applications*, Inst. Phys. Conf. Ser. No 137, pp. 625-627
16. P. A. Ivanov, N. S. Savkina, T. P. Samsonova, V. N. Panteleev and V. E. Chelnokov, *Junction field-effect transistor based on 4H-silicon carbide*, Inst. Phys. Conf. Ser. No 137, pp. 593-595
17. F. B. McLean, C. W. Tipton and J. M. McGarrity, *Electrical characterization of n-channel, 6H-SiC JFETs as a function of temperature*, Inst. Phys. Conf. Ser. No 137, pp. 507-510
18. R. Rupp, K. Dohnke, J. Voelkl and D. Stephani, *Normally off 6H-SiC JFET and its high-temperature operation*, Inst. Phys. Conf. Ser. No 137, pp. 503-506
19. K. Fujikawa, S. Harada, A. Ito, T. Kimoto and H. Matsunami, *600 V 4H-SiC RESURF-type JFET*, Material Science Forum Vols. 457-460 (2004) pp.1189-1192
20. T. Masuda, K. Fujikawa, K. Shibata, H. Tamaso, S. Hatsukawa, H. Tokuda, A. Saegusa, Y. Namikawa, H. Hayashi, *Low on-resistance in 4H-SiC RESURF JFETs fabricated with dry process for implantation metal mask*, Paper presented at International Conference on Silicon Carbide and Related Materials 2005, Pittsburgh, USA, Sept. 19-23, 2005
21. M. Mizukami, O. Takikawa, M. Murooka, S. Imai, K. Kinoshita, T. Hatakeyama, M. Tsukuda, W. Saito, I. Omura and T. Shinoe, *A 600 V deep-implanted gate vertical JFET*, Material Science Forum Vols. 457-460 (2004) pp.1217-1220
22. Y. Tanaka, K. Yano, M. Okamoto, A. Takatsuka, K. Fukuda, M. Kasuga, K. Arai and T. Yatsuo, *Fabrication of 700V SiC-SIT with ultra-low on-resistance of 1.01 mΩcm<sup>2</sup>*, Paper presented at International Conference on Silicon Carbide and Related Materials 2005, Pittsburgh, USA, Sept. 19-23, 2005
23. J. H. Zhao, K. Tone, X. Li, P. Alexandrov, L. Fursin and M. Weiner, *6A, 1kV 4H-SiC normally-off trenched-and-implanted vertical JFETs*, Material Science Forum Vols. 457-460 (2004) pp.1213-1216
24. E. Hanna, H.-R. Chang, A. V. Radun, Q. Zhang and M. Gomez, *Static and dynamic characterization of 20A, 600V SiC MOS-enhanced JFET*, Materials Science Forum Vols. 457-460 (2004) pp. 1389-1392
25. L.Cheng, J.R.B Casady, M.S.Mazzola, I.Sankin, J.N Merret, V. Bondarenko, R.L.Kelley, J.B.Casady, *Fast switching, 300-600V 4H-SiC VJFETs with Low On-Resistance*, presented at the ICSCRM 2005, Pittsburgh, September 2005

26. P.Friedrichs, H.Mitlehner, R.Schörner, R.Elpelt, and D.Stephani, *Optimization of Vertical Silicon Carbide Field Effect Transistors towards a cost attractive SiC Power Switch*, Material Science Forum Vols. 457-460 (2004) pp.1201-1204
27. P. Friedrichs, *Charge controlled Silicon Carbide switching devices*, MRS Proceedings vol. 815, presented at the MRS Spring meeting 2004
28. US patent no.5,406,096, filed February the 9<sup>th</sup>, 1994 granted April the 11<sup>th</sup>, 1995
29. Fairchild Application note AN-7502, [www.fairchildsemi.com/an/AN/AN-7502.pdf](http://www.fairchildsemi.com/an/AN/AN-7502.pdf)
30. J.W. Kolar et al, *A gate drive circuit for silicon carbide JFET*, presented at the IECON November 2003,
31. [http://www.ssec.honeywell.com/hightemp/tech\\_paper.htm](http://www.ssec.honeywell.com/hightemp/tech_paper.htm)
32. M.K. Das, "Recent Advances in (0001) 4H-SiC MOS Device Technology" Material Science Forum Vols. 457-460 (2004) pp. 1275-1280
33. S. Krishnaswami et al., presented at Intl. Reliability Physics Symposium, San Jose, CA, USA, April 2005
34. P.Friedrichs, H.Mitlehner, W.Bartsch, K.O.Dohnke, R.Kaltschmidt, U.Weinert, B.Weis, D.Stephani, *Static and dynamic Characterisctics of 4H-SiC JFETs Designed for Different Blocking Categories* , Materials Science Forum, Vol. 338-342 (2000), pp.1243-1246.
35. P.Friedrichs, H.Mitlehner, R.Schörner, K.O.Dohnke, R.Elpelt, and D.Stephani, *Application oriented unipolar switching SiC devices* , Materials Science Forum, Vol. 389-393 (2002), pp.1185-1190.
36. J. M. Hancock *SiC Device Applications: Identifying and Developing Commercial Applications*, presented at the ICSCRM 2005, Pittsburgh, September 2005
37. P. Friedrichs and Tobias Reimann *Behavior of high voltage SiC VJFETs under avalanche conditions*, accepted for APEC 2006, March 2006, Dallas

## SiC BJTs

T. Paul Chow

Center for Integrated Electronics

Rensselaer Polytechnic Institute, Troy, New York 12180, U.S.A.

and

Anant K. Agarwal

Cree, Durham, NC 27703, U.S.A.

### 1. Introduction

Silicon has long been the dominant semiconductor of choice for high-voltage power electronics applications.<sup>1,2</sup> However, recently, wide bandgap semiconductors, particularly SiC and GaN, have attracted much attention because they are projected to have much better performance than silicon and the epi/substrate technology has matured to make device commercialization possible.<sup>3-7</sup> Compared to silicon, these wide bandgap semiconductors, SiC, GaN and InN can be categorized into one group while diamond, BN and AlN into another because the former has bandgaps of 2-3.5 eV and the latter 5.5-6.5 eV. Group IV or IV-IV semiconductors have indirect bandgaps whereas most of the Group III-nitrides are direct (except BN). The superior physical properties of these semiconductors offer a lower intrinsic carrier concentration (10 to 35 orders of magnitude), a higher electric breakdown field (4-20 times), a higher thermal conductivity (3-13 times), a larger saturated electron drift velocity (2-2.5 times), when compared to silicon (See Table 1). SiC has over 150 polytypes (which are different crystal structures with the same stoichiometry of a compound semiconductor). Also, only the 6H- and 4H-SiC polytypes are available commercially in both bulk wafers (up to 4" in diameter at present) and custom epitaxial layers (up to at least 100 $\mu$ m at present) while 3C-SiC is available as heteroepitaxial layers on large-diameter silicon substrates. Between the two polytypes, 4H-SiC has become preferred due to the more isotropic nature of many of its electrical properties. Besides these properties, the impact ionization coefficients of electron and hole are also very important for power device considerations. The experimental coefficients, usually extracted from breakdown characteristics of reverse-biased pn or Schottky junctions, are shown in Fig. 1 for both 6H- and 4H-SiC.<sup>8-10</sup> Also included in the figure is the average ionization coefficient for 6H-SiC. Such an average ionization coefficient, usually modeled by a power law dependence on the electric field ( $\alpha \propto E^n$ , where n is 5 or 7), allows one to estimate analytically the breakdown voltage and depletion width at breakdown. (See reference<sup>11</sup> for 6H-SiC and reference<sup>12</sup> for 4H-SiC.) It should be noted that, unlike in silicon, the hole ionization coefficient is higher than the electron coefficient in both 4H-SiC and 6H-SiC. Such trends have significant impact on bipolar transistor structure (npn vs. pnp) considerations, as will be discussed later. Another important parameter is minority carrier lifetime, and SiC, like silicon, is an indirect semiconductor. Consequently, SiC can have relatively long minority carrier lifetimes and homojunction bipolar switching devices are feasible. Experimentally, recombination lifetimes  $> 1 \mu\text{s}$  have been extracted in 4H-SiC.<sup>13</sup>

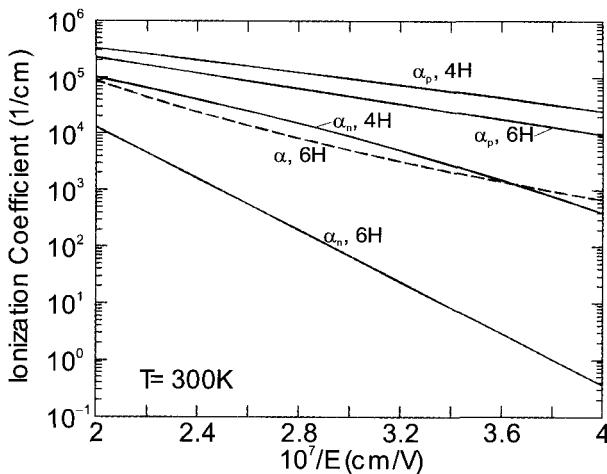
Fig. 1 Experimental impact ionization coefficients of electron and hole in 6H- and 4H-SiC.<sup>8,9</sup>

Table 1 Physical properties of important semiconductors for high-voltage power devices.

Material	$E_g$ (eV)	$n_i$ ( $\text{cm}^{-3}$ )	$\epsilon_r$	$\mu_n$ ( $\text{cm}^2/\text{V}\cdot\text{s}$ )	$E_c$ (MV/cm)	$v_{sat}$ ( $10^7 \text{ cm/s}$ )	$\lambda$ (W/cm-K)	Direct/ Indirect
Si	1.1	$1.5 \times 10^{10}$	11.8	1350	0.3	1.0	1.5	I
Ge	0.66	$2.4 \times 10^{13}$	16.0	3900	0.1	0.5	0.6	I
GaAs	1.4	$1.8 \times 10^6$	12.8	8500	0.4	2.0	0.5	D
GaP	2.3	$7.7 \times 10^{-1}$	11.1	350	1.3	1.4	0.8	I
InN	0.7	$\sim 10^{13}$	9.6	3000	0.1*	2.5	-	D
GaN	3.39	$1.9 \times 10^{-10}$	9.0	900	3.3	2.5	1.3	D
3C-SiC	2.2	6.9	9.6	900	1.2	2.0	4.5	I
4H-SiC	3.26	$8.2 \times 10^{-9}$	10	720 <sup>a</sup> 650 <sup>c</sup>	2.0	2.0	4.5	I
6H-SiC	3.0	$2.3 \times 10^{-6}$	9.7	370 <sup>a</sup> 50 <sup>c</sup>	2.4	2.0	4.5	I
Diamond	5.45	$1.6 \times 10^{-27}$	5.5	1900	5.6	2.7	20	I
BN	6.0	$1.5 \times 10^{-31}$	7.1	5	10	1.0*	13	I
AlN	6.1	$\sim 10^{-31}$	8.7	1100	11.7	1.8	2.5	D

Notes:  $E_g$  is the energy bandgap $n_i$  is the intrinsic carrier concentration $\epsilon_r$  is the relative permittivity $\mu_n$  is the electron mobility $E_c$  is the critical avalanche electric field $v_{sat}$  is the electron saturation velocity $\lambda$  is the thermal conductivity $a$  — mobility along a-axis,  $c$  — mobility along c axis, \*— estimate.

In this chapter, the figures of merit for power switching SiC BJTs will be first briefly reviewed to demonstrate the potential performance. Then, the basic physics of operation and key device design parameters of power bipolar transistors will be presented. Recent experimental highlights on high-voltage switching and high-frequency amplifying 4H-SiC BJTs are summarized. Finally, the future trend in device development and outstanding material and processing issues that need to be overcome for bipolar transistor commercialization will be discussed.

## 2. Figures of Merit

To quantify the potential performance enhancement possible with SiC, several unipolar and bipolar figures of merit have been proposed.<sup>3-7</sup> Bipolar transistors, such as BJT, IGBT and HBT, need to use bipolar figures of merit.<sup>5,6</sup> Among bipolar transistors, we can classify them into two groups, those with odd number and those with even number of junctions. The BJT has an even number of junctions and hence its on-state voltage can be minimized through cancellation of junction voltages when it is in saturation. In this case, SiC clearly excels over Si over all switching frequencies and the power dissipation is clearly smaller in SiC transistors, as shown in Table 2. By contrast, the Insulated-Gate Bipolar Transistor (IGBT), which is the dominant silicon power transistor structure, has an odd number of junctions in its structure and its forward drop cannot be reduced to less than a diode drop.<sup>2</sup> Since SiC has a large diode turn-on voltage due to its larger bandgap, its conduction loss cannot be less than the silicon device at low to medium current density and only yields a lower total power loss when the switching frequency exceeds a certain frequency,  $f_{\min}$ .<sup>5,6</sup> This  $f_{\min}$ , at which the conduction loss is equal to the switching loss (at 50% duty cycle), has been considered as the bipolar figure of merit, and, in the case of a 1000V IGBT, is about 20kHz for SiC when compared to silicon.<sup>5,6,12</sup> Similarly, this bipolar figure of merit can be applied to thyristors. However, no figure of merit applicable to any bipolar heterojunction transistor structure has been proposed.

Table 2 Comparisons of bipolar figures of merit applied to the power npn BJT  
(calculated at  $J_F = 100 \text{ A/cm}^2$ ,  $BV = 1000\text{V}$ ,  $\beta = 10$ )<sup>6,12</sup>

Name	$N_D$ ( $\text{cm}^{-3}$ )	$W_{pp}$ ( $\mu\text{m}$ )	$V_F$ (V)	$J_{OFF}$ ( $\text{A/cm}^2$ )	$t_S$ ( $\mu\text{s}$ )	$t_f$ ( $\mu\text{s}$ )	$E_{OFF}$ ( $\text{mJ/cm}^2$ )	$P_1$ ( $\text{kW/cm}^2$ )	$P_{100}$ ( $\text{kW/cm}^2$ )
Si	$1.3 \times 10^{14}$	100	22	$2.0 \times 10^{-5}$	1.07	4.4	49	1.15	6
Ge	$4.4 \times 10^{13}$	200	50	$6.8 \times 10^{-2}$	1.0	3.4	41	2.49	6.5
3C-SiC	$3.8 \times 10^{15}$	16.7	0.24	$2.0 \times 10^{-15}$	1.16	5.7	60	0.072	6
6H-SiC	$2.6 \times 10^{16}$	8.33	0.19	$2.8 \times 10^{-21}$	0.88	1.6	17	0.027	1.7
4H-SiC	$1.1 \times 10^{16}$	10	0.18	$1.2 \times 10^{-24}$	0.91	2.1	22	0.031	2.2
Diamond	$1.2 \times 10^{17}$	2.3	0.12	$5.5 \times 10^{-44}$	0.78	$6 \times 10^{-3}$	0.05	$6 \times 10^{-3}$	$6.7 \times 10^{-3}$

Notes:  $N_D$  is the drift layer doping concentration

$W_{pp}$  is the depletion layer width at breakdown

$V_F$  is the forward voltage drop at  $100\text{A/cm}^2$

$J_{OFF}$  is the leakage current density

$t_S$  is the storage time during turn-off

$t_f$  is the fall time during turn-off

$E_{OFF}$  is the total energy dissipated during one turn-off cycle

$P_1$  and  $P_{100}$  is the power density dissipated at a switching frequency of 1 and 100 kHz.

Besides device type, npn BJTs are chosen over pnp counterparts in silicon. The reason for this is the higher electron mobility and lifetimes, resulting in higher current gain. On the other hand, the higher impact ionization of electrons leads to a poorer SOA or ruggedness. In SiC, the electron also has a higher mobility but has a lower impact ionization capability than holes. Consequently, npn BJTs are expected to be superior over pnp BJTs in all aspects.

As mentioned earlier, we have approximated the electron and hole ionization coefficients using a power law. Then, we obtain the ideal breakdown voltage ( $BV_{pp}$ ) and depletion layer width at breakdown ( $W_{pp}$ ) as a function of background doping, as shown in Fig. 2 for (0001) 6H- and 4H-SiC. The expressions for 4H-SiC and 6H-SiC are listed below:

$$W_{pp}(300K) = 7.151 \times 10^{10} \times N_D^{-6/7} \quad \text{for 4H-SiC} \quad (1)$$

$$W_{pp}(300K) = 1.74 \times 10^{11} \times N_D^{-7/8} \quad \text{for 6H-SiC} \quad (1)$$

$$BV_{pp}(300K) = 4.766 \times 10^{14} \times N_D^{-5/7} \quad \text{for 4H-SiC} \quad (2)$$

$$BV_{pp}(300K) = 2.81 \times 10^{15} \times N_D^{-3/4} \quad \text{for 6H-SiC} \quad (2)$$

where  $BV_{pp}$ ,  $N_D$ , and  $W_{pp}$  are expressed in volts,  $\text{cm}^{-3}$  and  $\text{cm}$ , respectively.

These analytical calculations have been corroborated well with numerical simulations and experimental results. It can be seen that, for the same background doping and along the c-axis, 6H-SiC has a 10-15% higher BV than 4H-SiC, despite the larger bandgap of the latter. Also, the effective avalanche field estimated for doping concentration of  $10^{15}$  to  $10^{17} \text{ cm}^{-3}$  is the range  $2.5$  to  $5 \times 10^6 \text{ V/cm}$ , close to the experimental value of  $2\text{-}3 \times 10^6 \text{ V/cm}$ . Also, like silicon, the breakdown voltage of SiC has been established to increase when temperature increases, or, in other words, has been shown to have a positive temperature coefficient.<sup>14</sup> Recent measurements of mesa p+n diodes indicated that the breakdown fields along various crystal orientations in 4H-SiC, 6H-SiC and 3C-SiC is about 75% that of 4H-SiC (0001) (Fig. 3).<sup>15</sup>

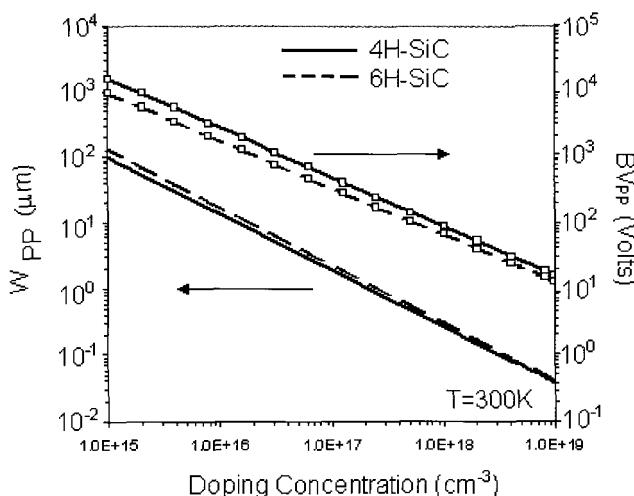


Fig. 2 Breakdown voltage of parallel-plane, one-sided abrupt junction ( $BV_{pp}$ ) and its depletion layer width at breakdown ( $W_{pp}$ ) for 6H- and 4H-SiC at 300K.

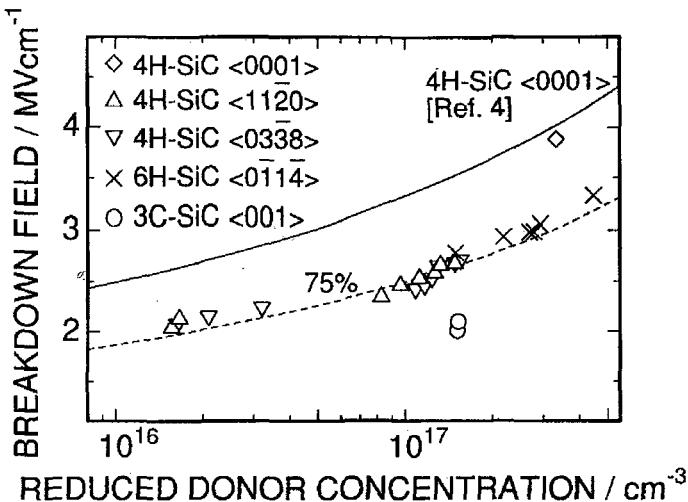


Fig. 3 Breakdown field along various crystal orientations in three SiC polytypes at room temperature.<sup>19</sup>

### 3. Power Bipolar Transistors

In general, power transistors can be classified into unipolar and bipolar transistor families. Within each family, they can be further divided into current- and voltage-controlled devices. The MOSFET and JFET are unipolar transistors that usually use voltage for control. On the other hand, the bipolar junction transistor and the IGBT are bipolar transistors, with the former using current for control and the latter using voltage control. A voltage-controlled transistor is often preferred for ease of integrating IC-based gate driving circuitry. A review of recent advances in the SiC unipolar transistors, such as MOSFETs and JFETs, can be found in another chapter of this book.

#### 3.1 Bipolar junction transistor (BJT)

In operation, as a high-voltage power switch, the BJT uses base current to controllably change from a high-resistance off condition to a low on-resistance conductive condition and vice versa. The lightly doped collector layer also causes the output I-V characteristics to have a “kink” (known as quasi-saturation) at high current, low to moderate collector bias conditions. As a high-frequency, small-signal amplifier, it is biased at the quiescent point with a dc base current and an additional high-frequency small-signal base current is applied as the input signal of the amplifier, resulting in an output small-signal collector current, which is superimposed on top of the dc collector current.

Since the power switching BJT is designed to support high voltages, a thick, lightly doped collector region, and a thin, moderately doped base region, is used, so as to maintain reasonable current gain in the on state while providing high voltage blocking in the off state.<sup>1</sup> Also, the base thickness and doping must be sufficient to prevent punch-through breakdown. The schematic cross-section of the basic high-voltage power Bipolar Junction Transistor (BJT) is shown in Fig. 4.<sup>1</sup> The details of the basic operation of the high-voltage power BJT can be found in.<sup>1,2,16</sup> By contrast, the power amplifying BJT is

designed to have high current gain and linearity over a broad range of frequencies but low (<300V) blocking voltages.

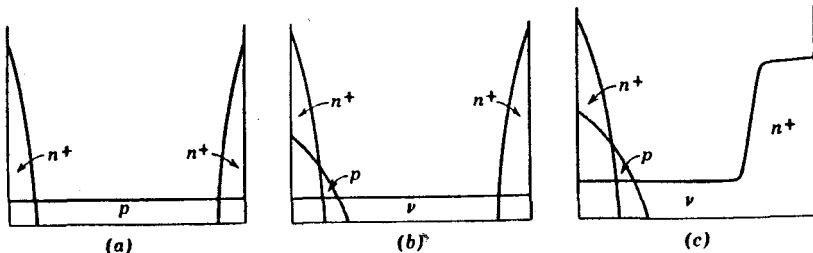


Fig. 4 Three different doping profiles of a high-voltage power BJT: (a) Frontside diffused emitter and backside diffused collector into a p-type substrate, (b) double diffused emitter and base on the frontside with backside diffused collector into a lightly doped n-type substrate, and (c) double diffused emitter and base on the frontside into a lightly doped n-type epi on n<sup>+</sup> substrate.

The breakdown voltages of bipolar transistor structures are generally lower than those of pn junctions due to current gain and are dependent on minority carrier diffusion length in the base. In addition, Fig. 5 shows the breakdown voltage of open base transistor in (0001) 4H-SiC for several minority carrier diffusion lengths. It can be shown that the open-base bipolar transistor breakdown voltage ( $BV_{CEO}$ ) design is related to the open-emitter BJT breakdown voltage ( $BV_{CBO}$ ) through

$$BV_{CBO}/BV_{CEO} = (\beta + 1)^{1/n} \quad (3)$$

where  $\beta$  is the common-emitter current gain,  $n$  is 4 for npn and 6 for pnp transistors in silicon.<sup>1,2</sup> The  $n$  factor depends on the multiplicative factor ( $M$ ) and hence the electron and hole ionization coefficients. For 4H-SiC, using the experimentally extracted impact ionization coefficients, we have found that the  $n$  factor for npn and pnp transistors in both 6H-SiC and 4H-SiC.<sup>9,17,18</sup> In Fig. 6, the common-emitter current gain,  $\beta$ , is plotted as a function of the ratio  $BV_{CBO}/BV_{CEO}$  for both npn and pnp in (0001)-oriented 4H-SiC. N-factors of are extracted for npn and pnp BJTs respectively and it can be clearly seen that the npn is more robust or rugged than the pnp, opposite to the trend observed for Si BJTs.<sup>1,2</sup> Similar trends have been determined for (11-20) 4H-SiC and (0001) 6H-SiC.<sup>18</sup> For planar devices with two- and three-dimensional junction curvatures, proper termination must also be designed and processed to minimize the effect of junction curvatures.<sup>1,2</sup>

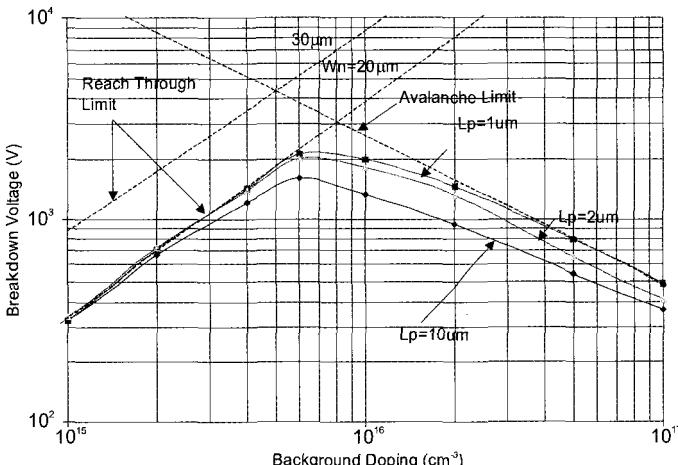
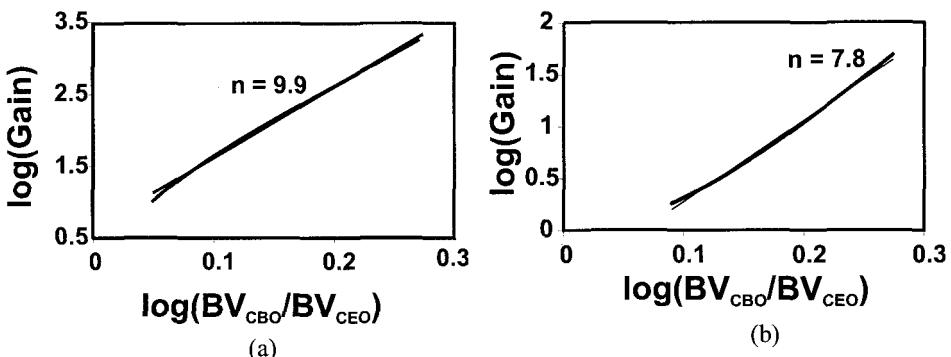


Fig. 5 Breakdown voltage of open base bipolar transistors in (0001) 4H-SiC.

Fig. 6 Extraction of n factor for (0001) 4H-SiC npn and pnp BJTs.<sup>18</sup>

The major distinguishing feature of the forward I-V characteristics of the high-voltage power BJT is the quasi-saturation region, which is a direct consequence of the lightly doped collector and is not present in low-voltage BJT's. This region reduces the output current and slows down the switching speed. The output I-V characteristics of this BJT is shown in Fig. 7 and it can be noted that the slope ( $dI/dV$ ) is proportional to the reciprocal of the collector region resistance.<sup>1</sup> At high current densities, part or the entire n<sup>-</sup> collector region is flooded with a e-h<sup>+</sup> plasma and is conductivity modulated and hence the voltage drop across it decreases.<sup>2</sup> Once the n<sup>-</sup> region is no longer highly resistive, the conventional saturation region commences and the base collector junction is forward biased, leading to a junction voltage cancellation and a low forward voltage drop. However, with increasing level of carrier injection, the recombination rate in the base/collector region increases, decreasing the current gain and requiring a larger base current drive. Other second order effects, such as emitter crowding, also need to be considered so as to avoid current non-uniformities and excessive local heating. Usually, an interdigitated emitter/base finger layout is adopted to maximize the emitter periphery per unit area and the emitter finger width is minimized. Another effect, known as the Kirk effect, shifts the peak electric field from the p base/n<sup>-</sup> collector junction to the n<sup>-</sup>/n<sup>+</sup> junction at high collector bias when the collector current density increases. Both of these

effects tend to lower the current gain and degrade the conduction performance of the BJT.

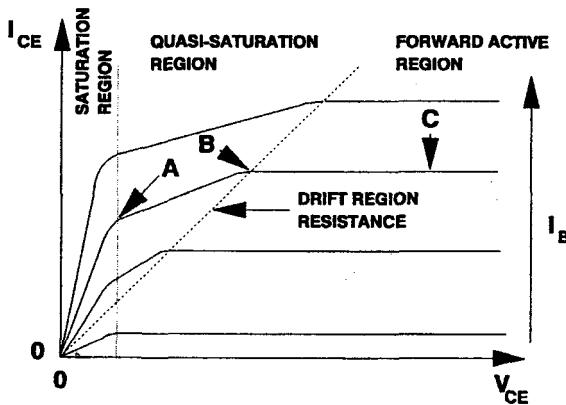


Fig. 7 Output I-V characteristics of a high-voltage power BJT, showing the quasi-saturation region.<sup>2</sup>

The key on-state device parameter of the high-voltage power BJT is the specific on-resistance ( $R_{on,sp}$ ), which is determined by the on-state resistance times the active area. Previously, several attempts have been made to relate this parameter to the device parameters, but we have found that refinements and/or corrections are needed to obtain an  $R_{on,sp}$  expression which is valid for high-level injection condition.<sup>2,12,16,19,20</sup> Specifically,

$$R_{on,sp} = V_{CE,sat} / J_C \quad (4)$$

$$\text{where } V_{CE,sat} = \frac{kT}{q} \ln \left( \frac{J_C W_B N_{AB}}{qD_{nB} n_i^2} \right) - \frac{2kT}{q} \ln \frac{N_{Dv}}{n_i} \quad (5)$$

where

$W_B$  Base width

$N_{AB}$  Acceptor doping concentration of the base

$D_{nB}$  Diffusion constant of electrons in the base

$N_{Dv}$  Donor doping concentration of the lightly doped collector

Using one dimensional numerical analysis, the forward voltage drop as a function of blocking voltage has been calculated for 4H-SiC BJTs up to 10kV and is shown in Fig. 8.<sup>12</sup> This intrinsic parameter has been estimated to be quite small and less than 0.25V for optimized SiC BJTs. It should be noted that any parasitic emitter resistance (such as emitter contact resistance and emitter probe or packaging wire resistance) leads to a further increase in the measured specific on-resistance.

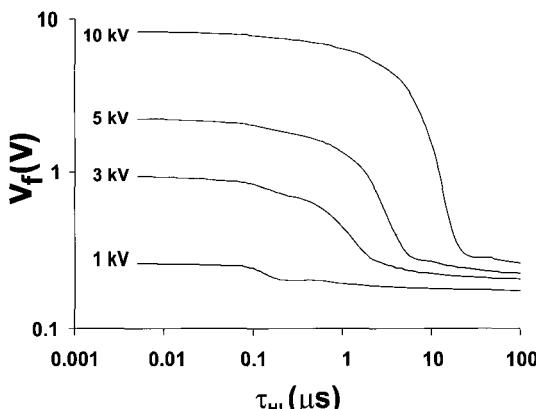


Fig. 8 Estimated forward voltage drop ( $V_f$ ) vs. high level lifetime in the drift region for 1-10kV 4H-SiC BJTs.<sup>12</sup>

The BJT can only be switched on by applying a base current but can be turned off either by removing the base current ( $I_B \rightarrow 0$ ) or by reversing the base current flow ( $I_B < 0$ ), as shown in Fig. 9. In the turn-on phase, the applied base current introduces excess majority carriers (holes for npn) into the base, causing minority carriers (electrons for npn) injection from the emitter. The collector voltage collapses from the blocking voltage to the on-state saturation voltage in several stages, the slowest of which is the time it takes transversing through the quasi-saturation region. Consequently, the rate of excess carrier built-up in the lightly doped collector critically determines the turn-on time,  $t_{ON}$ . The dynamics of the turn-on transient can be estimated using a charge-controlled approach.<sup>2</sup> The collector-to-emitter voltage,  $V_{CE}$ , can be shown to vary as

$$V_{CE}(t) = (J_C / q \mu_n N_D) \{ W_D - 2(D_n \tau_D J_{pC} / J_C)^{1/2} [1 - \exp(-t/\tau_D)] \} \quad (6)$$

where  $J_C$  is the collector current density,  $\mu_n$  the electron mobility,  $D_n$  the electron diffusion constant,  $N_D$  are the doping concentration and thickness of the lightly doped collector,  $\tau_D$  the minority carrier recombination lifetime and  $J_{pC}$  the steady-state base current for collector recombination.<sup>2</sup> At the end of the turn-on phase, the lightly doped collector has become an extended base region, with excess carrier concentrations increased well above the background doping concentration and yet maintaining quasi-space charge neutrality.

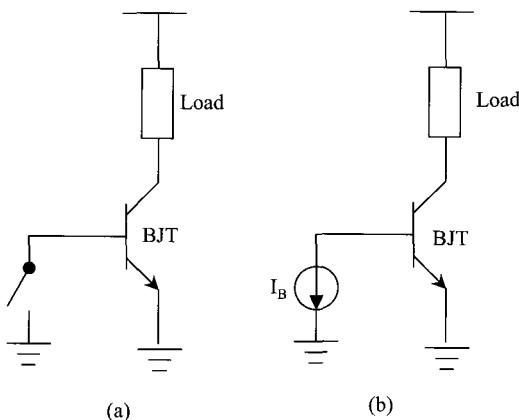
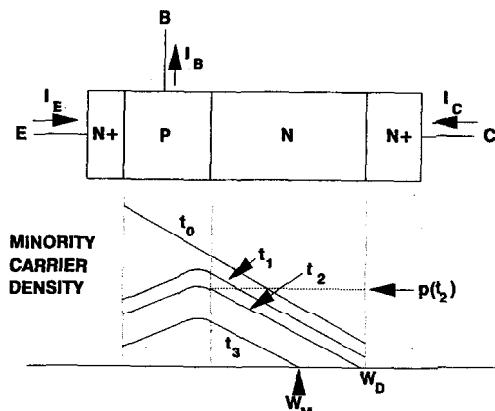


Fig. 9 Circuit schematics showing two modes of BJT turn-off: (a) Open base and (b) Reverse base turn-offs.

During turn-off, the BJT undergoes carrier removal also in several stages.<sup>2</sup> In addition, if an open base turn-off takes place, the excess carriers are removed with recombination. However, if a reverse base current is used, some of the excess carriers can be extracted from the device via the base terminal and their removal rate and hence turn-off time,  $t_{\text{off}}$ , are dependent on the magnitude of the reverse base current. The turn-off process can be divided into the two phases - the initial storage phase, followed by a decay phase. In the storage phase, the collector current remains constant while the excess carriers are removed from the modulated collector. The storage time,  $t_S$ , can be estimated, again using the charge-control approach, to be

$$t_S = J_{pC} \tau_D / J_{BR} - 1/4 (J_C / J_{BR}) (W_D^2 / (q D_n)) \quad (7)$$

where  $J_{BR}$  is the reverse base current density and it can be readily observed that  $t_S$  is proportional to  $\tau_D$  and to  $J_{BR}^{-1/2}$ .<sup>2</sup> When the carrier concentration in the collector starts to fall below the background doping level, the decay phase commences, with at first gradual and then more rapid decrease in the collector current. Both the base and collector current fall to less than 10% of the initial value when the decay phase terminates. The actual rate of voltage increase across the BJT is also dependent on the nature of the load, more rapidly for an inductive load than a resistive load. Due to the 10x reduced collector drift region to support the blocking voltage, the SiC BJT has less stored charge and can have a faster switching frequency than an equivalent Si BJT.

Fig. 10 Carrier profile in the lightly doped collector during BJT turn-off.<sup>2</sup>

Significant advances have been reported on high-voltage npn BJTs over the last few years. Table 3 summarizes the recent experimental results on bipolar power transistor structures in 4H-SiC.<sup>21-33</sup> In terms of device implementation, due to limited dopant diffusion, there are basically two approaches to implement SiC BJTs, with the emitter region either grown epitaxially or created with ion implantation (Fig. 11). In the epi emitter approach, the emitter and base regions are epitaxially grown and the base contacts are made by trench etching through the emitter region and p+ implantation. By contrast, the implanted emitter BJTs utilizes an epitaxial grown p+ contact layer, which is subsequently patterned and etched into the p-base layer so as to define the emitter areas. The emitter implant dosage and energy determines the resulting base width, offering processing flexibility. The main drawback of epi emitter BJTs is the base width determined with epi growth, which is inflexible, whereas that of implanted emitter BJTs is the incomplete removal of lattice damage from implantation, resulting in low base lifetime and hence current gain.

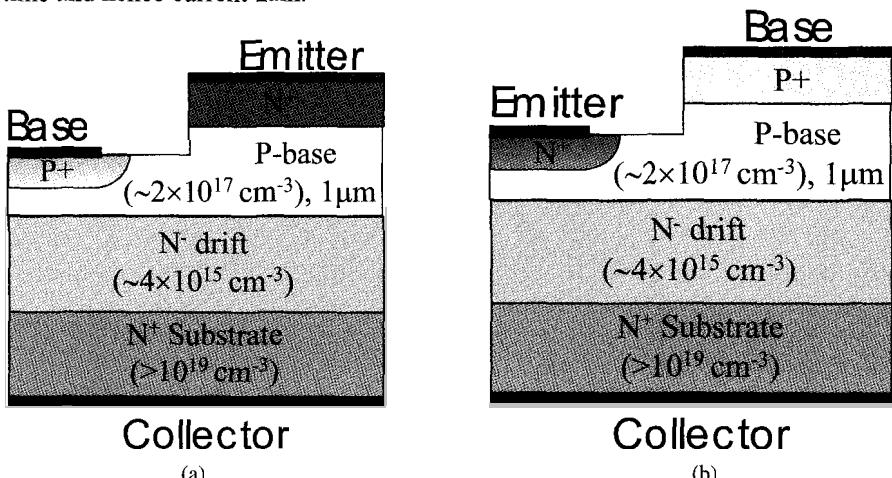


Fig. 11 Schematic cross-sections of (a) epitaxial emitter and (b) implanted emitter SiC BJTs.

Table 3 A list of SiC power bipolar transistors that have been experimentally demonstrated.

Device Type	Power Rating	Features	Researcher	Reference
BJT	60V	Implanted Emitter	RPI, 2000	[22]
	1800V, 3.8A	Epi Emitter, $10.8m\Omega\text{-cm}^2$	Cree, 2000	[23,25]
	900V	Epi Emitter	Rutgers, 2000	[21]
	500V	Implanted Emitter	RPI, 2001	[24,26]
	3200V	Epi Emitter, $78m\Omega\text{-cm}^2$ , $\beta \sim 15$	Purdue, 2002	[28]
	1300V, 17A	Epi Emitter, $8m\Omega\text{-cm}^2$ , $\beta \sim 11$	Cree/RPI, 2003	[29]
	1750V, 5A	Epi Emitter, $8.4m\Omega\text{-cm}^2$ , $\beta \sim 24$	Rutgers, 2003	[30]
	1400V, 20A	Epi Emitter, $5.4m\Omega\text{-cm}^2$ , $\beta \sim 14, V_F \sim 1.2V$	Cree/RPI, 2004	[31]
	1000V, 30A	Epi Emitter, $6m\Omega\text{-cm}^2$ , $\beta \sim 40$ , $\beta_{peak} \sim 120$	Cree/RPI, 2004	[32]
	9000V	Epi Emitter,	Rutgers, 2004	[44]
	4000V	Epi Emitter, $56m\Omega\text{-cm}^2$	RPI/Cree, 2005	[33]
	1600V, 40A	Epi Emitter, $4.5m\Omega\text{-cm}^2$ , $\beta \sim 40$	Cree/RPI, 2005	[45]
Darlington	1100V	Epi Emitter, $\beta \sim 64$	KTH/Acreo, 2005	[46]
	200-400V	Implanted Emitter, $\beta \sim 80$	RPI, 2002	[39]
	200-400V	Implanted Emitter, $\beta \sim 450, V_F \sim 7V$	RPI, 2003	[40]
	1400V, 20A	Epi Emitter, $\beta \sim 150, V_F \sim 4.3V$	Cree/RPI, 2004	[31]
	1000V, 30A	Epi Emitter, $\beta \sim 2400, V_F \sim 4V$	Cree/RPI, 2004	[32]

One of the highest reported BVs of epi emitter 4H-SiC BJTs is 3.2kV.<sup>19</sup> Two sizes (0.0072 and 1.05 mm<sup>2</sup>) of BJTs were fabricated. At room temperature, large devices show  $R_{on,sp}$  of 78mΩ·cm<sup>2</sup> and a β of 15 whereas the small devices have  $R_{on,sp}$  of 28mΩ·cm<sup>2</sup> and a β of 20. However, we have recently fabricated and characterized 4H-SiC BJTs with  $BV_{CEO}$  of 4.6kV and  $BV_{CEO}$  of 4kV, as shown in Fig. 12, with a collector region which is thinner and heavily doped than the 3.2kV devices.<sup>33</sup> The reason of the higher BV is due to a more optimal termination structure, which is a three-zone implanted JTE, and has been previously used for demonstration of 8kV 4H-SiC junction rectifiers.<sup>34</sup> We have measured a specific on-resistance of 56mΩ·cm<sup>2</sup> at room temperature and The largest current reported is a 1.6kV, 40A epitaxial emitter BJT, the forward conduction and blocking I-V characteristics of which are shown in Fig. 13.<sup>45</sup> A specific on-

resistance of  $4.5\text{m}\Omega\cdot\text{cm}^2$  has been obtained. Also, a peak current gain of 40 has been measured and shown to be insensitive to collector current and decrease with increasing temperature. The decreasing current gain with temperature has been correlated with increasing acceptor doping in the base and this unusual trend actually helps prevent thermal runaway and facilitates device paralleling. With process and design optimization, a current gain as high as 120 has been achieved for epi-emitter BJT test structures (Fig. 14).<sup>32</sup>

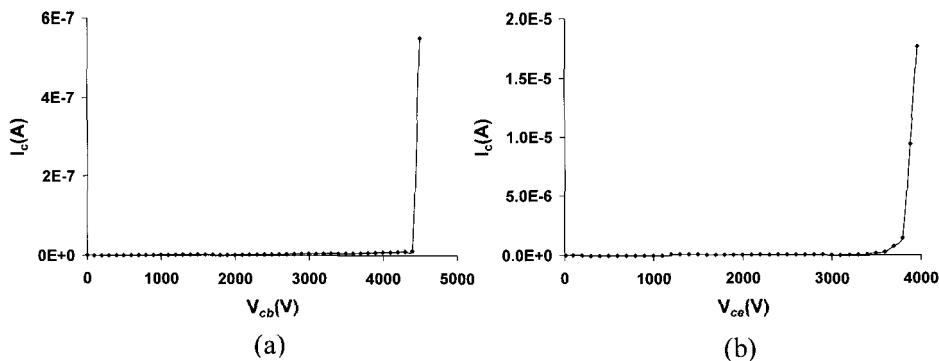


Fig. 12 (a)  $\text{BV}_{\text{CBO}}$  and (b)  $\text{BV}_{\text{CEO}}$  of a 4kV epi emitter BJT.<sup>33</sup>

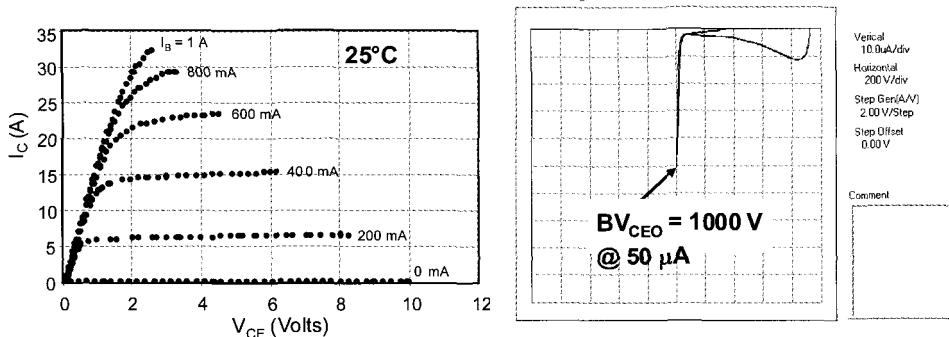


Fig. 13 Forward conduction and blocking I-V characteristics of a 30A, 1kV 4H-SiC epitaxial emitter BJT with an active area of  $3.4 \times 3.4 \text{mm}^2$  [32].

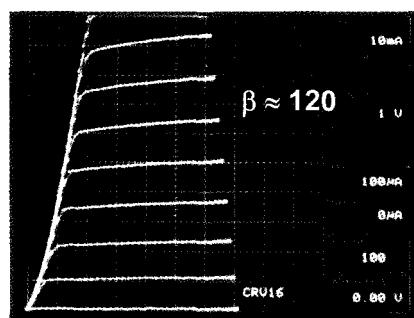


Fig. 14 Output characteristics of a test BJT showing a current gain of 120.<sup>32</sup>

The highest  $BV_{CEO}$  of implanted emitter BJTs is  $\sim 500V$  and is found to be  $\sim 70\%$  of  $BV_{CBO}$ .<sup>24,26</sup> However, the current gain is only about 6. We have also tried different emitter species (phosphorus, nitrogen and arsenic) and annealing temperature (1200 vs. 1600°C) and have found that phosphorus annealed at 1600°C to be most optimal. The specific on-resistance of high-voltage SiC BJTs vs. breakdown voltage is shown in Fig. 15.

It is worth pointing out that all the experimentally demonstrated 4H-SiC BJTs have specific on-resistances higher than the 4H-SiC *unipolar* limit. The reason for this is the lack of conductivity modulation in the collector and non-uniform current conduction. We have examined and analyzed the effect of minority carrier lifetime in the base and collector regions as well as surface recombination velocity in the base in detail.<sup>33</sup> The electron and hole concentrations in the collector region for a 4kV SiC BJT with minority carrier lifetimes of 0.1 and 50μs are shown in Figs. 16 and 17 respectively. While the minority carrier concentration in the collector region of the former does not rise above the background majority concentration, both hole and electron concentrations in the latter exceed significantly that of the background doping, hence reducing the resistance of the collector region. The corresponding specific on-resistances of these two BJTs are  $m\Omega\cdot cm^2$  and  $m\Omega\cdot cm^2$  respectively whereas the unipolar specific on-resistance of the collector region only is  $m\Omega\cdot cm^2$ , clearly showing that conductivity modulation is necessary to lower the  $R_{on,sp}$  below the 4H-SiC unipolar limit.

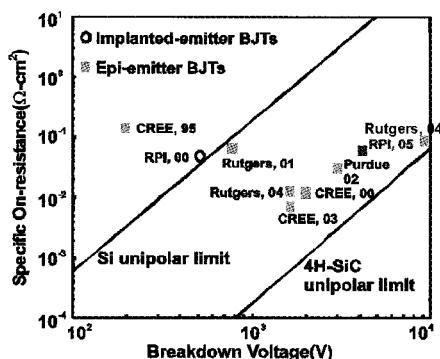


Fig. 15 Specific on-resistance of high-voltage SiC BJTs and other power bipolar transistors vs. breakdown voltage.

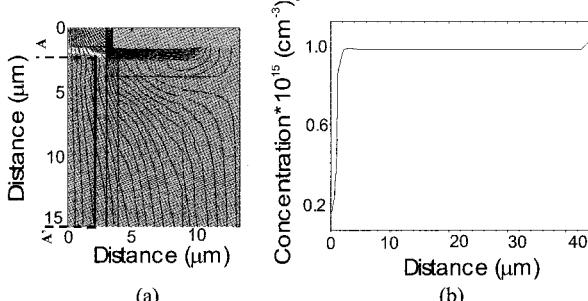


Fig. 16 (a) Electron concentration, current distribution and (b) carrier concentration (along AA') in the drift region at  $100A/cm^2$  ( $\tau_{no}=0.5\mu s$ ,  $\tau_{po}=0.05\mu s$ ,  $S=1\times 10^6\text{ cm/s}$ ,  $27\mu m$  pitch)

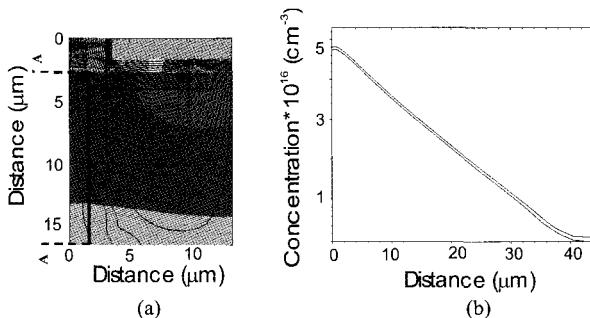


Fig. 17 (a) Electron concentration, current distribution and (b) carrier concentration (along AA') in the drift region at  $100 \text{ A/cm}^2$  ( $\tau_{\text{no}}=50 \mu\text{s}$ ,  $\tau_{\text{po}}=5 \mu\text{s}$ ,  $S=1 \times 10^6 \text{ cm/s}$ ,  $27 \mu\text{m}$  pitch)

Due to the 10x reduced collector drift region to support the blocking voltage, the SiC BJT has less stored charge and can have a switching frequency up to at least 200 kHz. Turn-on rise time of 365ns and turn-off fall time of 144ns were observed at 200°C for 1.3kV, 17A epi emitter BJTs (shown in Fig. 18).<sup>29</sup> We have also found that a turn-on time of 0.4 μs for 4kV epi-emitter BJTs but a long open-base turn-off time of 8μs.<sup>33</sup> By contrast, we have measured a typical turn-off less than 0.2μs on implanted-emitter BJTs, with references<sup>24,26</sup>, indicating the unrecovered implant damage helping to remove excess carriers. The turn-off time has been found to increase with temperature, similar to silicon devices, due to increased recombination lifetime.

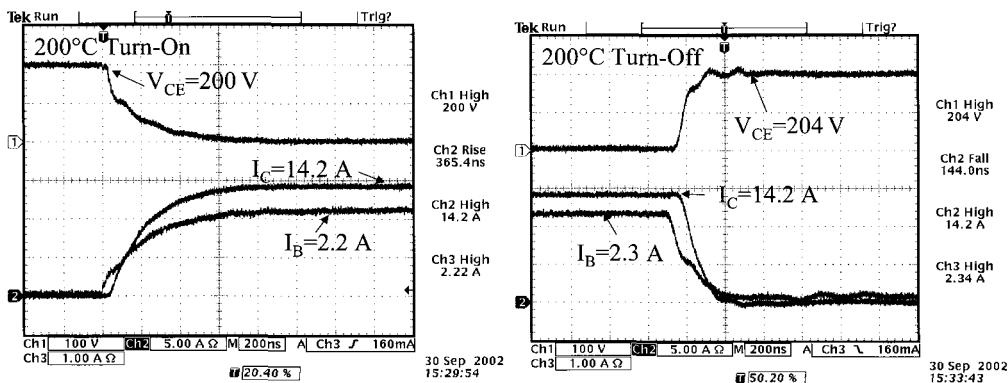


Fig. 18 Switching characteristics of a 1.3kV epi-emitter 4H-SiC BJT.<sup>29</sup>

When the BJT is designed and used as a high-frequency single-stage amplifier, the blocking voltage is usually low (<100V). So, the lightly doped collector region is thin (<10μm) and moderately doped ( $>10^{15} \text{ cm}^{-3}$ ) and the quasi-saturation effect observed for high-voltage power switching BJTs is absent. The power gain, G, is one of the most important design considerations in the design of a microwave power transistor. It is basically determined by the  $f_{\text{MAX}}$ , the maximum frequency of oscillation. Under small signal conditions, the highest power gain a transistor can achieve at frequency  $f_0$  is given by

$$G \approx \left( \frac{f_{MAX}}{f_0} \right)^2 \quad (8)$$

However, the above gain cannot be normally obtained due to parasitics. For large-signal Class C operation, the power gain is further reduced by the current and voltage saturation of the transistor. Therefore it is not unusual for a power transistor to have gain which is 3 to 4 dB lower than the above relation predicts. Assuming that we need a small signal gain of 12 dB at 400 MHz, the above relation dictates a  $f_{MAX}$  of at least 1.6 GHz.

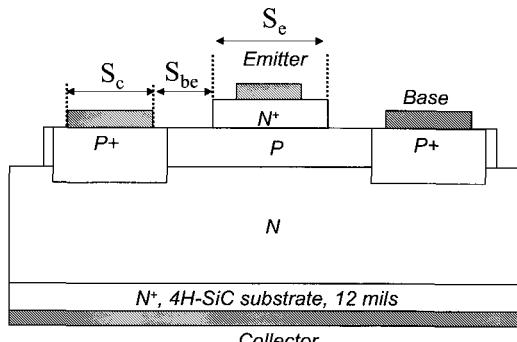


Fig. 19 Schematic cross-section of a BJT, showing the critical design parameters for rf transistors.

In order to design a transistor with a 1.6 GHz intrinsic  $f_{MAX}$ , we should examine the factors, which affect the  $f_{MAX}$  of the transistor. A simplified cross-section of the epitaxial emitter structure is shown in Fig. 19. The stripe geometry has been assumed. All microwave transistors are fabricated more or less with this geometry. The intrinsic part, directly under the emitter, is the active part of the transistor. The extrinsic part, which connects the intrinsic base (under the emitter) to the base contacts, is the parasitic part of the transistor. The effects of these two parts on the transistor  $f_{MAX}$  can be evaluated by the following formula:

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi \left( r_{con} C_t + \frac{r_{be} C_{be}}{2} + r_b C_i \right)}} \quad (9)$$

where, the various terms are defined below:

- $f_T$ : Current gain bandwidth of the transistor
- $r_{con}$ : Base contact resistance
- $r_{be}$ : Extrinsic base resistance
- $r_b$ : Intrinsic base resistance
- $C_t$ : Total base-collector capacitance
- $C_{be}$ : Collector base capacitance due to the extrinsic part of the base
- $C_i$ : Collector base capacitance due to the intrinsic part of the base

For interdigitated transistor structures, the device parameters in the above formula can be further expressed in terms of the transistor structure parameters.<sup>35</sup> Thus we have,

$$\begin{aligned}
 r_{con} C_t &= \frac{1}{2} R_c C_{cb} (S_c + 2S_{be} + S_e) \\
 r_{be} C_{be} &= \frac{1}{2} R_{be} C_{cb} S_{be}^2 \\
 r_b C_i &= \left( \frac{R_{be} S_{be}}{2} + \frac{R_b S_e}{12} \right) C_{cb} S_c
 \end{aligned} \tag{10-12}$$

where,

- $R_c$ : Base contact resistance per unit length in ohm-cm
- $R_b$ : Intrinsic base sheet resistance in ohm/sq
- $R_{be}$ : Extrinsic base sheet resistance in ohm/sq
- $C_{cb}$ : Collector Base capacitance in F/cm<sup>2</sup>
- $S_e$ : Emitter width (shown in Fig. 19)
- $S_c$ : Base contact width (shown in Fig. 19)
- $S_{be}$ : Spacing between emitter mesa and the base contact (shown in Fig. 19)

Assuming  $R_c \sim 1$  ohm-cm,  $R_b = R_{be} = 100,000$  ohm per sq. (for  $N_A = 2 \times 10^{18}$  cm<sup>-3</sup>),  $f_T = 2$  GHz,  $S_c = 2$   $\mu$ m, and  $W_c$ , depleted collector thickness of 2  $\mu$ m ( $C_{cb} = \epsilon_{SiC}/W_c$ ), the  $f_{MAX}$  was calculated for various values of  $S_e$  and  $S_{be}$ . The results are summarized in Fig. 20. Based on these calculations, it may be concluded that the  $f_{MAX}$  is limited by the extrinsic base resistance and not by the emitter width to the first order. Therefore we have chosen the emitter width,  $S_e = 2.5$   $\mu$ m for ease of fabrication. The nominal design uses  $S_{be} = 0.5$   $\mu$ m to assure that we get  $f_{MAX} > 1.6$  GHz.

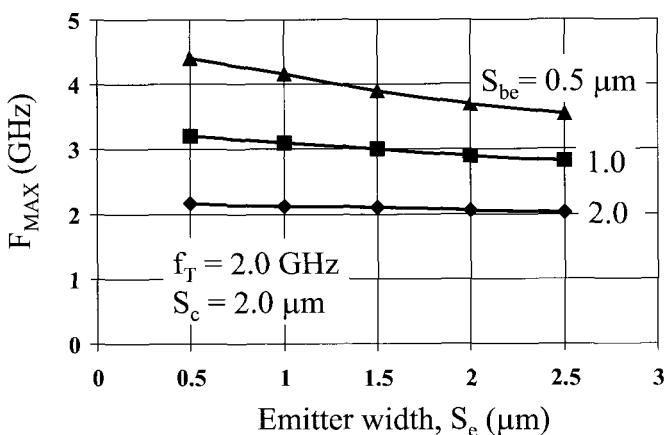


Fig. 20 Calculated  $f_{MAX}$  vs. emitter stripe width,  $S_e$ , with a variable spacing between emitter mesa and the base contact,  $S_{be}$ .

The cut-off frequency,  $f_T$ , may be estimated as follows:

$$\tau_{ec} = \frac{1}{2\pi f_T} = \frac{W_b^2}{2D_n} + \frac{W_C}{2\nu_s} + \frac{kT/q}{I_C} (C_{BE} + C_t) \tag{13}$$

where,

$\tau_{ec}$ :	Total delay between emitter to collector
$W_b$ :	Base thickness (500 – 2000 Å)
$D_n$ :	Diffusion coefficient of electrons in the base ( $1.95 \text{ cm}^2/\text{s}$ at $25^\circ\text{C}$ assuming electron mobility of $75 \text{ cm}^2/\text{V}\cdot\text{s}$ in the base doped at $2 \times 10^{18} \text{ cm}^{-3}$ )
$W_C$ :	Collector thickness (6 $\mu\text{m}$ )
$V_s$ :	Velocity of electrons in the collector ( $1.5 \times 10^7 \text{ cm/s}$ at $25^\circ\text{C}$ )
$I_c$ :	Collector current (50% of the maximum value at a current density of 6000 $\text{A/cm}^2$ )
$C_{BE}$ :	Total base-emitter junction capacitance
$C_t$ :	Total base-collector capacitance

The calculated values of  $f_T$  as a function of  $W_b$  at room temperature and  $250^\circ\text{C}$  junction temperature are shown in Fig. 21. We have chosen a nominal value of  $W_b \sim 1000\text{\AA}$  to provide a  $f_T \sim 2 \text{ GHz}$  at a junction temperature of  $250^\circ\text{C}$ . The collector thickness is chosen to be 6  $\mu\text{m}$  in order to provide a reasonably high  $V_{CEO}$  of around 600 V. It turns out that if a power supply voltage of 300 V is chosen for Class B operation, the output power density in BJT cells is very high. With approximately 50% power added efficiency, about the same amount of power is thermally dissipated. As a result, the junction temperature rises to above  $400^\circ\text{C}$ , which then reduces  $f_T$  and consequently  $f_{MAX}$  and power gain. Therefore, we have chosen a collector supply voltage of 80-100 V to minimize the thermal issues. This then dictates a  $V_{CEO}$  of approximately 200 V (assuming common emitter operation) and a  $V_{CBO}$  of approximately 250-300 V. Thus in future designs, the collector thickness may be reduced to 3  $\mu\text{m}$  resulting in further improvement in  $f_T$ . Although, reduction in collector thickness will increase the base-collector capacitance,  $C_t$ , its overall effect will be to improve both  $f_T$  and  $f_{MAX}$ .

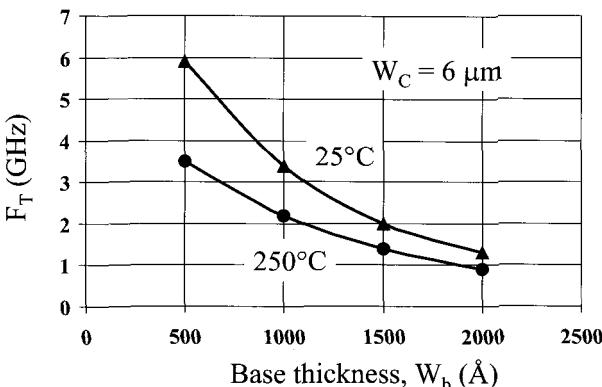


Fig. 21 Calculated values of  $f_T$  vs. base thickness for a rf 4H-SiC BJT.

Fig. 22 shows the I-V characteristics of a single epitaxial emitter cell. A maximum current gain of about 15 is obtained. This current gain is extremely sensitive to the base contact implant spacing from the edge of the emitter mesa (in the present design, it is 0.5  $\mu\text{m}$  as shown in Fig. 19). This indicates that the surface recombination is the limiting factor for current gain in the epitaxial emitter structure. Better passivation is needed to suppress the surface recombination and further improve the current gain. The common emitter breakdown voltage was in excess of 500 V consistent with the 5  $\mu\text{m}$  collector thickness.

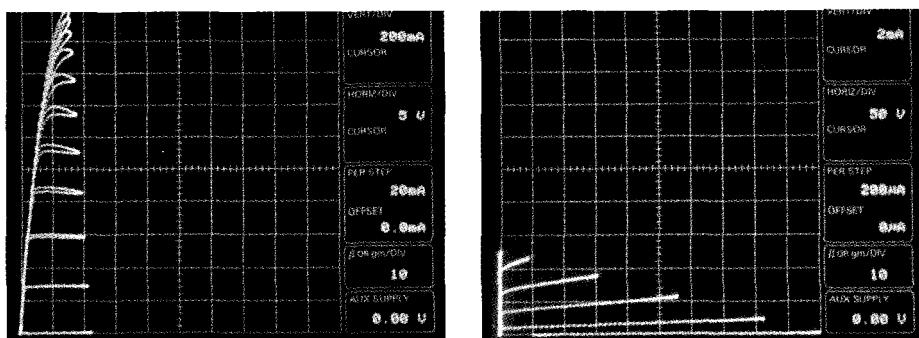


Fig. 22 Common Emitter (CE) I-V characteristics of a single epitaxial emitter BJT cell showing a maximum current of 2 A,  $\beta_{\max} \sim 15$  and a  $BV_{CEO} = 500$  V.

The  $f_T$  of the cell was measured as a function of the collector current with different collector supply voltages (Fig. 23). For  $V_{CC} = 20$  V,  $f_T$  peaks at about 1.5 GHz whereas for  $V_{CC} = 30$  V,  $f_T$  peaks at about 1.3 GHz. This reduction in  $f_T$  with collector voltage is expected as the electron transit delay in the collector depletion width increases with increasing collector bias. The sudden drop in  $f_T$  at high current for  $V_{cc}=30$  V is attributed to a hot spot on the device.

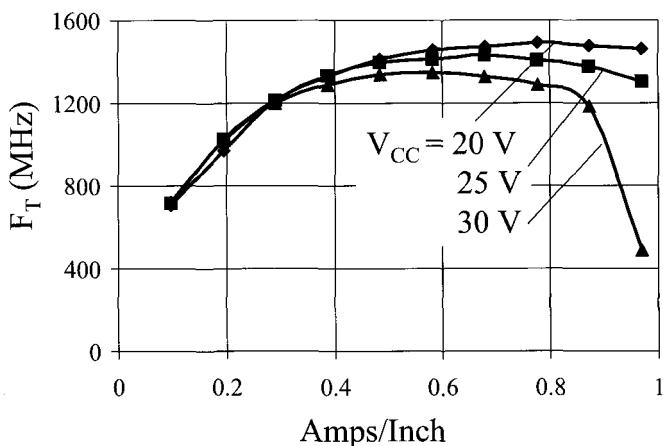


Fig. 23 Measured  $f_T$  as a function of collector current and the collector voltage.

A single cell was measured in common base (CB), class C mode at 425 MHz using a collector supply voltage of 80 V. The pulse width of 100  $\mu$ s with a duty cycle of 10% was used. The single measurement yielded a maximum power of 39.8 W with a power gain of 5.1 dB and a collector efficiency of 57.85% (see Fig. 24). The power gain in class C or class B is expected to be low due to a large input power required to turn-on the input base-emitter junction which has a turn-on voltage of about 3 V due to the wide bandgap of SiC. The output power level is consistent with the power triangle measured under DC conditions [40 W = (160 V x 2 A)/8].

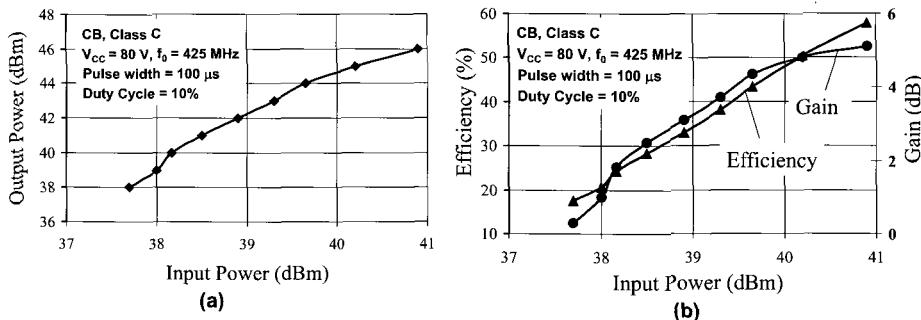


Fig. 24 (a) Output power vs. input power for a single cell in CB mode operated in class C mode at 425 MHz, pulse width 100  $\mu$ s, duty cycle 10%, and  $V_{CC} = 80$  V; (b) Collector efficiency and power gain vs. output power for conditions stated in (a).

A single cell was also measured in common emitter (CE) mode with a collector supply voltage of 80 V in class AB at 425 MHz. The device was biased in class AB mode with a collector bias current of about 50 mA, just enough to overcome the large 3 V turn-on voltage. A 100  $\mu$ s pulse width with 10% duty cycle was used. The results are shown in Fig. 25. A maximum output power of 50 W for a single cell was achieved. This represents an output power density of 47 kW/cm<sup>2</sup> when normalized by the active base area. The power density is more than five times higher than that typically obtained with Si BJTs at this frequency. The peak large-signal power gain was 9.6 dB. The collector efficiency at the power output of 50 W was 51% with a power gain of 9.3 dB.

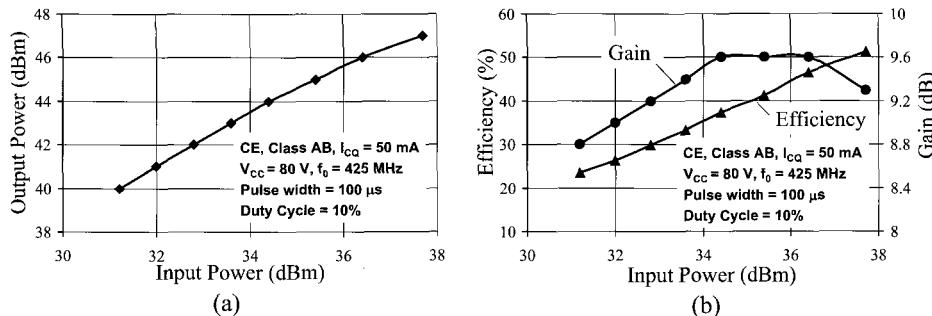


Fig. 25 Output power vs. input power for a single cell in CE mode operated in class AB mode at 425 MHz, pulse width 100  $\mu$ s, duty cycle 10%,  $V_{CC} = 80$  V and  $I_{CQ} = 50$  mA; (b) Collector efficiency and power gain vs. output power for conditions stated in (a).

This result is highly encouraging as it demonstrates the high power capability of the SiC RF-BJT devices along with acceptable power gain and efficiency. From thermal simulations, it is estimated that the junction temperature may reach a peak value of 171°C for pulse widths of 250  $\mu$ s and 6% duty cycle without any external cooling. Since SiC junctions can easily sustain a temperature of 250°C, there is room to increase the pulse width even further.

### 3.2 Darlington transistor

To enhance the current gain, a two-stage, Darlington configuration can be realized by cascading two BJT's with a common collector (Fig. 26).<sup>2</sup>

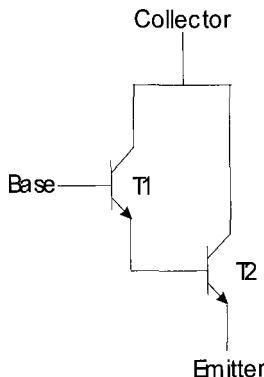


Fig. 26 Equivalent circuit diagram of a Darlington transistor.

This Darlington configuration has a current gain,  $\beta_D$ ,

$$\beta_D \sim \beta^2 \quad (14)$$

where  $\beta$  is the current gain each BJT stage, and the base current required is significantly reduced. However, in the on state, the forward voltage drop across a Darlington transistor can be expressed as

$$V_{CE,D} = V_{CE,BJT1} + V_{BE,BJT2} \quad (15)$$

where  $V_{CE,BJT1} = V_{CE,sat,BJT1}$ , which is the saturation voltage of the BJT in the first stage and has the same expression as Eq.(5) and has been shown to be less than 0.25V for optimized BJTs up to 10kV, but, on the other hand,  $V_{BE,BJT2} = V_{ON} \sim 2.5V$  (which is the diode turn-on knee voltage). It is clear from this discussion that the additional stage results in the turn-on knee in the Darlington output I-V characteristics and the forward drop is  $>2.5V$  in 4H-SiC (since

$$V_{ON} \sim 0.75 E_G/q \quad (16)$$

for any semiconductor).<sup>5,6,12</sup> Consequently, the Darlington transistor is only expected to be competitive at blocking voltages of 5kV or higher, similar to power devices with odd number of junctions between the main terminals, such as the IGBT and GTO Thyristor.<sup>36</sup>

A slower turn-off time is found in Darlington transistors because the fall time is determined by carrier recombination in the second stage, which cannot be assessed from the base terminal. To further optimize the turn-off time, a controlled resistance can be added between the emitter of the first stage and the base of the second stage so that some carriers of the second stage transistor can be extracted through the first stage transistor. However, this resistance must be low enough so as not to de-bias the base-emitter

junction too much during the on state because such a de-biasing leads to a higher forward drop.<sup>2</sup>

Conceptually, there are at least two possible structural variations of the Darlington transistor by replacing the first-stage BJT with a MOSFET, resulting in power transistors that are MOS gated and voltage controlled. If an n-channel MOSFET is used to drive a npn, such a transistor is called the MOS-Gated bipolar Transistor (MGT) (Fig. 27a), which has been demonstrated in Si monolithically with a DMOSFET and a lightly doped collector, high-voltage vertical npn.<sup>37</sup> The second MOSFET-BJT Darlington is to use an n-channel MOSFET to drive a pnp (Fig. 27b). In this case, the emitter of the pnp is actually connected to the high-voltage power rail of the system. The monolithic implementation of such a power transistor is the well-known IGBT, which has become the dominant Si power transistor in the last twenty years.<sup>2</sup> Since the MOSFET-BJT Darlington transistors mentioned above are beyond the scope of this chapter, we will only review the progress in monolithic and hybrid BJT-BJT Darlington transistors demonstrated in 4H-SiC. See reference<sup>38</sup> for a review of recent progress in the MOS-Darlington transistors such as the IGBT.

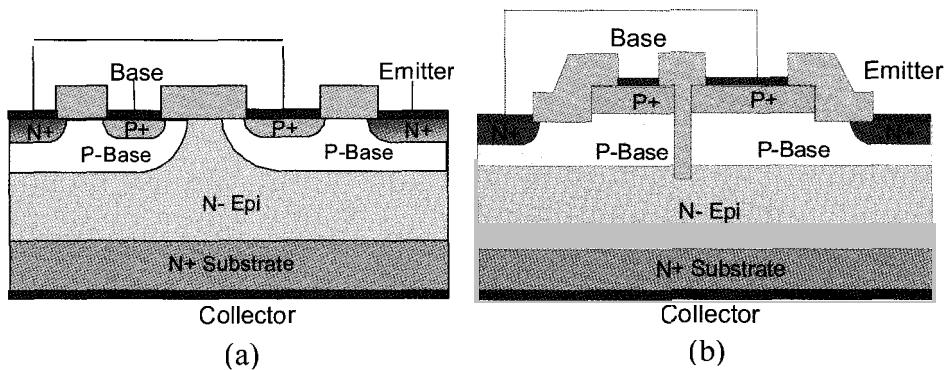


Fig. 27 Schematic cross-section of (a) planar Si and (b) oxide-trench isolated SiC monolithic Darlington transistors.

The first monolithic SiC Darlingtons with implanted-emitter BJTs and oxide-filled trenches used for interstage isolation have been reported.<sup>39-41</sup> A current gain of as high as 450 has been measured but the forward voltage is relatively high (7V at 0.3A ( $50\text{A}/\text{cm}^2$ )), with blocking voltages of 200-400V.<sup>39</sup> Recently, a 1kV, 30A Darlington using epi-emitter BJTs has been demonstrated and its output I-V characteristics are shown in Fig. 28.<sup>32</sup> A high current gain of 2400 and a forward drop less than 4V has been measured, indicating a substantial decrease in the gate drive power as well as a lower on-state conduction loss.<sup>32</sup>

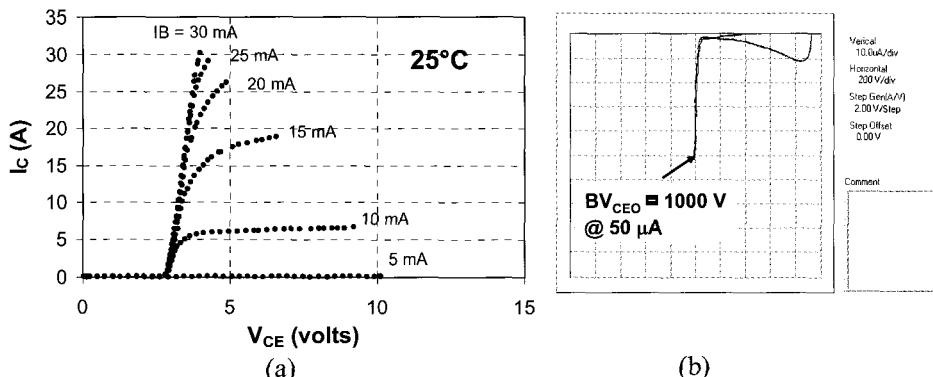


Fig. 28 (a) Forward conduction and (b) blocking I-V characteristics of a 1kV 4H-SiC Darlington transistor.<sup>32</sup>

Since the development of monolithic MOS-BJT Darlington transistors, such as the IGBT and the MGT, is still in its infancy, we have attempted to emulate the performance of these transistors with hybrid connections of separate MOSFET and BJT chips. We have demonstrated two different versions of hybrid MOSFET-BJT Darlington Transistors (see Fig. 29), both in the MGT type of configuration (in other words, n-MOSFET driving an npn BJT in a common collector/drain connection).

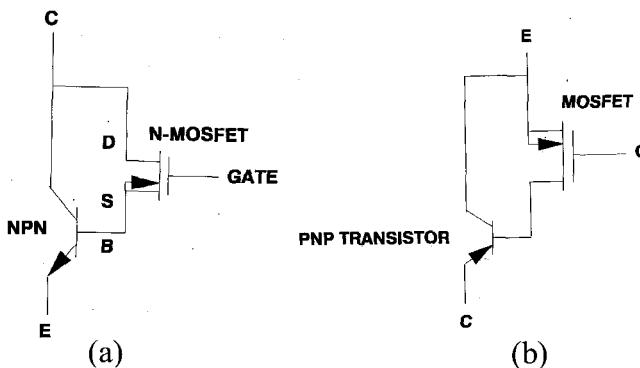


Fig. 29 Equivalent circuit connection of (a) MGT and (b) IGBT.

Theoretically, the on-state voltage of the MGT-type MOS-Darlington (Fig. 29a) can be written as

$$V_{F,MGT-MOSD} = V_{DS, MOSFET1} + V_{CE,BJT2} \quad (17)$$

and

$$V_{DS,MOSFET1} = V_{ch} + V_{JFET} + V_{drift} \quad (18)$$

where  $V_{ch}$ ,  $V_{JFET}$  and  $V_{drift}$  are the voltage drops across the channel, JFET and drift regions, respectively for a DMOSFET. For high-voltage (>100V) Si vertical DMOSFETs,

$$V_{DS,MOSFET1} \approx V_{drift} \quad (19)$$

where

$$V_{\text{drift}} = 5.93 \times 10^{-7} (\text{BV})^{2.5} \text{ (at } 100\text{A/cm}^2 \text{) in Si} \quad (20)$$

On the other hand, for 4H-SiC MOSFETs with  $\text{BV} < 1000\text{V}$ , the channel resistance cannot be ignored and

$$V_{\text{ch}} = I_{\text{DS}} L / (W \mu_{\text{ns}} C_{\text{ox}} (V_{\text{GS}} - V_{\text{T}})) \quad (21)$$

where

$L$  and  $W$  are the channel length and width respectively,

$\mu_{\text{ns}}$  is the inversion channel mobility,

$C_{\text{ox}}$  is the gate oxide capacitance,

$V_{\text{GS}}$  and  $V_{\text{T}}$  are the gate-source and threshold voltages respectively,

and

$$V_{\text{drift}} = 3.4 \times 10^{-12} (\text{BV})^{2.5} \text{ in 4H-SiC} \quad (22)$$

Also, a low-voltage turn-off MOSFET can also be connected between the base and emitter terminals of the second stage BJT in the MGT structure to facilitate device turn-off.

By contrast, in the IGBT-type MOS-Darlington, not only the second-stage is a pnp BJT, but this pnp has a wide, lightly doped base and heavily doped collector.<sup>2</sup> The MOSFET/BJT forward conduction model of the IGBT may be used for the hybrid IGBT-type MOS-Darlington.<sup>2</sup>

$$V_{\text{F,IGBT-MOSD}} = (2kT/q) \ln [I_C d / (2q W D_a n_i F(d/L_a))] + (1 - \alpha_{\text{PNP}}) I_C L_{\text{ch}} / [\mu_{\text{ns}} C_{\text{ox}} W (V_{\text{GS}} - V_{\text{T}})] \quad (23)$$

Also, because of its structural configuration, the turn-off process of the IGBT-type MOS-Darlington is always open-base turn-off of the second-stage pnp. Consequently, it is minority carrier recombination lifetime reduction is needed to speed up device turn-off, but at the expense of a higher forward drop. Calculated  $V_{\text{F}}$  vs.  $t_{\text{off}}$  tradeoff for a 5kV SiC IGBT has been performed.<sup>11</sup>

Experimentally, two reports of hybrid MOS-Darlington transistors using SiC BJTs have been reported.<sup>42,43</sup> In one case, a high-voltage Si commercial power DMOSFET is connected to an implanted-emitter 4H-SiC npn BJT.<sup>42</sup> The blocking voltages of both Si DMOSFET and 4H-SiC BJT are about 600V. The output I-V characteristics of such a hybrid Si/SiC MGT-type MOS-Darlington is shown in Fig. 30.<sup>42</sup> A forward drop of 4V at 1.4A ( $100\text{A/cm}^2$ ) has been measured. A turn-off time of  $2\mu\text{s}$  was obtained with open-base turn-off but it was reduced to  $0.5\mu\text{s}$  when a 50V Si MOSFET was used for active turn-off of the SiC BJT. In the second case, an all-SiC hybrid MGT-type MOS-Darlington was realized when a high-voltage lateral 6H-SiC MOSFET is connected to a 4H-SiC BJT.<sup>43</sup> Utilization of the most optimal device structures and SiC polytypes are the advantages of a hybrid implementation but the parasitic interconnecting resistances of these devices need to be minimized and is a major obstacle for current level scale-up.

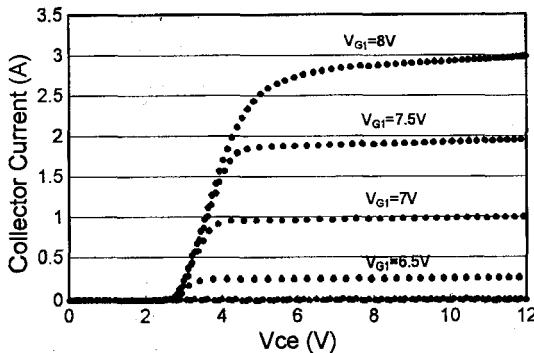


Fig. 30 Forward I-V characteristics of a hybrid 600V Si MOSFET/SiC BJT device.<sup>42</sup>

#### 4. Commercialization Challenges

While prototype power BJTs for both power switching and high-frequency amplification applications have been continuously improved, in increasing blocking voltages in the former and in cut-off frequencies in the latter, there are still technical barriers that need to be overcome. In particular, the minority carrier recombination lifetimes in the base and collector regions of the BJTs are determined by the epitaxial growth process, which needs to be more reproducible, and need to be sufficiently high for high current gain and adequate conductivity modulation of the collector in the on state. At present, only the epi emitter process yields acceptable current gain because the damages created with the implanted process have not been able to be annealed out. However, the epi emitter process is inflexible for device manufacturing and yields a non-planar process. Also, the reliability of SiC BJTs has not been studied and needs to be established. With the gate oxide reliability issue, particularly at elevated temperatures, is still impeding the SiC MOSFET development, SiC BJTs offer an alternate device choice in power switching and high-frequency amplifying applications.

#### References

1. S.K. Ghandhi, *Semiconductor Power Devices*, Wiley, 1977, republished 1998.
2. B.J. Baliga, *Physics of Semiconductor Power Devices*, JWS Publishing, 1996.
3. K. Shenai, R.S. Scott, and B.J. Baliga., IEEE Trans. Electron Devices, **36**, 1811 (1989).
4. B.J. Baliga, IEEE Electron Device Letters, **10**, 455 (1989).
5. A. Bhalla and T.P. Chow, "Examination of semiconductors for bipolar power devices," Inst. Phys. Conf. Ser. No. 137, p. 621, IOP Publishing Ltd., 1994.
6. A. Bhalla and T.P. Chow, Proc. 6th International Symp. Power Semiconductor Devices and ICs, pp. 287-292, 1994.
7. T.P. Chow and R. Tyagi, IEEE Trans. Electron Devices, **41**, 1481 (1994).
8. A.S. Kyuregyan and S.N. Yurkov, Sov. Phys. Semicond., **23**, 1126 (1989).
9. A.O. Konstantinov, Q. Wahab, N. Nordell, and U. Lindefelt, Appl. Phys. Lett., **71**, 90 (1997).
10. R. Raghunathan and B.J. Baliga, "Measurement of electron and hole impact ionization coefficients for SiC," Proc. 9th IEEE International Symposium on Power Semiconductor Devices and ICs, pp. 173-176, 1997.

11. N. Ramungul, R. Tyagi, A. Bhalla, T.P. Chow, M. Ghezzo, J. Kretchmer, W. Hennessy, "Design and Simulation of 6H-SiC UMOS FET and IGBT for High-Temperature Power Electronics Applications," Inst. Phys. Conf. Ser. No. 142, pp. 773-776, 1995.
12. Yi Tang, "High Voltage Implanted-Emitter Bipolar Junction Transistors and Darlington Transistors in 4H-SiC," Ph.D. Thesis, RPI, June, 2003.
13. See, for example, R. Singh, K.G. Irvine, O. Kordina, J.W. Palmour, M.E. Levenshtein, S.L. Rumyanetsev, "4H-SiC bipolar P-i-N Diodes with 5.5 KV blocking voltage," 56th Annual Device Research Conference Digest, pp.86-87 (1998).
14. P. Neudeck and C. Fazi, Electron Device Letters, **18**, 96 (1997).
15. S. Nakamura, H. Kumagai, T. Kimoto, and H. Matsunami, Mat. Sci. Forum, **389-393**, 651 (2002).
16. A. Blicher, *Field-Effect and Bipolar Power Transistor Physics*, Academic Press, 1981.
17. T. Hatakeyama, T. Watanabe, K. Kojima, N. Sano, K. Shiraihi, M. Kushibe, S. Imai, T. Shinohe, T. Suzuki, T. Tanaka and K. Arai, Mat. Sci. Forum, "Impact Ionization Coefficients of 4H-SiC," Mat. Sci. Forum, **457-460**, 673-676, (2004).
18. S. Balachandran, T.P. Chow, A. Agarwal, S. Scozzie, and K. A. Jones, "BV<sub>CEO</sub> versus BV<sub>CBO</sub> for 4H and 6H polytype SiC Bipolar Junction Transistors," Mat. Sci. Forum, **483-485**, 893-896 (2005).
19. J. G. Kassakian, M.F. Schlecht, and G.C. Verghese, *Principles of Power Electronics*, Addison-Wesley, 1991.
20. A.Q. Huang and B. Zhang, "Comparing SiC Switching Power Devices: MOSFET, NPN transistor and GTO Thyristor," Solid-State Electronics, 44, 325-340 (2000).
21. Y. Luo, L. Fursin, and J.H. Zhao, Electronics Letters, **36**, 1496 (2000).
22. Y. Tang, J.B. Fedison, and T.P. Chow, Electron Device Letters, **22**, 119 (2001).
23. S.-H. Ryu, A.K. Agarwal, R. Singh, and J.W. Palmour, Electron Device Letters, **22**, 124 (2001).
24. Y. Tang, J.B. Fedison, and T.P. Chow, Electron Device Letters, **23**, 16 (2002).
25. S.-H. Ryu, A.K. Agarwal, R. Singh, and J.W. Palmour and M.E. Levenshtein, "1.8kV, 3.8A bipolar junction transistors in 4H-SiC," Proc. International Symp. Power Semiconductor Devices and ICs, pp.37-40, 2001.
26. Y. Tang, J.B. Fedison, and T.P. Chow, Mat. Sci. Forum, **389-393**, 1329 (2002).
27. Y. Luo, L. Fursin, J.H. Zhao, P. Alexandrov, B. Wright, and M. Weiner, Mat. Sci. Forum, **389-393**, 1325 (2002).
28. C.-F. Huang and J.A. Cooper, "4H-SiC npn bipolar junction transistors with BV<sub>CEO</sub> > 3,200V," Proc. International Symp. Power Semiconductor Devices and ICs, pp. 57-60, 2002.
29. A.K. Agarwal, S.-H. Ryu, J. Richmond, C. Capell, J.W. Palmour, Y. Tang, S. Balachandran, and T.P. Chow, "Large Area, 1.3kV, 17A, Bipolar Junction Transistors in 4H-SiC," Proc. International Symp. Power Semiconductor Devices and ICs, pp.135-138, Cambridge, England, April 14-17, 2003.
30. J.H. Zhao, J. Zhang, P. Alexandrov, X. Li, and T. Burke, "A High Voltage (1,750V) and High Current Gain ( $\beta=24.8$ ) 4H-SiC Bipolar Junction Transistor Using a Thin (12 $\mu$ m) Drift Layer," Mat. Sci. Forum, **457-460**, 1173 (2004).

31. A.K. Agarwal, S.-H. Ryu, J. Richmond, C. Capell, J.W. Palmour, S. Balachandran, T.P. Chow, B. Geil, S. Bayne, C. Scozzie and K.A. Jones, "Recent Progress in SiC Bipolar Junction Transistors," Proc. International Symp. Power Semiconductor Devices and ICs, pp.361-364, Kitakyushu, Japan, May 24-27, 2004.
32. S. Krishnaswami, A.K. Agarwal, S.-H. Ryu, J. Richmond, C. Capell, J.W. Palmour, S. Balachandran, T.P. Chow, B. Geil, S. Bayne, C. Scozzie, and K.A. Jones, "1000V, 30A SiC Bipolar Junction Transistors and Integrated Darlington Pairs," Mat. Sci. Forum, **483-485**, 901 (2005).
33. S. Balachandran, T. P. Chow, A. Agarwal, C. Scozzie, and K.A. Jones, "4kV 4H-SiC Epitaxial Emitter Bipolar Junction Transistors," Proc. International Symp. Power Semiconductor Devices and ICs, Santa Barbara, CA, 2005.
34. P. Losee, S.K. Balachandran, L. Zhu, C. Li, J. Seiler, T.P. Chow, and I.B. Bhat, "High-Voltage 4H-SiC PiN Rectifiers with Single-Implant, Multi-Zone JTE Termination," Proc. International Symp. Power Semiconductor Devices and ICs, pp.301-304, Kitakyushu, Japan, May 24-27, 2004.
35. H-T. Yuan et al., IEEE Trans. Electron Devices, ED-25, pp. 731-736, 1978.
36. T.P. Chow, "Wide Bandgap Semiconductor High-Voltage Power Switching Transistors," Electrochemical Society Proc. Vol. 98-12, pp.16-29, 1998.
37. T. Tanaka, Y. Yasuda, and M. Ohayashi, IEEE Trans. Electron Devices, **ED-33**, 2041 (1986).
38. T.P. Chow, N. Ramungul, J. Fedison, and Y. Tang, "SiC Power Bipolar Transistors and Thyristors," in Silicon Carbide: Recent Major Advances, ed. W.J. Choyke, H. Matsunami, and G. Pensl, Springer, 2003.
39. Y. Tang and T.P. Chow, "Demonstration of Monolithic Darlington Transistors in 4H-SiC," Paper WeP2-23, European Conference on Silicon Carbide and Related Materials (ECSCRM), Linkoping, Sweden, September 1-5, 2002.
40. Y. Tang and T.P. Chow, "High Gain Monolithic 4H-SiC Darlington Transistors," Proc. International Symp. Power Semiconductor Devices and ICs, pp.383-386, Cambridge, England, April 14-17, 2003.
41. Y. Tang and T.P. Chow, "Monolithic 4H-SiC Darlington Transistors with a Peak Current Gain of 2000," Device Research Conference, Salt Lake City, UT, June 23-25, 2003.
42. Y. Tang, T.P. Chow, A.K. Agarwal, S.-H. Ryu, and J.W. Palmour, "Hybird MOS-Gated Bipolar Transistor Using 4H-SiC BJT," Mat. Sci. Forum, **389-393**, 1341-1344 (2002).
43. Y. Tang, S. Banerjee, and T.P. Chow, "Hybrid All-SiC MOS-Gated Bipolar Transistor," Proc. International Symposium on Power Semiconductor Devices and ICs, pp.53-56, Sante Fe, NM, June 4-7, 2002.



**World Scientific**

Connecting Great Minds



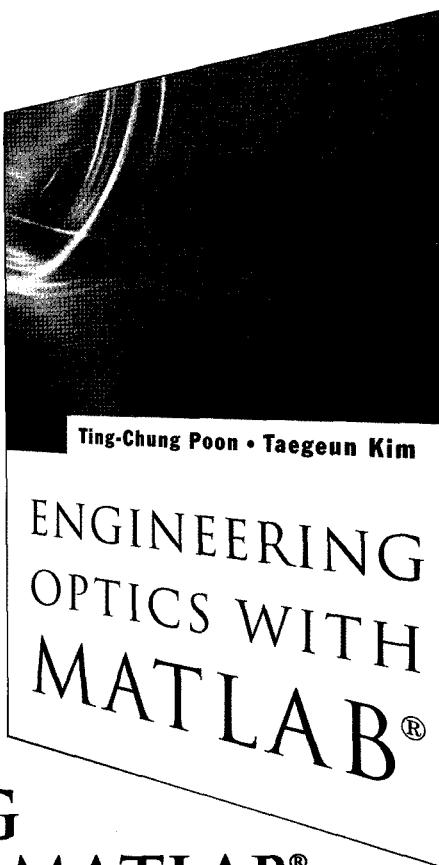
World Scientific

YEARS OF PUBLISHING

1 9 8 1 - 2 0 0 6

#### Key Features

- Treatment of each topic begins with the first principle; for example, geometrical optics starts with Fermat's principle, while acousto-optics and electro-optics starts with Maxwell equations
- MATLAB examples are presented throughout, including programs for some important topics like diffraction of Gaussian beams, split-step beam propagation method, and numerical calculation of up to 10-coupled differential equations in acousto-optics
- Covers acousto-optics with emphasis on modern applications such as spatial filtering and heterodyning
- Ideal as a general textbook for optics/optical engineering classes as well as acousto-optics and electro-optics for advanced students



# ENGINEERING OPTICS WITH MATLAB®

by **Ting-Chung Poon** (*Virginia Tech, USA*) & **Taegeun Kim** (*Sejong University, South Korea*)

This invaluable textbook serves two purposes. The first is to introduce some traditional topics such as matrix formalism of geometrical optics, wave propagation and diffraction, and some fundamental background on Fourier optics. The second is to present the essentials of acousto-optics and electro-optics, and provide the students with experience in modeling the theory and applications using a commonly used software tool MATLAB®. The book is based on the authors' own in-class lectures as well as researches in the area.

**Contents:** Geometrical Optics; Wave Propagation and Wave Optics; Beam Propagation in Inhomogeneous Media; Acousto-Optics; Electro-Optics.

**Readership:** First-year/senior graduate students in engineering and physics; scientists and engineers keen in the basics of acousto-optics and electro-optics.

**260pp**

**981-256-872-7**

**981-256-873-5(pbk)**

**Jul 2006**

**US\$68    £39**

**US\$34    £20**

This page intentionally left blank

# SiC MATERIALS AND DEVICES

Volume 2

**S**ilicon carbide is known to have been investigated since 1907 when Captain H J Round demonstrated yellow and blue emission by applying bias between a metal needle and an SiC crystal. The potential of using SiC in semiconductor electronics was already recognized half a century ago. Despite its well-known properties, it has taken a few decades to overcome the exceptional technological difficulties of getting silicon carbide material to reach device quality and travel the road from basic research to commercialization.

This second of two volumes reviews four important additional areas: the growth of SiC substrates; the deep defects in different SiC polytypes, which after many years of research still define the properties of bulk SiC and the performance and reliability of SiC devices; recent work on SiC JFETs; and the complex and controversial issues important for bipolar devices.

Recognized leaders in the field, the contributors to this volume provide up-to-date reviews of further state-of-the-art areas in SiC technology and materials and device research.

*The picture on the cover shows the first SiC power switch and diode co-pack announced by CREE, Inc. on October 27, 2006  
(picture courtesy of CREE, Inc.)*

**World Scientific**  
[www.worldscientific.com](http://www.worldscientific.com)  
6311 hc

ISBN-13 978-981-270-383-5

ISBN-10 981-270-383-7



9 789812 703835