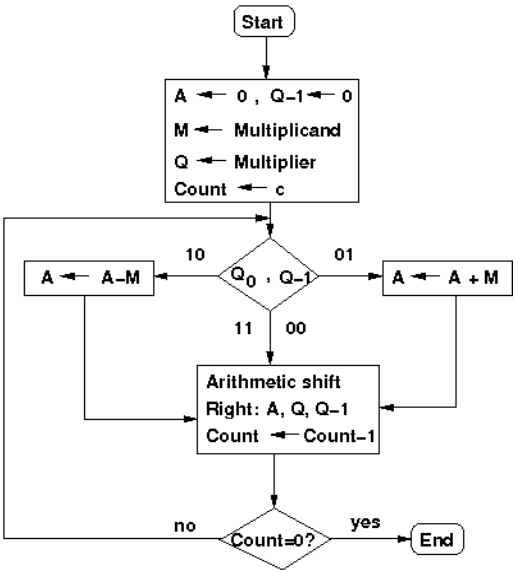
VIVEKANAND EDUCATION SOCIETY'S INSTITUTE OF TECHNOLOGY
Department of Information Technology

Class: D10A/B **Term Test 2(2022-23)** **Maximum marks:20**

Date: 27/2/2023 **Duration: 1 hr**

Subject: Computer Organization and Architecture **Semester: IV**

N.B. 1) All Questions are compulsory
2) assume suitable data wherever necessary.

Q.1	Answer Any Five	Marks	CO
a)	**Draw flowchart of Booth's Algorithm** 	2M	CO 4
b)	**Explain 6 stage instruction pipeline with suitable diagram** Pipeline processing can happen not only in the data stream but also in the instruction stream. To perform tasks such as fetching, decoding and execution of instructions, most digital computers with complicated instructions would require an instruction pipeline. In general, each and every instruction must be processed by the computer in the following order: 1. Fetching the instruction from memory 2. Decoding the obtained instruction 3. Calculating the effective address 4. Fetching the operands from the given memory 5. Execution of the instruction 6. Storing the result in a proper place	2M	CO 3

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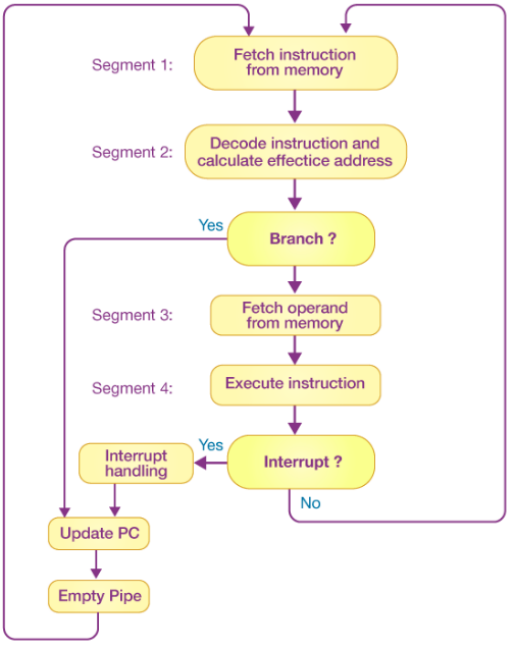
<td> 
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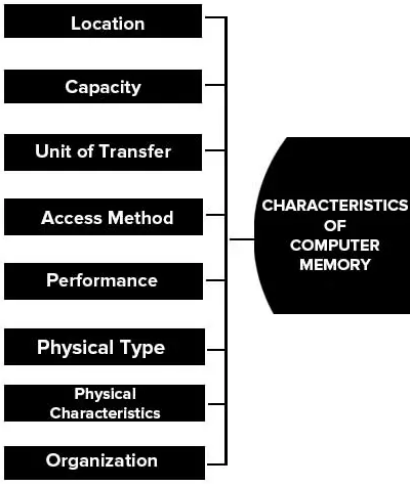
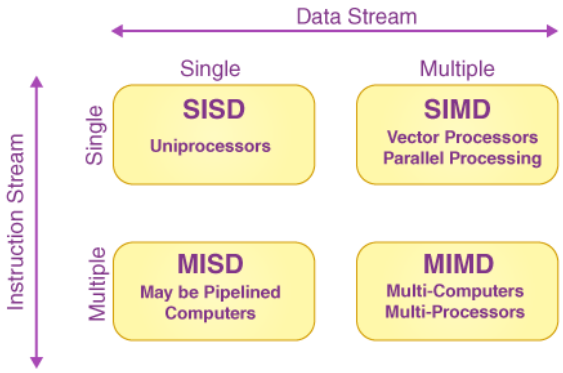
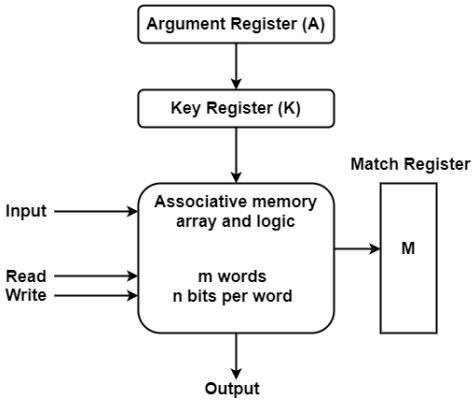
<td>c)</td>
<td>Comparison between Direct mapped, Fully associative and Set associative of cache memory mapping
<table>
<tr><th>Method</th><th>Mapping of main memory blocks to cache</th><th>Access using main memory address</th></tr>
<tr><td>Direct Mapped</td><td>Each block of main memory maps to unique line of cache</td><td>Line portion of address used to access cache line. Tag portion used to check for hit on that line</td></tr>
<tr><td>Fully Associative</td><td>Each block of main memory maps to any line of cache</td><td>Tag portion of address used to check every line for hit on that line</td></tr>
<tr><td>Set Associative</td><td>Each block of main memory maps to unique cache set</td><td>Line portion of address used to access cache set. Tag portion used to check every line in that set for hit on that line</td></tr>
</table></td>
<td>2M</td>
<td>CO 5</td>
</tr>
<tr>
<td>d)</td>
<td>Convert any one of below in IEEE 754 single precision standard
a) - 4.99 OR b) 28.75

Ans:
a) - 4.99
1-10000001-00111111010111000010100

b) 28.75
0-10000011-11001100000000000000000</td>
<td>2M</td>
<td>CO 4</td>
</tr>
<tr>
<td>e)</td>
<td>List and explain Key Characteristic of Computer Memory
 
</td>
<td>2M</td>
<td>CO 5</td>
</tr>
</table>

<table>
<tr><td>f)</td><td>Comparison between Hardwired Control Unit and Microprogrammed Control Unit
<table>
<tr><th>S.No.</th><th>Hardwired Control Unit</th><th>Microprogrammed Control Unit</th></tr>
<tr><td>1.</td><td>The hardwired control unit induces the control signals required for the processor.</td><td>The microprogrammed control unit induces the control signals through microinstructions.</td></tr>
<tr><td>2.</td><td>Hardwired control unit is quicker than a microprogrammed control unit.</td><td>Microprogrammed control unit is slower than a hardwired control unit.</td></tr>
<tr><td>3.</td><td>It is hard to modify.</td><td>It is easy to modify.</td></tr>
<tr><td>4.</td><td>It is more expensive as compared to the microprogrammed control unit.</td><td>It is affordable as compared to the hardwired control unit.</td></tr>
<tr><td>5.</td><td>It faces difficulty in managing the complex instructions because the design of the circuit is also complex.</td><td>It can easily manage complex instructions.</td></tr>
<tr><td>6.</td><td>It can use limited instructions.</td><td>It can generate control signals for many instructions.</td></tr>
</table></td><td>2M</td><td>CO 3</td></tr>
<tr><td>Q.2</td><td>Answer Any One</td><td></td><td></td></tr>
<tr><td>a)</td><td>Write note on Flynn’s Classification of parallel computer
 

Explanation of each type.</td><td>5M</td><td>CO 3</td></tr>
<tr><td></td><td>OR</td><td></td><td></td></tr>
<tr><td>b)</td><td>Discuss various pipeline hazards
1. Pipeline hazards are situations that prevent the next instruction in the instruction stream from executing during its designated clock cycles.
2. Any condition that causes a stall in the pipeline operations can be called a hazard.
3. There are primarily three types of hazards: (Explain each)
i. Data Hazards
ii. Control Hazards or instruction Hazards
iii. Structural Hazards.</td><td>5M</td><td>CO 3</td></tr>
<tr><td>Q.3</td><td>Answer Any One</td><td></td><td></td></tr>
<tr><td>a)</td><td>Write note on Interleaved and Associative memory
Associative memory:
● An associative memory can be treated as a memory unit whose saved information can be recognized for approach by the content of the information itself instead of by an address or memory location.
● Associative memory is also known as Content Addressable Memory (CAM).</td><td>5M</td><td>CO 5</td></tr>
</table>



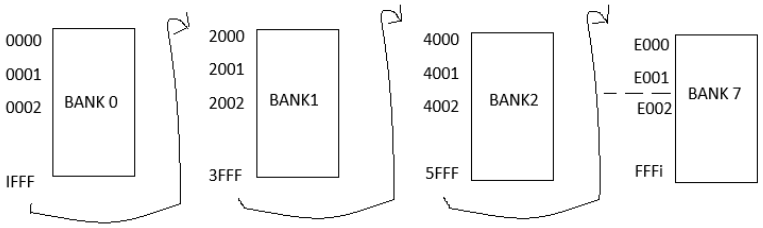
- It includes a memory array and logic for m words with n bits per word. The argument register A and key register K each have n bits, one for each bit of a word.
- The match register M has m bits, one for each memory word. Each word in memory is related in parallel with the content of the argument register.
- The words that connect the bits of the argument register set an equivalent bit in the match register. After the matching process, those bits in the match register that have been set denote the fact that their equivalent words have been connected.
- Reading is proficient through sequential access to memory for those words whose equivalent bits in the match register have been set.

Interleaved memory:

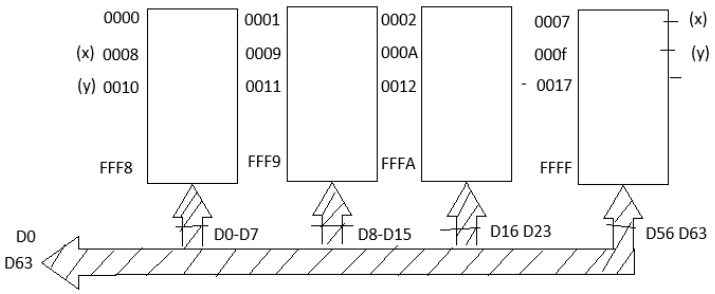
The memory system in which successive addresses are evenly spread across memory banks to compensate for the relatively slow speed of DRAM.

The contagious memory reads and writes are using each bank in term, resulting in higher memory throughputs due to reduced waiting for memory banks to become ready for desired operations.

1. **Low order Interleaving**



2. **High order Interleaving**



	OR		
b)	**Perform Restoring Division Algorithm on □ $(01111)_2 \div (00100)_2$** Ans: Q= 00011 AC = 00011	5M	CO 4