VIVEKANAND EDUCATION SOCIETY'S
INSTITUTE OF TECHNOLOGY
Department of Information Technology

Class: D10
Date: 20/02/2023
Name of Subject: **Computer Organisation and Architecture**

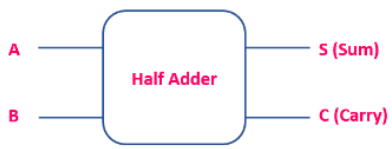
Term Test 1
(2022-23)

Maximum Marks: 20
Duration: 1 hr.
Semester: IV

N.B. 1) All Questions are compulsory
2) Assume suitable data wherever necessary.

Q.1	Answer Any Five	Marks	CO	BL
a)	Compare Computer Organization and Computer Architecture	2M	CO 2	BL1

S.No	Computer Architecture	Computer Organisation
1.	They explain what a computer does.	They explain how a computer actually does it.
2.	They majorly focus on the functional behaviour of computer systems.	They majorly focus on the structural relationship and deep knowledge of the internal working of a system.
3.	Computer architectures deal with high-level design matters.	They deal with low-level design matters.
4.	It comes before computer organisation.	It comes after the architecture part.
5.	It is also called instruction set architecture.	It is also called microarchitecture.
6.	It covers logical functions, such as registers, data types, instruction sets, and addressing modes.	It covers physical units like peripherals, circuit designs, and adders.
7.	They coordinate between the hardware and software of the system.	They manage the portion of the network in a system.

b)	Convert the following numbers *(..any one*) (25986)10 = (?)16 **OR** (428.10)10 = (?)2 $25986_{10} = 6582_{16}$ $428.10_{10} = 110101100.0001100110_2$	2M	CO 1	BL 2,6
c)	Explain Half Adder with diagram • Half Adder is the digital logic circuit that is used to implement the **binary addition**.  	2M	CO 1	BL 2

- It adds the two bits and generates the sum bit (S) and carry bit (C) as an output.

Inputs		Outputs	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Fig: Truth Table

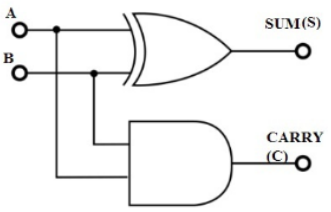


Fig: Half adder circuit

$S = A \oplus B$

$C = A \cdot B$

The main disadvantage of this circuit is that it can only add two inputs and if there is any carry, it is neglected. Thus, the process is incomplete.

To overcome this difficulty Full Adder is designed.

d) Discuss any 4 arithmetic instruction of 8086 with examples — 2M — CO 2 — BL 1,2

OPCODE	OPERAND	EXPLANATION	EXAMPLE
ADD	D, S	D = D + S	ADD AX,
SUB	D, S	D = D - S	SUB AX, [SI]
MUL	8-bit register	AX = AL * 8-bit reg.	MUL BH
DIV	8-bit register	AX = AX / 8-bit reg. ; AL = quotient ; AH = remainder	DIV BL

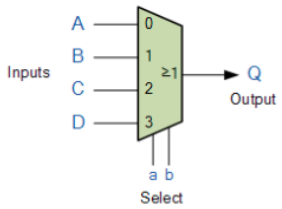
e) Explain multiplexer and demultiplexer — 2M — CO 1 — BL 1

- A multiplexer is a combinational circuit that has 2^n input lines and a single output line.
- Simply, the multiplexer is a multi-input and single-output combinational circuit.
- The binary information is received from the input lines and directed to the output line. On the basis of the values of the selection lines, one of these data inputs will be connected to the output. A multiplexer is also treated as **Mux**.

Multiplexer types

1. 2:1 multiplexer (1select line)
2. 4:1 multiplexer (2 select lines)
3. 8:1 multiplexer(3 select lines)
4. 16:1 multiplexer (4 select lines)

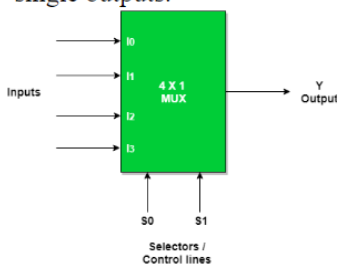
Multiplexer symbol-



Example:

4X1 Multiplexer

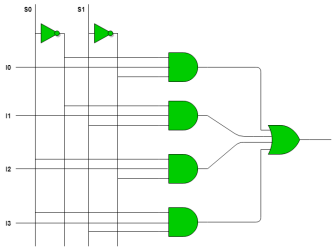
In 4×1 multiplexer, there are only 4 inputs, 2 selection line and single outputs.



Truth Table

S0	S1	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

So, final equation,
Y = S0'.S1'.I0 + S0'.S1.I1 + S0.S1'.I2 + S0.S1.I3



f)	Difference between Minimum and Maximum mode of 8086	2M	CO 2	BL 1

Minimum mode	Maximum mode
There can be only one processor.	There can be multiple processors.
Performance is slower.	Performance is faster.
The circuit is simple.	The circuit is complex.
Multiprocessing cannot be performed.	Multiprocessing can be performed.
MN/MX is 1 to indicate the minimum mode.	MN/MX is 0 to indicate the maximum mode
The 8086 generates INTA for interrupt acknowledgment.	The 8288 Bus Controller generates the interrupt acknowledgment signal (INTA).
The 8086 generates INTA for interrupt acknowledgment.	The 8288 Bus Controller generates the interrupt acknowledgment signal (INTA).
The 8086 itself provides an ALE for the latch.	Because there are several processors, the 8288 bus controller provides ALE for the latch.
The system is more affordable.	The system costs more money.
It is used for small systems.	It is used for large systems.
The multiprocessor setup is not supported.	The multiprocessor configuration is accepted.

Q.2	**Answer Any One**			
a)	Explain SR and JK flip flop with Truth Table and diagrams Answer: SR flip flop is the simplest type of flip flops. It stands for Set Reset flip flop. It is a clocked flip flop. SR Flip-Flop is Used as a storage device for a single data bit. Following are the two methods for constructing a SR flip flop- 1. By using NOR latch 2. By using NAND latch	5M	CO 1	BL 1

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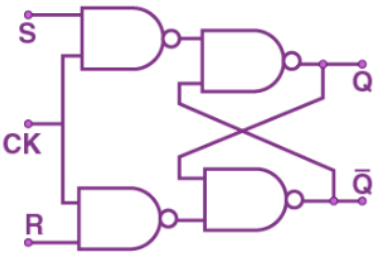
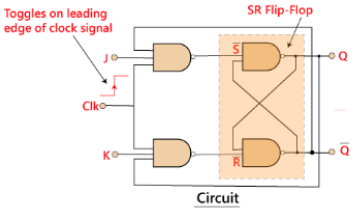
Truth Table

S	R	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-



JK flip flop is a refined & improved version of SR flip flop that has been introduced to solve the problem of indeterminate state that occurs in SR flip flop when both the inputs are 1.
There are following two methods for constructing a JK flip flop-



J	K	Q_n	Q_{n+1}	State
0	0	0	0	Q_n (Hold)
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	1	Toggel
1	1	1	0	

OR

b) Minimize the following Boolean function using K-map F(A,B,C,D) = m(0,2,8,10,14) +d(5,15) — 5M — CO 1 — BL 5

Q.3 Answer Any One

a) Explain any 5 following instruction of 8086 Microprocessor with one example each
STD, NOT, MOVSB, LEA, ROL, SBB, JMP, DAA — 5M — CO 2 — BL 3

Solution:
STD − Used to set the direction flag DF to 1.
Example:
DF=1

NOT − Used to invert each bit of a byte or word.
Example:
MOV AL, 00011011b
NOT AL ; AL = 11100100b
RET

MOVSB− Used to move the byte/word from one string to another.
Example:
ORG 100h CLD
LEA SI, a1
LEA DI, a2

MOV CX, 5
REP MOVSB

LEA − Used to load the address of operand into the provided register.
Example:

```
org 100h
LEA AX, m ; AX = offset of m
RET
m dw 1234h
END
```

ROL − Used to rotate bits of byte/word towards the left, i.e. MSB to LSB and to Carry Flag [CF].
Example:

```
MOV AL, 1Ch ; AL = 00011100b
ROL AL, 1 ; AL = 00111000b, CF=0.
RET
```

SBB − Used to perform subtraction with borrow.
Example:

```
STC
MOV AL, 5
SBB AL, 3 ; AL = 5 - 3 - 1 = 1
RET
```

JMP − Used to jump to the provided address to proceed to the next instruction.
Example:

```
mov    ax, 5        ; set ax to 5.
mov    bx, 2        ; set bx to 2.
jmp    calc         ; go to 'calc'.
back:  jmp stop     ; go to 'stop'.
calc:
add    ax, bx       ; add bx to ax.
jmp    back         ; go 'back'.
stop:
ret                 ; return to operating system.
```

DAA − Used to adjust the decimal after the addition/subtraction operation
Example:

```
MOV AL, 0Fh ; AL = 0Fh (15)
DAA ; AL = 15h
RET
```

OR

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b)	Identify addressing modes of the following instructions and explain their meaning a. MOV AX,89C5H - Immediate addressing mode b. MOV AX,[1234] -Direct addressing mode c. MOV CL,BH - Register Addressing mode d. MOV [BX],AX - Register indirect addressing mode e. MOV AX,[SI +200] -Indexed addressing mode	5M	CO 2	BL 1

**********ALL THE BEST**********

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b)	Convert the following numbers *(..any one*) (25986)10 = (?)16 **OR** (428.10)10 = (?)2	2M	CO 1
c)	Explain Half Adder with diagram	2M	CO 1
d)	Discuss any 4 arithmetic instruction of 8086 with examples	2M	CO 2
e)	Explain multiplexer and demultiplexer	2M	CO 1
f)	Difference between Minimum and Maximum mode of 8086	2M	CO 2
Q.2	**Answer Any One**		
a)	Explain SR and JK flip flop with Truth Table and diagrams	5M	CO 1
	OR		
b)	Minimize the following Boolean function using K-map F(A,B,C,D) = m(0,2,8,10,14) +d(5,15)	5M	CO 1
Q.3	**Answer Any One**		
a)	Explain any 5 following instruction of 8086 Microprocessor with one example each STD, NOT, MOVSB, LEA, ROL, SBB, JMP, DAA	5M	CO 2
	OR		
b)	Identify addressing modes of the following instructions and explain their meaning a. MOV AX,89C5H b. MOV AX,[1234] c. MOV CL,BH d. MOV [BX],AX e. MOV AX,[SI +200]	5M	CO 2

**********ALL THE BEST**********