EE112 project

Assignment 17

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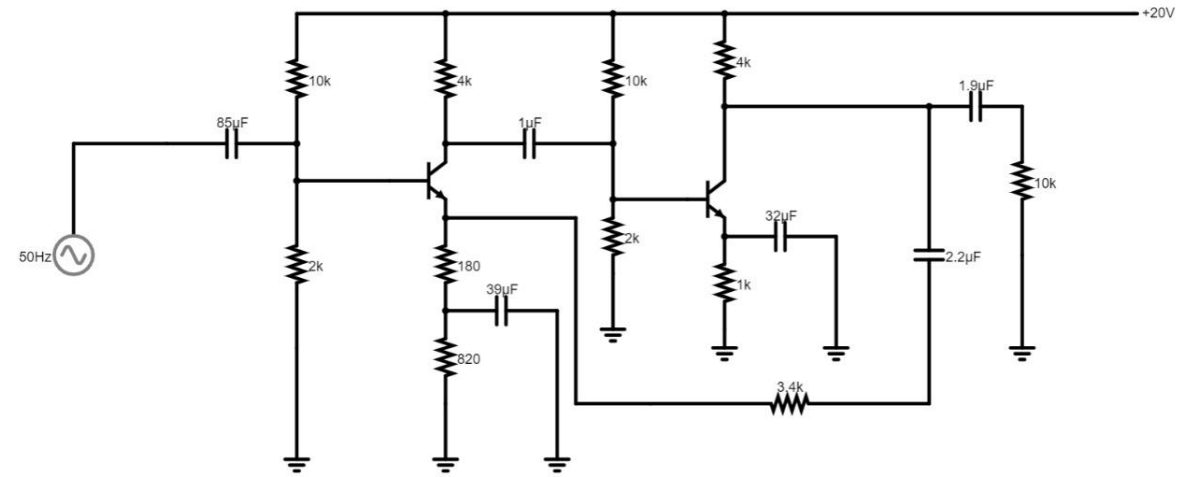
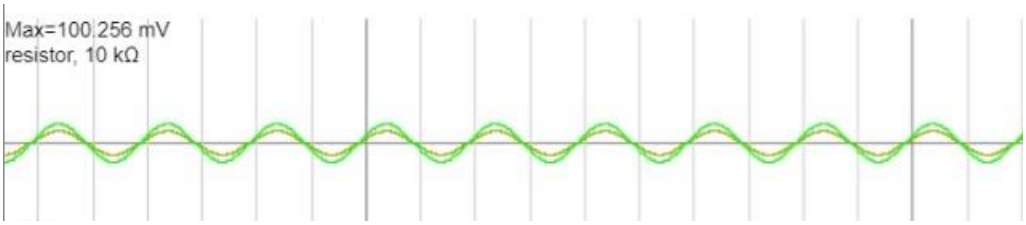
Design Requirements

A two stage CE amplifier with feedback and a voltage gain of 20.

Circuit Design





Circuit Analysis

Biasing and Coupling of transistors

A DC Voltage of 20V is applied for proper biasing of both the transistors, to obtain stable Q points for them to operate. For the input AC signal and the two stages to not to disturb Q points of transistor of the other stage , decoupling capacitors are used. Their capacitance can vary from 1µF to 100µF, depending on the frequency of the signal and resistances connected. So, in order to obtain the desired results, trial-error method has been used. Emitter resistance of 2^{nd} stage (R_{E2}=1kΩ) and that of the 1^{st} stage (R_{E1}=820 Ω) has been AC-grounded using bypass capacitors,chosen such that their capacitative reactance is approximately 10% of the resistance in parallel.

Feedback

Some part of the emitter resistor $r_e = 180\Omega$, of 1st stage, is unbypassed so that the AC voltage across it opposes any change in voltage gain. Another stage of feedback has been used, where output signal is coupled back through a feedback resistance $r_f = 3.4k\Omega$ to the emitter of the first stage.Because of the voltage divider, the AC voltage between the first emitter and ground is

$$v_{e1} = \frac{r_e}{r_e + r_f}\, v_{out} \tag{1}$$

Voltage Gain

The current i_f passing through r_f, is comparable to the collector current i_{c2} at the 2^{nd} stage. Also, the AC voltage of the base at the 2^{nd} stage is equal to that of the collector at the 1^{st} stage and,

$$v_{c1} = -i_{c1} R_{C1}$$

$$v_{b2} = i_{c2} r'_{e2}$$

where r'_{e2} is the AC emmitter resistance at the 2^{nd} stage. Therefore we conclude that $i_{c2} >> i_{c1}$ because $R_{C1} >> r'_{e2}$. Now since i_f is comparable to i_{c2}, $i_f >> i_{c1}$. Hence,

$$v_{out} = i_f(r_e + r_f) + i_{c1}(re) \approx i_f(r_e + r_f) \tag{2}$$

From 1 and 2,

$$v_{e1} = i_f r_e \tag{3}$$

Also,

$$v_{b1} - v_{e1} = i_{c1} r'_e \tag{4}$$

where v_{b1} and r'_e are base voltage and AC emitter resistance of the emitter diode, at the 1^{st} stage, respectively. From 3 and 4,

$$v_{b1} = i_f re + i_{c1} r'_e \approx i_f r_e \tag{5}$$

Now input voltage $v_{in} = v_{b1}$. Therefore, using equations 2 and 5, we get

$$Voltage\, gain = \frac{v_{out}}{v_{in}} = \frac{i_f(r_e + r_f)}{i_f(r_e)} = 1 + \frac{r_f}{r_e} = 1 + (3400/180) \approx 19.89 \approx 20$$