FREQUENCY GENERATION

Submitted by: Group 78

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Problem Statement:

Frequency generator

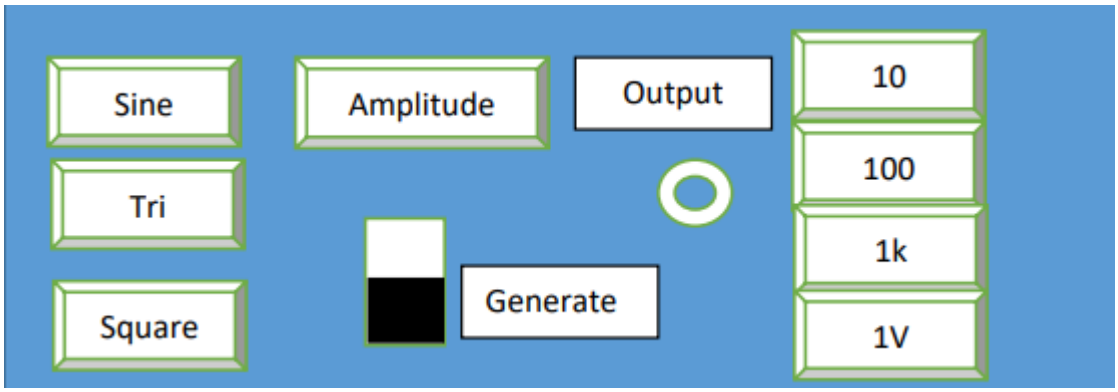
Design a System that senses that generates a Sine/Triangular/Square waveform

of frequencies ranging from 10Hz to 99KHz. Voltage is between 0-10V.

User Requirements & Technical Specifications

- On system power up the user has to configure the desired type of waveform (square/triangle/square), frequency, and amplitude.
- To generate a Square Waveform of Frequency 9.35 kHz the user has to press the square key, followed by 1K Key- 9 Times, 1K Key – 4 Times, 100 Key –3 Times 10 Key- 5 Times.
- To select the Amplitude the user will have to press the Amplitude key and then press the 1V key “n” number of times where “n” is the peak to peak amplitude of the waveform to be generated. (only integer values of output voltages need to be generated).
- When generating switch should be turned on and then the frequency generation is enabled i.e., the square waveform of that frequency will be generated.
- When frequency generation is enabled if the user wants to change the waveform into another type e.g. sine he just has to press sine.
- When a signal of a different type/amplitude /frequency has to be generated, the user will have to turn off the generate switch and then configure the function generator as mentioned above.

Diagram



Justification

1. Decoders aid in simplifying the circuit. Thus, we are using it in M/IO interfacing.
2. We are using DAC to convert digital values to analog for frequency generation.

Assumptions

The assumptions we have used in our project have been enlisted below:

- Once the user sets the initial frequency and amplitude, they can only transform the waveform.
- To reset the frequency and amplitude, the user needs to restart the program.
- There is no such limit on the amplitude as long as it can be stored in one byte of memory.
- At the location FFFF0h, where the instruction pointer points to RESET of the microprocessor, there exists a JUMP statement leading to the start of the code.

Address Map

Memory Map

ROM1(2716): 00000_H-$00FFF_H$

ROM2(2716): $FF000_H$-$FFFFF_H$

RAM1(6116): 01000_H-$01FFF_H$

ROM1

A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

RAM1

A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

ROM2

A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

I/O Map

8255:

Base Address 00H

It is I/O mapped I/O System.

The addresses of the ports are as follows:

PORT of 8255	Address
PORT A	00H
PORT B	02H
PORT C	04H
Control Register	06H

Data lines: D0-D7 data lines of the microprocessor (as it is connected in even bank).

Port Specification:

Group A: Mode 0

Group B: Mode 0

Port A: Input Port B: Output

Port C upper: Output Port Port C lower: Input Port

Hence, the control word is **10001010b**.This is written to control register.

8253: 08 – $0E_H$

COMPONENTS USED:

COMPONENT	QUANTITY	DESCRIPTION
8086 microprocessor	1	It is a 16-bit Microprocessor having 20 address lines
6116 - RAM	2	Smallest RAM chip available is 2 K and we need odd and even bank to temporary storage of data and stack
2716 - ROM	4	Smallest RAM chip available is 2 K and we need an odd and even bank to reset addresses which are at FFFF0H and 00000H
8255A - Programmable Peripheral Interface	1	Used for IO interfacing
8253A - Programmable Interval Timer	1	Used for generating time delays
DAC 0830 - Digital to Analog Convertor	1	Used to convert digital values to analog
Oscilloscope	1	Used for frequency generation
Keypad - Phone	1	Used for taking input from the user
741 - Operational Amplifier	1	Used to convert current to voltage
74LS138 - 3:8 Decoder	2	Used in memory/IO interfacing
74-LS373 Octal Latch	3	Used for demultiplexing address and data lines
74LS245 - Octal Bus Transceiver	2	74LS245 is an octal bus transceiver (Transmitter/Receiver) designed for asynchronous two-way communication between two data buses or input/output device.
OR Gate	4	LOGIC OR GATE

Switch	1	To complete the circuit and start the current flow
Resistor	2	10k ohm
8284	1	Used as a clock generator

Design

Complete design shown with proper labeling (design attached)

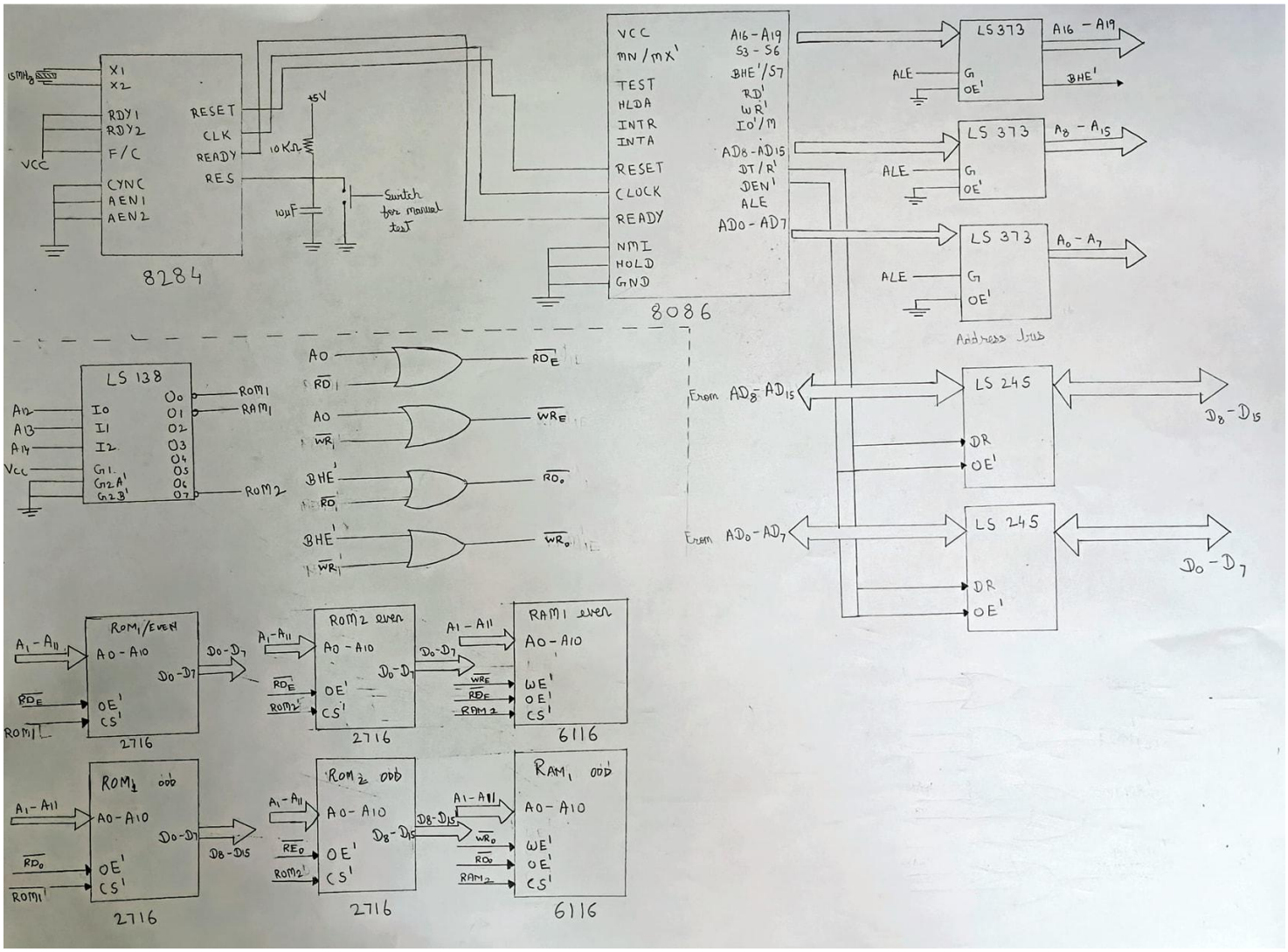


FIG: MEMORY INTERFACING+OCTAL LATCHES

Design

Complete design shown with proper labeling (design attached)

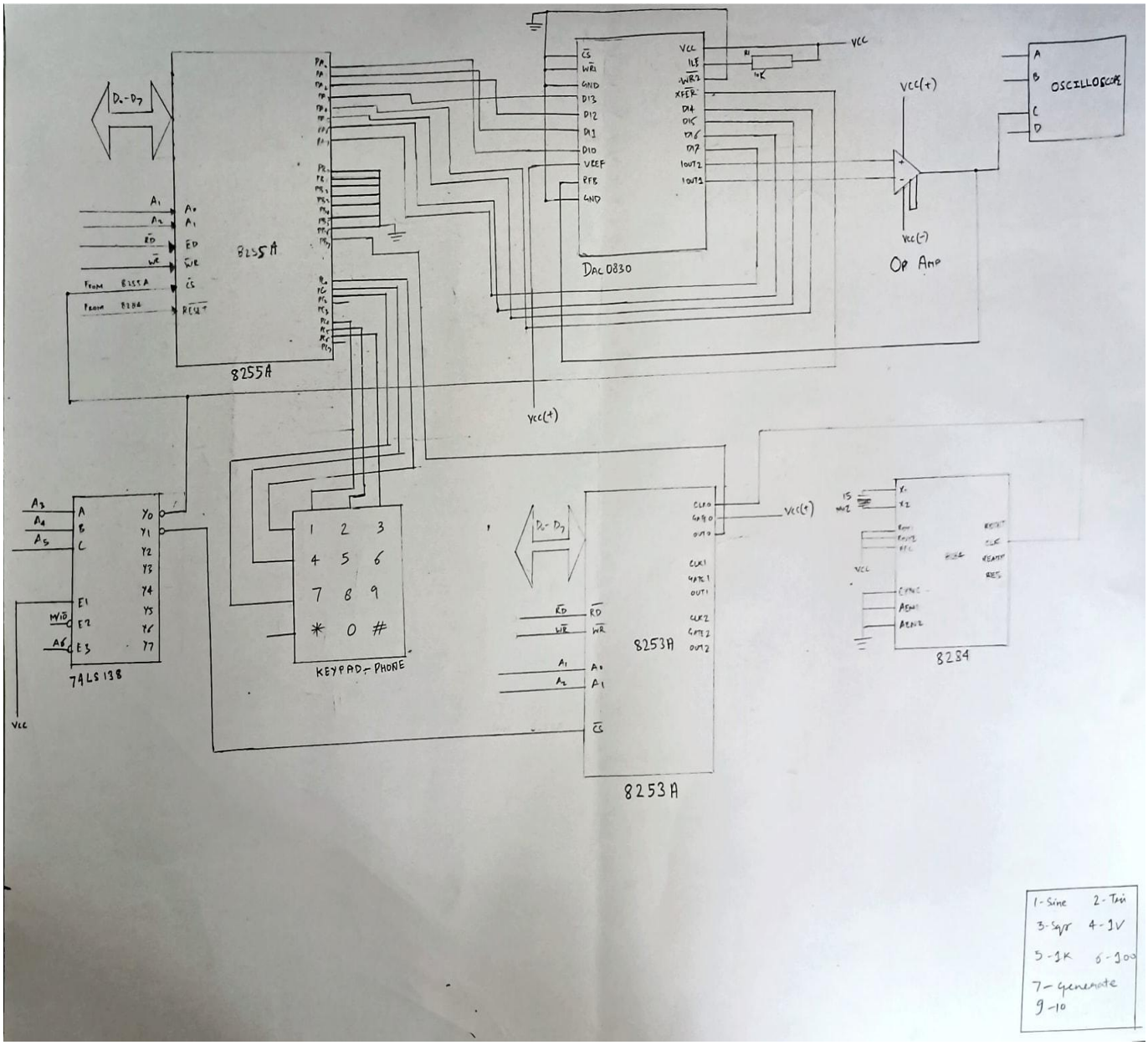
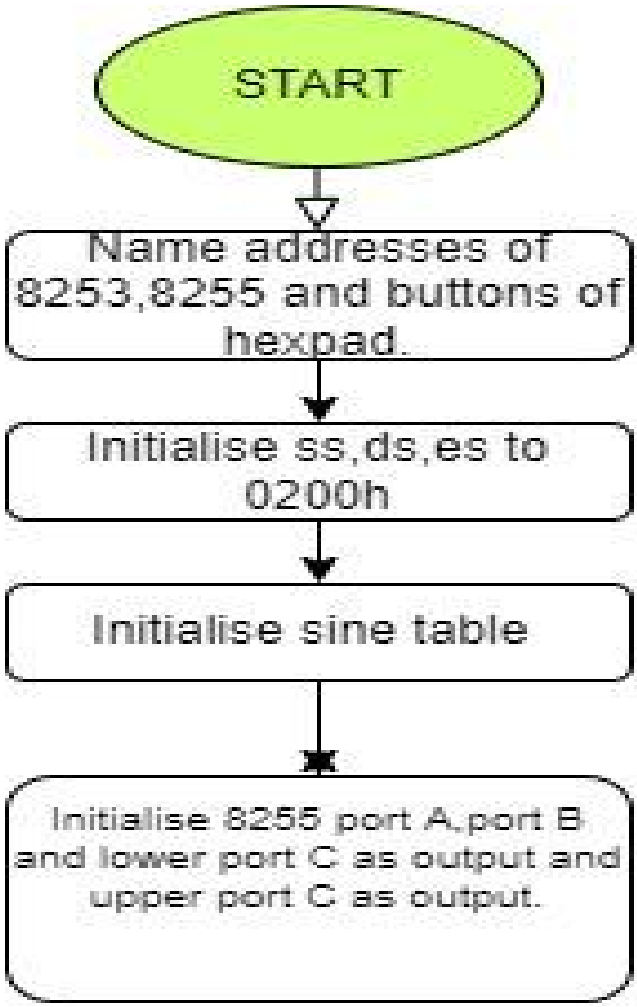


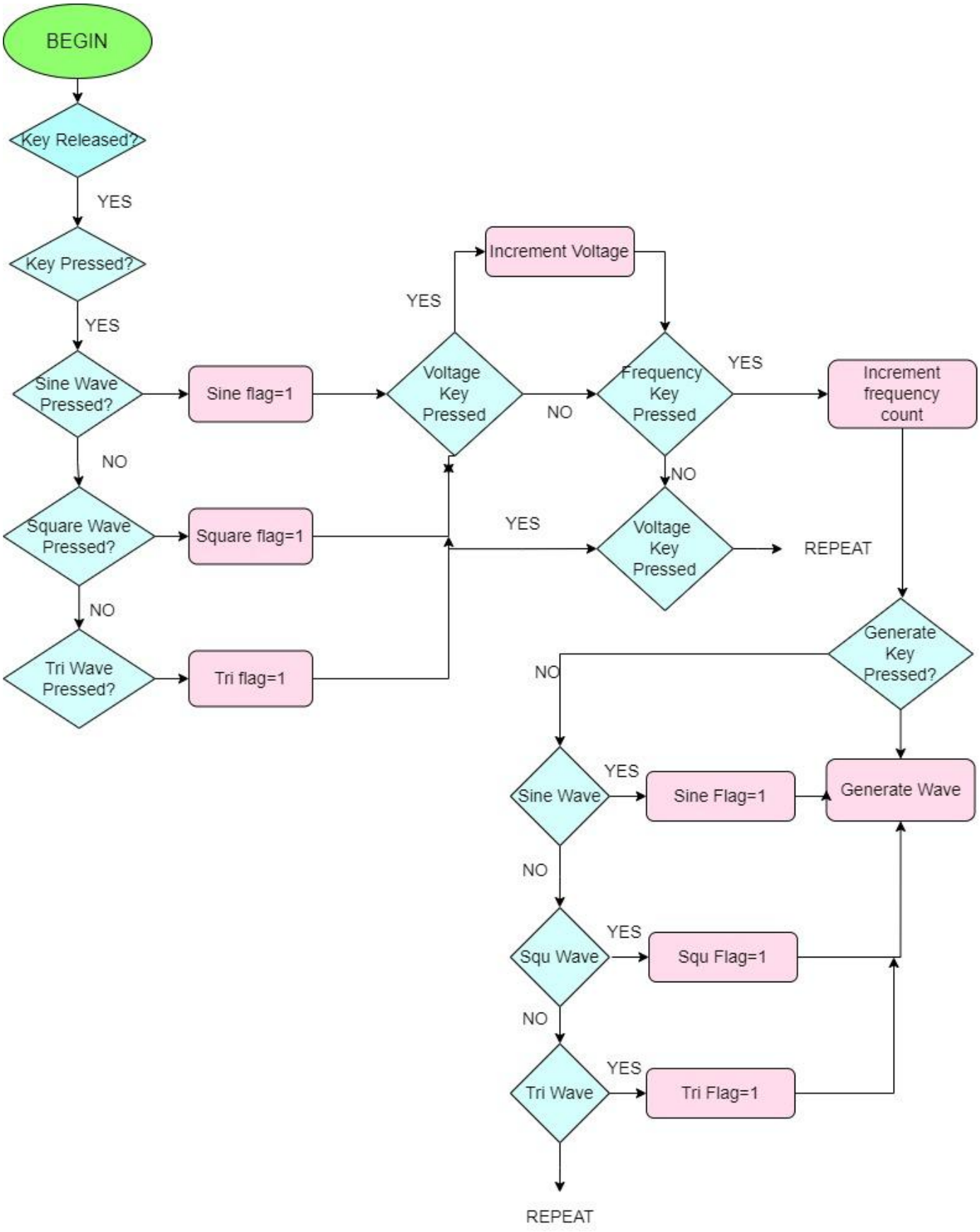
FIG:MAIN DESIGN

Flow Chart

Initialisation



MAIN PROGRAM



LIST OF ATTACHEMENTS:

1) DESIGN DIAGRAM (2 paper)