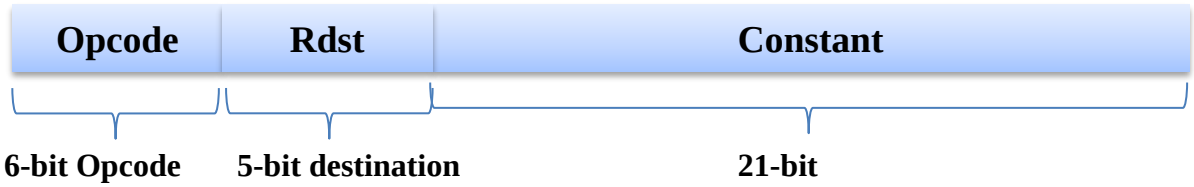
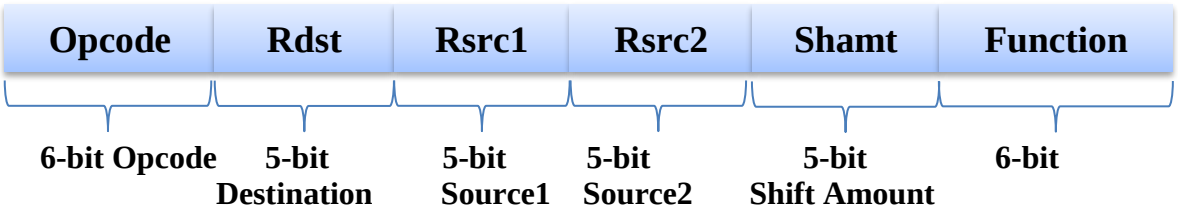
Assignment 1: Implementation of a processor (10Marks)

Design and implement (in Verilog) datapath and control unit for a single cycle processor (including instruction memory) which has two classes of instructions. The two classes of instructions along with the example usage and instruction decoding to be used are as below

1. **Immediate Type**
   Example: li r1, constant → loads immediate signed value specified in the instruction to the register R1



2. **Register Type (R-type)**
   Example: add r1, r2, r3 → adds the contents of registers r2 and r3. The result of addition is written in to the register r1



Assume there are 32 32-bit general purpose registers indicated by r0, r1, r2…r31 and corresponding register numbers (00000), (00001)……..(11111).
Assume the Opcode for Immediate type and R-type instructions as below

Instruction Class	Opcode
Immediate type	111111
Register Type	000000

Additionally R-type instructions have multiple variations defined by their function codes. The R-type instructions should include **add**, **sub**, **AND**, **OR**, **srl** (Shift right logical), **sll** (shift left logical) .The different R-type instructions that the processor should support are tabulated below.

R-type Instruction	Example usage	Opcode	Rdst	Rsrc1	Rsrc2	shamt	Function
add	**add r0, r1, r2**	**000000**	**00000**	**00001**	**00010**	**00000**	**100000**
sub	**sub r4, r5, r6**	**000000**	**00100**	**00101**	**00110**	**00000**	**100010**
AND	**and r8, r9, r10**	**000000**	**01000**	**01001**	**01010**	**00000**	**100100**
OR	**and r9, r8, r10**	**000000**	**01001**	**01000**	**01010**	**00000**	**100101**
sll	**sll r11, r6, 6**	**000000**	**01011**	**00110**	**00000***	**00110**	**000000**
srl	**srl r13, r9, 10**	**000000**	**01101**	**01001**	**00000***	**01010**	**000010**

*Second source is not used for shift operations

The processor module should have only two inputs CLK and Reset. When Reset is activated the Processor starts executing instructions from 0^{th} location of instruction memory.

As part of the assignment the following files should be submitted in zipped folder.

1. PDF version of this Document with all the Questions below answered with file name as **IDNO_NAME.pdf**.

2. Design Verilog Files for all the Sub-modules (including control unit).

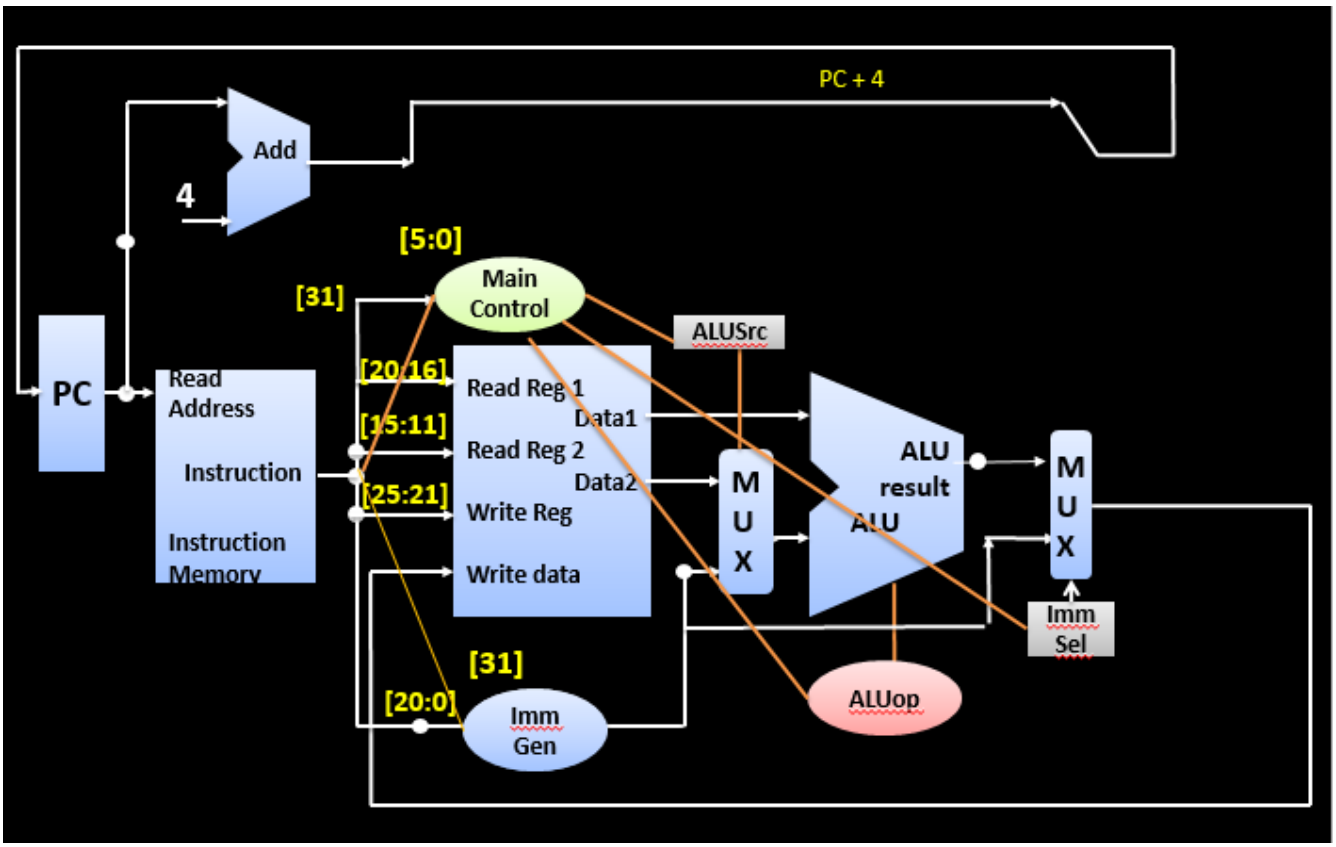
3. Design Verilog file for the main processor.

The name of the zipped folder should be in the format IDNO_NAME.zip

The due date for submission is 7-April-2020, 5:00 PM.

Q6.1. Draw the block level design of the processor (datapath + control unit) for above specifications. (you can modify the design given in the class ppts and copy the image of final design here)

Answer:



Q6.2. List the different blocks that will be required for implementation of datapath of the above processor.

Answer: instruction fetch unit,register file, ALU,two 2:1mux ,one 32-bit immediate generator block(named as sign extend in implementation)

Q6.3. Most of the datapath blocks that are listed above have already been implemented as part of previous labs. Implement the blocks which have not been implemented in the previous labs and copy the images of those Verilog codes here.

Answer: 2:1 writeback mux -

```
module writebackmux(
    input [31:0] data1,
    input [31:0] data2,
    input immsel,
    output reg [31:0] out
    );
always @(*)
begin
case(immsel)
0: out = data1;
1: out = data2;
endcase
end
endmodule
```

2:1 ALUinput mux-

```
module ALUsrcmux(
    input [31:0] data1,
    input [31:0] data2,
    input ALUsrc,
    output reg [31:0] aluinput
    );
always @(*)
begin
case(ALUsrc)
0: aluinput = data1;
1: aluinput = data2;
endcase
end

endmodule
```

sign extend block-

```
module signextend(
    input [20:0] imm,
    input insmsb,
    output reg [31:0] out
    );
reg [4:0] shamt;
always @(*)
begin
if(insmsb==1)
begin
out <= 32'b0+imm;
end
else
begin
shamt <= imm[10:6];
out <= 32'b0+shamt;
end
end

endmodule
```

control unit -

```
module controlunit(
    input insmsb,
    input [5:0] func,
    output reg ALUsrc,
    output reg [3:0] ALUop,
    output reg Immsel
    );
always @(*)
begin
if(insmsb==1)
begin
Immsel <= 1;
end
else
begin
ALUop <= {{func[5]},func[2:0]};
Immsel <= insmsb;
if(func[5]==0)
begin
ALUsrc = 1;
end
else
begin
ALUsrc = 0;
end
end
end
endmodule
```

Q6.4. Assume Main control unit generates all the control signals. List different control signals that will be required for the above processor. Also specify the value of the control signals for different

instructions.

Answer:

Control Signal Name →	**ALUop (4-bit)**	ALUsrc (1-bit)	Immsel (1-bit)		
li r1, 8	XXXX	X	1		
add r0, r1, r2	1000	0	0		
sub r4, r5, r6	1010	0	0		
and r8, r9, r10	1100	0	0		
and r9, r8, r10	1100	0	**0**		
sll r11, r6, 6	0000	1	0		
srl r13, r9, 10	0010	1	0		

Q6.5. Implement the main control unit and copy the <u>image</u> of Verilog code of Main control unit here.

Answer:

```
module controlunit(
    input insmsb,
    input [5:0] func,
    output reg ALUsrc,
    output reg [3:0] ALUop,
    output reg Immsel
    );
always @(*)
begin
if(insmsb==1)
begin
Immsel <= 1;
end
else
begin
ALUop <= {{func[5]},func[2:0]};
Immsel <= insmsb;
if(func[5]==0)
begin
ALUsrc = 1;
end
else
begin
ALUsrc = 0;
end
end
end
endmodule
```

Q6.6. Implement complete processor in Verilog (Instantiate all the datapath blocks and main control unit as modules). Copy the <u>image</u> of Verilog code of the processor here.

Answer:

```
21  module processor(
22      input clk,
23      input reset
24      );
25  wire [31:0] inscode;
26  wire [31:0] dataregl;
27  wire [31:0] data2;
28  wire [31:0] imm;
29  wire [31:0] muxinputALU;
30  wire [31:0] ALUoutput;
31  wire [31:0] writedata;
32  wire [3:0] ALUop;
33  wire ALUsrc;
34  wire [31:0] regtomux;
35  wire [31:0] muxtoalu;
36  wire Immsel;
37
38  insfetch il(.clk(clk),.reset(reset),
39  .inscode(inscode));
40
41  regfile id(.readregl(inscode[20:16]),.readreg2(inscode[15:11]),
42  .writereg(inscode[25:21]),.writedata(writedata),
43  .datal(dataregl),.data2(regtomux)
44  );
45
46  ALU i2(.datal(dataregl),.data2(muxtoalu),
47  .ALUop(ALUop),.result(ALUoutput)
48  );
49
50  signextend immgen(.imm(inscode[20:0]),.insmsb(inscode[31]),
51  .out(imm));
52
53  ALUsrcmux mux1(.datal(regtomux),.data2(imm),
54  .ALUsrc(ALUsrc),.aluinput(muxtoalu));
55
56  writebackmux wb(.datal(ALUoutput),.data2(imm),
57  .immsel(Immsel),.out(writedata));
58
59  controlunit cu(.insmsb(inscode[31]),.func(inscode[5:0]),
60  .ALUsrc(ALUsrc),.ALUop(ALUop),
61  .Immsel(Immsel));
62
63  always @(posedge clk)
64  begin
65  end
66
67  endmodule
```

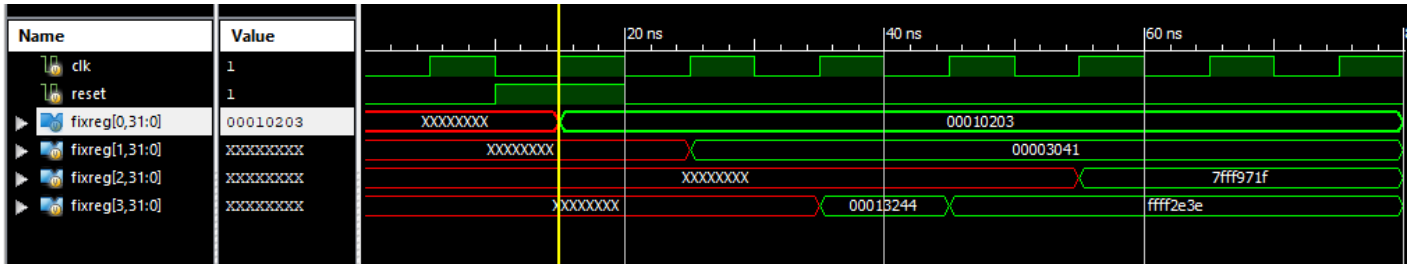
Q6.7. Test the processor design by initializing the instruction memory with a set of instructions (at least 5 instructions). List below the instructions you have used to initialize the instruction memory. Verify if the register file is changing according to the instructions. (Register file contains

unknowns, you can initialize the register file or you can load values into the register file using li instruction specified earlier).

Sequence of Instructions Implemented: li r0.0x10203
li r1,0x3041
add r3,r0,r1
sub r3,r1,r0
srl r2,r3,r1

Q6.8. Verify if the register file is getting updated according to your sequence of instructions (mentioned earlier).

Copy verified **Register file** waveform here (show only the Registers that get updated, CLK, and RESET):



Unrelated Questions

What were the problems you faced during the implementation of the processor?

Answer: verilog implementation of modules

Did you implement the processor on your own? If you took help from someone whose help did you take? Which part of the design did you take help for?

Answer: yes,took help from online sources like stackexchange,chipverify.com etc. and friends.Took help for the main processor block implementation and other verilog syntax related queries.

Honor Code Declaration by student:

- My answers to the above questions are my own work.
- I have not shared the codes/answers written by me with any other students. (I might have helped clear doubts of other students).
- I have not copied other's code/answers to improve my results. (I might have got some doubts cleared from other students).

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