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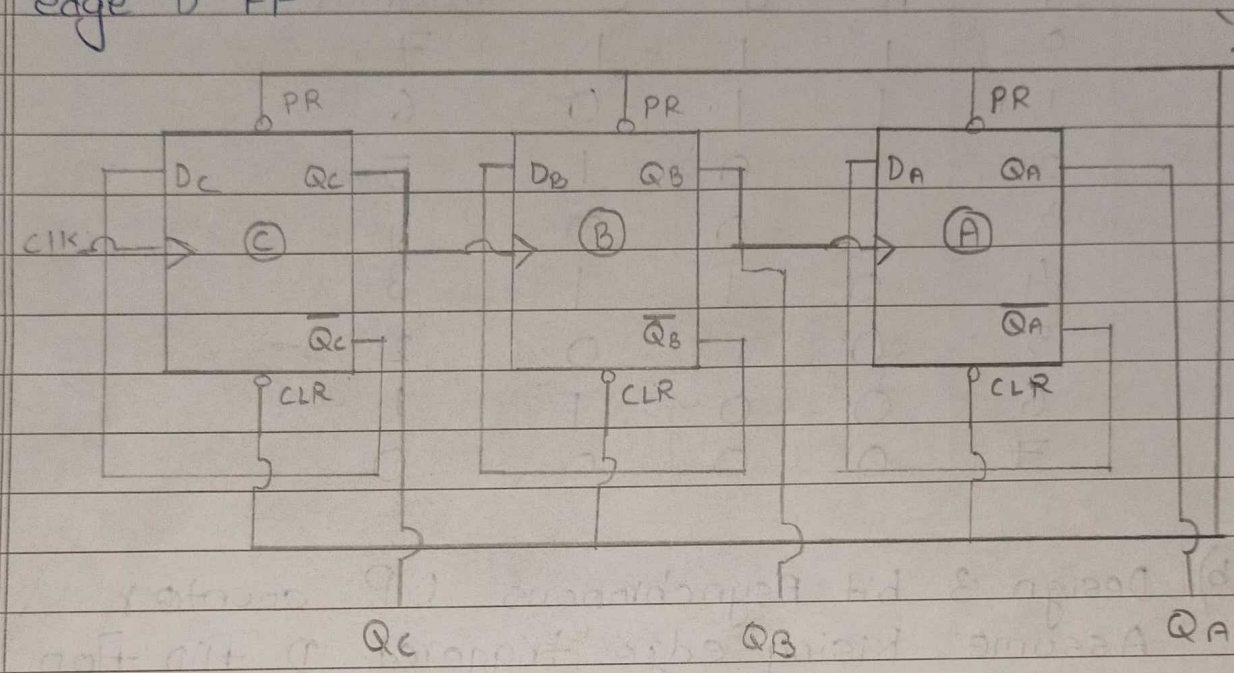
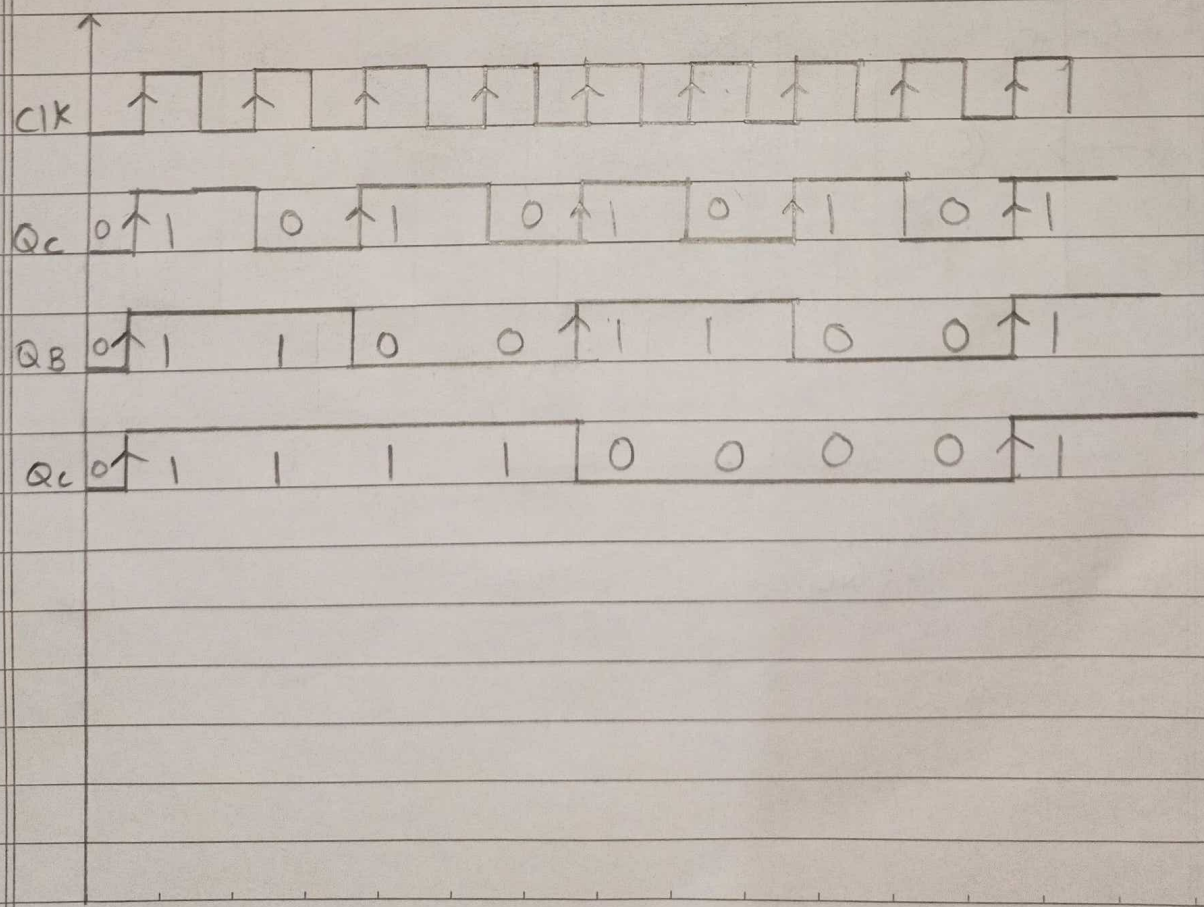
11/1/23

Digital Electronics TT-2

Q.1a) 3 bit Asynchronous down counter using rising edge D FF

→

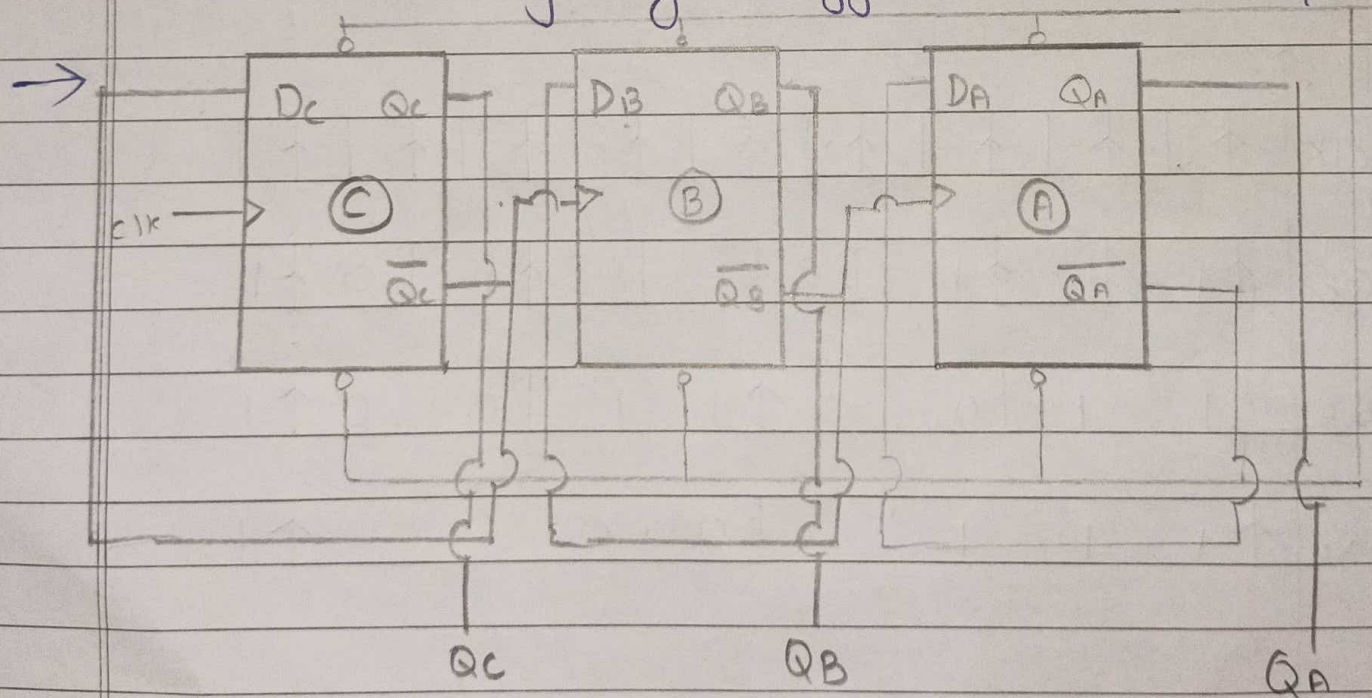


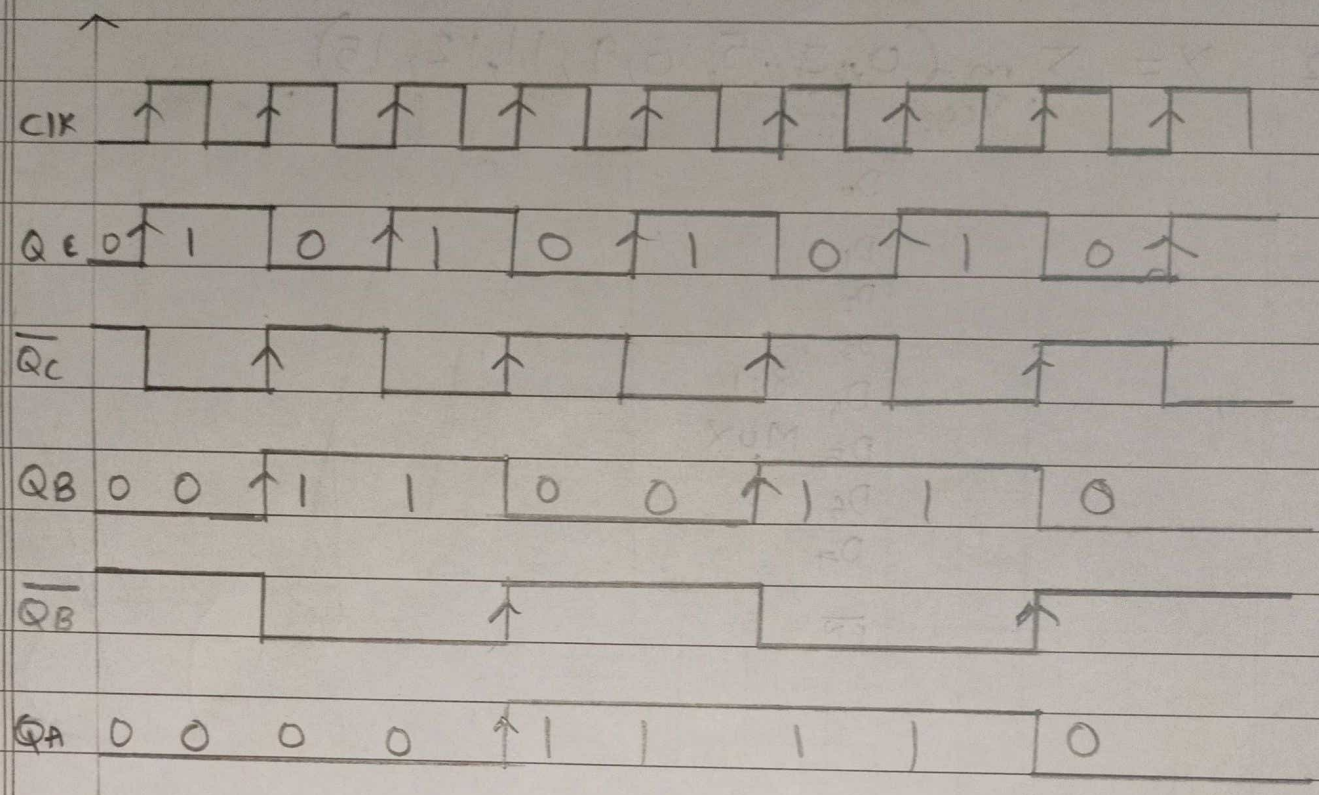


Observation Table.

CLK	A	B	C	Decimal
0	1	1	1	7
1	1	1	0	6
2	1	0	1	5
3	1	0	0	4
4	0	1	1	3
5	0	1	0	2
6	0	0	1	1
7	0	0	0	0

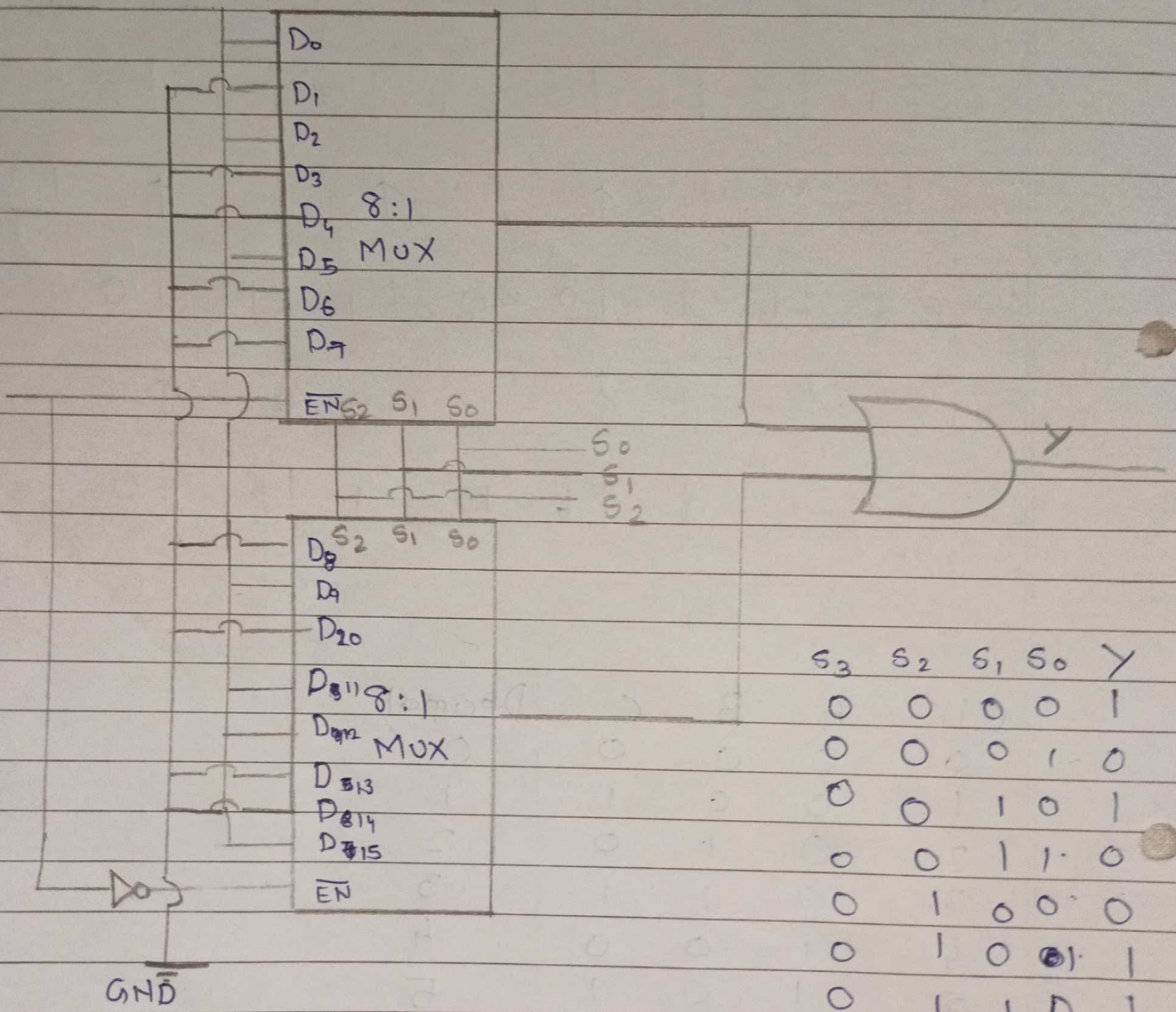
b) Design 3 bit Asynchronous UP counter
Assume Rising edge triggered D flip flop - logic





CLK	A	B	C	Decimal
0	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7

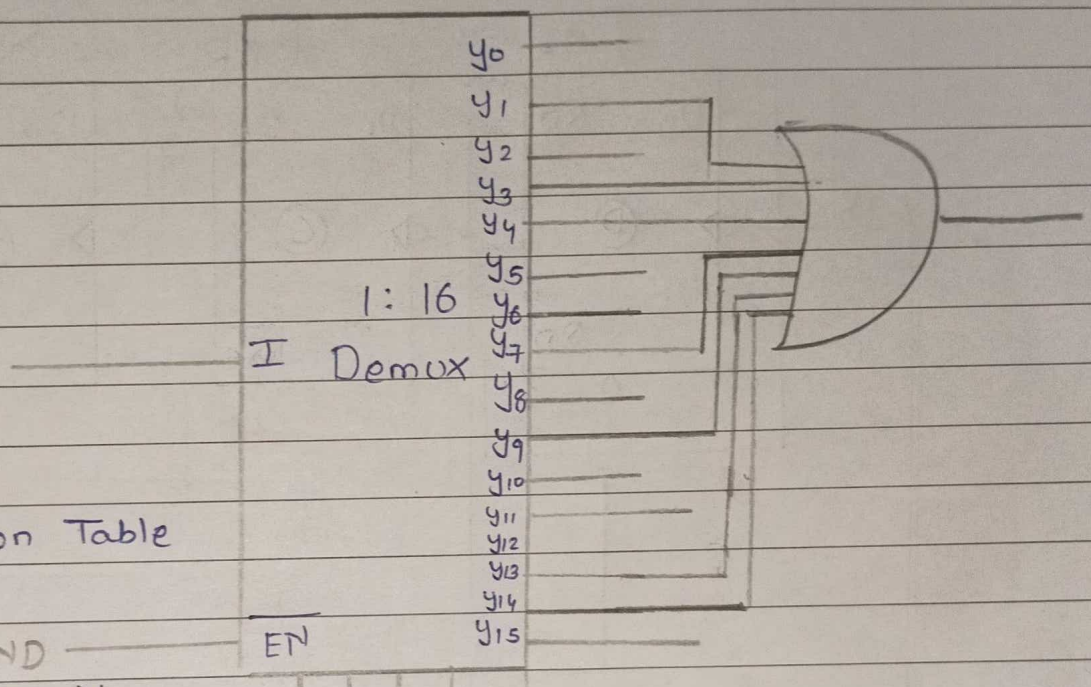
Q.2 $Y = \sum m (0, 2, 5, 6, 9, 11, 12, 15)$.



S_3	S_2	S_1	S_0	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

b) $Y = \Sigma m \, \Pi m (0, 2, 5, 6, 9, 11, 12, 15)$

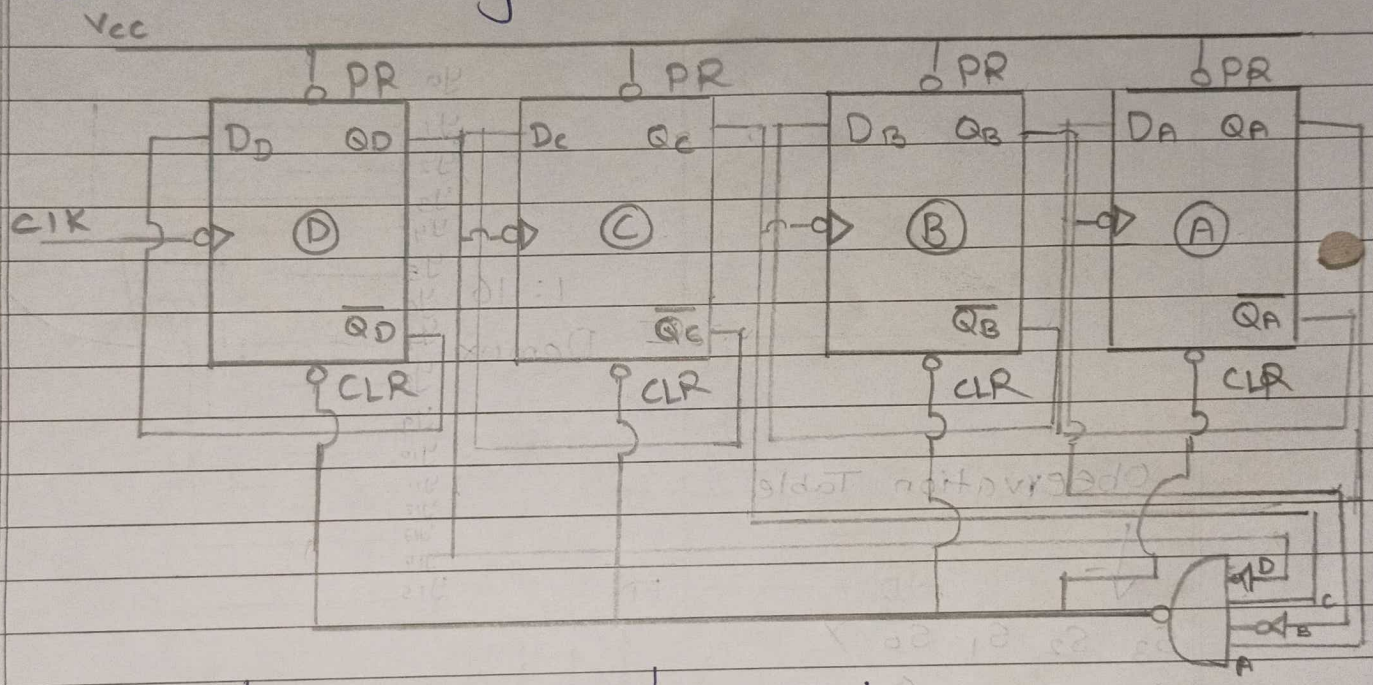
$Y = \Sigma m (1, 3, 4, 7, 8, 10, 13, 14)$.



Observation Table

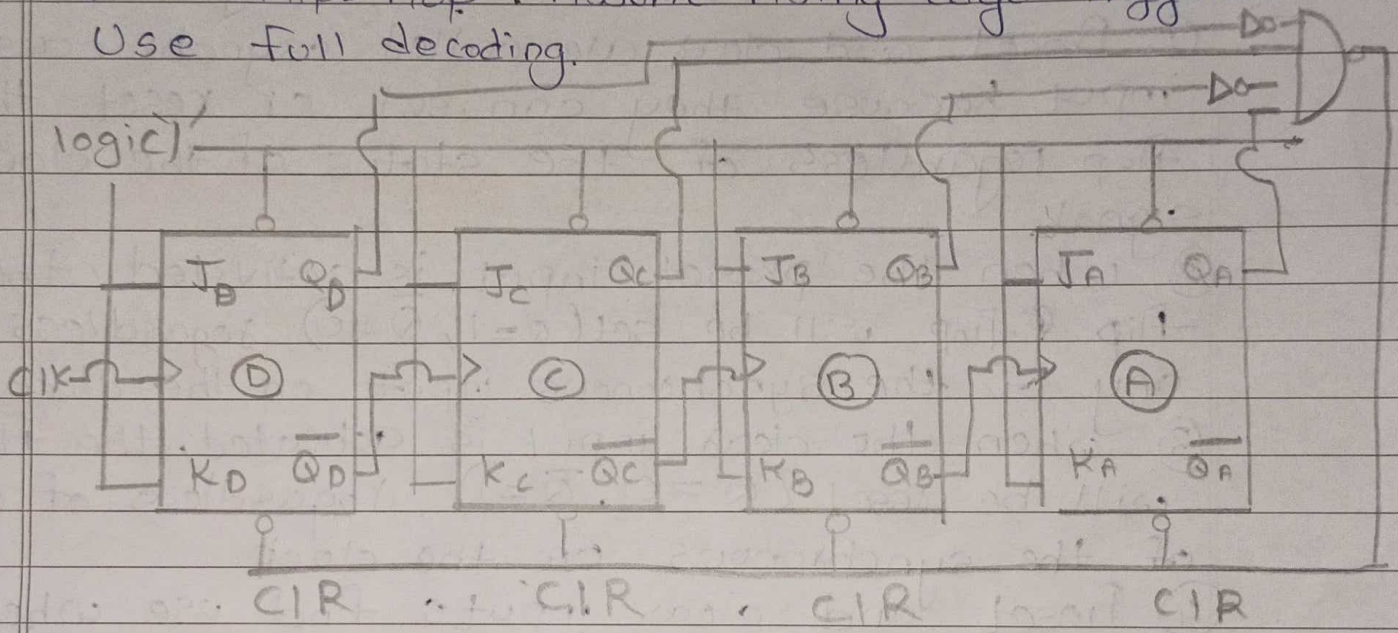
S_3	S_2	S_1	S_0	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Q.3a Design MoD 10 Asynchronous up-counter using D-flip-flop. Assume falling edge triggered. Use full decoding.



CLK	A	B	C	D	Decimal
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9
10	0	0	0	0	0

Q 3) Design MOD 10 Asynchronous up-counter using J-K flip-flop. Assume rising edge triggered. Use full decoding.



Observation Table:

CLK	A	B	C	D	Decimal
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	2
3	0	0	1	1	3
4	0	1	0	0	4
5	0	1	0	1	5
6	0	1	1	0	6
7	0	1	1	1	7
8	1	0	0	0	8
9	1	0	0	1	9
0	0	0	0	0	0

Q.4

a → Why are preset and clear referred as asynchronous inputs.

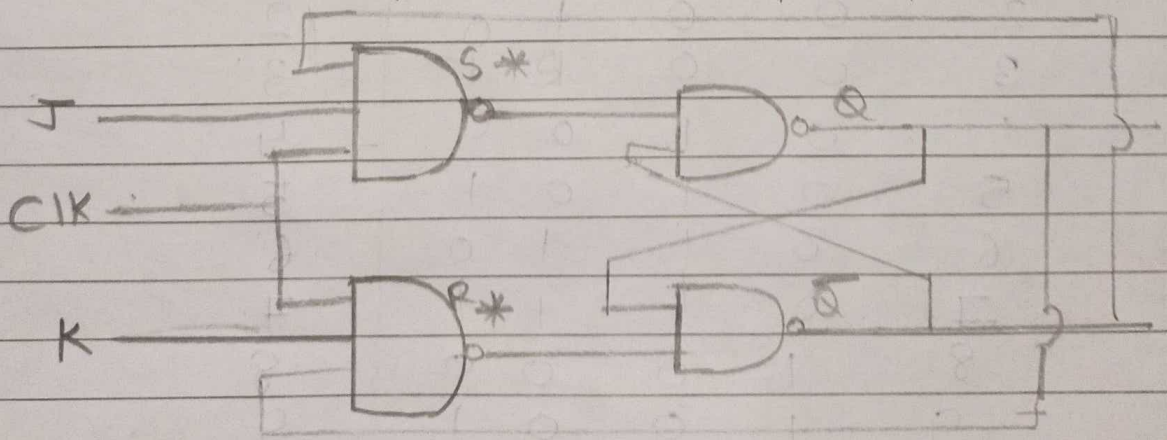
① Preset and clear are called asynchronous input because they can set or reset the flip flop regardless of the status of the clock signal.

② When the preset input is activated, the flip flop will be set ($Q=1, \overline{Q}=0$) regardless of any of the synchronous input on the clock.

③ When the clear input is activated, the flip flop will be reset ($Q=0, \overline{Q}=1$), regardless of any of the synchronous on the clock.

④ Preset and clear inputs find use when multiple flip-flops are ganged together to perform a function on a multi-bit binary word, and a single line is needed to set or reset them all at once.

Q.4 b) Draw and explain J-K flip flop.



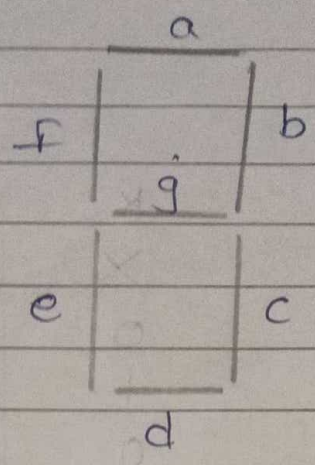
Truth Table:

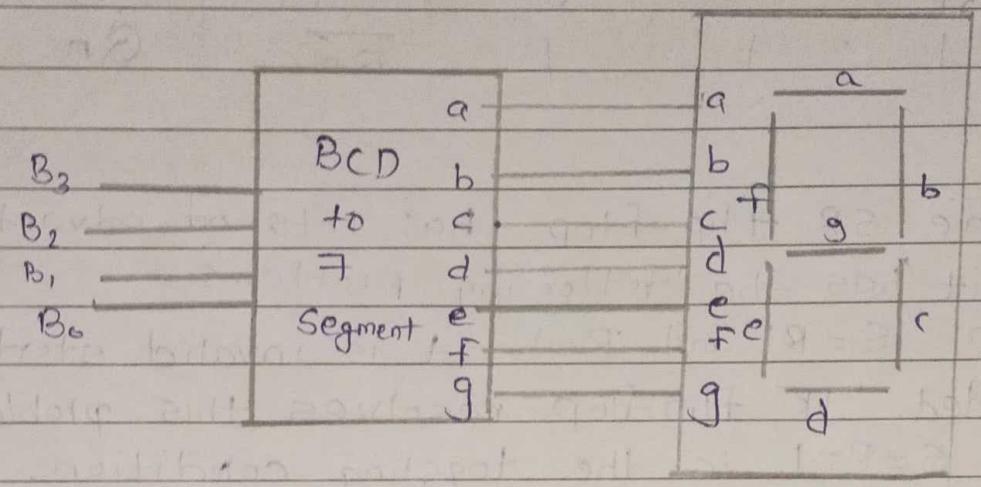
Clk	J	K	Q_{n+1}	$\overline{Q_{n+1}}$
0	X	X	Q_n	$\overline{Q_n}$
1	0	0	Q_n	$\overline{Q_n}$
1	0	1	0	1
1	1	0	1	0
1	1	1	$\overline{Q_n}$	Q_n

The SR flip flop has lots of advantages But it has the following problems.
when S = 1 and R = 1 it is invalid state and avoided. JK flip flop resolves this problem The S = R = 1 is the toggling condition.

Q.5 Explain seven segment display configuration. Also explain BCD to seven segment conversion.

→ ① Seven Segment display configuration has 7 LED lights and 1 (decimal point) LED.
② Each of the seven LED's is called a segment
③ Seven segment displays are used in digital clocks, basic calculators.
④ Segments are named from a to g.
⑤ According to the output required, we provide inputs to the seven segment and accordingly the LED's light up.





B_3	B_2	B_1	B_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

b) Explain way to achieve Binary to Excess-3 code

→ ① Excess-3 code can also be represented as XS-3 code.

② In Excess-3 code each digit of decimal number is represented by adding 3 in each decimal digit.

③ Following steps to convert the binary number into Excess-3 code

1) Convert the binary number into decimal
2) Add 3 in each digit of decimal numbet.
3) Find binary code of each digit of newly generated numbel.

Binary to Excess-3.

BCD				Excess-3			
A	B	C	D	w	x	y	z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

For W

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

$W = A + BD + BC$

For X

AB \ CD	00	01	11	10
00	0	1	1	1
01	1	0	0	0
11	X	X	X	X
10	0	1	X	X

$X = B\bar{C}\bar{D} + \bar{B}D + \bar{B}C$

For Y

AB \ CD	00	01	11	10
00	1	0	1	0
01	1	0	1	0
11	X	X	X	X
10	1	0	X	X

$Y = \overline{C\bar{D}} + CD$

For Z

AB \ CD	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

$Z = \overline{C\bar{D}} + C\bar{D}$