

## Experiment 1.

Aim : To study and verify the truth tables of various logic gates using ICs and to realize basic gates and universal gates.

7408 - AND

7432 - OR

7404 - NOT

7400 - NAND

7402 - NOR

7486 - XOR

747266 - XNOR

74151 - MUX 8:1

74138 - DeMUX 8:1

7474 - D flip flop (rising edge)

7476 - JK flip flop (falling edge)

### AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



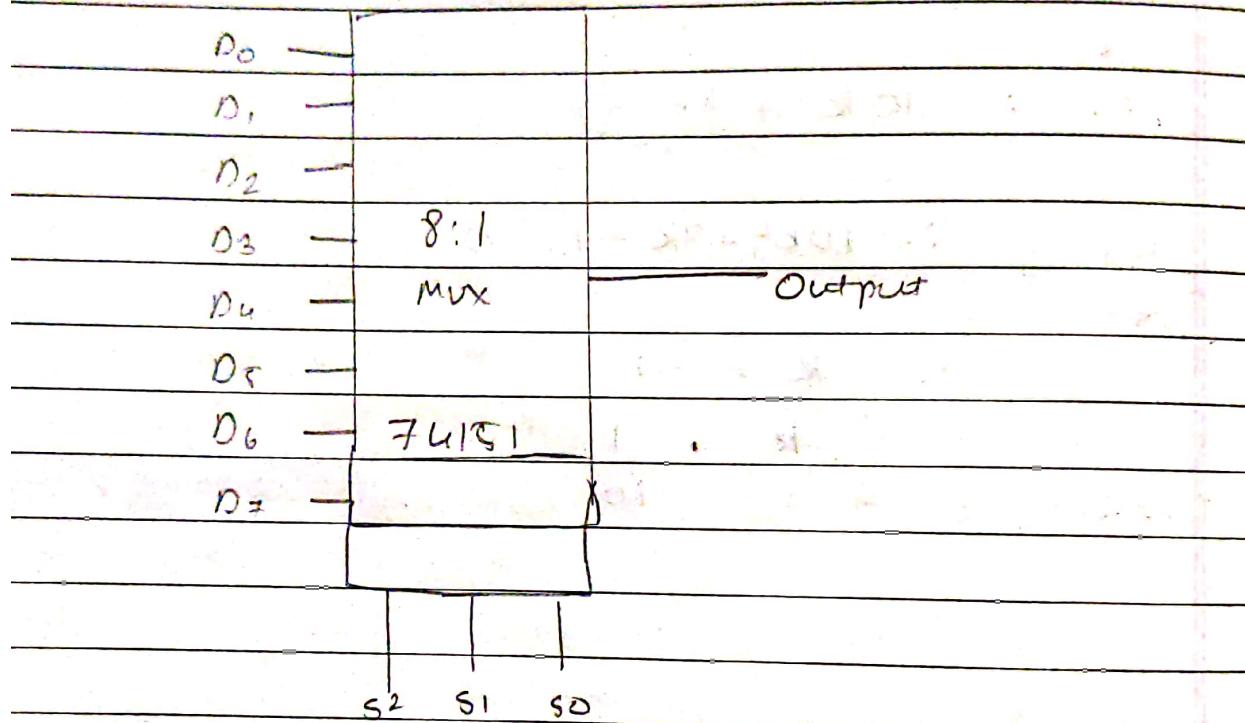
Symbol

### NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



Symbol



8:1 mux circuit diagram.

XOR

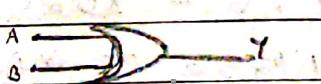
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



symbol

OR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



Symbol

NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



Symbol

NOT

A	B	Y
0		1
1		0



Symbol

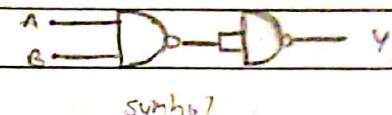
NOT using NAND

A	Y
0	1
1	0



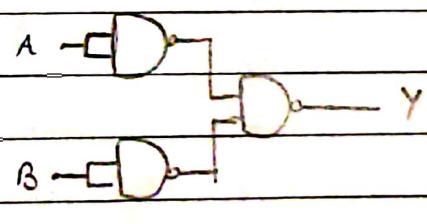
AND using NAND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



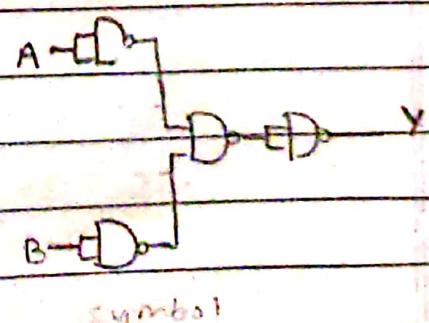
OR using NAND

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



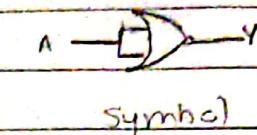
NOR using NAND

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



NOT using NOR.

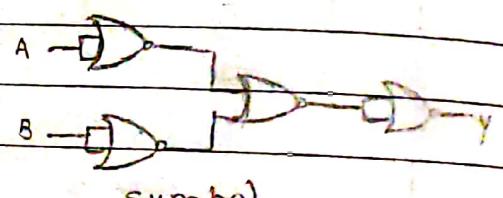
A	Y	
0	1	
1	0	



Symbol)

NAND using NOR

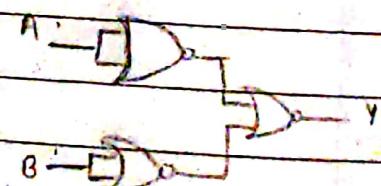
A	B	Y	
0	0	1	
0	1	1	
1	0	1	
1	1	0	



Symbol)

AND using NOR

A	Y	B	Y	
0	0	0	0	
0	1	1	0	
1	0	0	0	
1	1	1	1	



Symbol)

OR using NOR.

A	B	Y	
0	0	0	
0	1	1	
1	0	1	
1	1	1	



Symbol)

## Experiment 2

Aim: Logic Simplification, Implementation using basic gates.

Given Expression.

$$\rightarrow (A + C)(CD + AC)$$

$$ACD + AAC + CCD + ACC$$

$$ACD + AC + CD + AC$$

$$ACD + AC + AC + CD$$

$$AC + ACD + CD$$

$$AC(1 + D) + CD$$

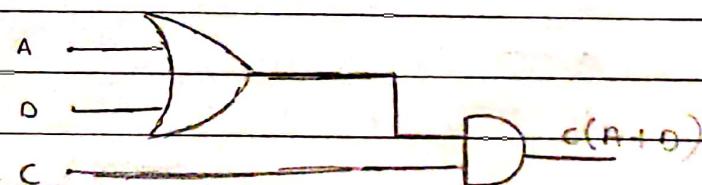
$$AC + CD$$

$$C(A + D)$$

Kmap

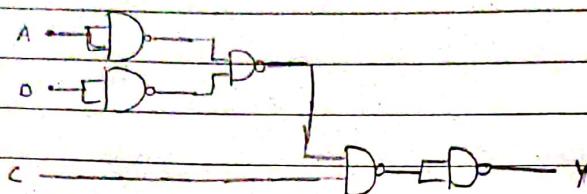
		CD	00	01	11	10
		A	0	0	0	1
C	D	0	0	0	1	0
		1	0	1	1	0

$$= C(A + D)$$

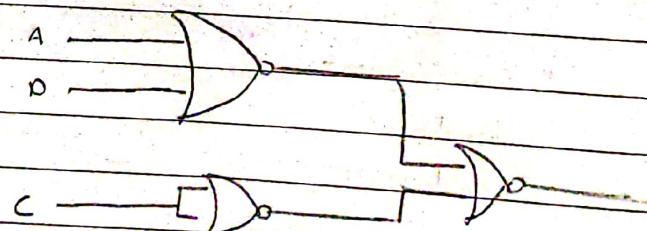
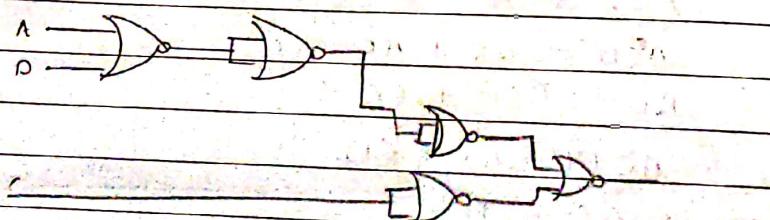


A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

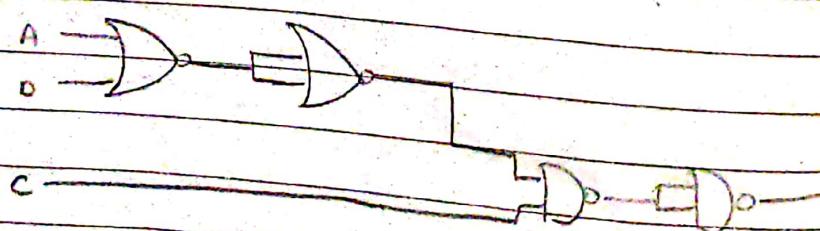
Given Expression using Universal Gates. (NAND)



Given Expression using Universal Gates (NOR)



Given Expression using Universal gates (NAND & NOR)

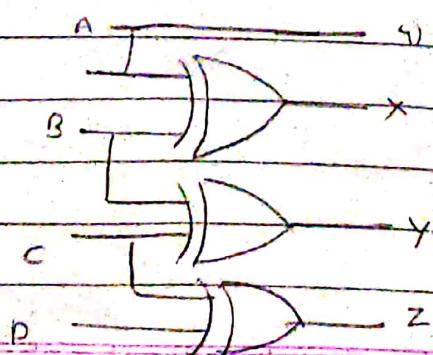


### Experiment 4:

Aim: To realize binary to gray code converter and gray code to binary converter.

#### Binary to Gray Converter

Binary to Gray Converter							
Binary	Gray						
A	B	C	D	w	x	y	z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0



Kmap

w

$\bar{A}B$	$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$
$\bar{A}B$	0 <sub>0</sub>	0 <sub>1</sub>	0 <sub>3</sub>	0 <sub>2</sub>
$\bar{A}B$	0 <sub>4</sub>	0 <sub>5</sub>	0 <sub>7</sub>	0 <sub>6</sub>
$AB$	1 <sub>12</sub>	1 <sub>3</sub>	1 <sub>15</sub>	1 <sub>14</sub>
$A\bar{B}$	1 <sub>8</sub>	1 <sub>9</sub>	1 <sub>11</sub>	1 <sub>10</sub>

$$= A$$

x

$\bar{A}B$	$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$
$\bar{A}B$	0	0	0	0
$\bar{A}B$	1	1	1	1
$AB$	0	0	0	0
$A\bar{B}$	1	1	1	1

$$\rightarrow \bar{A}B + A\bar{B}$$

$$\rightarrow A \oplus B$$

y

$\bar{A}B$	$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$
$\bar{A}B$	0	0	1	1
$\bar{A}B$	1	1	0	0
$AB$	1	1	0	0
$A\bar{B}$	0	0	1	1

$$\rightarrow B\bar{C} + C\bar{B}$$

$$\rightarrow B \oplus C$$

z

$\bar{A}\bar{B}$	$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$
$\bar{A}\bar{B}$	0 <sub>0</sub>	1 <sub>1</sub>	0 <sub>3</sub>	1 <sub>2</sub>
$\bar{A}B$	0 <sub>2</sub>	1 <sub>5</sub>	0 <sub>7</sub>	1 <sub>6</sub>
$AB$	0 <sub>14</sub>	1 <sub>8</sub>	0 <sub>15</sub>	1 <sub>16</sub>
$A\bar{B}$	0 <sub>8</sub>	1 <sub>9</sub>	0 <sub>11</sub>	1 <sub>10</sub>

Gray to Binary

w	x	y	z	A	B	C	D
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

A

	$\bar{y}_2$	$\bar{y}_2$	$\bar{y}_2$	$\bar{y}_2$	$\bar{y}_2$
$\bar{w}\bar{x}$	0	0	0	0	
$\bar{w}x$	0	0	0	0	
$w\bar{x}$	1	1	1	1	
$wx$	1	1	1	1	

w

$w$	$\bar{w}$	$y_1$	$\bar{y}_1$	$y_2$	$\bar{y}_2$	$y_3$	$\bar{y}_3$
$w_x$	0	0	0	0	0	0	0
$\bar{w}_x$	1	1	1	1	1	1	1
$w_x$	0	0	0	0	0	0	0
$\bar{w}_x$	1	1	1	1	1	1	1

$$\bar{w}_x + w\bar{x}$$

$$= w \oplus x$$

$w$	$\bar{w}$	$y_1$	$\bar{y}_1$	$y_2$	$\bar{y}_2$	$y_3$	$\bar{y}_3$
$\bar{w}_x$	0	0	1	1	1	1	1
$w_x$	1	1	0	0	0	0	0
$w_x$	0	0	1	1	1	1	1
$\bar{w}_x$	1	1	0	0	0	0	0

$$\rightarrow y$$

$$w \oplus x \oplus y$$

$w$	$\bar{w}$	$y_1$	$\bar{y}_1$	$y_2$	$\bar{y}_2$	$y_3$	$\bar{y}_3$
$\bar{w}_x$	0	1	0	1	0	1	0
$\bar{w}_x$	1	0	1	0	1	0	1
$w_x$	0	1	0	1	0	1	0
$w_x$	1	0	1	1	0	0	1

$$\rightarrow z$$

$$w \oplus x \oplus y \oplus z$$



w

$w \oplus x$



$w \oplus x \oplus y$



$w \oplus x \oplus y \oplus z$

Gray to Binary.

Gray

Binary

A	B	C	D		w	x	y	z
0	0	0	0		0	0	0	0
0	0	0	1		0	0	0	1
0	0	01	0		0	0	1	1
0	0	01	1		0	0	1	0
0	1	0	0		0	1	1	1
0	1	0	1		0	1	1	0
0	1	1	0		0	1	0	0
0	1	1	1		0	1	0	1
1	0	0	0		1	1	1	1
1	0	0	1		1	1	1	0
1	0	1	0		1	1	0	0
1	0	1	1		1	1	0	1
1	1	0	0		1	0	0	0
1	1	0	1		1	0	0	1
1	1	1	0		1	0	1	1
1	1	1	1		1	0	1	0

## Experiment 5

j) Half Adder.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

S

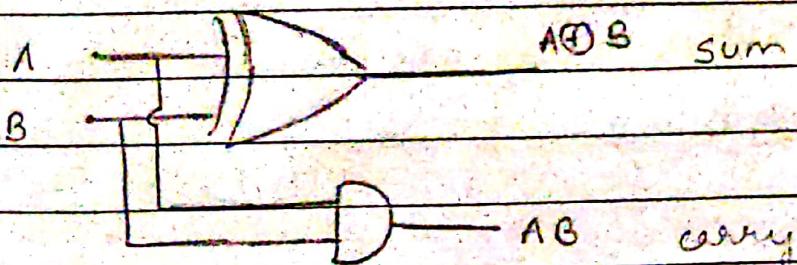
A	$\bar{B}$	B
$\bar{A}$	0	1
A	1	0

C

$\bar{A}$	$\bar{B}$	B
A	0	0
A	0	1

$$= A \oplus B$$

$$= AB$$



## ii) Full Adder

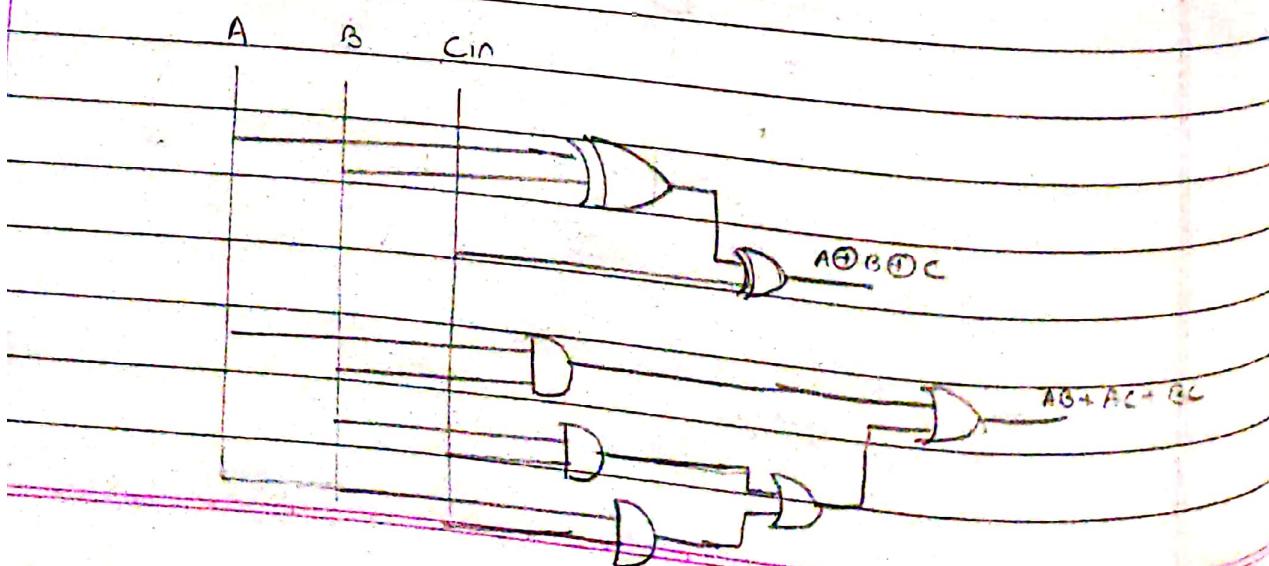
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

S	$\bar{B}\bar{C}in$	$\bar{B}Cin$	$B\bar{C}in$	$BC\bar{in}$
$\bar{A}$	0	1	0	1
A	1	0	1	0

$$= A \oplus B \oplus C_{in}$$

Cout	$\bar{B}\bar{C}in$	$\bar{B}Cin$	$B\bar{C}in$	$BC\bar{in}$
$\bar{A}$	0	0	1	0
A	0	1	1	1

$$= AB + A C_{in} + BC_{in}$$



### iii) Half Subtractor.

A	B	D	Bout
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

D

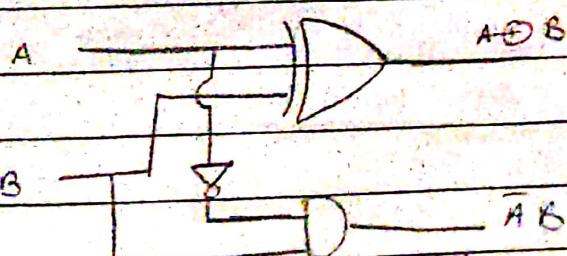
	$\bar{B}$	B
$\bar{A}$	0	1
A	1	0

$$= A \oplus B$$

Bout

	$\bar{B}$	B
$\bar{A}$	0	1
A	0	0

$$= \bar{A}B$$



## iv) Full Subtractor.

A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

D

	$\bar{B}B_{in}$	$\bar{B}B_{in}$	$BB_{in}$	$BB_{in}$
$\bar{A}$	0	1	0	1
A	1	0	1	0

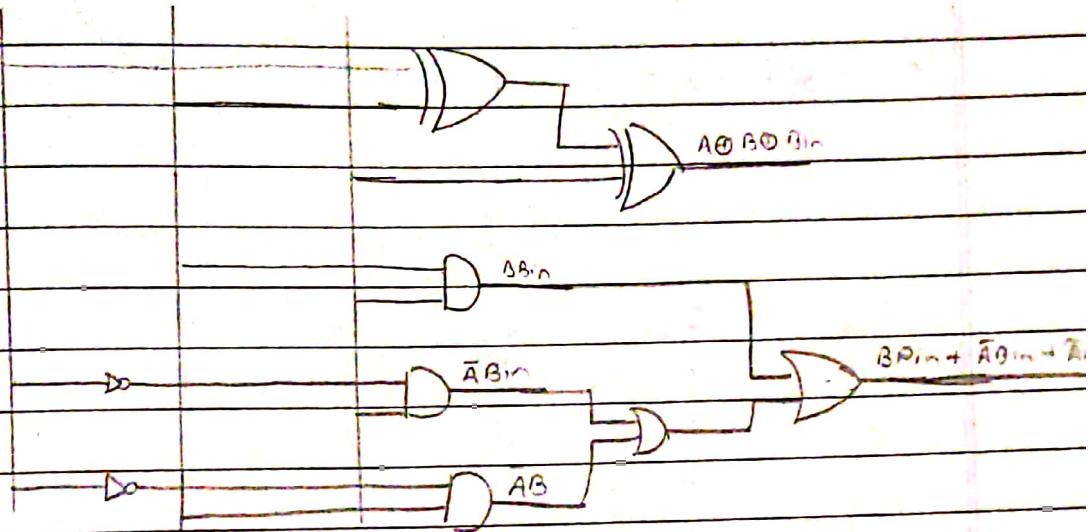
$$= A \oplus B \oplus B_{in}$$

Bout

	$\bar{B}B_{in}$	$\bar{B}B_{in}$	$BB_{in}$	$BB_{in}$
$\bar{A}$	0	1	1	1
A	0	0	1	0

$$= BB_{in} + \bar{A}B_{in} + AB$$

A      B      Bin

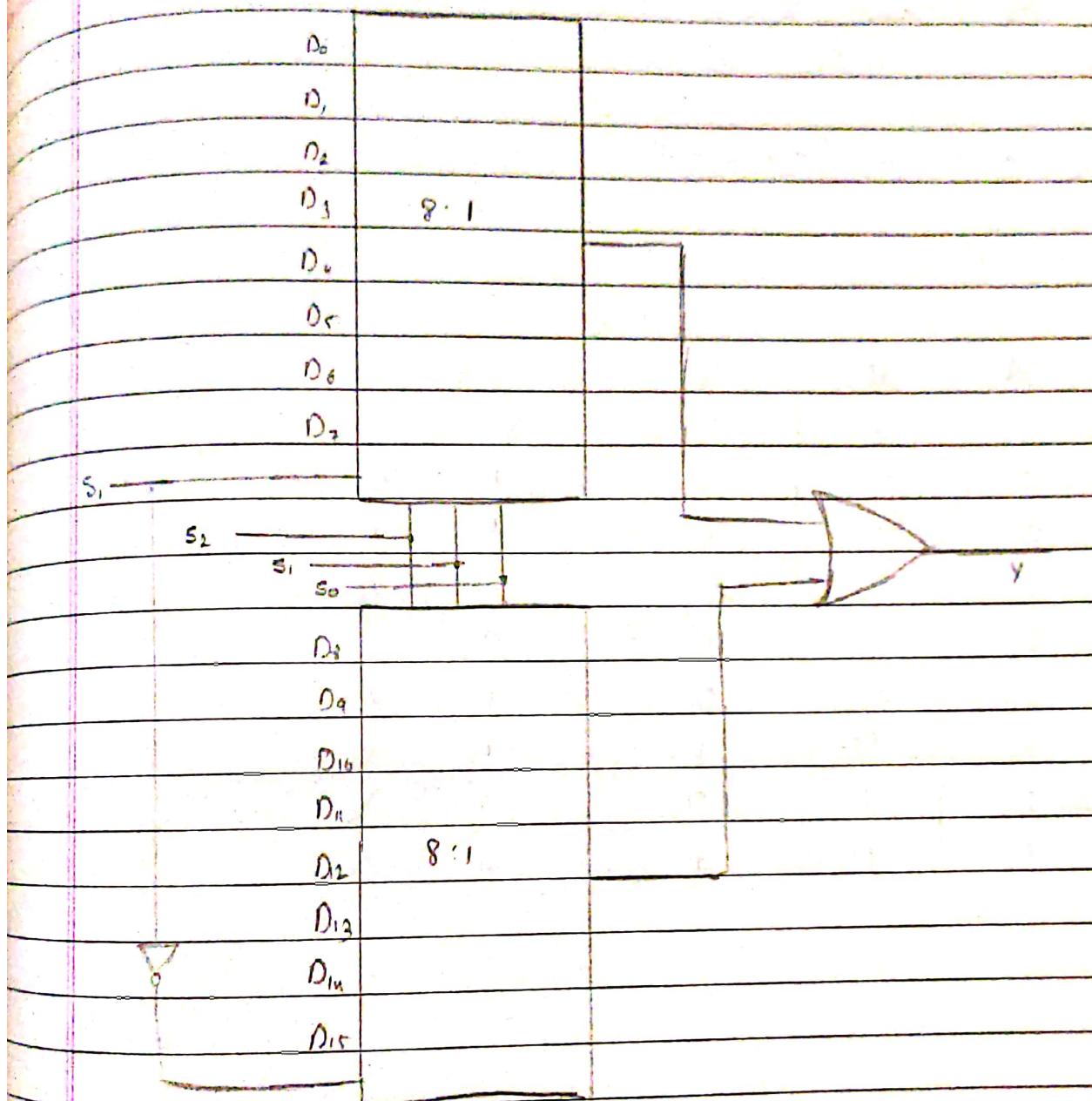


Full Subtractor

### Experiment 6.5

$$Y = \sum m (0, 5, 4, 6, 9, 11, 12)$$

$S_3$	$S_2$	$S_1$	$S_0$	$Y$	
0	0	0	0	1	$D_0$
0	0	0	1	0	$D_1$
0	0	1	0	0	$D_2$
0	0	1	1	0	$D_3$
0	1	0	0	1	$D_4$
0	1	0	1	1	$D_5$
0	1	1	0	1	$D_6$
0	1	1	1	0	$D_7$
1	0	0	0	0	$D_8$
1	0	0	1	1	$D_9$
1	0	1	0	0	$D_{10}$
1	0	1	1	1	$D_{11}$
1	1	0	0	1	$D_{12}$
1	1	0	1	0	$D_{13}$
1	1	1	0	0	$D_{14}$
1	1	1	1	0	$D_{15}$



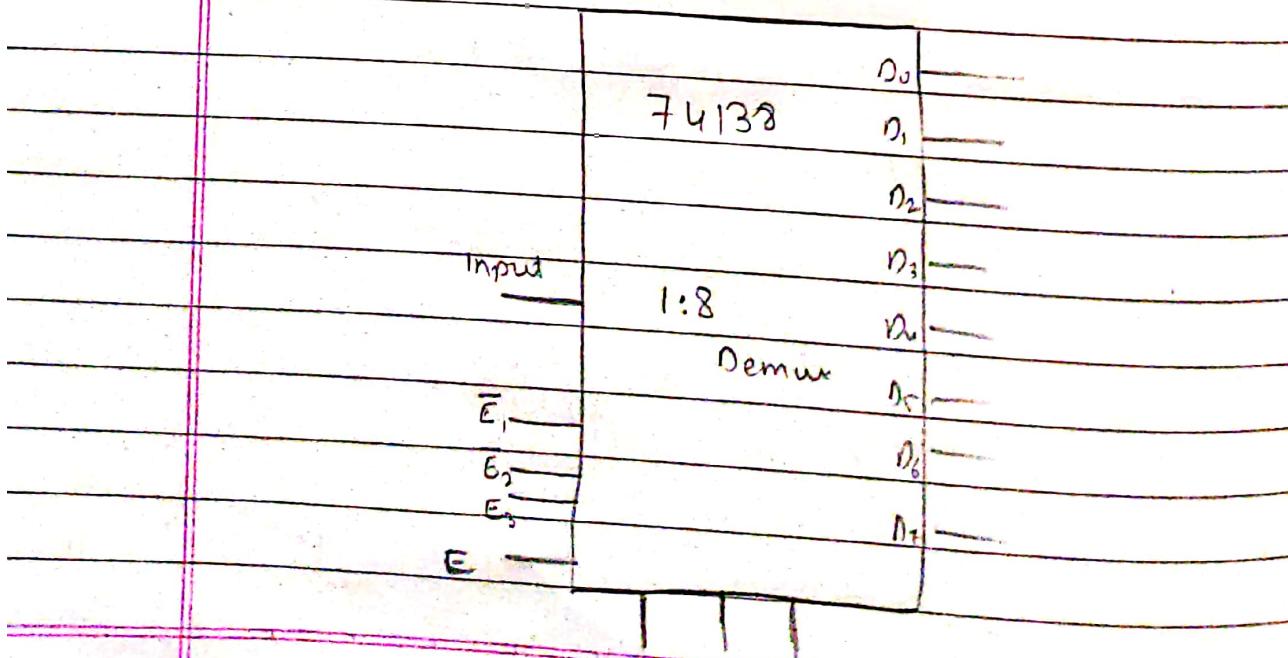
Circuit diagram of 16:1 using 8:1

### Experiment 6

$$y = \sum m(0, 1, 4, 5)$$

M

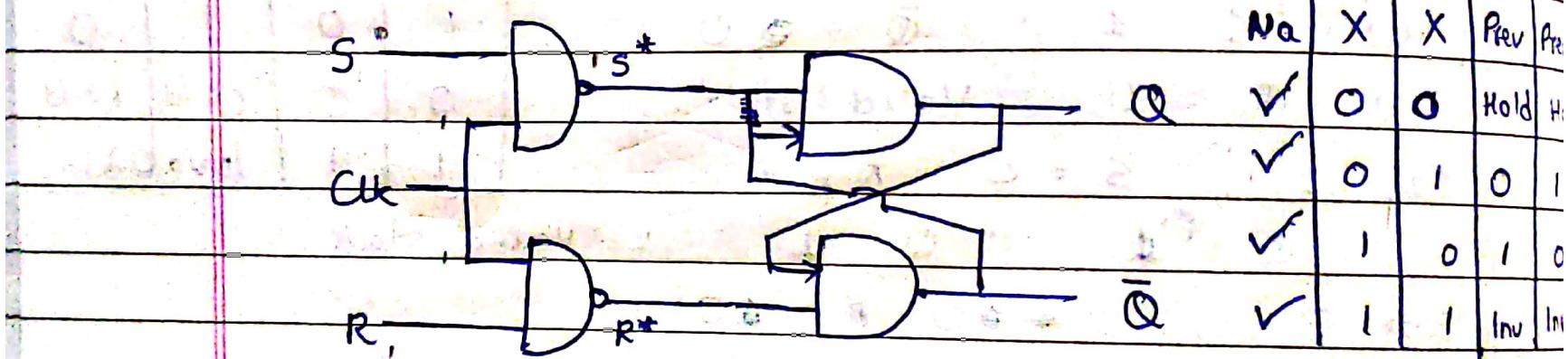
A	B	C		y	
S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>			
0	0	0		1	y <sub>0</sub>
0	0	1		1	y <sub>1</sub>
0	1	0		0	y <sub>2</sub>
0	1	1		0	y <sub>3</sub>
1	0	0		1	y <sub>4</sub>
1	0	1		1	y <sub>5</sub>
1	1	0		0	y <sub>6</sub>
1	1	1		0	y <sub>7</sub>



## → Flip Flop

- Basic digital memory circuit.
- Can be designed using NAND or NOR gates.
- One bit memory cell. (Stores one bit of binary memory)
- The value is maintained until changed.
- Multiple type.

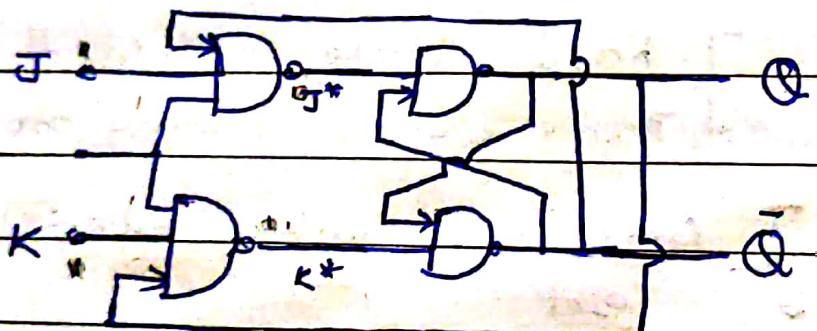
## → SR Flipflop. (using NAND)



The S & R are along with a clock signal. If there is no clock pulse, no difference is created by any value of S or R. The Output remains the same as it was.

A JK flip flop is 75% same as the SR flip flop. The first three cases in a JK flip flop are also same that of SR flip flop. But case 4 in SR flip flop is stated as invalid when value of S & R = 1.

This invalid issue caused due to SR flip flop is tried to be resolved using the JK flip flop.



C	J	K	Q	$\bar{Q}$
X	X	X	Prev	Prev
✓	0	0	hold	hold
✓	0	1	0	1
✓	1	0	1	0
✓	1	1	tog	tog

→ The first three cases of the JK flip flop remain the same as that of the SR flip flop however in the last state when  $S = 1$  &  $R = 1$  or  $J = 1$  &  $K = 1$

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- D flip flop. (Also called Transparent flipflops)
- single input d.
- clock.
- Output ( $Q$  &  $\bar{Q}$ )
- Whatever the input is, same is the output.

D	Q	$\bar{Q}$
0	0	1
1	1	0

The value of D remains same throughout.

### Characterisation Table,

D.	Q.	$Q_{n+1}$
0	0	0
0	1	0
1	0	1
1	1	1

No use of Q as whatever is the input, same is the output.

### Excitation table,

Q	$Q_{n+1}$	D
0	0	0
0	1	1
1	0	0
1	1	1

Because  $Q_{n+1}$  is the same as D.

D stays constant.

$$Q_{n+1} = D.$$

### T flip-flop

- Single Input t
- Toggle flip flop.
- clock.
- Output.
- $Q$  &  $\bar{Q}$

**④ ⑤ Converting flipflops -**

- use characterisation table of flipflop required
- use excitation table of flipflop given

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T	Q	$\bar{Q}$
0	Q	$\bar{Q}$
1	$\bar{Q}$	Q

When  $T = 0$ , output has no changes detected.

When  $T = 1$ , toggle takes place.

Characteristic Table

Excitation Table

T	Q	$Q_{n+1}$	T	Q	$Q_{n+1}$	T
0	0	0		0	0	0
0	1	1		0	1	1
1	0	1		1	0	1
1	1	0		1	1	0

$$Q_{n+1} = T \oplus Q_n$$

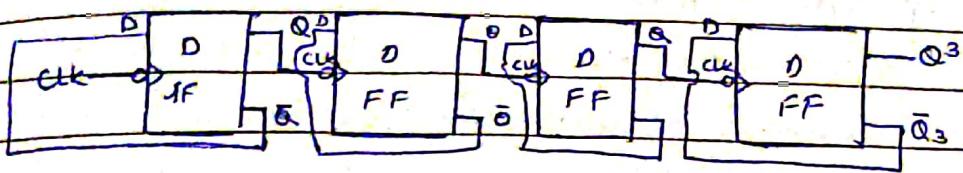
existing flipflops.

Now we are told to convert an SR flipflop or D flipflop to a given flipflop. The most important things are:-

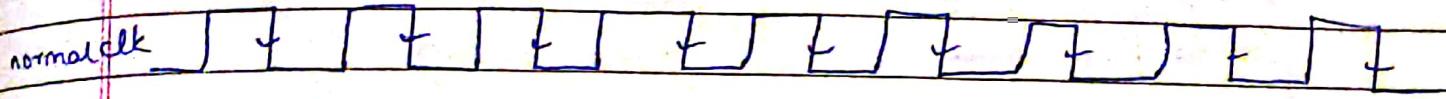
We mean that the SR flipflop should behave like a D flipflop. It should yield output as a D flipflop. We must know the characteristic & excitation table of both the flipflops. Similarly we can make K map of the characteristic equations, hence find the corresponding table matching the needs.

(contd.)

## → Asynchronous Timing (D flip flop)



clock is negative edge triggered



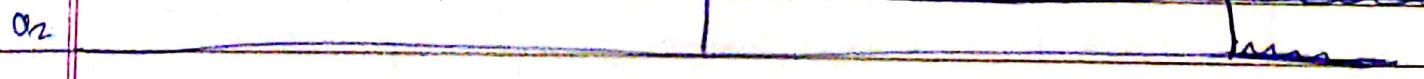
$Q_0$



$Q_1$



$Q_2$



$Q_3$

Here for  $Q_1$ , clock acts as  $Q_0$ , for  $Q_2$  clock is  $Q_1$  & so on.

→ Asynchronous Timing. (~~D flip flop~~)

Table

Clock	$Q_3$ $Q_2$ $Q_1$ $Q_0$	Decimal.
Initially	0   0   0   0	0
1st	0   0   0   1	1
2nd	0   0   1   0	2
3rd	0   0   0   1	1
4th	and so on ..	