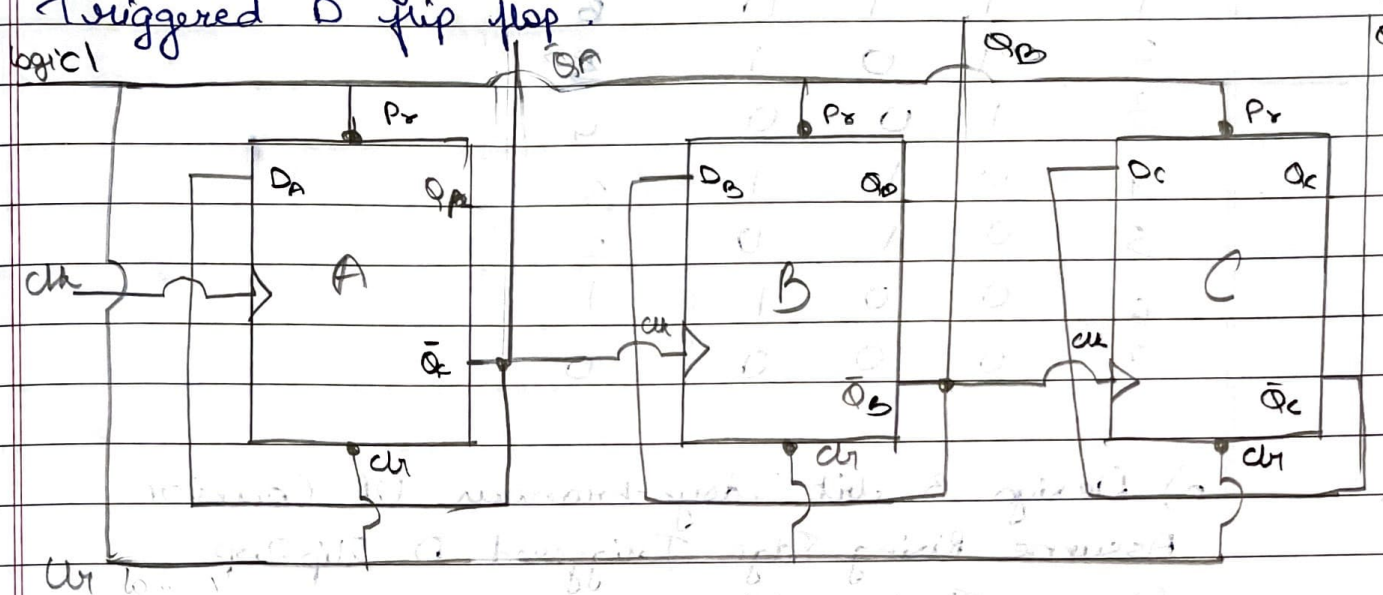
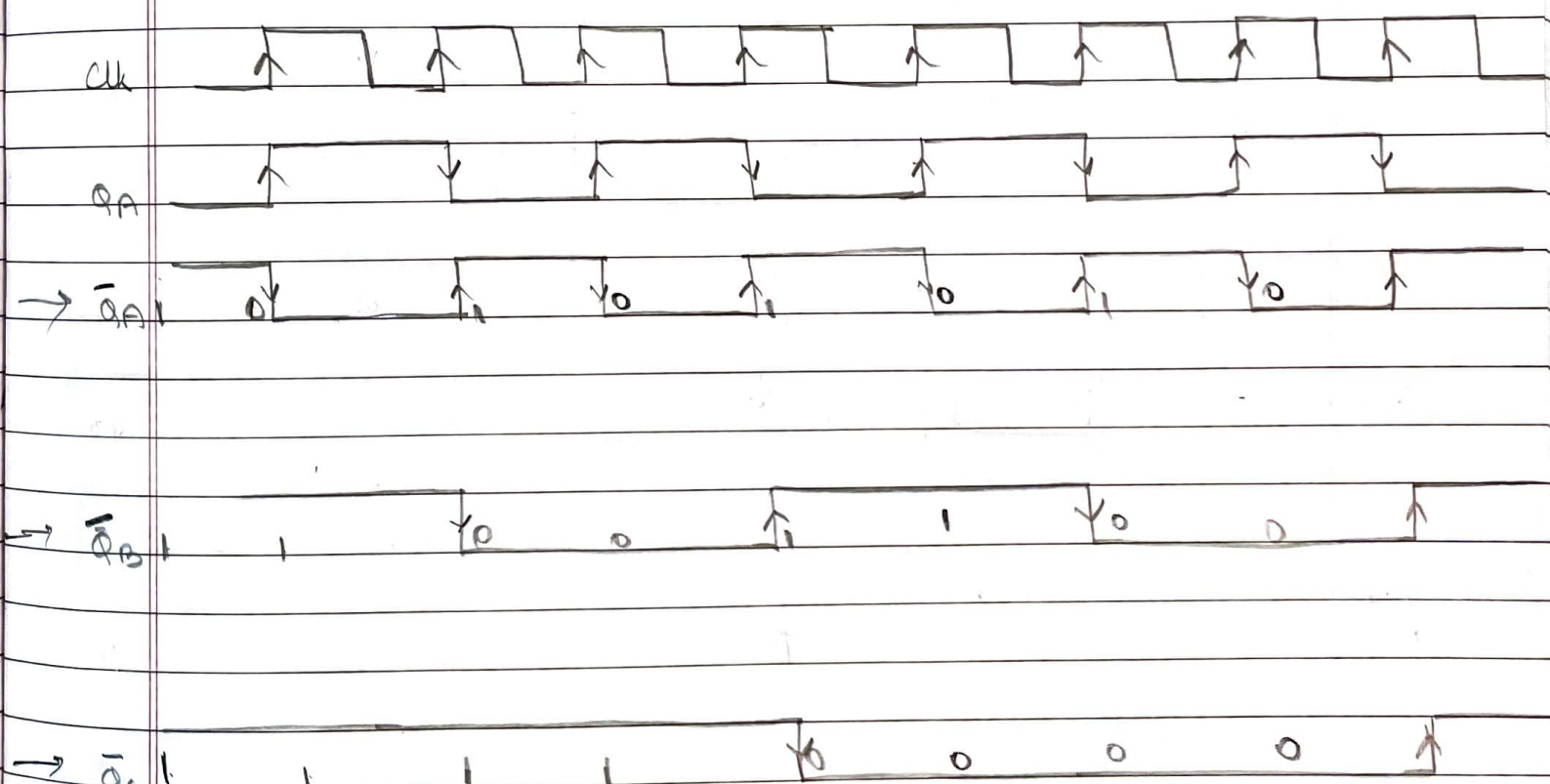
11/1/23 Digital Electronics. Term Test II

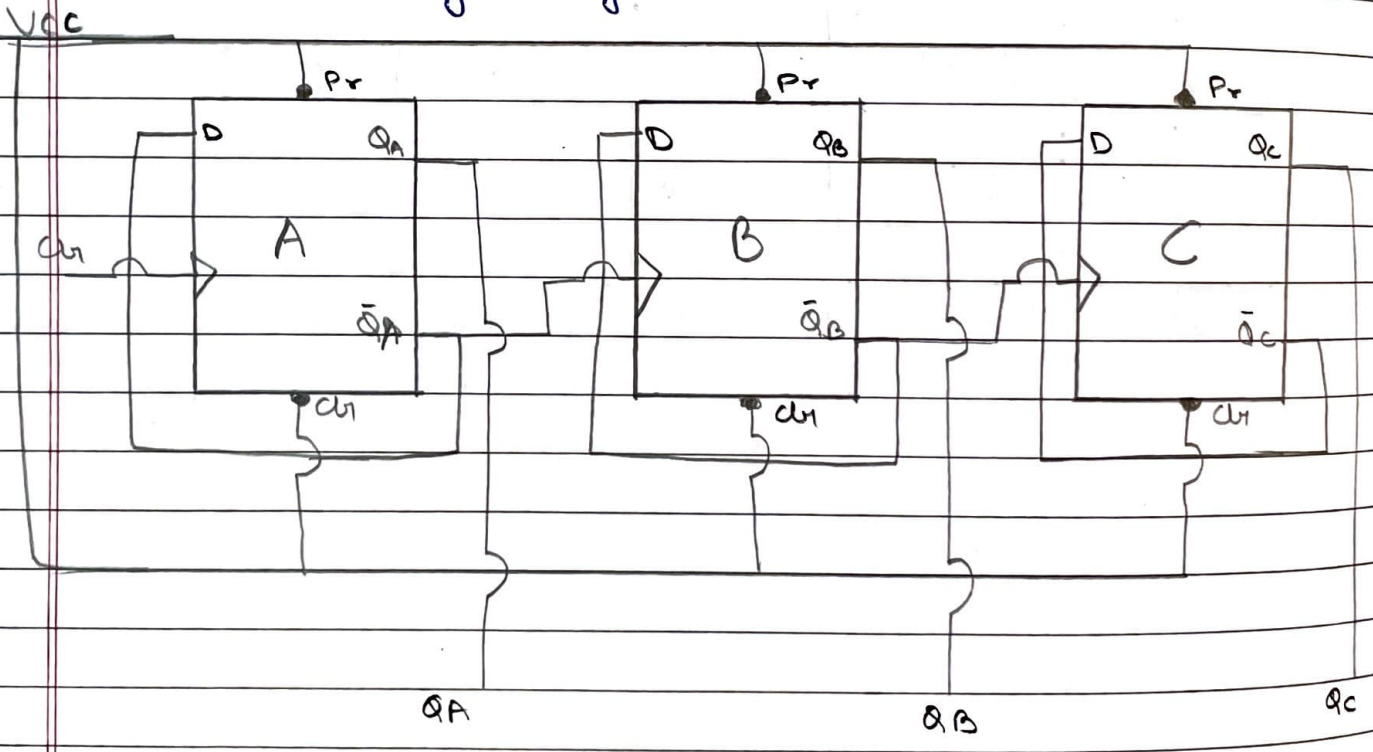
Q.1 a) 3 bit Asynchronous Down Counter, Rising edge Triggered D flip flop:

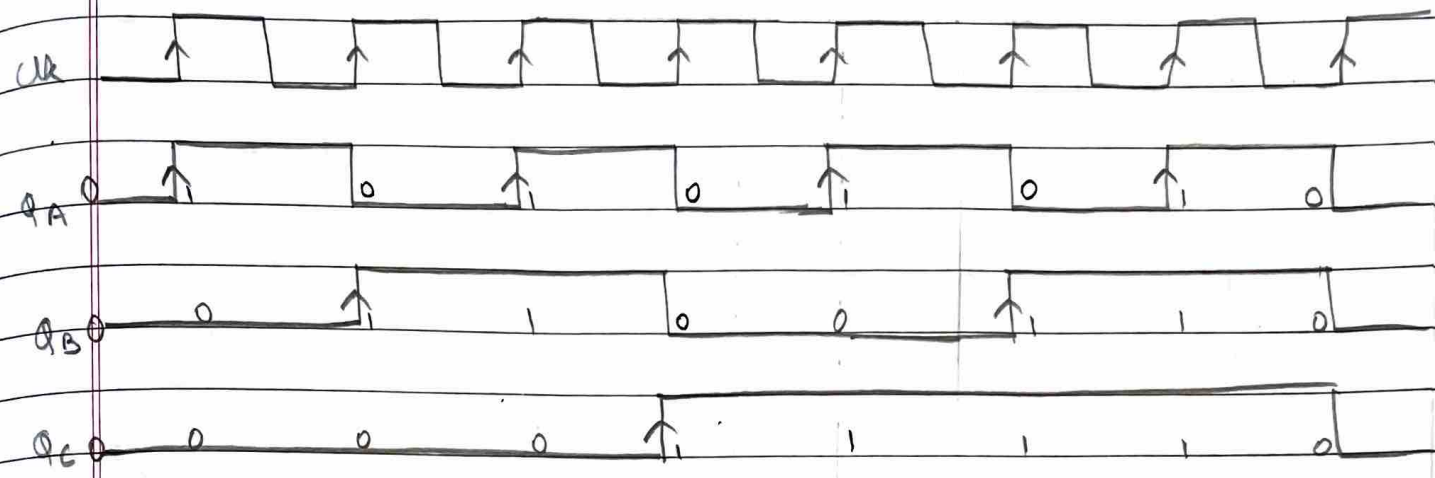




Clk	C	B	A	Decimal
0	1	1	1	7
1	1	1	0	6
2	1	0	1	5
3	1	0	0	4
4	0	1	1	3
5	0	1	0	2
6	0	0	1	1
7	0	0	0	0

Q.1 b) Design 3 bit Asynchronous UP Counter
Assume Rising Edge Triggered D FlipFlop
Draw Timing Diagram

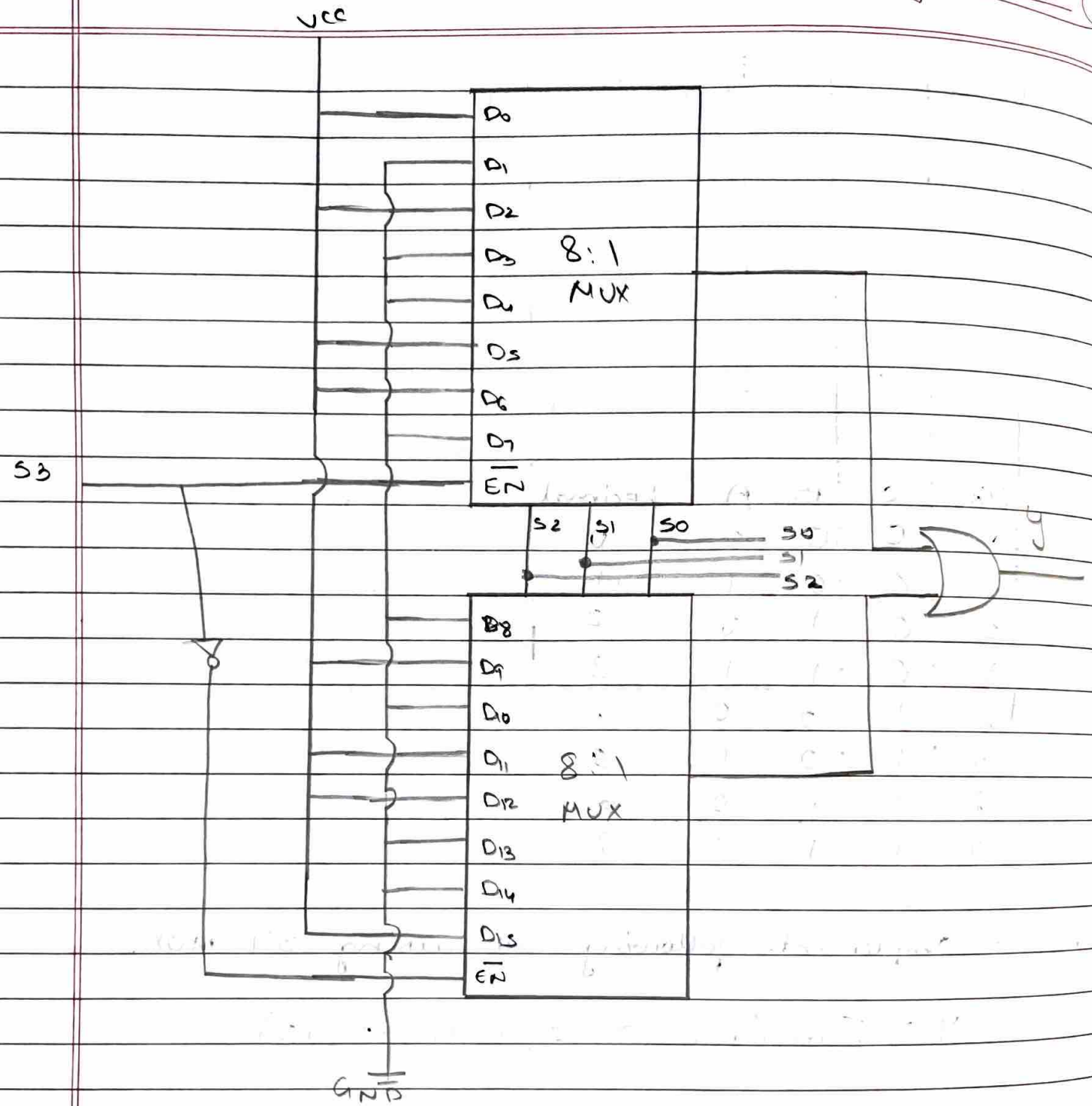




Clk	C	B	A	Decimal
0	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7

Q.2 a) Implement following SOP using 8:1 MUX.

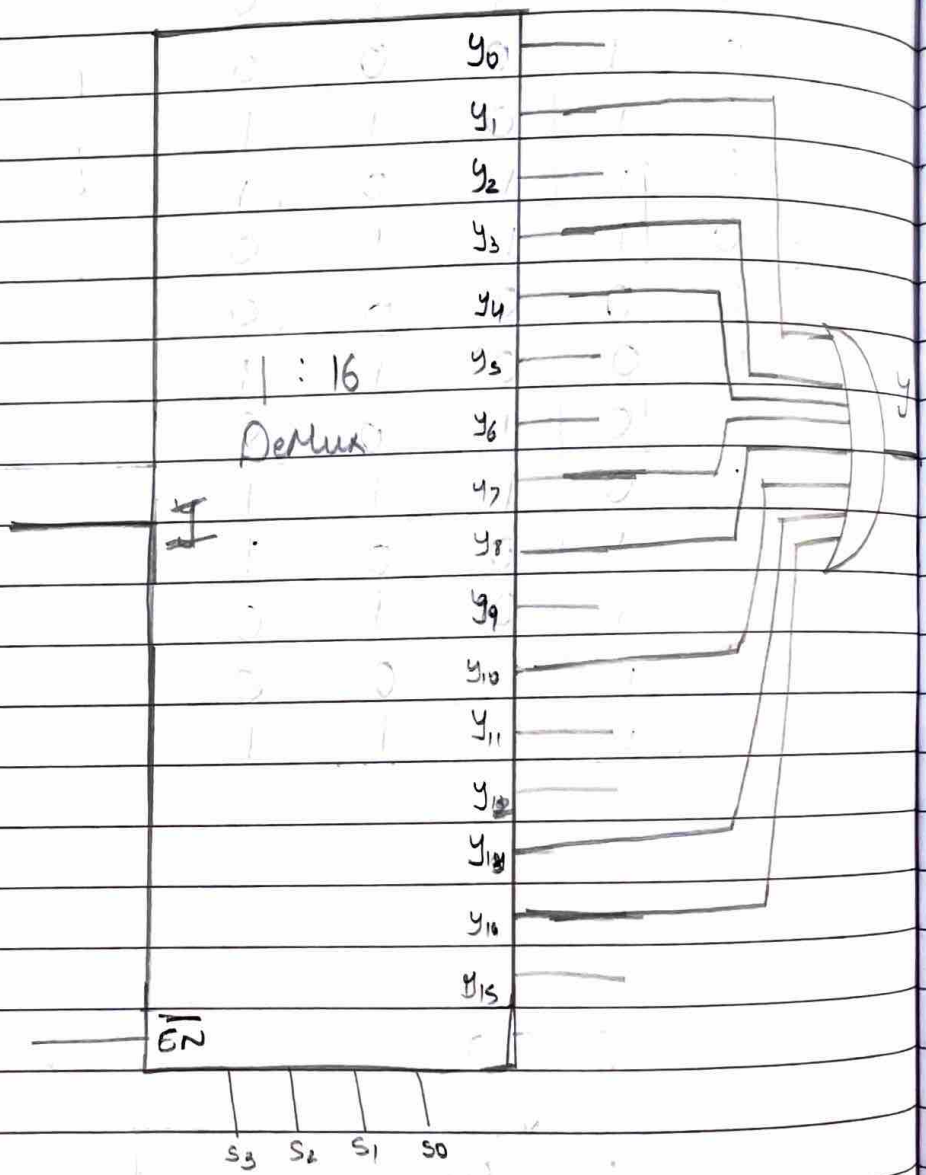
$$Y = \Sigma m (0, 2, 5, 6, 9, 11, 12, 15)$$


VCC
D0
D1
D2
D3
D4
D5
D6
D7
EN
8:1
MUX
S3
S2
S1
S0
S0
S1
S2
D8
D9
D10
D11
D12
D13
D14
D15
EN
8:1
MUX
GND

S_3	S_2	S_1	S_0	y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

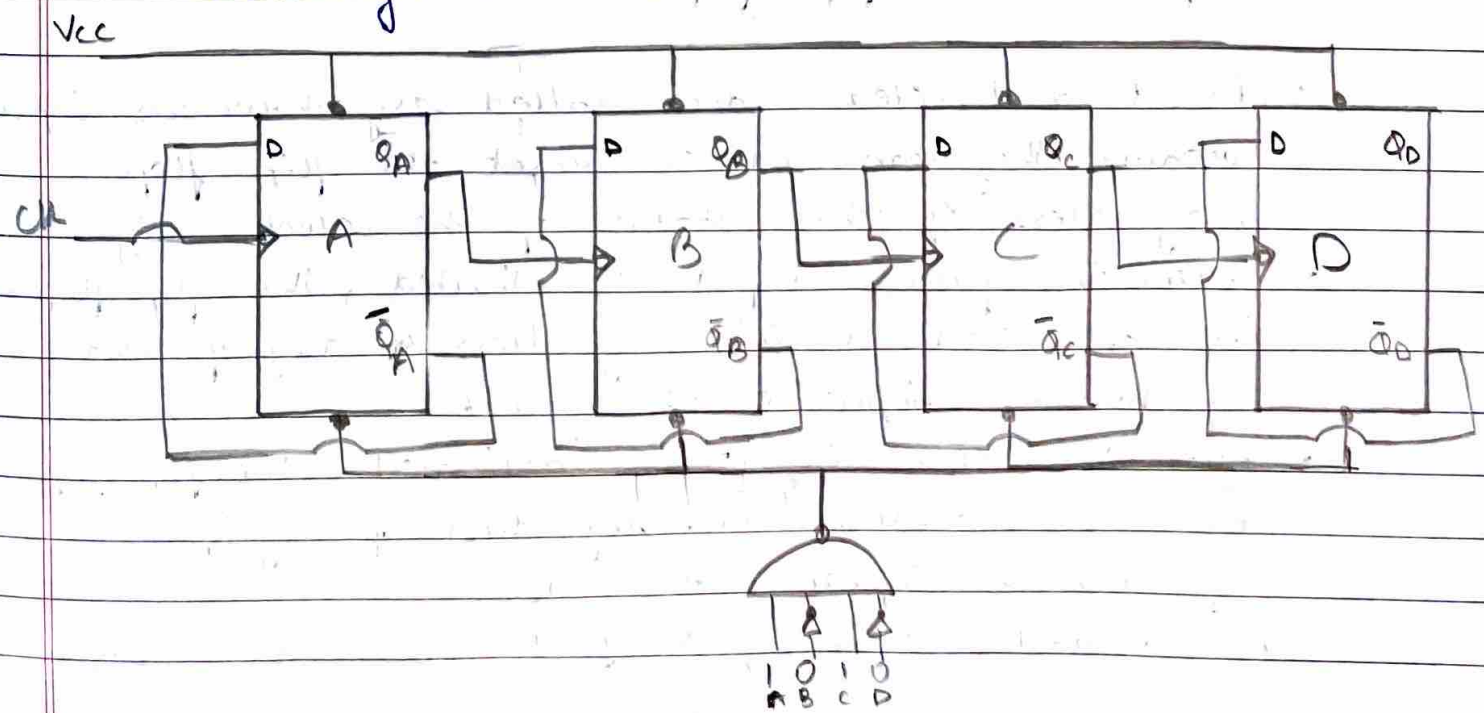
2) $Y = \Sigma\pi m(0, 2, 5, 6, 9, 11, 12, 15)$

$Y = \Sigma m(1, 3, 4, 7, 8, 10, 13, 14)$



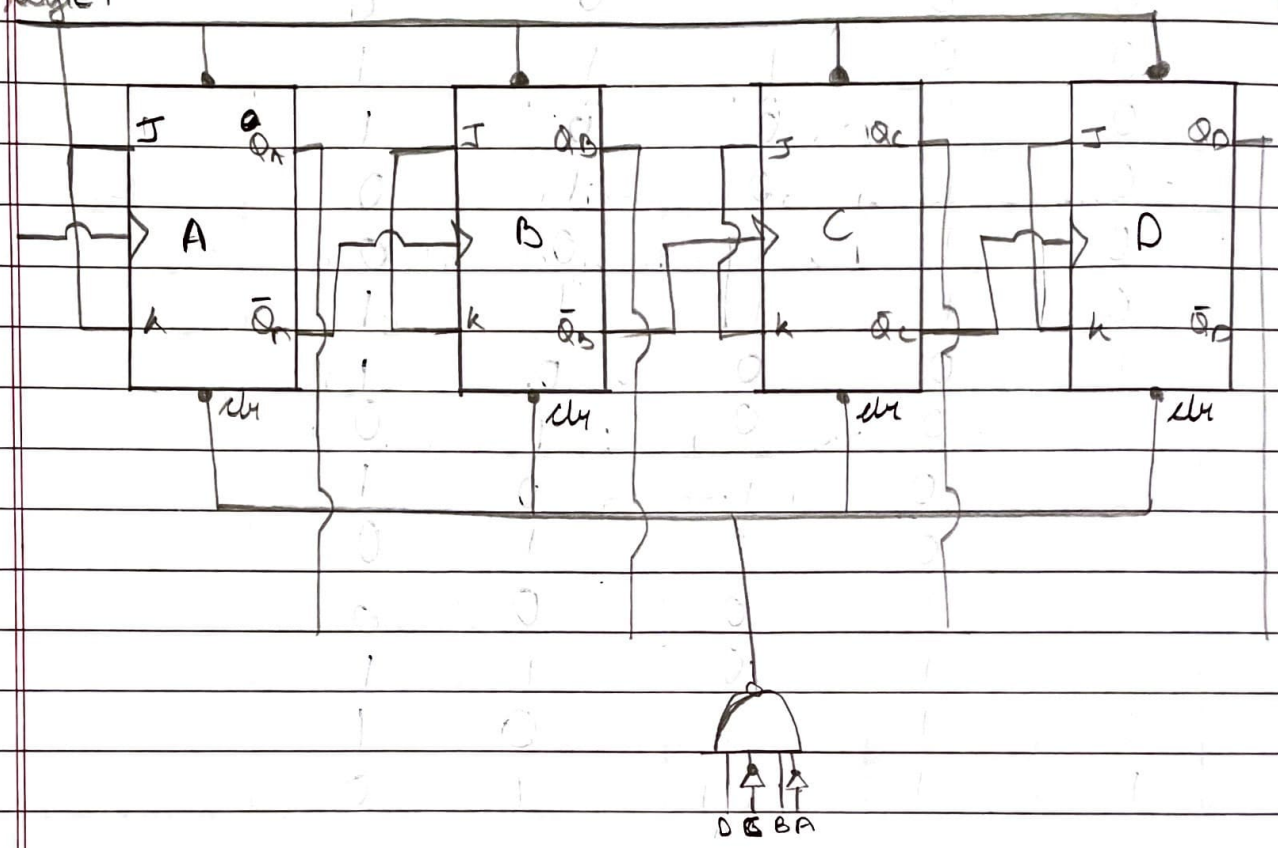
S_3	S_2	S_1	S_0	y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Q.3 a) Design MOD to synchronous up counter using D FF. Assume falling edge triggered. Use full decoding.



Q. 3 b) Design MOD 10 synchronous up-counter using J-K flip flop.

Assume rising edge triggered. Use full decoding.



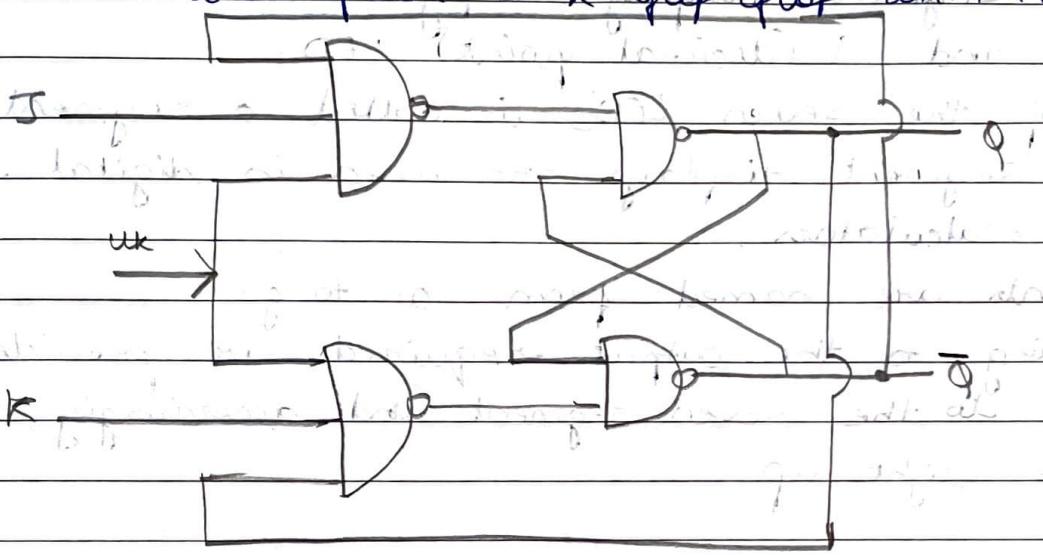
Q. 4

a) Why are preset and clear referred as asynchronous inputs in a flip flop.

- Preset and clear are called asynchronous input because they can set or reset the flip flop regardless of the status of the clock signal.
- When the preset input is activated, the flip flop will be set ($Q=1$, $\bar{Q}=0$) regardless of any of the synchronous input or the clock.
- When the clear input is activated, the flip flop will be reset ($Q=0$, $\bar{Q}=1$), regardless of any of the synchronous inputs or the clock.
- Preset and clear inputs find use when multiple

flip-flops are ganged together to perform a function on a multi-bit binary word, and a single line is needed to set or reset them all at once.

b) Draw and Explain J-k flip flop with truth table.



Truth Table :

Clk	J	k	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	0	Q_n	$\bar{Q}_n$
1	0	0	Q_n	$\bar{Q}_n$
1	0	1	0	1
1	1	0	1	0
1	1	1	Toggle ($\bar{Q}_n$)	

Excitation Table :

Q_n	Q_{n+1}	J	k
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Characteristics Table :

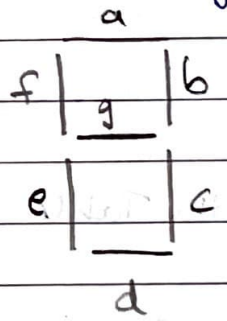
Q_n	J	k	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0

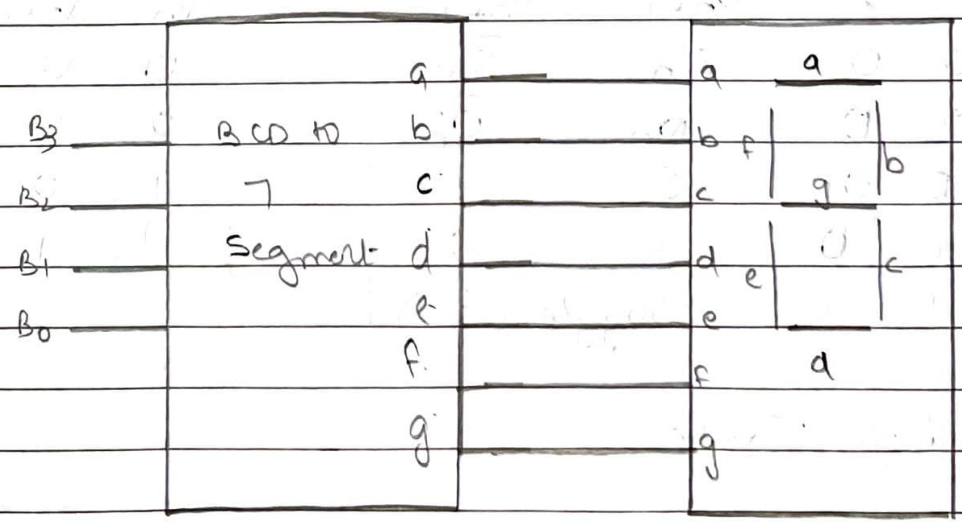
1	1	0	1
1	1	1	0

Q. 5

a) Explain Seven Segment display configuration. Also explain BCD to seven segment conversion.

- Seven Segment display configuration has 7 LED lights and 1 (decimal point) LED.
- Each of the seven LED's is called a segment.
- Seven Segment displays are used in digital clocks, basic calculators.
- Segments are named from a to g.
- According to the output required, we provide inputs to the seven segment and accordingly, the LED's light up.





B_3	B_2	B_1	B_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

b) Explain way to achieve Binary to Excess - 3 code.

→ • Excess - 3 code can also be representated as XS-3 code.

• In excess - 3 code each digit of decimal number is represented by adding 3 in each decimal digit.

• Following steps to convert the binary number into Excess-3 code:

1) Convert the binary number into decimal.
2) Add 3 in each digit of decimal number.
3) Find binary code of each digit of the newly generated number.

- Binary to Excess 3

BCD				Excess 3			
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0