

Deeds:

E-Learning Environment for Digital Design

Deeds is the acronym of
Digital Electronics Education and Design Suite

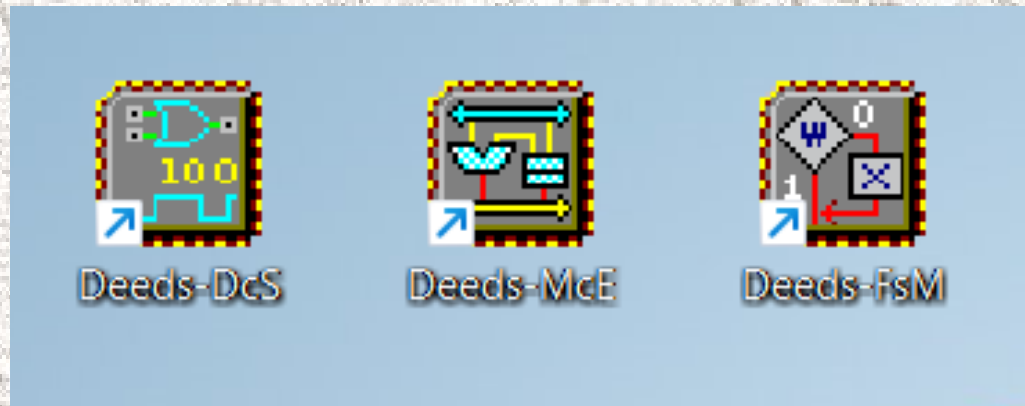


What is *Deeds*?

- *Deeds* is a set of educational tools for Digital Electronics, characterised by a “learn-by-doing” approach.
- *Deeds* covers the following areas:
 - combinational and sequential logic
 - finite state machines
 - microcomputers

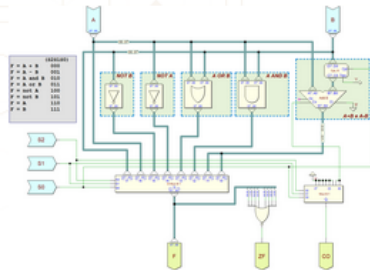
What is *Deeds*?

- *Deeds* includes three design tools:
 - **Deeds-DcS** (Digital Circuit Simulator)
 - **Deeds-FsM** (Finite State Machine Simulator)
 - **Deeds-McE** (Micro Computer Emulator)



What is **Deeds**?

- **Deeds** tools are available to the community of Digital Design teachers and students.
- **Deeds** learning materials can be shared within the community.
- **Deeds** website



- Home
- Deeds Simulator
- Downloads
- Version Notes
- Learning Materials
- Discussion Group
- Books & Digital Contents

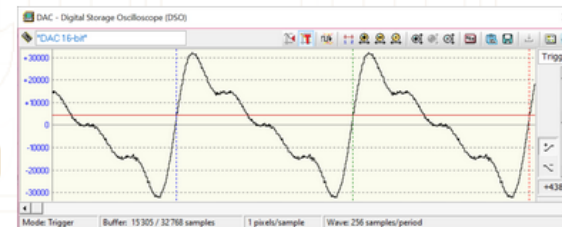
Welcome to Digital Electronics Deeds

(by Giuliano Donzellini)

In this web site you'll find **digital circuits**, **ideas**, **projects**, **tools for simulation** and **testing on FPGA**, and more. A complete learning path to understanding and designing digital systems, supported step-by-step by [Deeds simulator](#). We tried to do our best but... is up to you to judge if our "deeds" (literal meaning of the word!) are good or bad...

News

New Deeds version published (2.50.200)



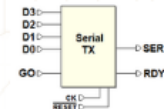
The new version introduces the *Digital Storage Oscilloscope (DSO)* (associated with the virtual DAC component) and the new *Attenuator* components... [\(read more\)](#).

Introduction to Microprocessor-based Systems Design

Ideas & Projects

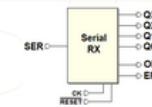
Synchronous Serial Transmitter (4 bits)

In this example, we'll design a simplified 4-bits synchronous serial transmitter... [\(read more\)](#).



Synchronous Serial Receiver (4 bits)

Let's design a 4-bits synchronous serial receiver. The unit will receive serial sequences on... [\(read more\)](#).



Synchronous Serial Communication System (4 bits)

In this example, starting from the



What **Deeds** includes? (1)

- The **Main Program** and the **Official Deeds** website, to navigate among lessons, exercises and laboratory assignments
- A **Digital Circuit Simulator**, that includes:
 - A schematic **Editor**
 - An interactive circuit **Animator**
 - An interactive **Timing Simulator**

What **Deeds** includes? (2)

- A **Finite State Machine** designer
- A **Microcomputer Board Emulator** (include a *code editor*, an *assembler* and an *interactive debugger*)
- A **Student Report Builder**

Interaction among the tools

- The **Main Program** and the **Official Deeds** website can launch the other tools
- The web browsers interact with editors and simulators, providing a true interaction between internet content and experiments
- Simulators interact with each other

Deeds as Learning Environment

- A collection of tools and text material that help students acquiring:
 - Theoretical foundations of the subject
 - Analysis capabilities
 - Ability to solve problems
 - Practical synthesis and design skills

Deeds - The online Learning Materials

- The [page](#) showing an index with aside a [lab exercises](#)
- All text and objects in the page can be [Active](#).
- By clicking on the schematics, the circuit shown will be loaded in the [Digital Circuit Simulator](#), ready to be tested or modified

Introduction to digital electronics

Introduction to the Digital Circuit Simulator

In this introductory exercise you will test the simple logic network represented in the figure below and, at the same time, you will gain confidence with the **Digital Circuit Simulator (d-DcS)** of the [Deeds](#). To open the file in the **d-DcS**, just click on the figure:

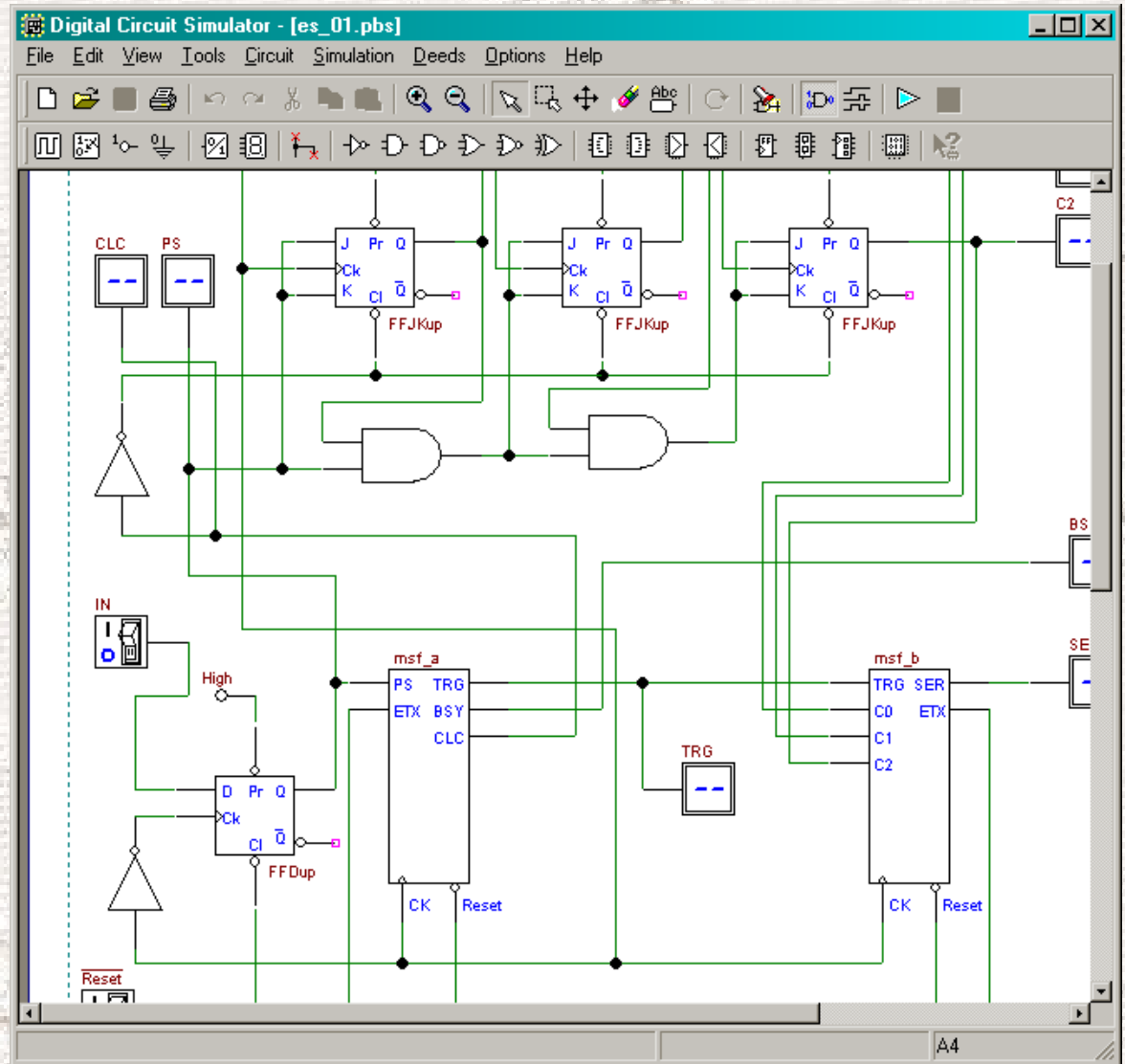
Next step is to check the behavior of the network. You will start the **functional simulation (Interactive Animation)** of the network by clicking, on the **d-DcS toolbar**, the command . Now the three input switches **A**, **B** and **C** can be toggled and the gate's output **OUT** will change accordingly. We suggest that you draw the truth table for a three variable boolean function and then fill the output column with the data resulting from the simulation.

Last task requested is the **timing simulation** of the same network. You start the timing simulation of the network by clicking, on the **d-DcS toolbar**, the command . The input values must be drawn directly on the **timing diagram window**. You should define the values versus time of the three inputs, such as all the possible combinations of **A**, **B** and **C** are tested.

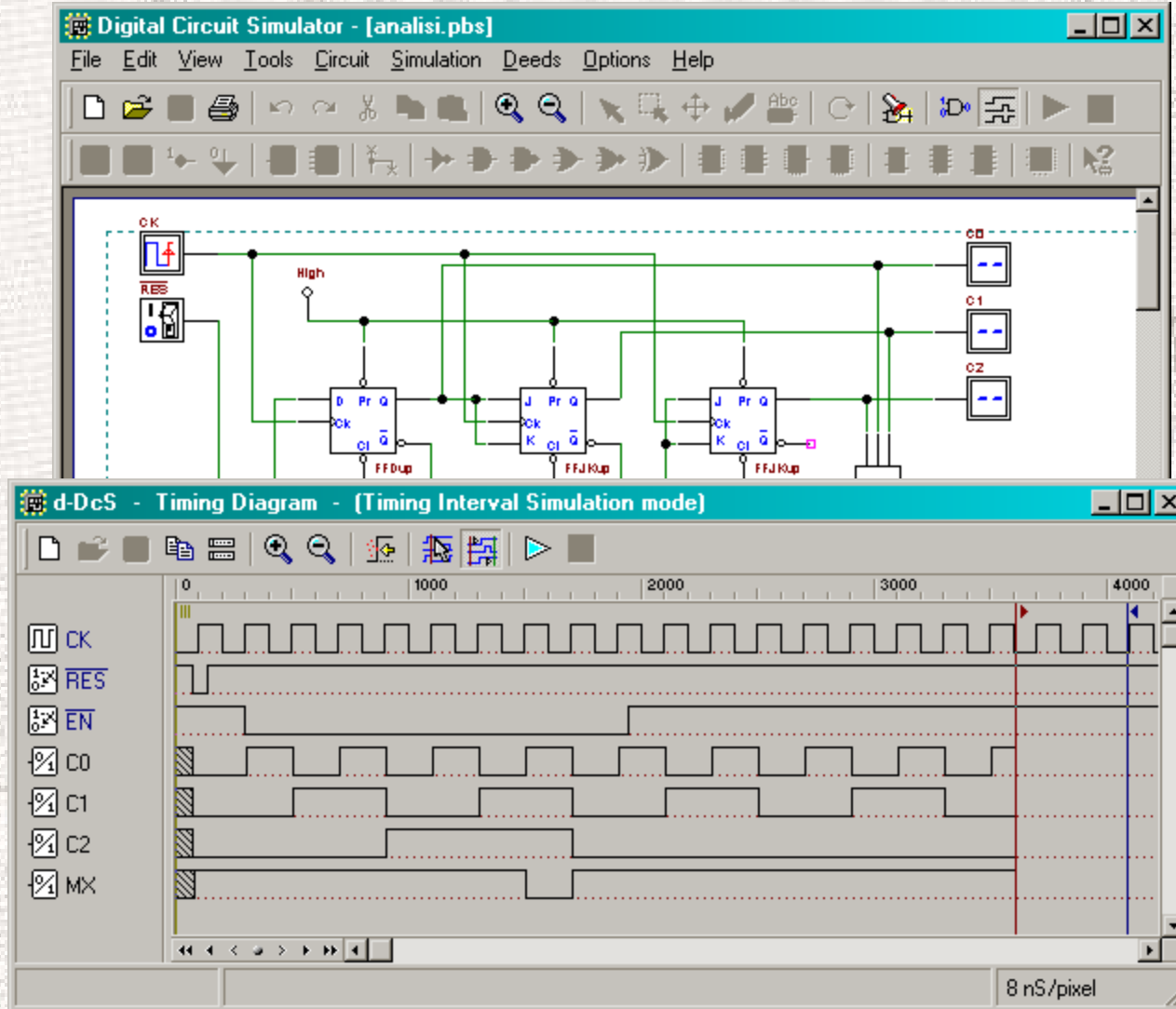
Learning Materials		
		Download
1	Introduction to digital electronics	Download
1.1	Introduction to the Digital Circuit Simulator	001001
1.2	Analysis of simple logic gates	001002
2	Multiplexers and Demultiplexers	Download
2.1	Analysis of a multiplexer (2 to 1)	005030
2.2	Analysis of a demultiplexer (1 to 2)	005040
2.3	Analysis of a simplified shared-line communication channel	005050
3	Applications of Boolean Algebra	Download

Deeds - The d-DcS Digital Circuit Simulator

- The **basic operations** of professional tools have been adapted to the **educational needs**
- The components available on the bin are **simple to understand**
- We avoided complex real components, that could confuse the beginner
- Two simulation mode are available:
 - a) *Interactive Animation*
 - b) *Timing diagram*

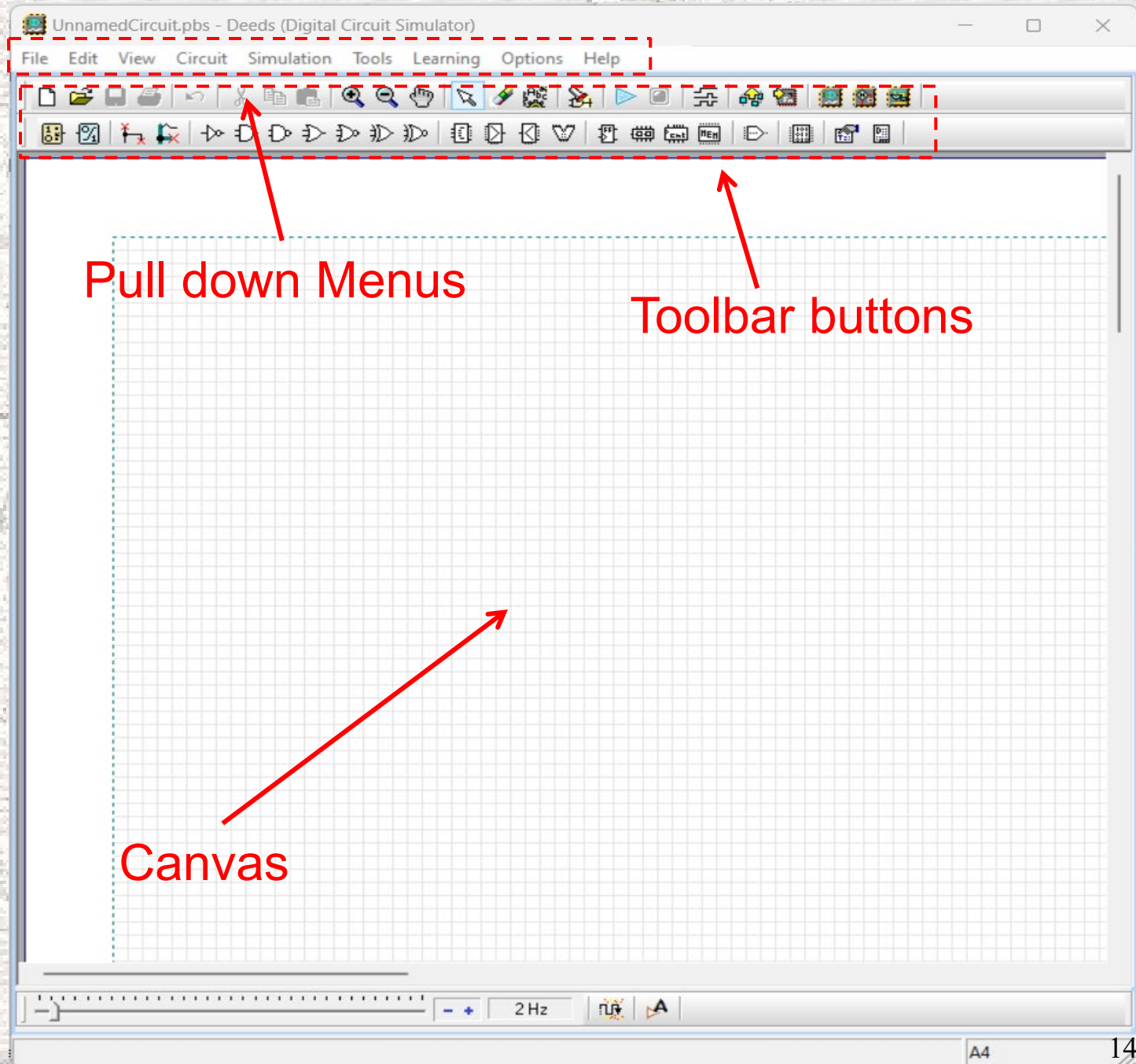


Deeds - The d-DcS Timing Simulator



- Timing simulation can be executed in various operation modes
- Clock and input signals can be easily edited
- Timing simulation can be **interactive**, for the beginners, with a event-by-event approach, or can be launched defining a time interval, as in professional tools

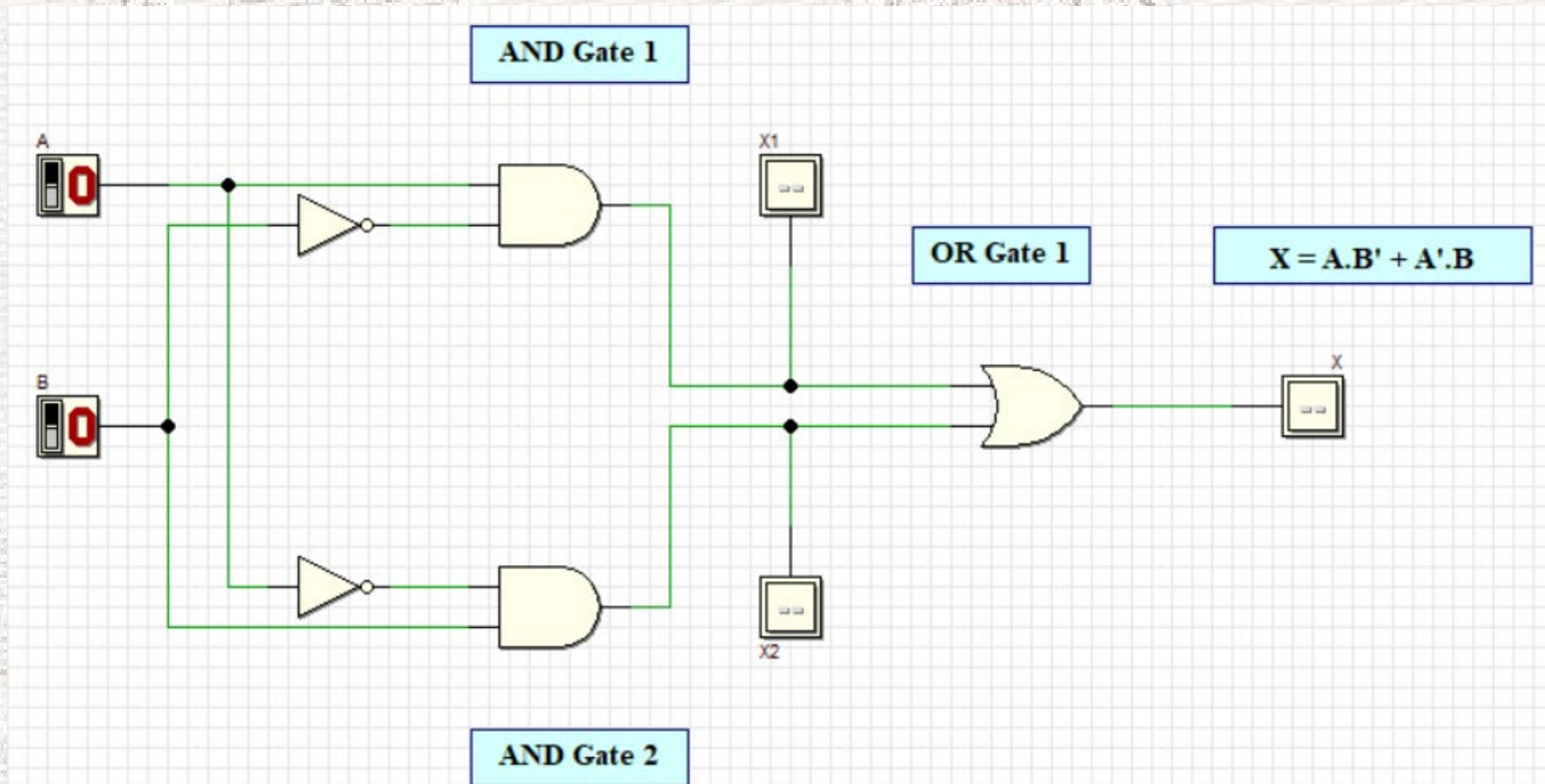
Deeds - The interface





Demo session

Demo: XOR circuit



Exercise: Create this circuit

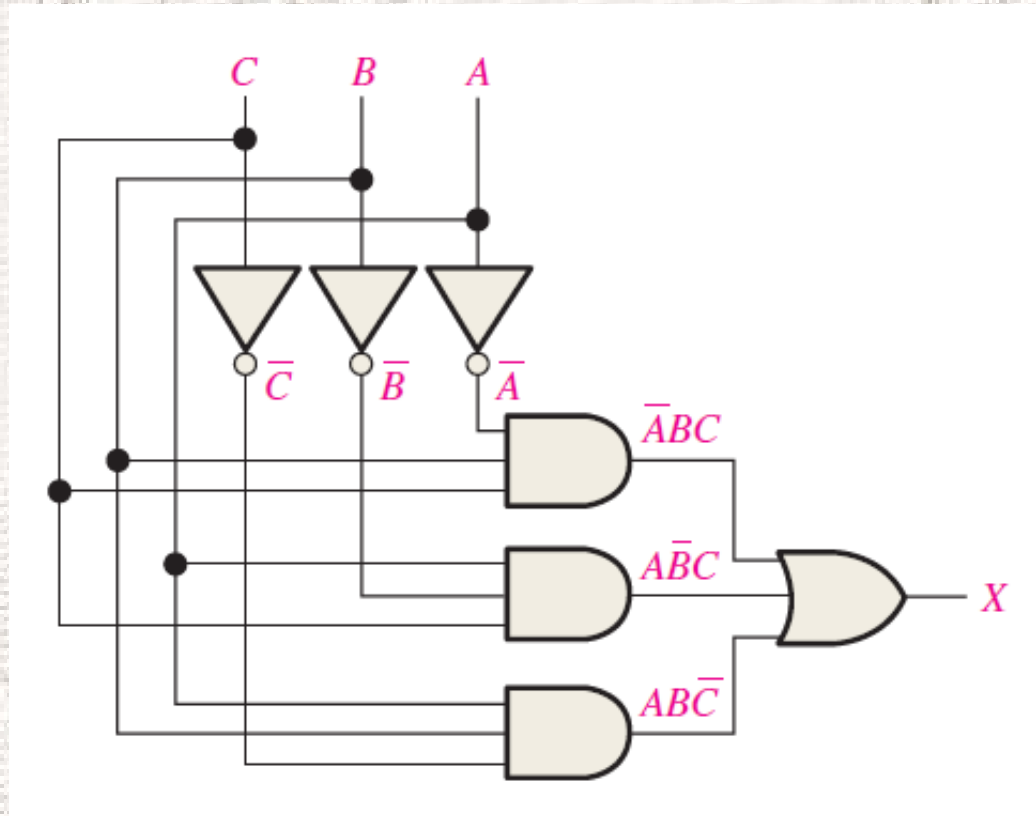


 Image Upload

Exercise:

- Verify your circuit with this Truth Table

TABLE 5-4				
Inputs			Output	
<i>A</i>	<i>B</i>	<i>C</i>	<i>X</i>	Product Term
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	$\bar{A}BC$
1	0	0	0	
1	0	1	1	$A\bar{B}C$
1	1	0	1	$AB\bar{C}$
1	1	1	0	