SPECIFICATION

NVIDIA Jetson TX2 Developer Kit Carrier Board

Abstract

This document contains recommendations and guidelines for Engineers to follow to create modules for the expansion connectors on the NVIDIA® Jetson™ TX2 Developer Kit carrier board (P2597), as well as information about the capabilities of its other dedicated interface connectors and associated power solutions. The Jetson TX2 Developer Kit carrier board supports Jetson TX2, Jetson TX2 4GB & Jetson TX2i.

Note: Jetson TX2 Series modules utilize Tegra X2 which is a Parker series SoC.

CAUTION:

1. ALWAYS CONNECT JETSON MODULE & ALL EXTERNAL PERIPHERAL DEVICES BEFORE CONNECTING THE POWER SUPPLY TO THE AC POWER JACK. Connecting a device while powered on may damage the Developer Kit carrier board, Jetson module or peripheral device. In addition, the carrier board should be powered down and the power removed before plugging or unplugging devices or add-on modules into the headers. Wait for the red power VDD_IN LED (See Figure 1) to turn off or wait for 5 minutes if your system does not have a power LED. This includes the Jetson module, the camera & display headers, the M.2 connector, the PCIe® x4 connector, SATA & the other expansion connectors/headers. For the PCIex4 & SATA connector, also wait for the PCIe/SATA 12V LED to turn off (See Figure 1)

2. The Jetson Developer Kit carrier board contains ESD-sensitive parts. Always use appropriate anti-static and grounding techniques when working with the system. Failure to do so can result in ESD discharge to sensitive pins, and irreparably damage your Jetson carrier board. NVIDIA will not replace units that have been damaged due to ESD discharge.

Document Change History

Date	Description
MAY, 2017	Initial Release
JUN, 2017	**M.2, Key E Expansion Slot** - Updated figure, Pin Descriptions table & notes to show I2C on pins 58/60 at 1.8V level by default. **Display** - Changed headings to to make DSI & DP/eDP sections more clear - Corrected lane order in eDP Connection example figure in eDP Connector block.
JUN, 2017	**Expansion Header & GPIO Expansion Header** - Updated main tables o Removed column for device connected and put the information in the notes instead. o Added column for signal voltage level at header & updated note 3 to mention voltage selector jumper J24. - Added tables for Jetson TX1 & TX2 to provide signal details (Name, Tegra Ball, Tegra GPIO, POR, etc.)
OCT, 2017	**Introduction** - Updated introduction paragraph(s)
MAR, 2018	**General** - Added Jetson TX2i mention throughout doc - Updated main power input range to include separate, more limited range for TX2i **Intro** - Added Jetson TX2i Top View figure - Added Carrier Board revision differences section - Added note describing how to power on a P2597 B02/B04 platform with Jetson TX2i installed **HDMI** - Updated figure to show required series resistors on high-speed signals **Expansion Header** - Corrected Tegra GPIO port # for AUDIO_I2S_MCLK_3V3 signal on header (Pin 7)
JUNE, 2018	**Introduction** - Added P2597_C02 carrier board placement figure & table. - Added P2597_C02 differences in Carrier Board Revision Differences section. **Gigabit LAN Connections** - Updated figure to show separate capacitors at CT inputs of Magnetics to match the P2597_C02 design. **Display Expansion Connector** - Changed usage/descriptions in table to match module pin name numbering. - Corrected module pin names for DSI[3,1]_CLK+/-. **Camera Expansion Connector** - Changed usage/descriptions in table to match module pin name numbering. **Expansion Header** - Added note/highlighting to Exp. Header Pin Desc. & Signal Details Tables related to TX1 support on AO_DMIC pins. - Added GPIO port info for AO_DMIC pins (Tegra CAN_GPIO[1:0]) in TX2/TX2i Exp. Header Signal Details table. **Buttons, Jumpers & Indicators** - Added separate sections in Jumpers table for P2597 B02/B04 & C02 carrier boards. - Added table for combined power, force off, recovery & reset header (C02 only).
DEC, 2018	**General** - Removed Jetson TX1 mention & added Jetson TX2 Series (including TX2/TX2 4GB/TX2i) - Removed Debug Connector mention throughout document. - Added notes in Carrier Board Revision Differences and Charger Control Header sections that Auto-Power-On support on Jetson TX2 is not compatible with the P2597_C02 carrier board.
MAR, 2019	**General** - Added Appendix to describe rework required on Jetson TX2 Developer Kit carrier board P2597_C02 to support Auto-Power-On.
MAR, 2020	**General** - Updated maximum VDD_IN voltage for Jetson TX2 4GB/TX2i to match Jetson TX2 - Updated names of J21 to be 40-pin Expansion Header & J26 to be Secondary Expansion Header - Updated name of J20 to be Automation Header - Removed connection figures for most connectors - Updated pin desc. tables to remove 2nd column containing net names & added module pin # columns. - Updated carrier board signal delay tables to show only a single worst-case delay per interface. **Introduction** - Updated Figure 1: Jetson Carrier Board Placement (Top View) and J24 description below. **40-Pin Expansion Header**

Date	Description
	- Updated table to add note 9 (strapping related) for UART0_RTS. - Updated power pin capabilities to 2A each. - Combined 40-Pin Expansion Header Pin Descriptions and Signal Details tables, removed signal name column, and added module pin #, Alternate usage columns. **Secondary Expansion Header** - Updated power pin capabilities to 2A each.

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Table of Contents

1.0 INTRODUCTION

The NVIDIA® Jetson TX2 Developer Kit carrier board is ideal for software development within the Linux environment. Standard connectors are used to access Jetson module features and interfaces, enabling a highly flexible and extensible development platform. (The Jetson TX2 Developer Kit is not intended for production purposes.)

Go to https://developer.nvidia.com/jetpack for access to JetPack SDK. Use the JetPack installer to flash your Jetson Developer Kit with the latest OS image, to install developer tools for both host PC and Developer Kit, and to install the libraries and APIs, samples, and documentation needed to jumpstart your development environment.

1.1 Jetson Module Feature List

Applications Processor
- Tegra X2

Memory
- LPDDR4 DRAM & eMMC 5.1
- Memory sizes for DDR & eMMC vary depending on module – Check the Jetson Serie Data Sheet

Network
- 10/100/1000 BASE-T Ethernet

Connectivity
- Jetson TX2 only: Dual U.FL RF connectors: Connects to 802.11a/b/g/n/ac WLAN/Bluetooth enabled devices.

Advanced power management
- Dynamic voltage and frequency scaling
- Multiple clock and power domains
- Thermal Transfer Plate & optional Fan/Heatsink

1.2 Carrier Board Feature List

Connection to Jetson Module
- 400-pin (8x50) Board-Board Connector

Storage
- Full Size SD Card Slot
- SATA Connector (Power & TX/RX)

USB
- USB 2.0 Micro AB (Host & Device)
- USB 3.0 Type A (Host only)

Wired Network
- Gigabit Ethernet (RJ45 Connector w/LEDs)

Display Expansion Connector
- 120-pin (2x60) Board-Board
- DSI (2x4 lanes)
- eDP/DP/HDMI
- Backlight: PWM/Control
- Touch: SPI/I2C

HDMI Type A

PCIe
- Standard PCIe® x4 connector

M.2 Key E Connector
- PCIe x1, SDIO (Jetson TX2 4GB/TX2i only)
- USB 2.0, I2S, UART, I2C, Control

Camera Expansion Connector
- 120-pin (2x60) Board-Board
- CSI: 6, x2 – 3, x4
- Camera CLK, I2C & Control
- I2S, UART, SPI
- Digital Mic

40-Pin Expansion Header
- 40-pin (2x20) header
- I2C, SPI, UART, I2S, Audio Clock/Control
- Digital Mic

Secondary Expansion Header
- 30-pin (2x15) header
- I2S, GPIOs
- Digital Speaker

UI & Indicators
- Power, Reset & Force Recovery Buttons
- LEDs: Main DC input, Main 3.3V (Power)/SOC Enables, M.2 Activity, PCIe/SATA 12V rail

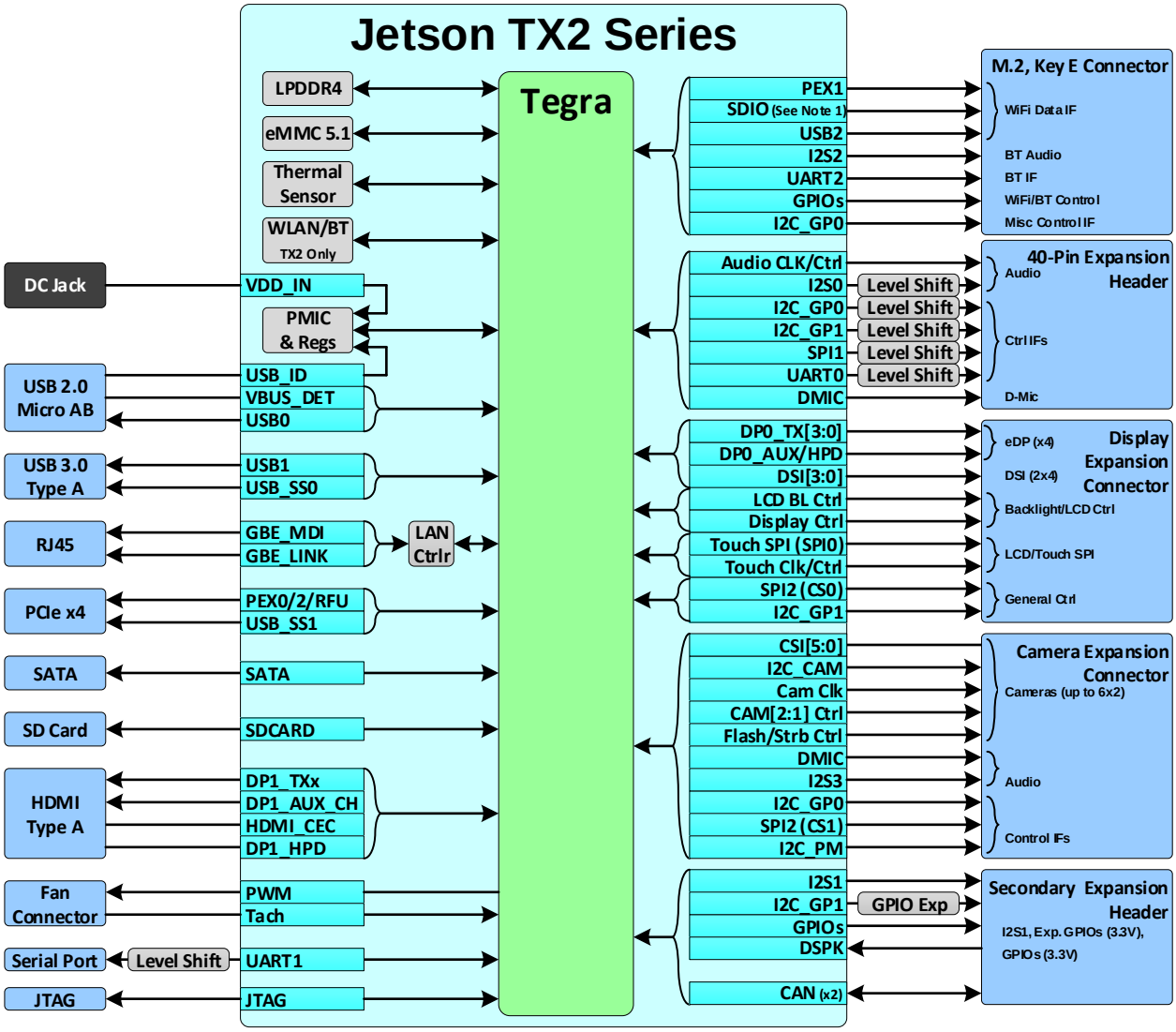
Debug/Serial
- JTAG Connector (Standard 20-pin header)
- Serial Port Signals (1x6 header)

Miscellaneous
- Fan Connector: 5V, PWM & Tach

Power
- DC Jack: TX2: 5.5V-19.6V
TX2 4GB/TX2i: 9V-19.6V
- Main 3.3V/5V Buck Supplies: 2xTPS53015
- Main 1.8V Buck Supply: APW8805
- USB VBUS Load Switches: RT9715 & APL3511
- 12V Boost (PCIe & SATA): LM3481
- Load Switches/LDOs (SD/HDMI/Display/Camera)
- Charge Control Header: 10-pin Flex Receptacle

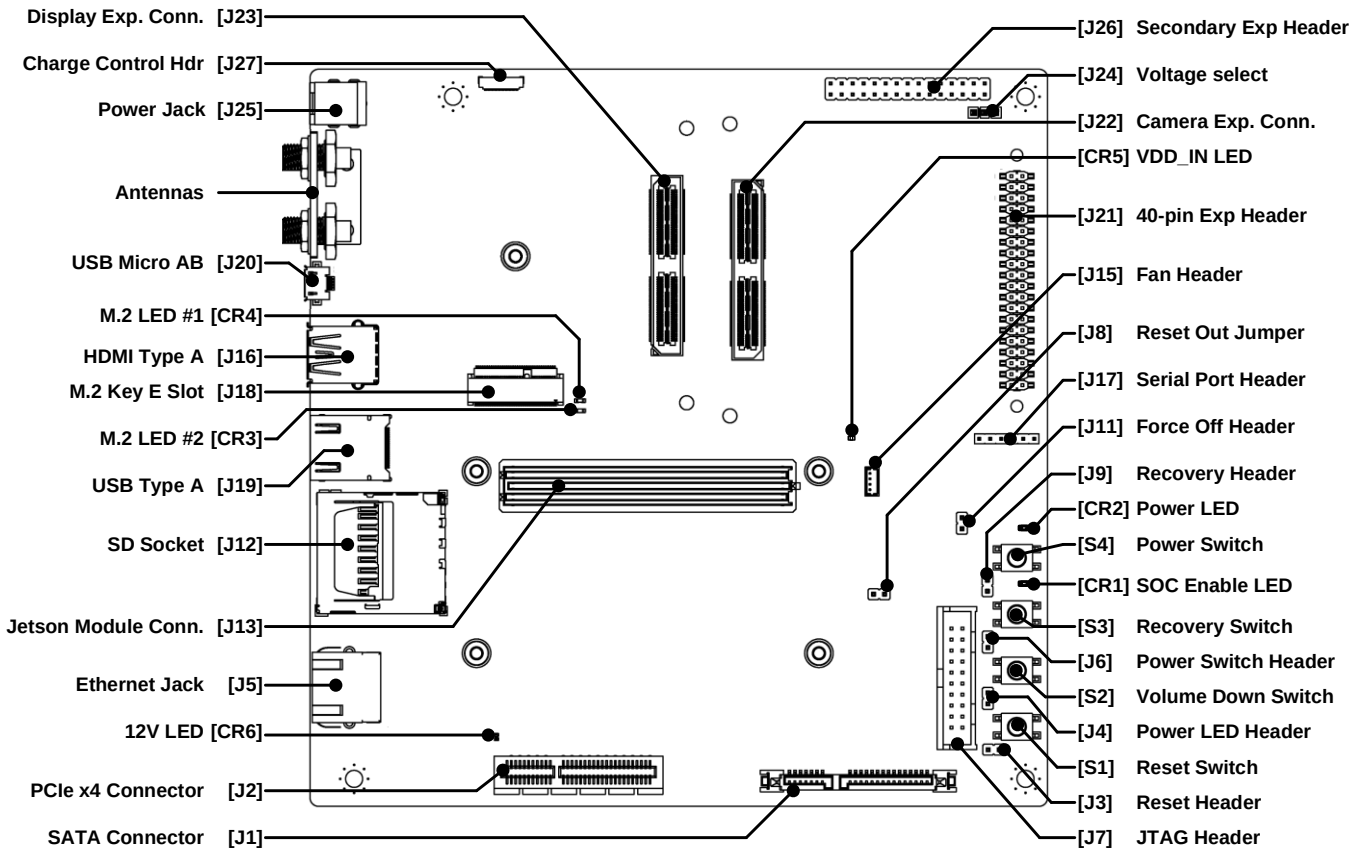
Developer Kit Operating Temperature Range
- 0ºC to 50ºC

1.3 Jetson Carrier Board Block Diagram



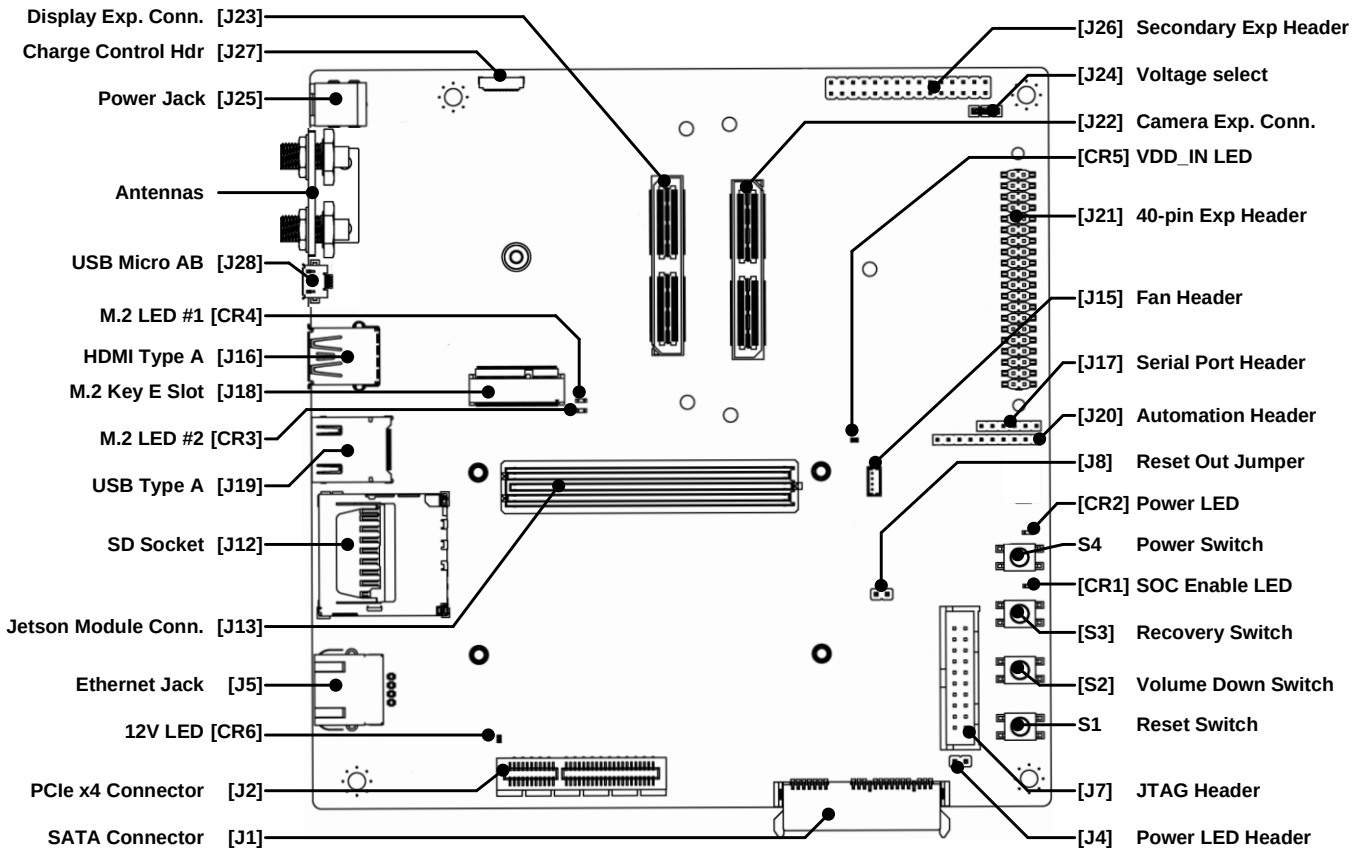
Notes: The additional SDIO interface is supported at the module pins for Jetson TX2 4GB/TX2i only

Figure 1. Jetson Carrier Board Placement (Top View) for P2597 B02/B04



J1	SATA Connector (22-pin Inc. Power)
J2	PCIe x4 Connector
J3	Reset Switch Header (1x2, 2.54mm pitch)
J4	Power LED Header (1x2, 2.54mm pitch)
J5	RJ45 Ethernet Jack
J6	Power Switch Header (1x2, 2.54mm pitch)
J7	JTAG Header (2x10, 2.54mm pitch)
J8	Reset Out Header (1x2, 2.54mm pitch)
J9	Force Recovery Header (1x2, 2.54mm pitch)
J11	Force Off Header (1x2, 2.54mm pitch)
J12	SD Socket (Full Size)
J13	Main Module Connector (8x50, 1.27mm pitch)
J15	Fan Header (4-pin, 1.25mm pitch)
J16	HDMI Type A
J17	Serial Port Header (1x6, 2.54mm pitch)
J18	M.2 Key E Connectivity Connector (75-pin)
J19	USB 3.0 Type A
J20	Micro AB USB
J21	40-Pin Expansion Header (2x20, 2.54mm pitch)
J22	Camera Expansion Connector (2x60, 0.5mm pitch)
J23	Display Expansion Connector (2x60, 0.5mm pitch)
J24	Voltage select for SPI/I2C Level Shifter (1x3, 2.54mm pitch)
J25	Power Jack
J26	Secondary Expansion Header (2x15, 2.54mm pitch)
J27	Charge Control Header (10-pin Flex Recep., 0.8mm pitch)
S1	Reset Switch
S2	Volume Down (Sleep) Switch
S3	Recovery Switch
S4	Power Switch
CR1	SOC Enable LED (Green)
CR2	Power LED (Green)
CR3	M.2 LED #2 (Green)
CR4	M.2 LED #1 (Green)
CR5	VDD_IN LED (Red – Not available on P2597 B02)
CR6	PCIe/SATA 12V LED (Red - Not available on P2597 B02)
	Wireless Connector Assembly (for Jetson TX2 only)

Figure 2. Jetson Carrier Board Placement (Top View) for P2597 C02



J1	SATA Connector (22-pin Inc. Power)
J2	PCIe x4 Connector
J4	Power LED Header (1x2, 2.54mm pitch)
J5	RJ45 Ethernet Jack
J7	JTAG Header (2x10, 2.54mm pitch)
J8	Reset Out Header (1x2, 2.54mm pitch)
J12	SD Socket (Full Size)
J13	Main Module Connector (8x50, 1.27mm pitch)
J15	Fan Header (4-pin, 1.25mm pitch)
J16	HDMI Type A
J17	Serial Port Header (1x6, 2.54mm pitch)
J18	M.2 Key E Connectivity Connector (75-pin)
J19	USB 3.0 Type A
J20	Automation Header (1x10, 2.54mm pitch)
J21	40-Pin Expansion Header (2x20, 2.54mm pitch)
J22	Camera Expansion Connector (2x60, 0.5mm pitch)
J23	Display Expansion Connector (2x60, 0.5mm pitch)
J24	Voltage select for Level Shifters (1x3, 2.54mm pitch)
J25	Power Jack
J26	Secondary Expansion Header (2x15, 2.54mm pitch)
J27	Charge Control Header (10-pin Flex Recep., 0.8mm pitch)
J28	Micro AB USB
S1	Reset Switch
S2	Volume Down (Sleep) Switch
S3	Recovery Switch
S4	Power Switch
CR1	SOC Enable LED (Green)
CR2	Power LED (Green)
CR3	M.2 LED #2 (Green)
CR4	M.2 LED #1 (Green)
CR5	VDD_IN LED (Red)
CR6	PCIe/SATA 12V LED (Red)
	Wireless Connector Assembly (for Jetson TX2 only)

Figure 3. Jetson TX2 Wireless Connector Placement (Top View)

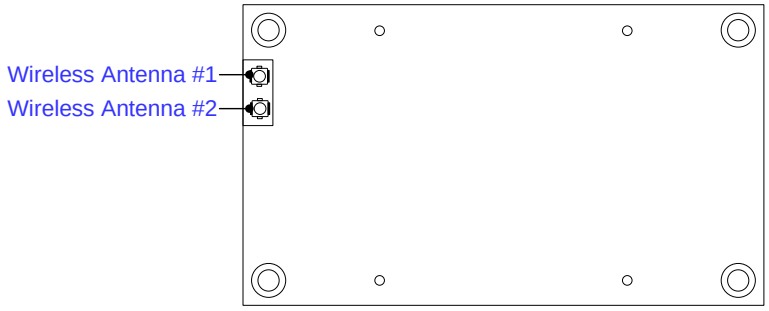


Figure 4. Jetson TX2 4GB/TX2i (Top View)

Note: Jetson TX2 4GB/TX2i do not include on-module wireless support, so there are no Antenna or cutout on TTP.

1.4 Carrier Board Revision Differences

Two versions of the P2597 carrier board have been shipped as part of the Jetson TX2 Developer Kit. They are P2597_B02 & P2597_B04. The main differences between B02 & B04 are:

- Red LED (CR5) added to indicate main power source is active/connected.
- Red LED (CR6) added to indicate 12V supply to PCIe & SATA connectors is active.
- Various minor circuit changes to improve power-on reliability.

The C02 revision of P2597 includes changes in support of Jetson TX2i and Jetson TX2 4GB modules. The main changes compared to B04 are:

- Added Power-on mechanism selection strapping pin – MOD_PWR_CFG_ID at RSVD module pin B49. Jetson TX2 and Jetson TX2 4GB/TX2i have different Power Management ICs (PMICs) which have different power-on requirements. Jetson TX2 4GB has logic to make it compatible with Jetson TX2. The MOD_PWR_CFG_ID pin is pulled high on the carrier board and strapped either low (TX2i) or left unconnected (TX2/TX2 4GB)
- Added SYS_WAKE# signal at RSVD module pin 848. This is only supported on Jetson TX2i.
- 2-pin headers for Reset (J3), Power (J6), Force Recovery (J9) and Force Power Off (J9) headers are replaced with a single 10-pin header (Automation Header - J20).
- Power LED header moved near one end of the JTAG header (J7).
- SATA connector changed to Right Angle type to avoid possible conflict with PCIe card.
- The Auto-Power-On option designed into the Jetson TX2 module will not work with the C02 carrier board due to the power-on type control circuitry. See Appendix: P2597_C02 Auto-Power-On Rework for instructions for modifying P2597_C02 boards to support Auto-Power-On.

Note: When Jetson TX2i is used with a P2597 C02 carrier board, the system can be powered on with just a momentary press of the power button (same as the Jetson TX2/TX2 4GB with the P2597 B02/B04 carrier boards). When Jetson TX2i is installed in a P2597 B02/B04 carrier board, the system will power on as soon as the main power is connected due to the different PMIC on the TX2i module which has a level based on input instead of pulse based. If the power button is pressed, the module and system will power off. The power button cannot be used to put the system in a sleep mode.

2.0 JETSON CARRIER BOARD STANDARD CONNECTORS

The Jetson carrier board provides several standard connectors to support additional functionality. This includes:

- USB 2.0: Micro AB Connector
- USB 3.0: Type A Connector
- Gigabit Ethernet: RJ45 Connector
- SATA: Standard SATA Connector, 22-pin including power
- SD Card (Full size) Connector/Cage
- HDMI: Type A Connector
- M.2, Key E Socket
- PCIe® x4 Connector
- JTAG header, 2x10, 2.54mm pitch

2.1 USB Ports

The carrier board supports two USB Connectors. One is a USB 2.0 Micro AB connector (J20 on P2597_B02/B04 – J28 on P2597_C02) supporting Device/Host modes as well as USB Recovery mode. The other is a USB 3.0 Type A connector (J19) supporting Host mode only.

Table 1. USB 2.0 Micro AB Connector Pin Descriptions

Connector Pin #	Jetson Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
1	–	–	VBUS Supply	Power
2	USB0_D–	B39	USB 2.0 #0 Data	Bidir
3	USB0_D+	B40		
4	USB0_OTG_ID	A36	USB 2.0 #0 Identification	Input
5	–	–	Ground	Ground
–	USB0_VBUS_DET	B37	USB VBUS Detect	Input
–	USB0_EN_OC#	A17	USB Enable/Overcurrent #0. Connected to Enable & OC pins of VBUS load switch.	Bidir

Table 2. USB 3.0 Type A Connector Pin Descriptions

Connector Pin #	Jetson Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
1	–	–	VBUS Supply	Power
2	USB1_D–	A39	USB 2.0 #1 Data	Bidir
3	USB1_D+	A38		
4	–	–	Ground	Ground
5	USB_SS0_RX–	F44	USB 3.0 #0 Receive	Input
6	USB_SS0_RX+	F43		
7	–	–	Ground	Ground
8	USB_SS0_TX–	C44	USB 3.0 #0 Transmit	Output
9	USB_SS0_TX+	C43		
–	USB1_EN_OC#	A18	USB Enable/Overcurrent #1. Connected to Enable & OC pins of VBUS load switch.	Bidir

Legend Ground | Power | Reserved

Note: In the Type/Dir column, Output is to USB Connectors. Input is from USB Connectors. Bidir is for Bidirectional signals.

2.2 Gigabit Ethernet

The carrier board implements an RJ45 connector (J5) along with the necessary magnetics device.

Table 3. Ethernet RJ45 Connector Pin Descriptions

Connector Pin #	Jetson Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
1	GPE_MDI0+	E48	Gigabit Ethernet MDI 0+	Bidir
2	GPE_MDI0–	E49	Gigabit Ethernet MDI 0–	Bidir
3	GPE_MDI1+	F47	Gigabit Ethernet MDI 1+	Bidir
4	GPE_MDI2+	F48	Gigabit Ethernet MDI 2+	Bidir
5	GPE_MDI2–	G48	Gigabit Ethernet MDI 2–	Bidir
6	GPE_MDI1–	G49	Gigabit Ethernet MDI 1–	Bidir
7	GPE_MDI3+	H47	Gigabit Ethernet MDI 3+	Bidir
8	GPE_MDI3–	H48	Gigabit Ethernet MDI 3-	Bidir
9	GBE_LINK_ACT	E47	Connected to LED #1 through resistor	Output OD
10	–	–	Connected to VDD_3V3_SYS	–
11	GBE_LINK100	F50	Connected to LED #2 through resistor	Output OD
12	–	–	Connected to VDD_3V3_SYS	–
13	–	–	Ground	Ground
14	–	–	Ground	Ground

Legend	Ground	Power	Reserved

Notes: In the Type/Dir column, Output is to RJ45 Connector. Input is from RJ45 Connector. Bidir is for Bidirectional signals.

2.3 SATA

The Jetson carrier board has a standard SATA connector (J1 - both Data & Power) as shown below.

Table 4. SATA Connector Pin Descriptions

Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	–	–	Ground	Ground	8	–	–	Unused	Unused
2	SATA_TX+	D45	SATA Transmit	Output	9				
3	SATA_TX–	D46			10	SATA_DEV_SLP	D47	SATA Device Sleep	Output
4	–	–	Ground	Ground	11	–	–	Ground	Ground
5	SATA_RX–	G45	SATA Receive	Input	12				
6	SATA_RX+	G46			13				
7	–	–	Ground	Ground	14	–	–	Gated version of Main 5.0V Supply	Power
					15				
					16				
					17	–	–	Ground	Ground
					18	–	–	Unused	Unused
					19	–	–	Ground	Ground
					20	–	–	12V Supply (From Boost on carrier board)	Power
					21				
					22				

Legend	Ground	Power	Reserved

Notes: In the Type/Dir column, Output is to SATA Connector. Input is from SATA Connector. Bidir is for Bidirectional signals.

2.4 SD Card

A full-size SD Card (J12) is implemented, supporting up to SDR104 mode (UHS-1).

Table 5. SD Card Socket Pin Descriptions

Connector Pin #	Jetson Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
1	SDCARD_D3	F18	SD Card Data #3	Bidir
2	SDCARD_CMD	G19	SD Card Command	Bidir
3	–	–	Ground	Ground
4	–	–	SD Card Power	Power
5	SDCARD_CLK	G18	SD Card Clock	Output
6	–	–	Ground	Ground
7	SDCARD_D0	H18	SD Card Data #0	Bidir
8	SDCARD_D1	H17	SD Card Data #1	Bidir
9	SDCARD_D2	F19	SD Card Data #2	Bidir
10	SDCARD_CD#	F17	SD Card, Card Detect	Input
11	–	–	Ground	Ground
12	SDCARD_WP	F20	SD Card Write Protect	Input
13/14/15	–	–	Ground	Ground
–	SDCARD_VDD_EN	H16	SD Card load switch Enable	Output

Legend	Ground	Power	Reserved

Notes: In the Type/Dir column, Output is to SD Card Socket. Input is from SD Card Socket. Bidir is for Bidirectional signals.

2.5 HDMI

A standard HDMI type A connector (J16) is supported.

Table 6. HDMI Connector Pin Descriptions

Connector Pin #	Jetson Module Pin Name	Module Pin #	Usage/Description	Type/Dir Default
1	DP1_TXD0+	E39	HDMI Transmit Data 2+	Output
2	–		Ground	Ground
3	DP1_TXD0–	E38	HDMI Transmit Data 2–	Output
4	DP1_TXD1+	C38	HDMI Transmit Data 1+	Output
5	–		Ground	Ground
6	DP1_TXD1–	C37	HDMI Transmit Data 1–	Output
7	DP1_TXD2+	D37	HDMI Transmit Data 0+	Output
8	–		Ground	Ground
9	DP1_TXD2–	D36	HDMI Transmit Data 0–	Output
10	DP1_TXD3+	E36	HDMI Transmit Clock+	Output
11				
12	DP1_TXD3–	E35	HDMI Transmit Clock–	Output
13	HDMI_CEC	B33	HDMI CEC	Bidir
14	–	–	Unused	Unused
15	DP1_AUX_CH+	A35	HDMI DDC Clock	Output /OD
16	DP1_AUX_CH–	A34	HDMI DDC Data	Bidir/OD
17	–	–	Ground	Ground
18	–	–	HDMI 5V Power	Power
19	DP1_HPD	A33	Hot Plug Detect	Input
–	–	–	HDMI Termination Enable (GPIO Expander P14)	Output

Legend	Ground	Power	Reserved

Notes: In the Type/Dir column, Output is to HDMI Connector. Input is from HDMI Connector. Bidir is for Bidirectional signals.

2.6 M.2, Key E Expansion Connector

The Jetson carrier board includes a M.2, Key E Slot Mini-PCIe Expansion connector (J18). This includes interface options for WLAN/BT including PCIe (x1), SDIO (4-bit, Jetson TX2 4GB/TX2i only), USB 2.0, UART, I2S & I2C.

Table 7. M.2, Key E Expansion Connector Pin Descriptions

Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	–	–	Ground	Ground		–	–	–	–
3	USB2_D+	B42	USB 2.0 #2 Data	Bidir	2	–	–	Main 3.3V Supply	Power
5	USB2_D–	B43			4				
7	–	–	Ground	Ground	6	–	–	LED #1 (CR4 – Green) Enable	Output
9	SDIO_CLK	B30	SDIO Clock	Output	8	I2S2_CLK	G5	I2S #2 Clock	Bidir
11	SDIO_CMD	B29	SDIO Command	Bidir	10	I2S2_LRCLK	H5	I2S #2 Left/Right Clock	Bidir
13	SDIO_D0	B32	SDIO Data 0	Bidir	12	I2S2_SDIN	G6	I2S #2 Data In	Input
15	SDIO_D1	A32	SDIO Data 1	Bidir	14	I2S2_SDOUT	H6	I2S #2 Data Out	Bidir
17	SDIO_D2	A31	SDIO Data 2	Bidir	16	–	–	LED #2 (CR3 – Green) Enable	Output
19	SDIO_D3	A30	SDIO Data 3	Bidir	18	–	–	Ground	Ground
21	GPIO10_WIFI_WAKE_AP	B20	WLAN M.2 Wake AP	Input	20	GPIO13_BT_WAKE_AP	B22	Bluetooth #2 Wake AP	Input
23	SDIO_RST	A29	WLAN M.2 Enable	Output	22	UART2_RX	B15	UART #2 Receive	Input
25	–	–	Unused	Unused	24	–	–	Unused	Unused
27					26				
29					28				
31					30				
33	–	–	Ground	Ground	32	UART2_TX	B16	UART #2 Transmit	Output
35	PEX1_TX+	E41	PCIe #1 Transmit	Output	34	UART2_CTS#	A15	UART #2 Clear to Send	Input
37	PEX1_TX–	E42			36	UART2_RTS#	A16	UART #2 Request to Send	Output
39	–	–	Ground	Ground	38	–	–	Unused	Unused
41	PEX1_RX+	H41	PCIe #1 Receive	Input	40				
43	PEX1_RX–	H42			42				
45	–	–	Ground	Ground	44				
47	PEX1_REFCLK+	B45	PCIe #1 Reference clock	Output	46				
49	PEX1_REFCLK–	B46			48				
51	–	–	Ground	Ground	50	(32.768KHz OSC)	–	Suspend Clock (32KHz)	Output
53	PEX1_CLKREQ#	C47	PCIe #1 Clock Request	Bidir	52	PEX1_RST	E50	PCIe Reset	Output
55	PEX_WAKE#	D48	PCIe Wake	Input	54	GPIO12_BT_EN	B21	WLAN Disable #2	Output
57	–	–	Ground	Ground	56	(3.3V GPIO Exp. P00)	–	WLAN Disable #1	Output
59	–	–	Unused	Unused	58	I2C_GP0_DAT	D15	General I2C #0 Data. See note.	Bidir/OD
61					60	I2C_GP0_CLK	E15	General I2C #0 Clock. See note.	Bidir/OD
63	–	–	Ground	Ground	62	(3.3V GPIO Exp. P10)	–	M.2, Key E Connector Alert	Input
65	–	–	Unused	Unused	64	–	–	Unused	Unused
67					66				
69	–	–	Ground	Ground	68				
71	–	–	Unused	Unused	70				
73					72	–	–	Main 3.3V Supply	Power
75	–	–	Ground	Ground	74				

Legend

Ground	Power	Not available on Jetson TX2 (TX2 4GB/TX2i only)	Reserved

Notes:
- In the Type/Dir column, Output is to M.2 Module. Input is from M.2 Module. Bidir is for Bidirectional signals.
- Prior to the M.2 Key E revision 1.1 spec., the I2C interface was referenced to 3.3V. The 1.1 revision changes this to 1.8V. By default, the carrier board connects these pins to the 1.8V level I2C interface. Stuffing resistors can be changed to connect to the I2C interface through level shifters for 3.3V operation instead.

Check the Jetson TX2 Series OEM Product Design Guide for M.2 connection details and routing guidelines for the different interfaces supported. For routing max length/delay calculations, include the worst-case carrier board PCB trace delays in the table below when calculating max trace length.

Table 8. M.2 Related Carrier Board PCB Trace Delays

Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for M.2 Module (ps)		Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for M.2 Module (ps)	
PCIe	540	880	340		**SDIO**		**≤ SDR50**	**>SDR50**	**≤ SDR50**	**>SDR50**
USB	175	960	785		SDIO	240	876	521	636	281
I2S2	970	3600	2630							

Notes: The SDIO interface is not available on Jetson TX2.

2.7 PCIe x4 Connector

The Jetson carrier board includes a standard 4-lane PCIe connector (J2).

Table 9. PCIe 4-lane Connector Pin Descriptions

Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir
A1	–	–	Ground	Ground	**B1**	–	–	12V Supply	Power
A2	–	–	12V Supply (Boost)	Power	**B2**				
A3					**B3**				
A4	–	–	Ground	Ground	**B4**	–	–	Ground	Ground
A5	–	–	Unused	Unused	**B5**	I2C_GP0_CLK	E15	General I2C #0 Clock	Bidir/OD
A6					**B6**	I2C_GP0_DAT	D15	General I2C #0 Data	Bidir/OD
A7					**B7**	–	–	Ground	Ground
A8					**B8**	–	–	3.3V supply – off in Deep Slp	Power
A9	–	–	3.3V supply - off in Deep Slp	Power	**B9**	–	–	Pulled to GND	–
A10					**B10**	–	–	Main 3.3V Supply	Power
A11	PEX0_RST#	C49	PCIe Lane 0 Reset	Output	**B11**	PEX_WAKE#	D48	PCIe Wake (Shared)	Input
A12	–	–	Ground	Ground	**B12**	PEX0_CLKREQ#	C48	PCIe Ctlr 0 Clock Req.	Bidir
A13	PEX0_REFCLK+	A44	PCIe Ctlr 0 Reference Clock	Output	**B13**	–	–	Ground	Ground
A14	PEX0_REFCLK–	A45			**B14**	PEX0_TX+	E44	PCIe Ctlr 0 Lane 0 Transmit	Output
A15	–	–	Ground	Ground	**B15**	PEX0_TX–	E45		
A16	PEX0_RX+	H44	PCIe Ctlr 0 Lane 0 Receive	Input	**B16**	–	–	Ground	Ground
A17	PEX0_RX–	H45			**B17**	–	–	Unused	Unused
A18	–	–	Ground	Ground	**B18**	–	–	Ground	Ground
A19	–	–	Unused	Unused	**B19**	USB_SS1_TX+	D42	PCIe Ctlr 0 Lane 1 Transmit	Output
A20	–	–	Ground	Ground	**B20**	USB_SS1_TX–	D43		
A21	USB_SS1_RX+	G42	PCIe Ctlr 0 Lane 1 Receive	Input	**B21**	–	–	Ground	Ground
A22	USB_SS1_RX–	G43			**B22**				
A23	–	–	Ground	Ground	**B23**	PEX2_TX+	C40	PCIe Ctlr 0 Lane 2 Transmit	Output
A24					**B24**	PEX2_TX–	C41		
A25	PEX2_RX+	F40	PCIe Ctlr 0 Lane 2 Receive	Input	**B25**	–	–	Ground	Ground
A26	PEX2_RX–	F41			**B26**				
A27	–	–	Ground	Ground	**B27**	PEX_RFU_TX+	D39	PCIe Ctlr 0 Lane 3 Transmit	Output
A28					**B28**	PEX_RFU_TX–	D40		
A29	PEX_RFU_RX+	G39	PCIe Ctlr 0 Lane 3 Receive	Input	**B29**	–	–	Ground	Ground
A30	PEX_RFU_RX–	G40			**B30**	–	–	Unused	Unused
A31	–	–	Ground	Ground	**B31**				
A32	–	–	Unused	Unused	**B32**	–		Ground	Ground

Legend Ground | Power | Reserved

Notes: In the Type/Dir column, Output is to the PCIe Connector. Input is from the PCIe Connector. Bidir is for Bidirectional signals.

Check the Jetson TX2 Series OEM Product Design Guide for PCIe connection details and routing guidelines. For routing max length/delay calculations, include the worst-case carrier board PCB trace delays in the table below when calculating max trace length.

Table 10. PCIe x4 Related Carrier Board PCB Trace Delays

Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for PCI Board (ps)
PCIe	540	880	340

2.8 JTAG

The Jetson carrier board has a standard 20-pin (2x10, 2.54mm pitch) JTAG header (J7).

Table 11. JTAG Header Descriptions

Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	–	–	Main 1.8V Supply	Power	2	–		Main 1.8V Supply	Power
3	–	–	JTAG Test Reset	Output	4	–	–	Ground	Ground
5	JTAG_TDI	B12	JTAG Test Data In	Input	6				
7	JTAG_TMS	A12	JTAG Test Mode Select	Input	8				
9	JTAG_TCK	B11	JTAG Test Clock	Input	10				
11	JTAG_RTCK	A14	JTAG Test Return Clock	Output	12				
13	JTAG_TDO	A13	JTAG Test Data Out	Output	14				
15	RESET_IN#	A47	Main carrier board reset	Input	16				
17	–	–	Pulled-down	–	18				
19	–	–	Pulled-down	–	20				
–	JTAG_GP1		JTAG General Purpose #1 (NV JTAG Select)	Input					

Legend

Ground	Power	Reserved

Notes: In the Type/Dir column, Output is to JTAG header. Input is from JTAG header. Bidir is for Bidirectional signals.

3.0 CARRIER BOARD CUSTOM EXPANSION CONNECTIONS

The Jetson carrier board supports several custom expansion headers:

- Jetson Module Connector, 8x50, 1.27mm pitch
- Display Expansion Connector, 2x60, 0.5mm pitch
- Camera Expansion Connector, 2x60, 0.5mm pitch
- 40-Pin Expansion Header, 2x20, 2.54mm pitch
- Serial Port Header, 1x6, 2.54mm pitch
- Secondary Expansion Header, 2x15, 2.54mm pitch
- Charge Control Connector, 10-pin Flex Receptacle, 0.8mm pitch
- Fan Header, 4-pin, 1.25mm pitch
- DC Power Jack

The Routing Guidelines for the interfaces supported on the expansion connectors can be found in the Jetson TX2 Series OEM Product Design Guide (OEM DG). Those guidelines cover the PCB routing from the Jetson module to the peripheral device or actual device connector. When designing modules for one of the Jetson module expansion connectors, the routing on the carrier board must be accounted for. Tables are provided for the critical interfaces that provide the PCB delays on the carrier board. These delays are subtracted from the delays allowed in the OEM DG routing guidelines. The tables also include the max trace guidelines and remaining max trace delay allowed on the peripheral modules. See the OEM DG for other requirements (Impedance, trace spacing, skews between signals, etc.).

3.1 Module Connector

The carrier board interfaces to the Jetson module using a 400-pin (8 x 50) connector (J13). The part number for the connector used on the carrier board can be found in the Jetson TX2 Series Supported Component List (SCL) document. This interfaces with the module which has a Samtec REF-186137-01 connector. The connector pinout can be found in the OEM DG.

3.2 Display Expansion Connector

The Jetson carrier board includes a 120-pin (2x60, 0.5mm pitch) Display Expansion Connector (J23). The connector used on the carrier board is a Samtec QSH-060-01-H-D-A. The mating connector is a Samtec QTH-060-01-H-D-A. This expansion connector includes interface options for an embedded display and touch controller including:

- DSI 2 x4
- eDP
- eDP HPD
- eDP AUX
- LCD BL EN/PWM
- LCD EN/TE/BIAS EN
- SPI0, SPI2
- I2C_GP1
- Touch INT/RST/CLK
- Display control

Table 12. Display Expansion Connector Pin Descriptions

Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	DSI3_D1–	E30	DSI 3 Data 3	Output	2	–	–	Backlight power from Main DC supply	Power
3	DSI3_D1+	E29			4				
5	–	–	Ground	Ground	6				
7	DSI3_D0–	C32	DSI 3 Data 2	Output	8	LCD_BKLT_EN	B28	Backlight Enable	1.8V Output
9	DSI3_D0+	C31			10	LCD_BKLT0_PWM	B27	Backlight PWM	1.8V Output
11	–	–	Ground	Ground	12	LCD_VDD_EN	B26	LCD Enable	1.8V Output
13	DSI3_CLK–	D31	DSI 3 Clock	Output	14	LCD_TE	A25	LCD Tearing Effect	1.8V Input
15	DSI3_CLK+	D30			16	–	–	3.3V supply - off in Deep Slp	Power

Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir
17	–	–	Ground	Ground	18	(1.8V GPIO Exp. P15)	–	Bridge Enable	1.8V Output
19	DSI2_D1–	H30	DSI 2 Data 1	Output	20	(1.8V GPIO Exp. P17)	–	Bridge Interrupt	1.8V Input
21	DSI2_D1+	H29			22	I2C_GP0_CLK	E15	General I2C #0 Clock	1.8V Bidir/OD
23	–	–	Ground	Ground	24	I2C_GP0_DAT	D15	General I2C #0 Data	1.8V Bidir/OD
25	DSI2_D0–	F32	DSI 2 Data 0	Output	26	–	–	3.3V supply for touchscreen	Power
27	DSI2_D0+	F31			28	–	–	1.8V supply for touchscreen	
29	–	–	Ground	Ground	30	I2C_GP1_CLK	A21	General I2C #1 Clock	3.3V Bidir/OD
31	DSI1_D1–	E33	DSI 1 Data 3	Output	32	I2C_GP1_DAT	A20	General I2C #1 Data	3.3V Bidir/OD
33	DSI1_D1+	E32			34	GPIO6_TOUCH_INT	B25	Touchscreen Interrupt	1.8V Input
35	–	–	Ground	Ground	36	GPIO7_TOUCH_RST	B23	Touchscreen controller Reset	1.8V Output
37	DSI1_D0–	C35	DSI 1 Data 2	Output	38	SPI0_CLK	E3	Touchscreen SPI Clock	1.8V Bidir
39	DSI1_D0+	C34			40	SPI0_MISO	E4	Touchscreen SPI MISO	1.8V Bidir
41	–	–	Ground	Ground	42	SPI0_MOSI	F4	Touchscreen SPI MOSI	1.8V Bidir
43	DSI0_CLK–	G34	DSI 0 Clock	Output	44	SPI0_CS0#	F3	Touchscreen SPI Chip Select	1.8V Bidir
45	DSI0_CLK+	G33			46	–	–	Unused	Unused
47	–	–	Ground	Ground	48	–	–	Ground	Ground
49	DSI0_D1–	H33	DSI 0 Data 1	Output	50	TOUCH_CLK	B24	Touchscreen Controller Clock	1.8V Output
51	DSI0_D1+	H32			52	–	–		Ground
53	–	–	Ground	Ground	54	–	–	Gated 3.3V analog supply	Power
55	DSI0_D0–	F35	DSI 0 Data 0	Output	56				Power
57	DSI0_D0+	F34			58	–	–	Gated 1.8V supply	
59	–	–	Ground	Ground	60	–	–	Ground	Ground
61	–	–	Main 3.3V Supply (Switcher)	Power	62	LCD_VDD_EN	B26	LCD Power Enable	1.8V Output
63					64	–	–	Unused	Unused
65	–	–	Ground	Ground	66	DSI1_CLK+	D33	Display DSI 1 Clock	Output
67					68	DSI1_CLK-	D34		
69	–	–	Main 1.8V Supply (Switcher)	Power	70	–	–	Ground	Ground
71					72	DSI3_CLK+	D30	Display DSI 3 Clock	Output
73	–	–	Ground	Ground	74	DSI3_CLK-	D31		
75					76	–	–	Ground	Ground
77	–	–	1.2V Display Supply (LDO)	Power	78				
79					80	–	–	Main 5.0V Supply (Switcher)	Power
81	–	–	Ground	Ground	82	–	–	Unused	Unused
83					84				
85	DP_HPD	B36	Display Port 0 Hot Plug Det.	Input	86	CHARGER_PRSNT	A49	AC OK	5V Output
87	DP0_AUX_CH–	B34	Display Port 0 Aux Channel	Bidir	88	(1.8V GPIO Exp. P04)	–	LCD BIAS Enable	1.8V Output
89	DP0_AUX_CH+	B35			90	–	–	Ground	Ground
91	–	–	Ground	Ground	92	GSYNC_VSYNC	A27	GSYNC Vertical sync	1.8V Output
93	DP0_TX0+	H39	Display Port 0 Data Lane 0	Output	94	GSYNC_HSYNC	A26	GSYNC Horizontal sync	1.8V Output
95	DP0_TX0–	H38			96	–	–	Ground	Ground
97	–	–	Ground	Ground	98	(1.8V GPIO Exp. P16)	–	NV Sensor Interrupt	1.8V Input
99	DP0_TX1+	F38	Display Port 0 Data Lane 1	Output	100	LCD_BKLT1_PWM	A24	Backlight PWM	1.8V Output
101	DP0_TX1–	F37			102	–	–	Ground	Ground
103	–	–	Ground	Ground	104	SPI2_SCK	H14	SPI #2 Clock	1.8V Bidir
105	DP0_TX2+	G37	Display Port 0 Data Lane 2	Output	106	SPI2_MISO	H15	SPI #2 Master In, Slave Out	
107	DP0_TX2–	G36			108	SPI2_MOSI	G15	SPI #2 Master Out, Slave In	
109	–	–	Ground	Ground	110	SPI2_CS0#	G16	SPI #2 Chip Select	
111	–	–	Unused	Unused	112	–	–	Ground	Ground
113					114	–	–	Unused	Unused
115	–	–	Ground	Ground	116				
117	DP0_TX3+	H36	Display Port 0 Data Lane 3-	Output	118				
119	DP0_TX3–	H35			120				

Legend Ground | Power | Reserved

Notes: In the Type/Dir column, Output is to Display Module. Input is from Display Module. Bidir is for Bidirectional signals.

The DevKit carrier board display connector supports eight total MIPI DSI data lanes and two clock lanes, allowing up to two 4-lane interfaces. These can be used for two separate displays, or together for a single display (clock lane per 4 data lanes still applies for the single display case. Each data lane has peak bandwidth up to 1.5Gbps. In addition, the display connector supports a DP/eDP interface. Check the Jetson TX2 Series OEM Product Design Guide for DSI and DP/DP connection details and routing guidelines. For routing max length/delay calculations, include the worst-case carrier board PCB trace delays in the following tables when calculating max trace lengths.

Table 13. Display Connector Interface Related Carrier Board PCB Trace Delays (DSI & SPI)

Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Display Module (ps)
DSI	500	1100	600
SPI[2,0]	760	1760	1000

Notes: Max Trace Delay Allowed for SPI assumes a single load case. If two loads are implemented, See the Jetson TX2 Series OEM Product Design Guide for details.

Table 14. Display Connector Interface Related Carrier Board PCB Trace Delays (DP0)

Jetson Module Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for Display Module (ps)	
		RBR/HBR Stripline	RBR/HBR uStrip	RBR/HBR Stripline	RBR/HBR uStrip
DP0	660	1138	975	477	315
DP0_AUX	529	1138	975	608	446

3.3 Camera Expansion Connector

The Jetson carrier board includes a 120-pin (2x60, 0.5mm pitch) Camera Expansion Connector (J22). The connector used on the carrier board is a Samtec QSH-060-01-H-D-A. The mating connector is a Samtec QTH-060-01-H-D-A. The expansion connector includes interface options for multiple cameras as well as some for audio (I2S & DMIC):

- CSI up to 6x2 lane
- CAM_I2C, Clock & Control GPIOs for the Cameras
- Digital Microphone IF
- I2S
- SPI
- I2C
- UART

Table 15. Camera Expansion Connector Pin Descriptions

Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	CSI0_D0+	F29	CSI 0 Data 0	Input	2	CSI1_D0_P	C29	CSI 1 Data 0	Input
3	CSI0_D0–	F28			4	CSI1_D0_N	C28		
5	–	–	Ground	Ground	6	–	–	Ground	Ground
7	CSI0_CLK+	G28	CSI 0 Clock	Input	8	CSI1_CLK_P	D28	CSI 1 Clock	Input
9	CSI0_CLK–	G27			10	CSI1_CLK_N	D27		
11	–	–	Ground	Ground	12	–	–	Ground	Ground
13	CSI0_D1+	H27	CSI 0 Data 1	Input	14	CSI1_D1_P	E27	CSI 1 Data 1	Input
15	CSI0_D1–	H26			16	CSI1_D1–	E26		
17	–	–	Ground	Ground	18	–	–	Ground	Ground
19	CSI2_D0+	F26	CSI 2 Data 0	Input	20	CSI3_D0+	C26	CSI 3 Data 0	Input
21	CSI2_D0–	F25			22	CSI3_D0–	C25		
23	–	–	Ground	Ground	24	–	–	Ground	Ground
25	CSI2_CLK+	G25	CSI 2 Clock	Input	26	CSI3_CLK+	D25	CSI 3 Clock	Input
27	CSI2_CLK–	G24			28	CSI3_CLK–	D24		
29	–	–	Ground	Ground	30	–	–	Ground	Ground
31	CSI2_D1+	H24	CSI 2 Data 1	Input	32	CSI3_D1+	E24	CSI 3 Data 1	Input
33	CSI2_D1–	H23			34	CSI3_D1–	E23		
35	–	–	Ground	Ground	36	–	–	Ground	Ground

Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir
37	CSI4_D0+	F23	CSI 4 Data 0	Input	38	CSI5_D0+	C23	CSI 5 Data 0	Input
39	CSI4_D0–	F22			40	CSI5_D0–	C22		
41	–	–	Ground	Ground	42	–	–	Ground	Ground
43	CSI4_CLK+	G22	CSI 4 Clock	Input	44	CSI5_CLK+	D22	CSI 5 Clock	Input
45	CSI4_CLK–	G21			46	CSI5_CLK–	D21		
47	–	–	Ground	Ground	48	–	–	Ground	Ground
49	CSI4_D1+	H21	CSI 4 Data 1	Input	50	CSI5_D1+	E21	CSI 5 Data 1	Input
51	CSI4_D1–	H20			52	CSI5_D1–	E20		
53	–	–	Ground	Ground	54	–	–	Ground	Ground
55	–	–	Unused	Unused	56	–	–	Unused	Unused
57					58				
59	–	–	Camera UART Present – Direction control for level shifter to prevent contention.	–	60				
61	–	–	Camera UART TX/RX/CTS/RTS – Can optionally be brought to Serial port connector (J13).	Output	62	SPI2_CLK	H14	SPI #2 Clock	Bidir
63	–	–		Input	64	SPI2_MISO	H15	SPI #2 MISO	Bidir
65	–	–		Input	66	SPI2_CS1#	F16	SPI #2 Chip Select	Bidir
67	–	–		Output	68	SPI2_MOSI	G15	SPI #2 MOSI	Bidir
69	–	–	Ground	Ground	70	–	–	Ground	Ground
71	AO_DMIC_IN_CLK	E16	Digital Mic Input Clock	Output	72	I2S3_CLK	E6	I2S #3 Clock	Bidir
73	AO_DMIC_IN_DAT	D16	Digital Mic Input Data	Input	74	I2S3_LRCLK	F5	I2S #3 Left/Right Clock	Bidir
75	I2C_CAM_CLK	C6	Camera I2C clock	Bidir	76	I2S3_SDIN	E5	I2S #3 Serial Data In	Input
77	I2C_CAM_DAT	C5	Camera I2C data	Bidir	78	I2S3_SDOUT	F6	I2S #3 Serial Data Out	Bidir
79	–		Ground	Ground	80	–	–	Ground	Ground
81	(AVDD_CAM)	–	2.8V Camera supply (LDO)	Power	82	(AVDD_CAM)	–	2.8V Camera supply (LDO)	Power
83					84	(VDD_3V3_SLP)	–	3.3V rail - off in Deep Sleep	Power
85	–	–	Camera auto-focus powerdn	Output	86	CAM_VSYNC	E8	Camera Vertical Sync	Output
87	I2C_PM_CLK	A6	Power Monitor I2C Clock	Bidir/OD	88	CAM1_MCLK	F8	Camera #1 Master Clock	Output
89	I2C_PM_DAT	B6	Power Monitor I2C Data	Bidir/OD	90	GPIO1_CAM1_PWR	F7	Camera #1 Powerdown	Output
91	CAM0_MCLK	F9	Camera #0 Master Clock	Output	92	GPIO3_CAM1_RST	H7	Camera #1 Reset	Output
93	GPIO0_CAM0_PWR	G8	Camera #0 Powerdown	Output	94	CAM2_MCLK	E7	Camera #2 Master Clock	Output
95	GPIO2_CAM0_RST	H8	Camera #0 Reset	Output	96	(1.8V GPIO Exp. P07)	–	Camera #2 Powerdown	Output
97	GPIO5_CAM_FLASH_EN	D7	Flash Enable	Output	98	(1.8V GPIO Exp. P10)	–	Camera #2 Reset	Output
99	–	–	Ground	Ground	100	–	–	Ground	Ground
101	(DVDD_CAM_IO_1V2)	–	1.2V digital Camera supply	Power	102	(DVDD_CAM_IO_1V8)	–	Switched 1.8V supply.	Power
103	–	–	Flash Inhibit	Output	104	(1.8V GPIO Exp. P05)	–	Torch Enable	Output
105	I2C_GP0_CLK	E15	General I2C #0 Clock	Bidir/OD	106	GPIO4_CAM_STROBE	G7	Flash Strobe	Output
107	I2C_GP0_DAT	D15	General I2C #0 Data	Bidir/OD	108	(VDD_3V3_SLP)	–	3.3V supply – off in Deep Slp	Power
109	–	–	Main 5.0V Supply (Switcher)	Power	110				
111	–	–	Unused	Unused	112	GPIO9_MOTION_INT	G14	Motion Sensor Interrupt	Input
113					114	–		Unused	Unused
115	–	–	Ground	Ground	116	–		Ground	Ground
117	GPIO17_MDM2AP_READY	B9	Modem to Tegra Ready	Input	118	(VDD_5V0_IO_SYS)	–	Main 5.0V Supply (Switcher)	Power
119	(1.8V GPIO Exp. P03)	–	System power enable	Output	120				

Legend Ground | Power | Reserved

Notes: In the Type/Dir column, Output is to Camera Module. Input is from Camera Module. Bidir is for Bidirectional signals.

See the Jetson TX2 Series OEM Product DG for CSI connection and routing guidelines. For routing, include the worst-case carrier board PCB trace delays per interface in the following table when calculating max trace lengths.

Table 16. Camera Expansion Connector Related Carrier Board PCB Trace Delays

Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Camera Module (ps)		Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Camera Module (ps)
CSI0	627	1100	473		CSI4	54	1100	559
CSI1	627	1100	473		CSI5	541	1100	559
CSI2	588	1100	512		I2S3	500	3600	3100
CSI3	588	1100	512		SPI2	660	1760	1100

Notes: Max Trace Delay Allowed for SPI assumes a single load case. If two loads are implemented, See the Jetson TX2 Series OEM Product Design Guide for details.

3.4 40-Pin Expansion Header

The Jetson carrier board includes a 40-pin (2x20, 2.54mm pitch) Expansion Header (J21). The connector used on the carrier board is a Samtec TSM-120-01-S-DV-TR. The expansion header includes various audio & control interfaces including:

- I2S, Audio Clock/Control & Digital Microphone IF
- I2C (x2), SPI & UART

Note: Some of these interfaces can be 1.8V or 3.3V. J24 is a 3-pin header that is used to control the voltage of the level shifter these interfaces pass through. If J24 pin 1-2 are shorted, the interfaces are level shifted to 3.3V. If pins 2-3 are shorted, the interfaces are 1.8V. The 3.3V only interfaces/signals are I2C_GP[1:0]_x, UART0_x, GPIO_EXP_P[17:16], GPIO9_MOTION_INT, and GPIO8_ALS_PROX_INT.

Table 17. 40-Pin Expansion Header Pin Descriptions

Hdr Pin #	Module Pin Name	Mod. Pin #	Tegra Pin Name	Default Usage/Desc.	Alternate Usage/Desc.	Type/ Direction (Default)	Voltage Level	GPIO (I_{OL}/I_{OH}) or Power Pin Current Cap.	Tegra GPIO Port #	Power on/ Pinmux Defaults	PU/PD on (module) & carrier board	Notes
1	–	–	–	3.3V Supply	–	Power	–	2A	–	–	–	1
2	–	–	–	5.0V Supply	–	Power	–	2A	–	–	–	1
3	I2C_GP0_DAT	B6	GEN2_I2C_SDA	I2C	GPIO	Bidir-OD	3.3V	3mA / -3mA	–	Z	(1kΩ to 1.8V)	2
4	–	–	–	5.0V Supply	–	Power	–	2A	–	–	–	1
5	I2C_GP0_CLK	A6	GEN2_I2C_SCL	I2C	GPIO	Bidir-OD	3.3V	3mA / -3mA	–	Z	(1kΩ to 1.8V)	2
6	–	–	–	Ground	–	Ground	–	–	–	–	–	–
7	AUDIO_MCLK	F1	AUD_MCLK	GPIO	Audio Clock	Input	1.8/3.3V	20uA / -20uA	J.04	PD/PU	1MΩ to GND	3
8	UART0_TX	H12	UART1_TX	UART	GPIO	Output	3.3V	24mA / -24mA	T.00	PU	PU or PD	4, 9
9	–	–	–	Ground	–	Ground	–	–	–	–	–	–
10	UART0_RX	G12	UART1_RX	UART	GPIO	Input	3.3V	–	T.01	PU	100kΩ to 3.3V	4
11	UART0_RTS#	G11	UART1_RTS	GPIO	UART	Input	3.3V	24mA / -24mA	T.02	PD	PU or PD	4, 9
12	I2S0_CLK	G2	DAP1_SCLK	GPIO	I2S	Input	1.8/3.3V	20uA / -20uA	J.00	PD	1MΩ to GND	3
13	GPIO20_AUD_INT	H3	GPIO_AUD0	GPIO	–	Input	1.8/3.3V	20uA / -20uA	J.05	PD	1MΩ to GND	3
14	–	–	–	Ground	–	Ground	–	–	–	–	–	–
15	(3.3V GPIO Exp. P17)	–	–	GPIO	GPIO	Bidir	3.3V	25mA / -10mA	–	Z	1MΩ to GND	5, 10
16	AO_DMIC_IN_DAT	D16	CAN_GPIO0	GPIO	DMIC	Input	1.8/3.3V	20uA / -20uA	AA.00	PD	1MΩ to GND	3
17	–	–	–	3.3V Supply	–	Power	–	2A	–	–	–	1
18	GPIO16_MDM_WAKE_AP	A10	GPIO_MDM2	GPIO	–	Input	1.8/3.3V	20uA / -20uA	Y.01	PD	1MΩ to GND	3
19	SPI1_MOSI	F13	GPIO_CAM6	GPIO	SPI	Input	1.8/3.3V	20uA / -20uA	N.05	PD	1MΩ to GND	3
20	–	–	–	Ground	–	Ground	–	–		–	–	–
21	SPI1_MISO	F14	GPIO_CAM5	GPIO	SPI	Input	1.8/3.3V	20uA / -20uA	N.04	PD	1MΩ to GND	3
22	(3.3V GPIO Exp. P16)	–	–	GPIO	GPIO	Bidir	3.3V	25mA / -10mA	–	Z	1MΩ to GND	5, 10
23	SPI1_CLK	G13	GPIO_CAM4	GPIO	SPI	Input	1.8/3.3V	20uA / -20uA	N.03	PD	1MΩ to GND	3
24	SPI1_CS0#	E14	GPIO_CAM7	GPIO	SPI	Input	1.8/3.3V	20uA / -20uA	N.06	PU	1MΩ to GND	3
25	–	–	–	Ground	Ground	Ground	–	–	–	–	–	–
26	–	–	–	Not Used	–	–	–	–	–	–	–	–
27	I2C_GP1_DAT	20	GEN1_I2C_SDA	I2C	GPIO	Bidir-OD	3.3V	3mA / -3mA	–	Z	(1kΩ to 3.3V)	6
28	I2C_GP1_CLK	A21	GEN1_I2C_SCL	I2C	GPIO	Bidir-OD	3.3V	3mA / -3mA	–	Z	(1kΩ to 3.3V)	6
29	GPIO19_AUD_RST	F2	GPIO_AUD1	GPIO	–	Input	1.8/3.3V	20uA / -20uA	J.06	PD/PU	1MΩ to GND	3
30	–	–	–	Ground	–	Ground	–	–	–	–	–	–

Hdr Pin #	Module Pin Name	Mod. Pin #	Tegra Pin Name	Default Usage/Desc.	Alternate Usage/Desc.	Type/ Direction (Default)	Voltage Level	GPIO (I_{OL}/I_{OH}) or Power Pin Current Cap.	Tegra GPIO Port #	Power on/ Pinmux Defaults	PU/PD on (module) & carrier board	Notes
31	GPIO9_MOTION_INT	G14	CAN_GPIO2	GPIO	–	Input	3.3V	1mA / -1mA	AA.02	Z/PU	47kΩ to 3.3V	2
32	AO_DMIC_IN_CLK	E16	CAN_GPIO1	GPIO	DMIC	Input	1.8/3.3V	20uA / -20uA	AA.01	PD	1MΩ to GND	3
33	GPIO11_AP_WAKE_BT	B19	GPIO_PQ5	GPIO	–	Input	1.8/3.3V	20uA / -20uA	I.05	PD	1MΩ to GND	3
34	–	–	–	Ground	–	Ground	–	–	–	–	–	–
35	I2S0_LRCLK	H1	DAP1_FS	GPIO	I2S	Input	1.8/3.3V	20uA / -20uA	J.03	PD	1MΩ to GND	3
36	UART0_CTS#	H11	UART1_CTS	GPIO	UART	Input	3.3V	–	T.03	PD	100kΩ to 3.3V	4
37	GPIO8_ALS_PROX_INT	H13	GPIO_PQ4	GPIO	–	Input	3.3V	1mA / -1mA	I.04	PD	47kΩ to 3.3V	2
38	I2S0_SDIN	G1	DAP1_DIN	GPIO	I2S	Input	1.8/3.3V	20uA / -20uA	J.02	PD	1MΩ to GND	3
39	–	–	–	Ground	–	Ground	–	–		–	–	–
40	I2S0_SDOUT	H2	DAP1_DOUT	GPIO	I2S	Input	1.8/3.3V	20uA / -20uA	J.01	PD	1MΩ to GND	3

Legend Ground | Power | Reserved

Notes:
1. This is current capability per power pin.
2. These pins are connected to Tegra through either an I2C (PCA9306) or FET (FDV301N) level shifter. They are open-drain.
3. These pins connect to TI TXB0108 level translators. The voltage level at the header pins can be selected by J24 to be 1.8V (2-3) or 3.3V (1-2). Due to the design of these devices, the output drivers are very weak, so they can be overdriven by another connected device output for bidirectional support.
4. These pins connect to a SN74LVC2T45 buffer, which is powered at 3.3V on the Expansion Header side.
5. These signals come from the TCA9539 GPIO expanders.
6. These pins are directly connected to Tegra. The max drive that meets full Data Sheet V_{OL}/V_{OH} is 1mA. 2mA drive is supported at restricted V_{OL}/V_{OH} levels. See the associated OEM Product Design Guide Pads section for details.
7. In the Type/Dir column, Output is to Exp. Module. Input is from Expansion Module. Bidir is for Bidirectional signals.
8. PD = Tegra Internal Pull-down, PU - Tegra Internal Pull-up, Z – Tristate
9. This pin is used for RAM Code strapping on the module and may be pulled up to 1.8V or pulled down with 4.7kΩ resistors. Care must be taken to make sure these signals are not pulled or driven up/down by any device connected to these pins during initial power-on.
10. These are not Jetson module signals but are included for completeness.

40-Pin Expansion Header Interface Guidelines

See the Jetson TX2 Series OEM Product DG for Routing Guidelines. Include the worst-case carrier board PCB trace delays in the following table when calculating max trace lengths.

Table 18. 40-Pin Expansion Header Related Carrier Board PCB Trace Delays

Module Interfaces	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Expansion Module (ps)
I2S	150	3600	3450
SPI	800	1760	960

Notes: Max Trace Delay Allowed for SPI assumes a single load case. If two loads are implemented, See the associated OEM Product Design Guide for details.

3.5 Serial Port

UART1 from the Jetson module is routed through level shifters to a 6-pin, 2.54mm pitch male Serial Port header (J17). The connector used on the carrier board is a Samtec HTSW-106-07-FM-S. The voltage levels at the connector are 3.3V.

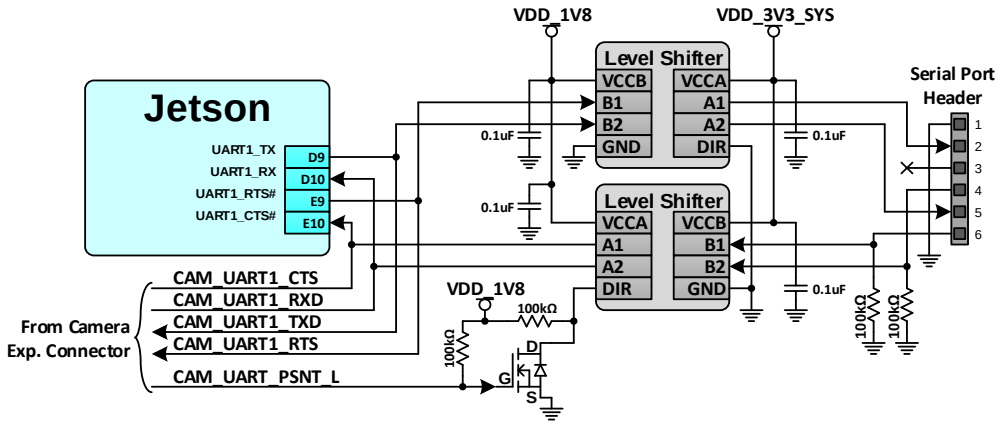
Table 19. Serial Port Header Descriptions

Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	–		Ground	Ground
2	UART1_RTS#	E9	UART #1 Request to Send	Output
3	–		Unused	Unused
4	UART1_RX	D10	UART #1 Receive	Input
5	UART1_TX	D9	UART #1 Transmit	Output
6	UART1_CTS#	E10	UART #1 Clear to Send	Input

Legend Ground | Power | Reserved

Notes: In the Type/Dir column, Output is to Serial Port header. Input is from Serial Port header. Bidir is for Bidirectional signals.

Figure 5. Serial Port Header Connections



3.6 Secondary Expansion Header

The carrier board includes a 30-pin (2x15, 2.54mm pitch) Secondary Expansion Header (J26) including an I2S IF and several GPIOs.

Table 20. Secondary Expansion Header Pin Descriptions

Hdr Pin #	Module Pin Name	Mod. Pin #	Tegra Pin Name	Default Usage/Desc.	Alternate Usage/Desc.	Type/ Direction (Default)	Voltage Level	GPIO (I_{OL}/I_{OH}) or Power Pin Current Cap.	Tegra GPIO Port #	Power on/ Pinmux Defaults	PU/PD on (module) & carrier board	Notes
1	CAN_WAKE	C20	CAN_GPIO4	GPIO	–	Input	3.3V	1mA / -1mA	AA.04	Z/PU	–	2
2	–	–	–	3.3V Supply	–	Power	–	2A	–	–	–	1
3	–	–	–	Unused	–	Unused	–	–	–	–	–	–
4	–	–	–	1.8V Supply	–	Power	–	2A	–	–	–	1
5	CAN0_RX	D18	CAN_GPIO4	CAN	–	Input	3.3V	1mA / -1mA	–	PU	–	2
6	GPIO15_AP2MDM_READY	A9	CAN_GPIO4	GPIO	–	Output	–	1mA / -1mA	BB.00	Drive 0	–	2
7	CAN0_TX	D19	CAN_GPIO4	CAN	–	Output	3.3V	1mA / -1mA	–	PU	–	2
8	–	–	–	5.0V Supply	–	Power	–	2A	–	–	–	1
9	CAN0_ERR	E18	CAN0_GPIO5	GPIO	–	Bidir	3.3V	1mA / -1mA	AA.05	Z	–	2
10	–	–	–	–	–	Ground	–	–	–	–	–	–
11	–	–	–	–	–	Ground	–	–	–	–	–	–
12	I2C_GP2_CLK	C11	GEN7_I2C_SCL	I2C	GPIO	Bidir-OD	1.8V	1mA / -1mA	L.00	Z	(1kΩ to 1.8V)	2
13	CAN1_STBY	C17	CAN0_GPIO6	GPIO	–	Output	3.3V	1mA / -1mA	AA.06	PD/Drive 0	–	2
14	I2C_GP2_DAT	C10	GEN7_I2C_SDA	I2C	GPIO	Bidir-OD	1.8V	1mA / -1mA	L.01	Z	(1kΩ to 1.8V)	2
15	CAN1_RX	D17	CAN0_DIN	CAN	–	Input	3.3V	1mA / -1mA	–	PU	–	2
16	WDT_TIME_OUT#	C9	GPIO_SEN7	WDT	GPIO	Output		1mA / -1mA	V.07	Drive 1	–	2
17	CAN1_TX	C18	CAN0_DOUT	CAN	–	Output	3.3V	1mA / -1mA	–	PU	–	2
18	I2C_GP3_CLK	C12	GEN9_I2C_SCL	I2C	GPIO	Bidir-OD	1.8V	1mA / -1mA	L.02	Z	(1kΩ to 1.8V)	2
19	CAN1_ERR	C19	CAN0_GPIO3	GPIO	–	Bidir	3.3V	1mA / -1mA	AA.03	Z	–	2
20	I2C_GP3_DAT	C13	GEN9_I2C_SDA	I2C	GPIO	Bidir-OD	1.8V	1mA / -1mA	L.03	Z	(1kΩ to 1.8V)	2

Hdr Pin #	Module Pin Name	Mod. Pin #	Tegra Pin Name	Default Usage/Desc.	Alternate Usage/Desc.	Type/ Direction (Default)	Voltage Level	GPIO (I_{OL}/I_{OH}) or Power Pin Current Cap.	Tegra GPIO Port #	Power on/ Pinmux Defaults	PU/PD on (module) & carrier board	Notes
21	–	–	–	–	–	Ground	–	–	–	–	–	–
22	SLEEP#	E2	GPIO_SW2	GPIO	–	Input	1.8V	1mA / -1mA	FF.02	PU	–	2,5
23	I2S1_CLK	C15	DAP2_SCLK	I2S	–	Output	1.8V	1mA / -1mA	–	PD	–	2
24	I2S1_SDOUT	D14	DAP2_DOUT	I2S	–	Output	1.8V	1mA / -1mA	–	PD	–	2
25	I2S1_SDIN	C14	DAP2_DIN	I2S	–	Input	1.8V	1mA / -1mA	–	PD/PU	–	2
26	I2S1_LRCLK	D13	DAP2_FS	I2S	–	Output	1.8V	1mA / -1mA	–	PD	–	2
27	DSPK_OUT_CLK	G4	GPIO_AUD3	DSPK	GPIO	Output	1.8V	1mA	K.00	PU	–	2
28	–	–	–	–	–	Ground	–	–	–	–	–	–
29	DSPK_OUT_DAT	H4	GPIO_AUD2	DSPK	GPIO	Output	1.8V	1mA	J.07	PD	–	2
30	Reserved	–	–	–	–	–	–	–	–	–	–	–

Legend Ground | Power | Reserved/Not Available

Notes:
1. This is current capability per power pin.
2. These pins are directly connected to Tegra. The max drive that meets full Data Sheet V_{OL}/V_{OH} is 1mA. 2mA drive is supported at restricted V_{OL}/V_{OH} levels. See the associated OEM Product Design Guide Pads section for details.
3. In the Type/Dir column, Output is to Exp. Module. Input is from Exp. Module. Bidir is for Bidirectional signals.
4. PD = Tegra Internal Pull-down, PU - Tegra Internal Pull-up, Z – Tristate.
5. This pin is used for RAM Code strapping on the module and may be pulled up or down with 4.7kΩ resistors. Care must be taken to make sure this signal is not pulled or driven up/down by any device connected to these pins during initial power-on.

Secondary Expansion Header Interface Guidelines

See the Jetson TX2 Series OEM Product DG for Routing Guidelines. Include the worst-case carrier board PCB trace delays for I2S and CAN[1:0] in the following table when calculating max trace length & for skew matching.

Table 21. Secondary Expansion Header Related Carrier Board PCB Trace Delays

Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Avail. Trace Delay for GPIO Module (ps)
I2S1	920	3600	2680
CAN[1:0]	890	1360	470

3.7 Charge Control Receptacle

The Jetson carrier board includes a 10-pin, 0.8mm pitch flex receptacle (J27) including an I2C IF & charge control/status signals.

Table 22. Charge Control Receptacle Pin Descriptions

Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level (V)
1	CHARGER_PRSNT#	A49	Charger Present / AC power OK	Input	5.0
2	CHARGING#	A7	Charging indicator	Input	1.8
3	BATLOW#	C7	Low Battery indicator	Input	1.8
4	–	–	Ground	Ground	–
5	I2C_PM_CLK	A6	I2C (Power Monitor) Clock	Bidir/OD	1.8
6	I2C_PM_DAT	B6	I2C (Power Monitor) Data	Bidir/OD	1.8
7	RSVD (C8)	C8	SOC THERM on Tegra. BATT_OC on PMIC	Input	1.8
8	–	–	Battery Detect – Pulled up to VDD_3V3_SYS	Na	3.3
9	(1.8V GPIO Exp. P0)	–	Type C Interrupt from 1.8V GPIO Exp. P0	Output	1.8
10	(1.8V GPIO Exp. P14)	–	Charge Present from 1.8V GPIO Exp. P14	Output	1.8

Legend Ground | Power | Reserved

Notes: - In the Type/Dir column, Output is to Charger Ctrl board. Input is from Charger Ctrl board. Bidir is for Bidirectional signals.

- When a Jetson TX2/TX2 4GB module is used in a P2597_B02/B04 carrier board, the Auto-Power-On option can be enabled by tying the CHARGER_PRSNT# pin to GND. This can be accomplished by installing a 0Ω resistor at R313. This will allow the Developer Kit carrier board to power on immediately after the main power is connected (without the need for a power button press). This will not work with the P2597_C02 carrier board or with Jetson TX2i modules. See Appendix: P2597_C02 Auto-Power-On Rework for instructions for modifying P2597_C02 boards to support Auto-Power-On.

3.8 Fan Connector

The Jetson carrier board includes a 4-pin Fan Header (J15).

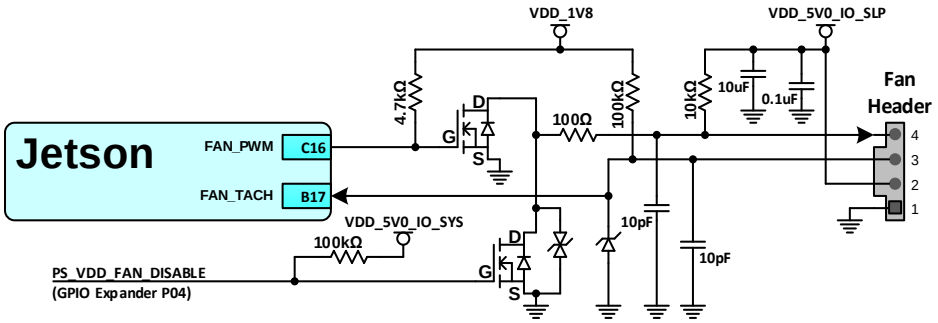


Table 23. Fan Connector Pin Descriptions

Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir	Voltage Level (V)
1	–	–	Ground	Ground	
2	–	–	Gated version of Main 5.0V Supply (Enabled by VDD_3V3_SLP)	Power	
3	FAN_TACH	B17	Fan Tachometer signal	Input	1.8
4	FAN_PWM	C16	Fan Pulse Width Modulation signal	Output	1.8

Legend Ground | Power | Reserved

Notes: In the Type/Dir column, Output is to Fan Connector. Input is from Fan Connector. Bidir is for Bidirectional signals.

3.9 DC Power Jack

The Jetson carrier board uses a DC power jack (J25) to bring in the power from the included DC power supply. The jack used on the Carrier board is a Singatron Enterprise 2DC-213-B51. The mating plug is the Singatron Enterprise 2DP-313-B01.

Table 24. DC Jack Pin Descriptions

Conn. Pin #	Module Pin Name	Module Pin #	Usage/Description	Type/Dir
1	–	A1, A2, B1, B2, C1, C2	Main DC input supplying VDD_IN/VDD_MOD	Power
2	–	–	Ground	Ground
3	–	–	Ground	Ground
4	–	–	Ground	Ground
5	–	–	Ground	Ground
6	–	–	Ground	Ground

4.0 MISCELLANEOUS

4.1 GPIO Expanders

The carrier board design includes two I2C interface controlled GPIO expander ICs. One operates at 1.8V and the other at 3.3V. The GPIO pins on the expanders are either used to interface to onboard devices/supplies or are routed to several of the expansion connectors. The connections are shown in the figures & tables below. The I2C address for the 1.8V GPIO Expander is strapped to be 7'h77, while the address for the 3.3V GPIO expander is strapped to 7'h74.

Figure 6. GPIO Expander (1.8V)

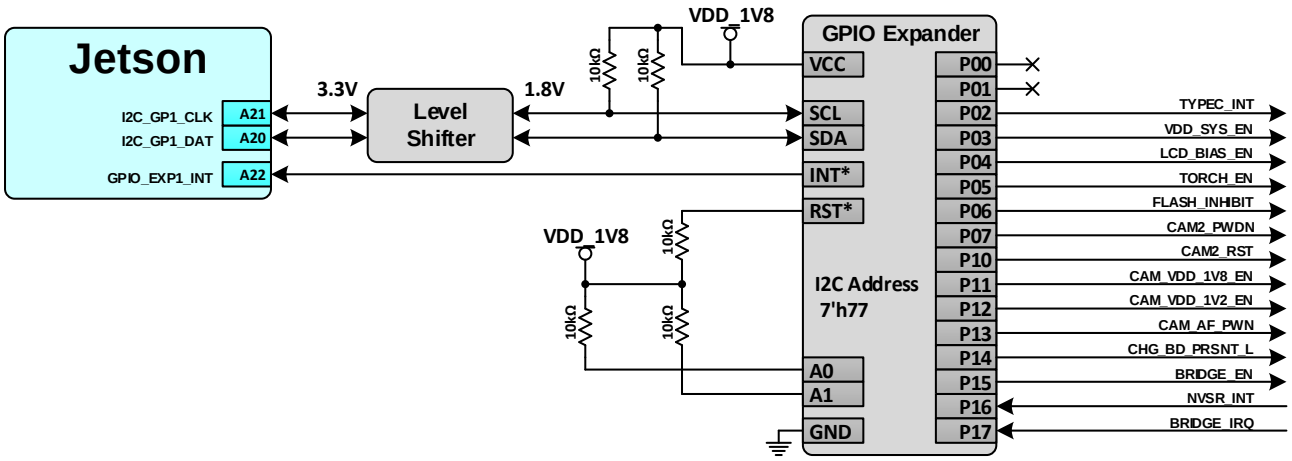


Table 25. 1.8V GPIO Expansion Signal Descriptions

Expander GPIO #	Carrier Board Signal Name	Usage/Description	Direction
P00	No connect	Not available for use	NA
P01	No connect	Not available for use	NA
P02	TYPEC_INT	Type C Interrupt – to pin 9 of Charger Control header (J27)	Output
P03	VDD_SYS_EN	VDD_SYS enable - to pin 119 of Camera Expansion connector (J22)	Output
P04	LCD_BIAS_EN	LCD Bias Enable - to pin 88 of Display Expansion connector (J23)	Output
P05	TORCH_EN	Torch Enable - to pin 104 of Camera Expansion connector (J22)	Output
P06	FLASH_INHIBIT	Flash inhibit - to pin 103 of Camera Expansion connector (J22)	Output
P07	CAM2_PWDN	Camera #2 Power-down - to pin 96 of Camera Expansion connector (J22)	Output
P10	CAM2_RST	Camera #2 Reset - to pin 98 of Camera Expansion connector (J22)	Output
P11	CAM_VDD_1V8_EN	Camera 1.8V supply enable – to ON pin of load switch supplying DVDD_CAM_IO_1V8 to Camera Expansion connector (J22) on carrier board.	Output
P12	CAM_VDD_1V2_EN	Camera 1.2V supply enable – to chip enable of 1.2V LDO supplying DVDD_CAM_IO_1V2 to Camera Expansion connector (J22) on carrier board.	Output
P13	CAM_AF_PWDN	Camera Autofocus Power-down - to pin 85 of Camera Expansion connector (J22)	Output
P14	CHG_BD_PRSNT_L	Type C Interrupt – to pin 10 of Charger Control header (J27)	Output
P15	BRIDGE_EN	Bridge Enable - to pin 18 of Display Expansion connector (J23)	Output
P16	NVSR_INT	Nvidia Sensor Interrupt - to pin 98 of Display Expansion connector (J23)	Input
P17	BRIDGE_IRQ	Bridge Interrupt - to pin 20 of Display Expansion connector (J23)	Input

Notes: In the Direction column, Output is from GPIO expander. Input is to GPIO expander. Bidir is for Bidirectional signals.

Figure 7. GPIO Expander (3.3V)

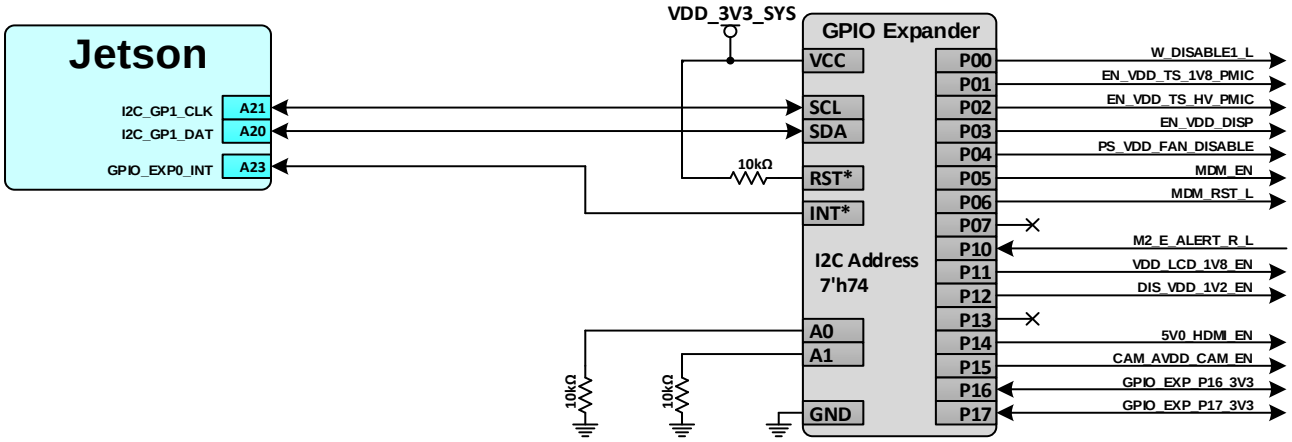


Table 26. 3.3V GPIO Expansion Signal Descriptions

Expander GPIO #	Carrier Board Signal Name	Usage/Description	Direction
P00	W_DISABLE1_L	WLAN Disable 1 - to pin 56 of M.2 Key E connector (J18)	Output
P01	EN_VDD_TS_1V8_PMIC	Touchscreen 1.8V supply enable – to ON pin of 1.8V load switch supplying VDD_TS_1V8 to Display Expansion connector (J23) on carrier board.	Output
P02	EN_VDD_TS_HV_PMIC	Touchscreen 3.3V supply enable – to ON pin of 3.3V load switch supplying AVDD_TS_DIS to Display Expansion connector (J23) on carrier board.	Output
P03	EN_VDD_DISP	Display 3.3V supply enable – to ON pin of load switch supplying VDD_DIS_3V3_LCD to Display Expansion connector (J23) on carrier board.	Output
P04	PS_VDD_FAN_DISABLE	Fan disable – Enables/Disables PWM going to fan header (J15)	Output
P05	MDM_EN	Modem Enable – Not assigned (goes to unstuffed R526)	Output
P06	MDM_RST_L	Modem Reset – Not assigned (goes to unstuffed R527)	Output
P07	No connect	Not available for use	NA
P10	M2_E_ALERT_R_L	M2 Key E alert – from pin 62 of M.2 connector (J18)	Input
P11	VDD_LCD_1V8_EN	LCD 1.8V supply enable – to ON pin of load switch supplying VDD_LCD_1V8_DIS to Display Expansion connector (J23) on carrier board.	Output
P12	DIS_VDD_1V2_EN	LCD 1.2V supply enable – to chip enable of LDO supplying VDD_1V2 to Display Expansion connector (J23) on carrier board.	Output
P13	5V0_HDMI_EN	HDMI 5V Enable – to enable of load switch supplying VDD_5V0_HDMI_CON on carrier board.	Output
P14	No connect	Not available for use	NA
P15	CAM_AVDD_CAM_EN	Camera analog supply enable – to enable of 2.8V LDO supplying AVDD_CAM to Camera Expansion connector (J22) on carrier board.	Output
P16	GPIO_EXP_P16_3V3	GPIO expander P16 – connects to Expansion Header (J21) pin 22.	Bidir
P17	GPIO_EXP_P17_3V3	GPIO expander P17 – connects to Expansion Header (J21) pin 15.	Bidir

Notes: In the Direction column, Output is from GPIO expander. Input is to GPIO expander. Bidir is for Bidirectional signals.

4.2 Buttons, Jumpers & Indicators

Table 27. Buttons (switches)

Button	Description	Usage
S1	Reset button	Used to force a full system reset.
S2	Volume down (Sleep) button	Used to put system into sleep mode.
S3	Recovery button	Used to enter Force Recovery Mode. Button is held down while either system is first powered on, or by pressing & releasing reset button while Recovery button is pressed.
S4	Power button	Used to power system up if off, or power down if on. If held for >10 seconds, will force a full system power cycle.

Table 28. Jumpers

Jumper	Description	Usage
J4	Power LED header	Available to connect to remote Power LED
J8	Reset out Header	Used to hold Tegra in reset
J24	Voltage select header	Selects the level shifter voltage on the non-Jetson module side of the level shifters for the signals listed below. When a jumper is on pins 1-2, 3.3V level is selected. When on pins 2-3, 1.8V level is selected. - AUDIO_I2S_MCLK/SFSYNC/SOUT/SIN/SRCLK, AUDIO_CDC_IRQ, AUD_RST - MDM_WAKE_AP_1V8 - SPI1_MOSI/MISO/SCK/CS0/CS1 - AP_WAKE_BT AO_DMIC_IN_CLK/DAT
P2597 B02/B04 Only		
J3	Reset switch header	Available if a remote reset button is required.
J6	Power switch header	Available if a remote power button is required.
J9	Force recovery header	Available if a remote force recovery button is required.
J11	Force off header	Can be jumpered to force system to off state. Also available if a remote button is required to force system off.
P2597 C02 Only		
J20	Combined Power Switch, Force off, Force recovery & Reset switch header	Available to support remote reset, power & force recovery & force off activation.

Table 29. Automation Header Pin Descriptions (P2597 C02 only)

Pin #	Carrier Board Net Name	Jetson Module Pin Name	Usage
Power Button Header			Available if a remote power button is required.
1	GND	–	Ground
2	POWER_BTN_R	POWER_BTN#	
Force Power Off Button Header			Available if a remote button is required to force system off.
3	GND	–	Ground
4	D_FORCE_OFF_L	–	
Force Recovery Button Header			Available if a remote force recovery button is required.
5	GND	–	Ground
6	FORCE_RECOVERY_R_L	FORCE_RECOV#	
Reset Button Header			Available if a remote reset button is required. Connect normally open button or equivalent across the signal & GND.
7	GND	–	Ground
8	RESET_IN_R_L	RESET_IN#	
Additional Grounds			
9	GND	–	Ground
10	GND	–	Ground

Table 30. Indicators (LEDs)

LEDs	Description	Usage
CR1	SOC Enable LED (Green)	Indicates when the VDD_CORE (SOC) supply is active.
CR2	Power LED (Green)	Indicates when the carrier board is powered on (VDD_1V8 & VDD_3V3_SYS rails are valid).
CR3	M.2 LED #2 (Green)	Indicates when the M.2 Key E LED2# is active.
CR4	M.2 LED #1 (Green)	Indicates when the M.2 Key E LED1# is active.
CR5	VDD_IN LED (Red – not available on P2597 B02)	Indicates when main supply is active and connected to the carrier board.
CR6	PCIe/SATA 12V LED #2 (Red– not available on P2597 B02)	Indicates when the 12V supply for PCIe/SATA is active.

4.3 Power Monitors

There are two Power monitors on the Jetson carrier board. One monitors the main DC input (VDD_MUX), the main 5V IO supply (VDD_5V0_IO_SYS) and the main 3.3V system supply (VDD_3V3_SYS). The other monitors the 3.3V Run Supply (VDD_3V3_SLP), the main 1.8V system supply (VDD_1V8) and the M.2 3.3V supply (VDD_3V3_SYS_M2). The I2C interface used for both monitors is I2C_GP1. The I2C address for the first power monitor is 7'h42 and for the second power monitor is 7'h43.

Figure 8. Power Monitor (VDD_MUX, VDD_5V0_IO_SYS, VDD_3V3_SYS)

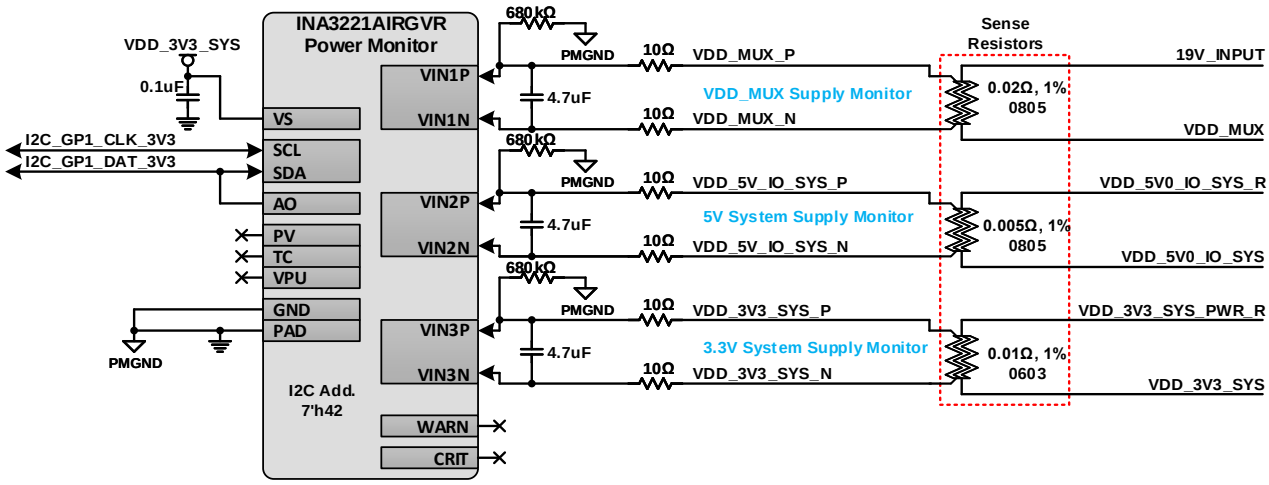
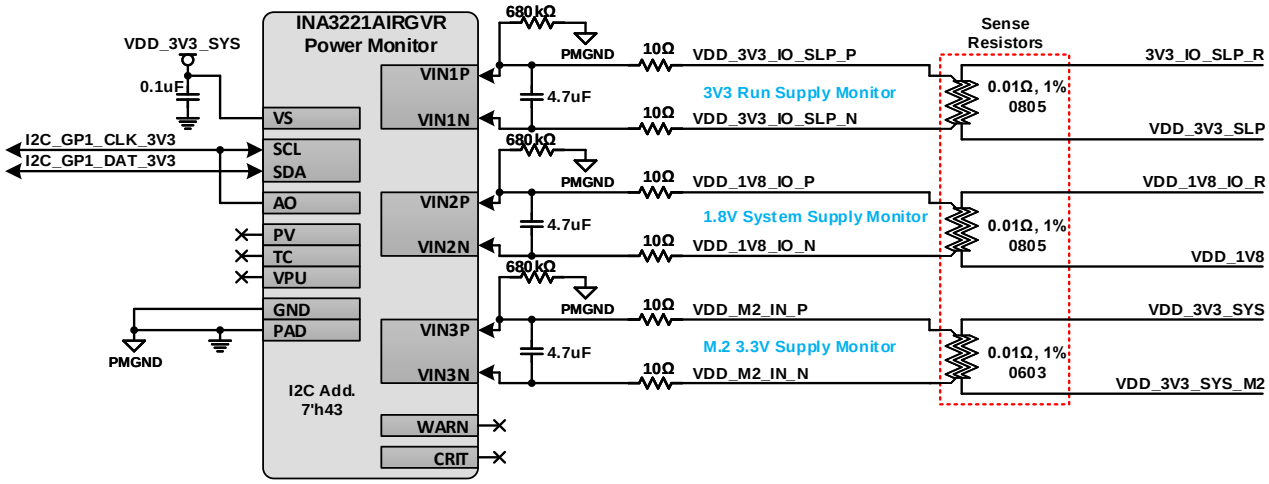
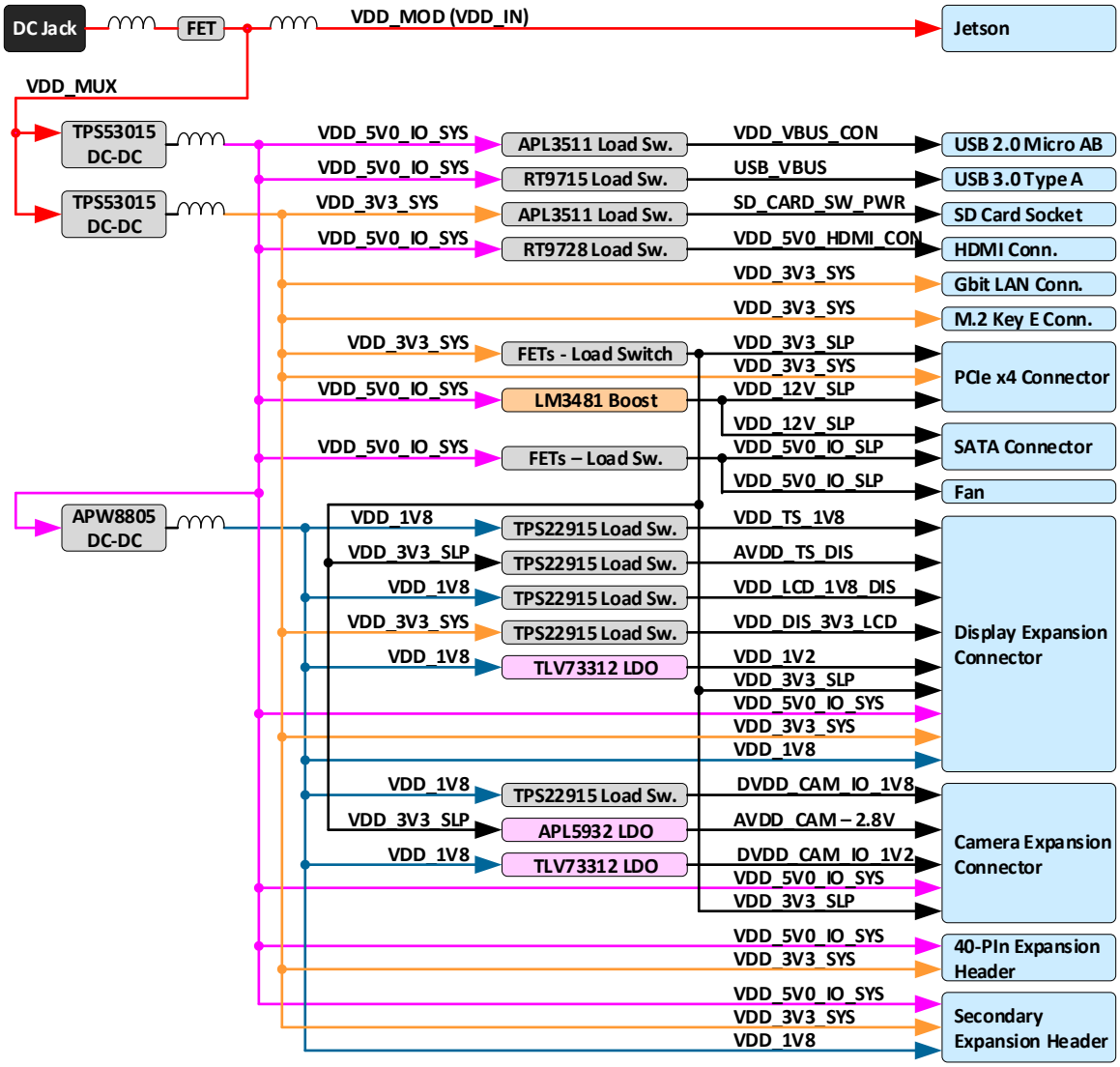


Figure 9. Power Monitor (VDD_3V3_SLP, VDD_1V8, VDD_3V3_SYS_M2)



5.0 INTERFACE POWER

Figure 10. Interface Connector Power Diagram



The tables below show the allocation of supplies to the connectors on the Jetson carrier board and current capabilities.

Table 31 Interface Power Supply Allocation

Power Rails	Usage	(V)	Power Supply/Gate	Source	Enable
VDD_IN/VDD_MUX	Main power input from DC Adapter	TX2: 5.5-19.6 TX2 4G/TX2i: 9.0-19.6	FETs	**DC Adapter**	
VDD_5V0_IO_SYS	Main 5V supply	5.0	TPS53015	**VDD_MUX**	CARRIER_PWR_ON
VDD_3V3_SYS	Main 3.3V supply	3.3	TPS53015	**VDD_MUX**	3V3_SYS_BUCK_EN
VDD_1V8	Main 1.8V supply	1.8	APW8805	**VDD_5V0_IO_SYS**	1V8_IO_VREG_EN (VDD_3V3_SYS_PG)
VDD_3V3_SLP	3.3V rail, off in Sleep (various)	3.3	FETs	**VDD_3V3_SYS**	SOC_PWR_REQ
VDD_5V0_IO_SLP	5V rail, off in Sleep (SATA/FAN)	5.0	FETs	**VDD_5V0_IO_SYS**	SOC_PWR_REQ
VDD_12V_SLP	12V rail, off in Sleep (PCIe® x4 & SATA)	12.0	LM3481MMX Boost	**VDD_5V0_IO_SYS**	VDD_3V3_SLP
VDD_VBUS_CON	5V VBUS for USB 2.0 Type AB conn.	5.0	APL3511CBI Load SW	**VDD_5V0_IO_SYS**	USB_VBUS_EN0
USB_VBUS	5V VBUS for USB 3.0 Type A conn.	5.0	RT9715 Load SW	**VDD_5V0_IO_SYS**	USB_VBUS_EN1
SD_CARD_SW_PWR	SD Card power rail	3.3	APL3511DBI Load SW	**VDD_3V3_SYS**	SDCARD_VDD_EN
VDD_5V0_HDMI_CON	5V rail for HDMI connector		RT9728 Load SW	**VDD_5V0_IO_SYS**	5V0_HDMI_EN (GPIO Expander U32, P14)
VDD_TS_1V8	1.8V rail for touch screen		TPS22915 Load SW	**VDD_1V8**	EN_VDD_TS_1V8_PMIC (GPIO Expander U32, P01)
AVDD_TS_DIS	High voltage rail for touch screen	3.3	TPS22915 Load SW	**VDD_3V3_SLP**	EN_VDD_TS_HV_PMIC (GPIO Expander U32, P02)
VDD_LCD_1V8_DIS	1.8V rail for panel		TPS22915 Load SW	**VDD_1V8**	VDD_LCD_1V8_EN (GPIO Expander U32, P11)
VDD_DIS_3V3_LCD	High voltage rail for panel		TPS22915 Load SW	**VDD_3V3_SYS**	EN_VDD_DISP (GPIO Expander U32, P03)
VDD_1V2	Generic 1.2V display rail	1.2	TLV73312 LDO	**VDD_1V8**	DIS_VDD_1V2_EN (GPIO Expander U32, P12)
VDD_SYS_BL	Rail to LCD backlight driver	Device Dep.	Stuffing option Resistors	**VDD_MUX** **VDD_5V0_IO_SYS**	Na
DVDD_CAM_IO_1V8	1.8V rail for camera I/O	1.8	TPS22915 Load SW	**VDD_1V8**	CAM_VDD_1V8_EN (GPIO Expander U31, P11)
AVDD_CAM	High voltage rail for cameras	2.8	APL5932	**VDD_3V3_SLP**	CAM_AVDD_CAM_EN (GPIO Expander U32, P15)
DVDD_CAM_IO_1V2	1.2V rail for camera I/O	1.2	TLV73312	**VDD_1V8**	CAM_VDD_1V2_EN (GPIO Expander U31, P12)

Table 32 Interface Supply Current Capabilities

Power Rails	Usage	(V)	Max Current (mA)
VDD_IN/VDD_MUX	Main power input from DC Adapter	TX2: 5.5-19.6 TX2 4GB/TX2i: 9.0-19.6	~4000
VDD_5V0_IO_SYS	Main 5V supply	5.0	7000
VDD_3V3_SYS	Main 3.3V supply	3.3	7000
VDD_1V8	Main 1.8V supply	1.8	2000
VDD_12V_SLP	12V rail for PCIe x4 & SATA	12.0	2300
DVDD_CAM_IO_1V8	1.8V rail for camera I/O	1.8	1000
AVDD_CAM	High voltage rail for cameras	2.8	1000
DVDD_CAM_IO_1V2	1.2V rail for camera I/O	1.2	200

Notes:
1. When operated near the minimum voltage (TX2 only), the power supported by some supplies may be reduced.
2. The supplied power adapter is rated to 90W.
3. The values shown in the “Supported Current” column indicate the total power available on the expansion connectors (not per pin).
4. If a given voltage rail cannot provide enough current, a possible solution is for the user to use a regulator from VDD_5V0_IO_SYS, VDD_3V3_SYS or VDD_1V8 to generate the desired rail.

6.0 APPENDIX: P2597_C02 AUTO-POWER-ON REWORK

The Jetson TX2 Developer Kit carrier board P2597_C02, implemented features that made it incompatible with the Auto-Power-On options for the Jetson TX2 Series modules. Circuitry was added to determine whether a Jetson TX2 (or TX2 4GB) or Jetson TX2i is installed, and to route the signals correctly to power on when the power button is pressed. Also, a protection circuit was added to keep the socket unpowered until the power button is pressed. This was to protect against damage to the module or carrier board if the module was installed or removed when the power source was already connected. Both these circuits kept the mechanisms for supporting Auto-Power-On from working.

Rework can be performed to allow the Jetson TX2 carrier board P2597_C02 to support Auto-Power-On. The rework disables the hot-plug protection and forces the carrier board to "see" a Jetson TX2i module as a Jetson TX2 module. This will allow the Auto-Power-On to work the same as it does on the P2597_B04 carrier board with any of the Jetson TX2 Series modules. The rework is listed below:

1. Install 0 Ohm, 0402 resistor at R313
   Asserts ACOK to allow Jetson TX2 or Jetson TX2 4GB to Auto-Power-On.
2. Move R501, 10k, 0402, resistor to R287
   Enables the VDD_IN supply to the module connector as soon as the power is applied (disables hot-plug protection)
3. Remove R383
   Disables the ON control from the pushbutton Micro-Controller
4. Remove R384
   Removes the VDD_IN Bleeder resistor to keep this from consuming power during normal operation.
5. Add wire across Q47 pin 2 and 3.
   Force Button Micro-Controller in Mobile PMIC Mode (allows Jetson TX2i to function as if it were in a P2597_B04 carrier board – will boot when power is attached without button press)

Figure 11. P2597_C02 Auto-Power-On Support Top Side Rework

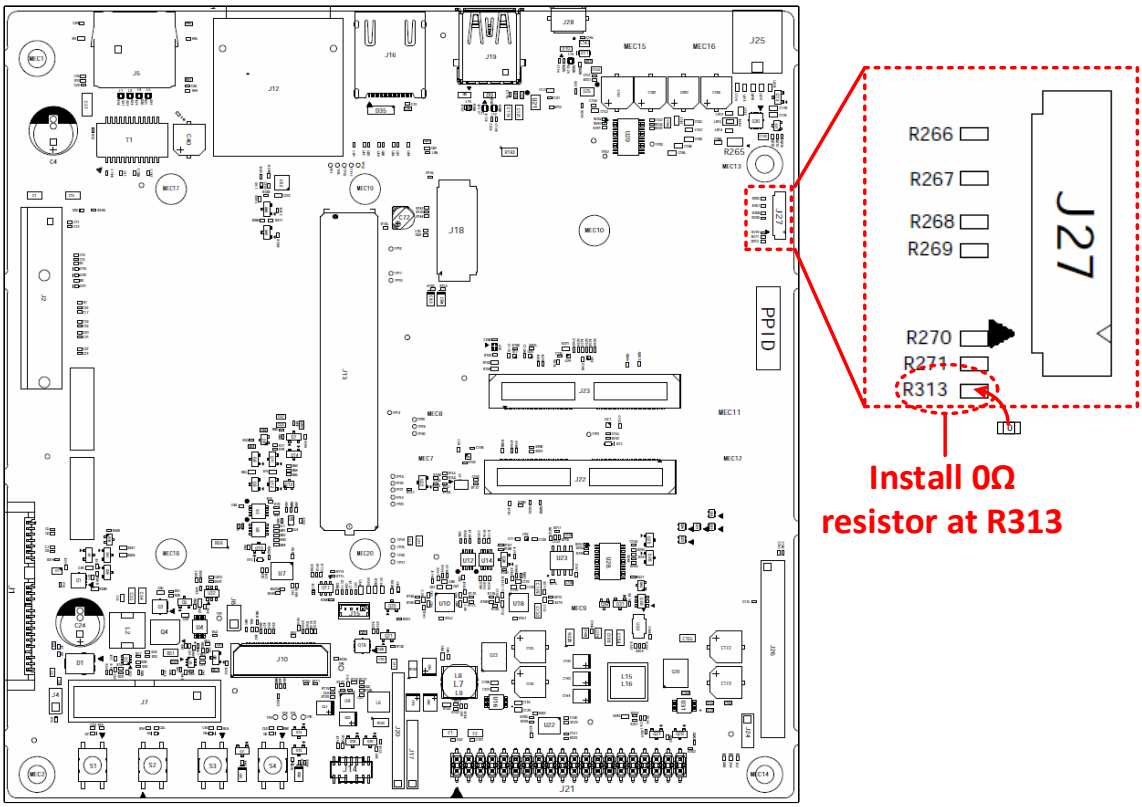
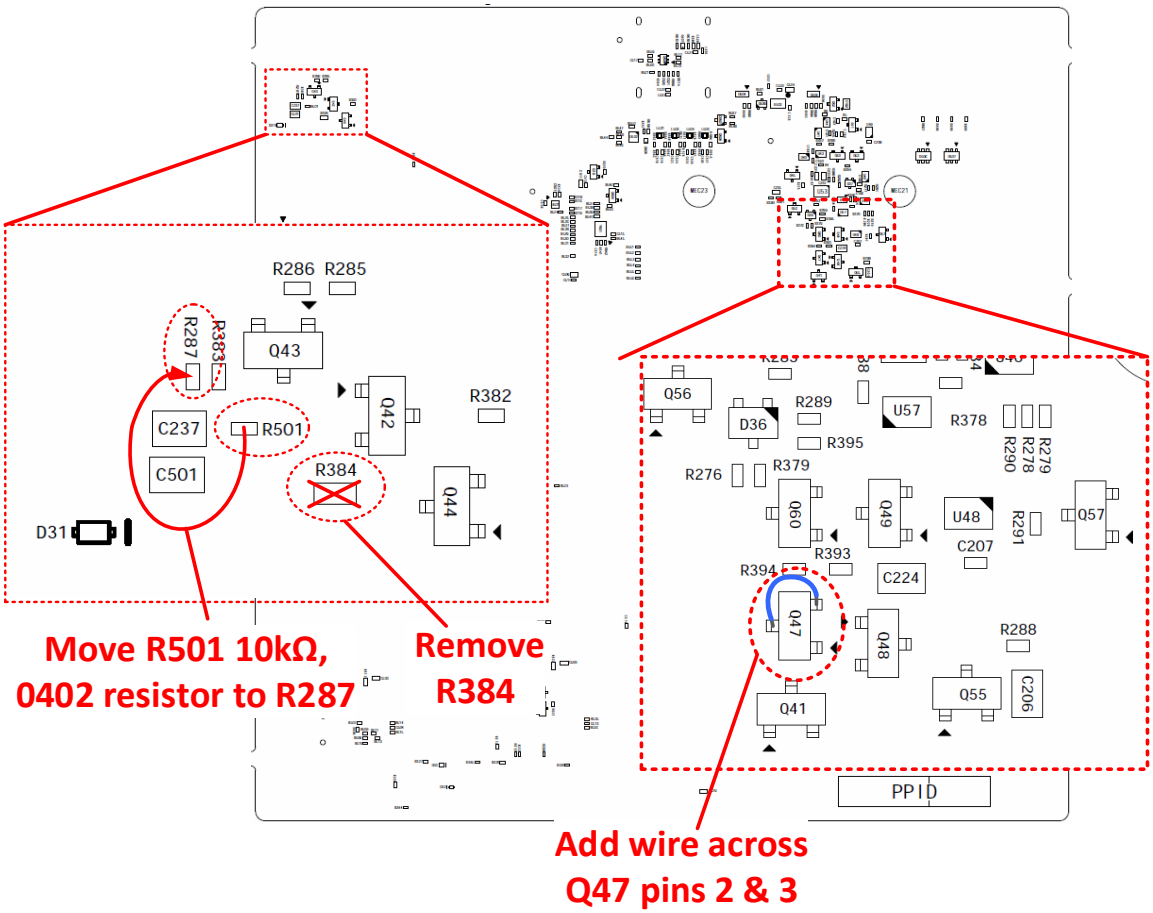


Figure 12. P2597_C02 Auto-Power-On Support Bottom Side Rework



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