```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
ENTITY dec2to4 IS
        PORT ( w        : IN    STD_LOGIC_VECTOR(1 DOWNTO 0) ;
                En      : IN    STD_LOGIC ;
                y       : OUT   STD_LOGIC_VECTOR(0 TO 3) ) ;
END dec2to4 ;

ARCHITECTURE Behavior OF dec2to4 IS
        SIGNAL Enw : STD_LOGIC_VECTOR(2 DOWNTO 0) ;
BEGIN
        Enw <= En & w ;
        WITH Enw SELECT
                y <=    "1000" WHEN "100",
                        "0100" WHEN "101",
                        "0010" WHEN "110",
                        "0001" WHEN "111",
                        "0000" WHEN OTHERS ;
END Behavior ;
```

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
ENTITY dec2to4Equations IS
        PORT ( w        : IN    STD_LOGIC_VECTOR(1 DOWNTO 0) ;
                En      : IN    STD_LOGIC ;
                y       : OUT   STD_LOGIC_VECTOR(0 TO 3) ) ;
END dec2to4Equations ;

ARCHITECTURE Behavior OF dec2to4Equations IS
        SIGNAL Enw : STD_LOGIC_VECTOR(2 DOWNTO 0) ;
BEGIN
        y(0) <= En AND NOT w(1) AND NOT w(0);
        y(1) <= En AND NOT w(1) AND     w(0);
        y(2) <= En AND      w(1) AND NOT w(0);
        y(3) <= En AND     w(1) AND      w(0);

END Behavior ;
```

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
ENTITY dec2to4When IS
        PORT ( w        : IN    STD_LOGIC_VECTOR(1 DOWNTO 0) ;
                En      : IN    STD_LOGIC ;
                y       : OUT   STD_LOGIC_VECTOR(0 TO 3) ) ;
END dec2to4When ;

ARCHITECTURE Behavior OF dec2to4When IS
        BEGIN
                y <=    "1000" WHEN En = '1' AND W="00" ELSE
                        "0100" WHEN En = '1' AND W="01" ELSE
                        "0010" WHEN En = '1' AND W="10" ELSE
                        "0001" WHEN En = '1' AND W="11" ELSE
                        "0000";
END Behavior ;
```