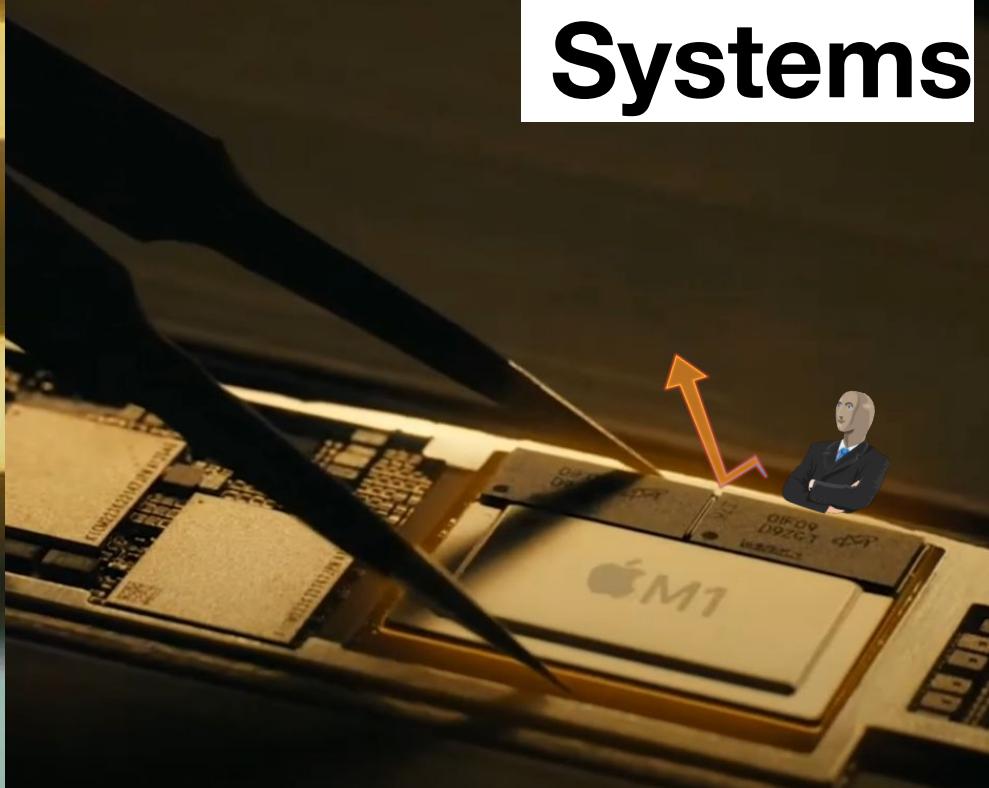


# Mobile & Embedded Systems

Lecture 17  
SoC, boot, systemd



# Fun Times Last Halloween

TheVerge / Tech / Reviews / Science / Entertainment / More +

TRANSPO / AUTONOMOUS CARS / TECH

## George Hotz, iPhone hacker and Elon Musk antagonist, is leaving Comma AI



Hotz founded the driver-assist technology company as an attempt to make a product that was better than Tesla's Autopilot. But he said he doesn't feel capable of running the company anymore.

By ANDREW J. HAWKINS / @andyjayhawk  
Oct 31, 2022, 12:44 PM CDT | □ 0 Comments / 1 New

Photo by Michael Zelenko / The Verge

Note: George predicted that Tesla would go E2E too, and they did

# More Recent Fun Times

The screenshot shows a news article from Electrek. At the top left is the Electrek logo with a dropdown menu and a search bar. Below the header, the main title reads "Let's talk about Elon Musk's potato livestream of Tesla FSD v12". Underneath the title is a timestamp and comment count: "Fred Lambert | Aug 28 2023 - 6:38 am PT | 330 Comments". The main content area features a video thumbnail showing a view from inside a Tesla car driving on a road. The car's infotainment screen displays the navigation map and driving information. Below the video thumbnail is a caption: "Elon Musk finally did his promised livestream of a drive on Tesla's Full Self-Driving (FSD) Beta v12. Here's the video and my impressions." At the bottom of the article, there is a note: "After three years of FSD being in beta, Tesla CEO Elon Musk says that Tesla's Full Self-Driving package is about to get out of beta with the version 12 update."

"The main problem was the quality of the video, both the filming – which wasn't ideal to get a look at the performance of the update – and the actual video quality of the streaming, which looked like it was filmed in a potato phone from the 2000s."

"Another problem is that Musk appears to be operating the phone by hand in the driver's seat, which is both a driving violation and against Tesla's own driver manual."

"A much bigger problem was at about 19:58 when Musk had to disengage the system as the car tried to drive on a red light after detecting a green light that was for another lane."

Elon Musk's post on X:  
<https://x.com/elonmusk/status/1695247110030119054?s=20>

# Today

 ARS TECHNICA [SUBSCRIBE](#) [SIGN IN](#)

TAXIS OUT OF SERVICE —

## California suspends Cruise robotaxis after car dragged pedestrian 20 feet

Horrifying hit-and-run triggers California suspension of Cruise robotaxis.

ASHLEY BELANGER · 10/25/2023, 9:34 AM



[Enlarge](#)

Less than three months after the California Public Utilities Commission [approved robotaxi-service Cruise's plan to provide around-the-clock driverless rides](#) to passengers in San Francisco, the California Department of Motor Vehicles (DMV) has shut down Cruise's driverless operations in the state.

Yesterday, the California DMV suspended Cruise's permits for autonomous vehicle deployment and driverless testing "effective immediately" over pedestrian safety concerns.

"Less than three months after the California Public Utilities Commission approved robotaxi-service Cruise's plan to provide around-the-clock driverless rides to passengers in San Francisco, the California Department of Motor Vehicles (DMV) has shut down Cruise's driverless operations in the state."

"According to Cruise, its autonomous vehicle (AV) detected the collision and stopped on top of the pedestrian, then veered off the road, dragging the pedestrian about 20 feet."

Picture taken  
in Midtown by  
Joe's toaster:



# Today

**ars TECHNICA** [SUBSCRIBE](#)

WHOOPS —

## Valve begins reversing CS2 bans caused by AMD's "Anti-Lag+" driver

Overzealous DLL alterations have been suspended in a subsequent driver update.

KYLE ORLAND - 10/23/2023, 10:10 AM



[Enlarge](#) / The red eyes represent the mark of VAC for Anti-Lag+ players.

Valve has announced that it will begin reversing bans incurred by *Counter-Strike 2* players that used an AMD "Anti-Lag+" driver, which started setting off the Valve Anti-Cheat (VAC) system earlier this month.

AMD took down version 23.10.1 of its AMD Adrenalin Edition graphics driver shortly after its October 11 launch, following reports that Valve was banning *Counter-Strike 2* players that used the driver's Anti-Lag+ Technology.

"Valve has announced that it will begin reversing bans incurred by *Counter-Strike 2* players that used an AMD "Anti-Lag+" driver, which started setting off the Valve Anti-Cheat (VAC) system earlier this month."

 **CS2** @CounterStrike

AMD's latest driver has made their "Anti-Lag/+" feature available for CS2, which is implemented by detouring engine dll functions.

If you are an AMD customer and play CS2, DO NOT ENABLE ANTI-LAG/+; any tampering with CS code will result in a VAC ban.

Once AMD ships an update we can do the work of identifying affected users and reversing their ban. [@AMD](#)

11:59 AM · Oct 13, 2023 · 3.9M Views

---

1,652 Reposts 560 Quotes 19.6K Likes 704 Bookmarks

Screenshot of post on X from user @CounterStrike. URL:  
<https://twitter.com/CounterStrike/status/1712875606776729832>

# Housekeeping

- **Project 2 to be posted soon**
  - gpiod - welcome to the driver side

# Questions Will Be Answered & Answers Will Be Questioned

- gpio addressing -

<https://www.kernel.org/doc/Documentation/devicetree/bindings/gpio/gpio-o-map.txt>

# Extra Note On Device Tree & GPIO: BeagleBone Black

```
gpio@4804c000 {  
    compatible = "ti,omap4-gpio",  
    ...  
    ti,hwmods = "gpio2";  
    gpio-controller;  
    #interrupt-cells = < 0x02 >;  
    interrupts = < 0x62 >;  
    phandle = < 0x58 >;  
    reg = < 0x4804c000 0x1000 >;  
    #gpio-cells = < 0x02 >;  
    interrupt-controller;  
};
```

Why is this gpio2 and not 1?

Table 2-3. L4\_PER Peripheral Mem

Device Name	Start_address (hex)	End_address (hex)
DMTIMER5	0x4804_6000	0x4804_6FFF
	0x4804_7000	0x4804_7FFF
DMTIMER6	0x4804_8000	0x4804_8FFF
	0x4804_9000	0x4804_9FFF
DMTIMER7	0x4804_A000	0x4804_AFFF
	0x4804_B000	0x4804_BFFF
GPIO1	0x4804_C000	0x4804_CFFF
	0x4804_D000	0x4804_DFFF

Table screenshot from page 182 of:

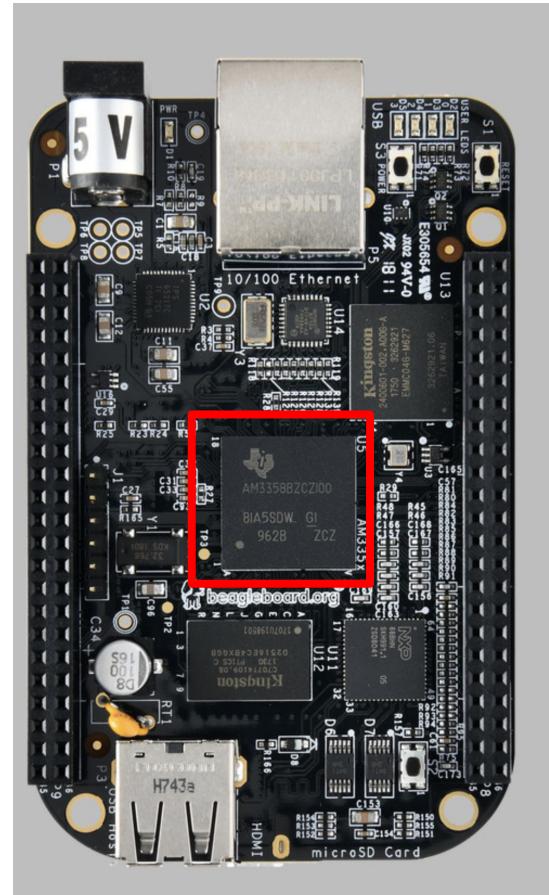
AM335x and AMIC110 Sitara™ Processors Technical Reference Manual from TI. URL:  
[https://www.ti.com/lit/ug/spruh73g/spruh73g.pdf?ts=1635670146546&ref\\_url=https%253A%252F%252Fwww.ti.com%252Fstesearch%252Fdocs%252Funiversalsearch.tsp%253FlangPref%253Den-US%2526searchTerm%253Dam335x%2Btechnical%2Breference%2Bmanual%2526n%253D231](https://www.ti.com/lit/ug/spruh73g/spruh73g.pdf?ts=1635670146546&ref_url=https%253A%252F%252Fwww.ti.com%252Fstesearch%252Fdocs%252Funiversalsearch.tsp%253FlangPref%253Den-US%2526searchTerm%253Dam335x%2Btechnical%2Breference%2Bmanual%2526n%253D231)

# Extra Note On Device Tree & GPIO: Raspberry Pi Zero W

```
gpio@7e200000 {
    compatible = "bcm,bcm2835-gpio";
    gpio-line-names = "ID_SDA\0ID_SCL\0SDA1\0SCL1\0GPIO_GCLK...";
    gpio-controller;
    gpio-ranges = <0x07 0x00 0x00 0x36>;
    #interrupt-cells = <0x02>;
    interrupts = <0x02 0x11 0x02 0x12>;
    phandle = <0x07>;
    reg = <0x7e200000 0xb4>;
    #gpio-cells = <0x02>;
    pinctrl-names = "default";
    interrupt-controller;
```

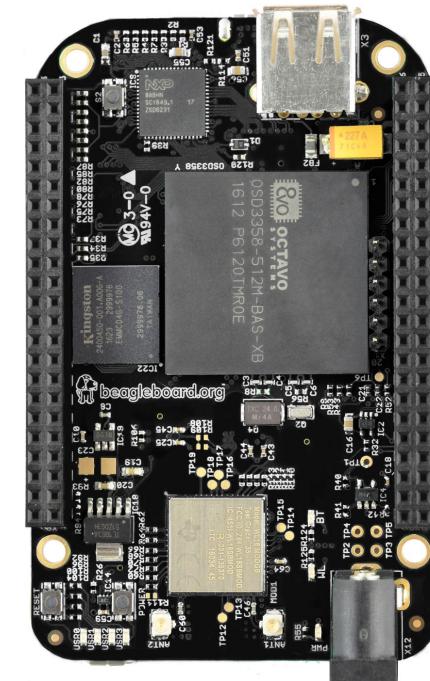
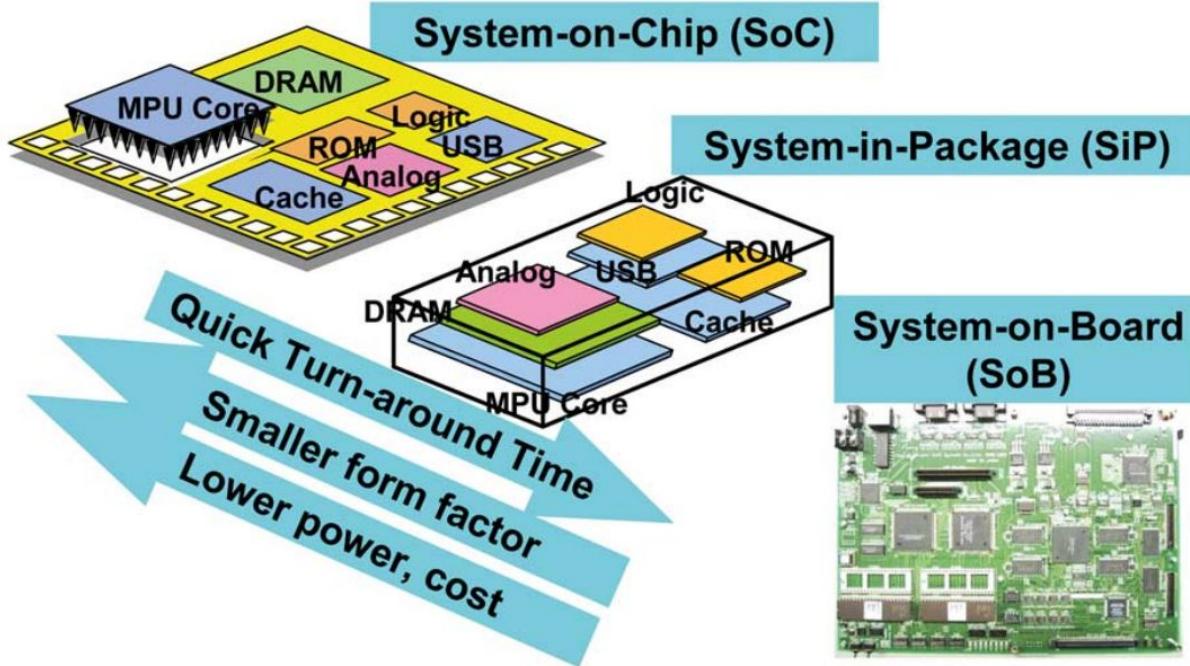
# Device Tree

- It describes hardware
- What's the most important piece of hardware in our BBB?
- **Processor**
- What's the most important piece of hardware in our RPi?
- **System on a chip (SoC)**



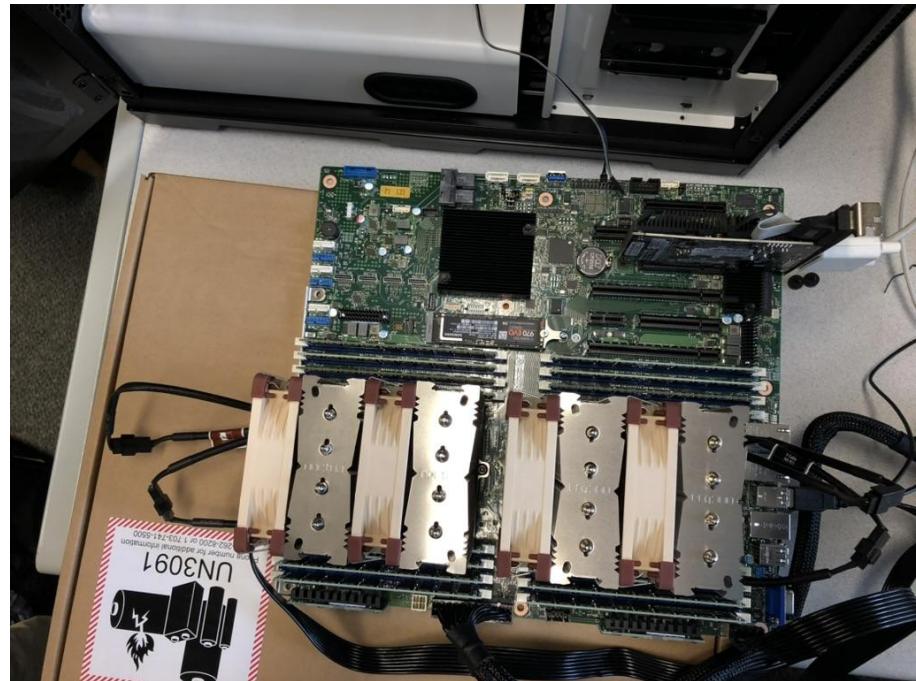
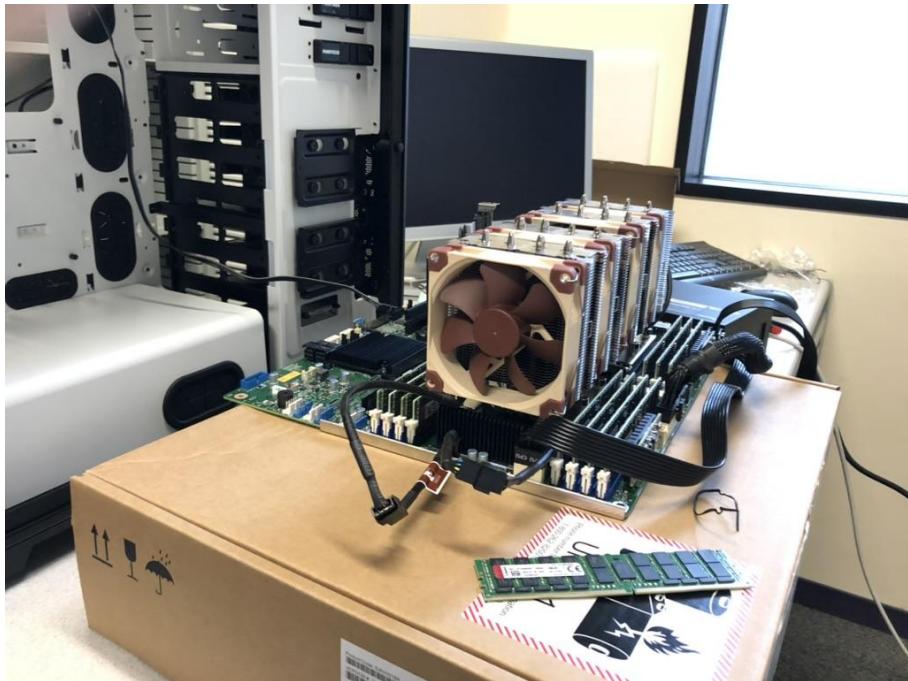
<https://beagleboard.org/black>

# What Is System On Chip (SoC)



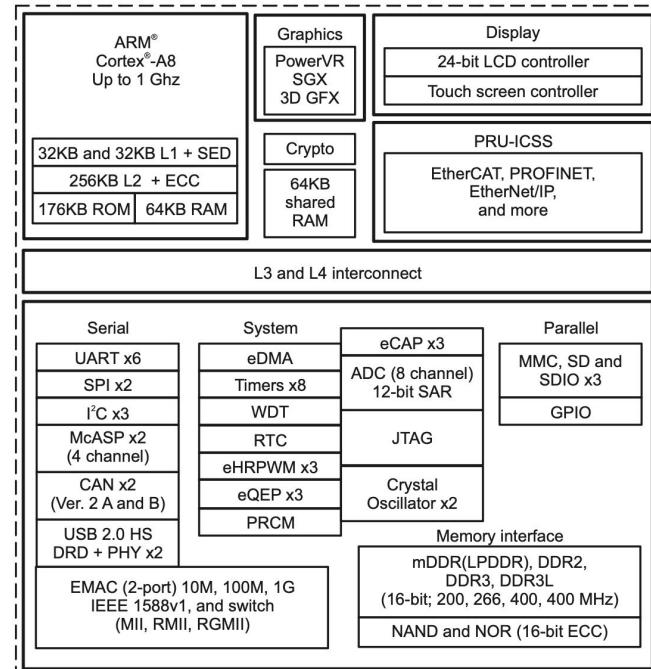
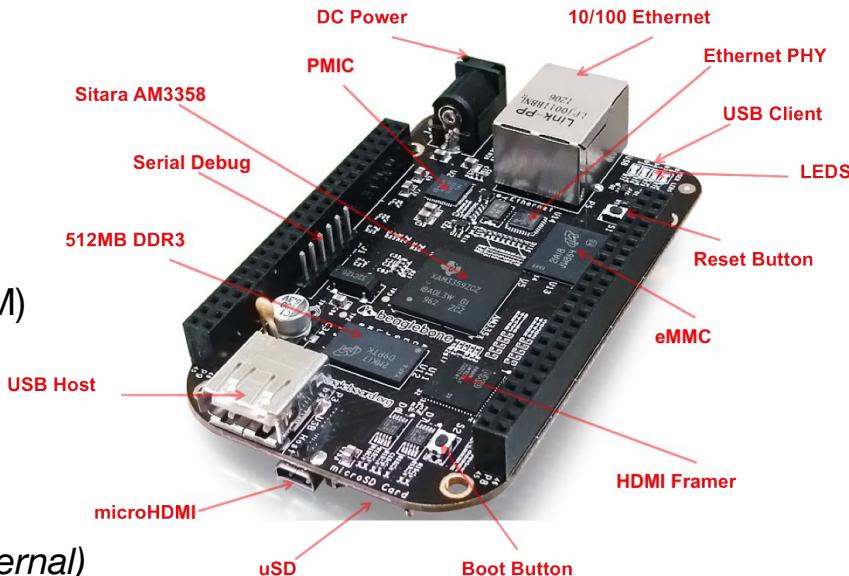
<https://beagleboard.org/black-wireless>

# For Reference: Motherboards



# BBB Processor: AM335x

- AM3358
- Arm Cortex-A8
- 1 GHz
- 32-bit RISC processor (ARM)
- 64KB RAM
  - BBB has 512 MB RAM (external)
- 176KB Boot ROM



Picture in middle from BeagleBoard.org. URL: <https://beagleboard.org/support/bone101>

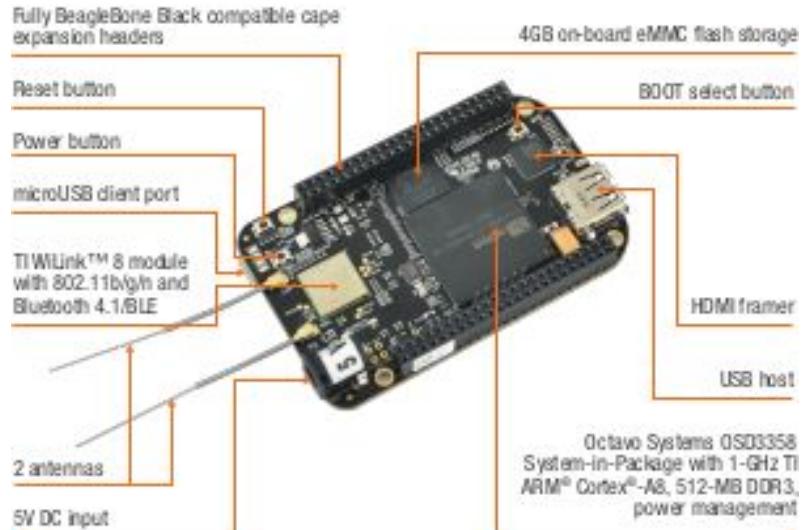
Diagram on right from TI - URL: [https://www.ti.com/lit/ds/symlink/am3358.pdf?ts=1635700794742&ref\\_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FAM3358](https://www.ti.com/lit/ds/symlink/am3358.pdf?ts=1635700794742&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FAM3358)

Info from the following two sources: (1) TI. URL: <https://www.ti.com/product/AM3358#features> (2) BeagleBoard. URL: <https://beagleboard.org/boards>

# BBB WiFi - SiP

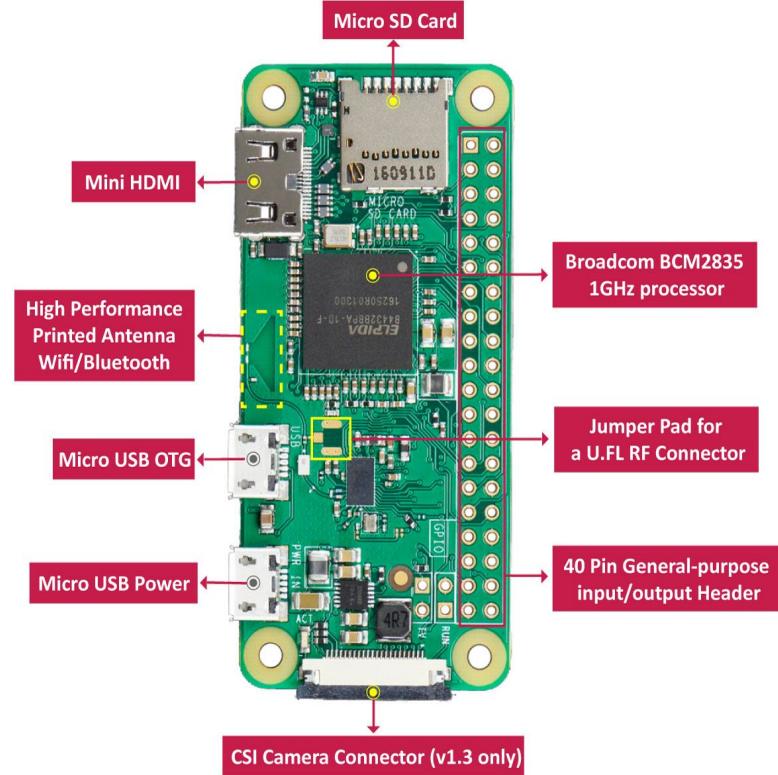
- Like BBB but uses SiP

## BeagleBone Black Wireless



# BBB SoC: AM335x

Specification		Details
Platform	Processor	Broadcom BCM2835
	Frequency	1GHz, Single-core CPU
Memory	Capacity	512MB
	Technology	LPDDR2 SDRAM
Wireless	Wi-Fi	2.4GHz IEEE 802.11b/g/n
	Bluetooth	Bluetooth 4.1, BLE



Picture on right and table from Seeed Studio. URL:  
[https://www.seeedstudio.com/Raspberry-Pi-Zero-W-p-4257.html?queryID=7708c9ab74277e080647299c28660b64&objectID=4257&indexName=bazaar\\_retailer\\_products](https://www.seeedstudio.com/Raspberry-Pi-Zero-W-p-4257.html?queryID=7708c9ab74277e080647299c28660b64&objectID=4257&indexName=bazaar_retailer_products)

# **SoC Enables Smartphones**

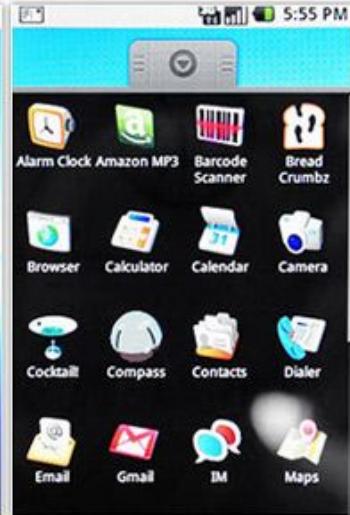
# 2007 - iPhone SoC

- Samsung S5L8900 SoC
- iPhone RAM has never been part of SoC
- Apple implements package on package (PoP)
  - Less integrated than SoC
  - Different from Apple Silicon/M-series approach



# 2008 - HTC Dream/G1

- First Android phone
- Qualcomm MSM7201A SoC



**>>> Fast Forward >>>**

# SoC's Are a Big Deal: Snapdragon 888 (2020)

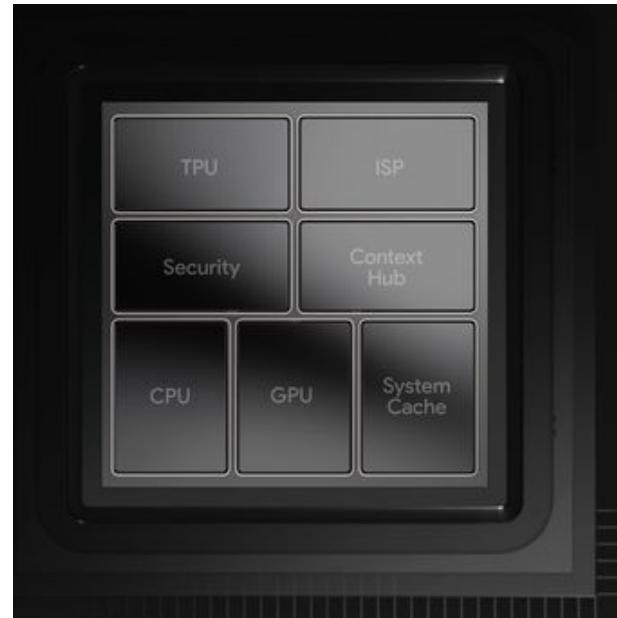
- “Our latest flagship 8 series 5G platform transforms your device into a professional-quality camera, intelligent personal assistant, and elite gaming rig—all connected with truly global 5G multi-gigabit speeds for the premium experiences you deserve.”



Ars Technica. URL:  
<https://arstechnica.com/gadgets/2020/11/apple-dishes-details-on-its-new-m1-chip/>

# SoC's Are a Big Deal: Google's Tensor Chip (2021)

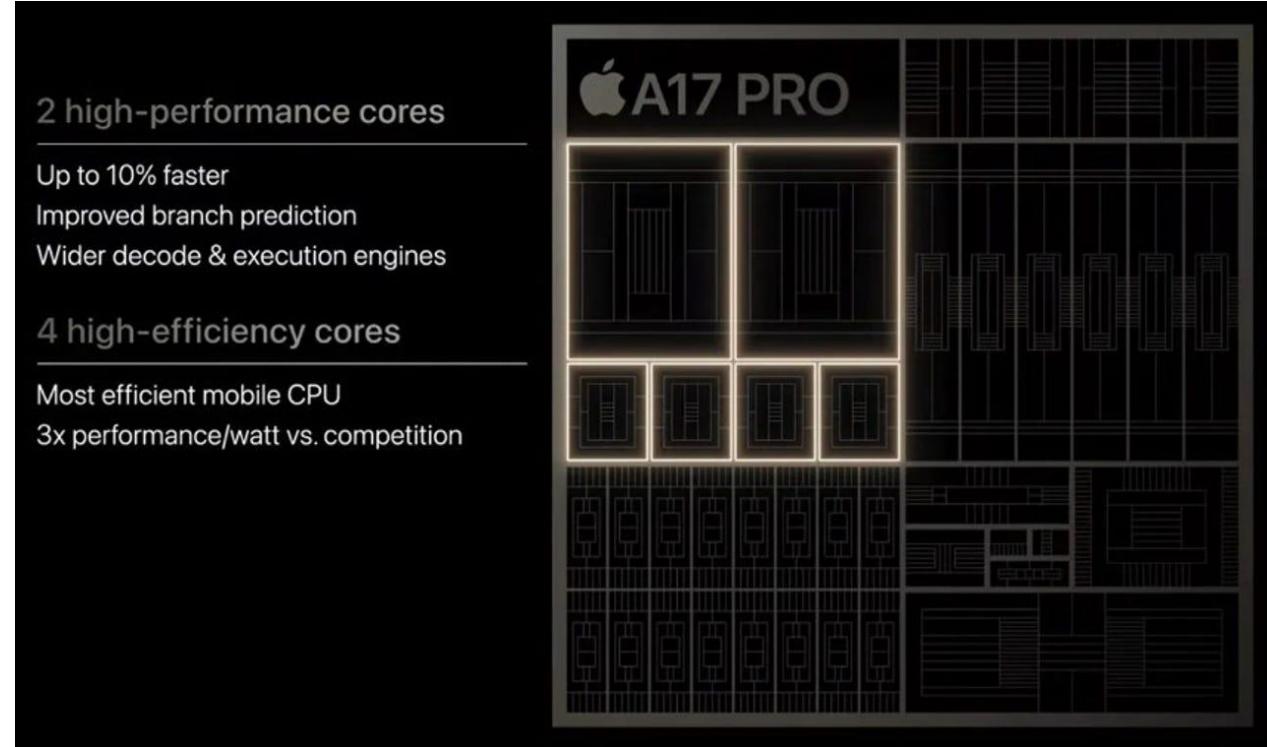
- Pixel 6
- “Google Tensor running more advanced, state-of-the-art ML models but at lower power consumption compared to previous Pixel phones”
- “For example, Google Assistant on Google Tensor uses the most accurate Automatic Speech Recognition (ASR) ever released by Google. And for the first time we can use a high quality ASR model even for long-running applications such as Recorder or tools such as Live Caption without quickly draining the battery.”



Monika Gupta, “Google Tensor is a milestone for machine learning”. URL:  
<https://blog.google/products/pixel/introducing-google-tensor/>

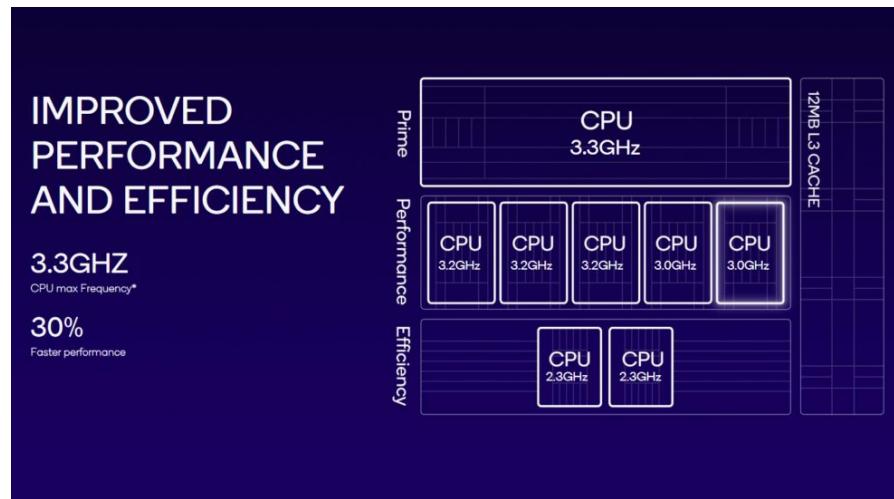
# SoC's Are a Big Deal: Apple A17 Pro (2023)

- 6 cores
  - 2 high-performance
  - 4 efficiency
- 3 nm



# SoC's Are a Big Deal: Snapdragon 8 Gen 3 (2023)

- “This will show up in most flagship Android devices in 2024 and promises around 30 percent performance improvements”
- 4 nm
- “Qualcomm spent most of its presentation talking about AI features”

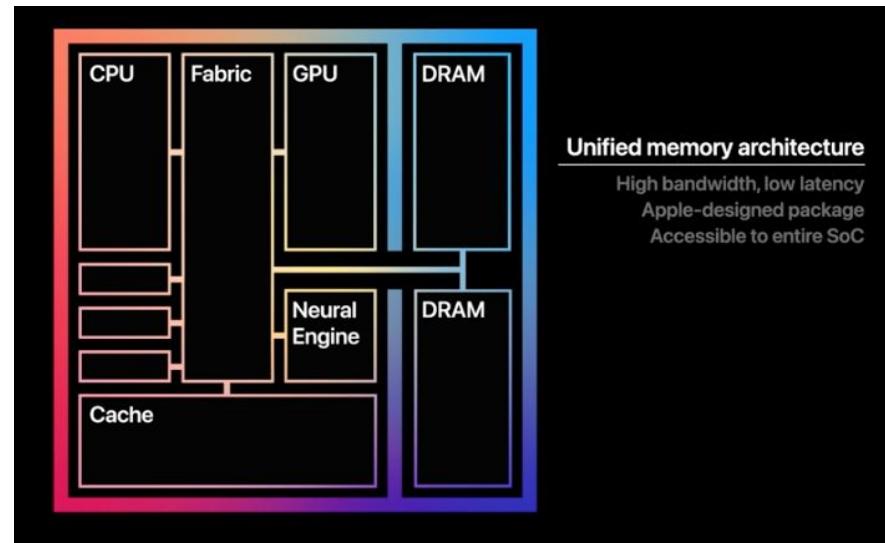


From Qualcomm, found on Ars Technica. Found at URL:  
<https://arstechnica.com/gadgets/2023/10/qualcomms-snapdragon-8-gen-3-promises-30-percent-faster-cpu/>

# **SoC Breaks Into The Laptop**

# Apple's M1 Chip (2020)

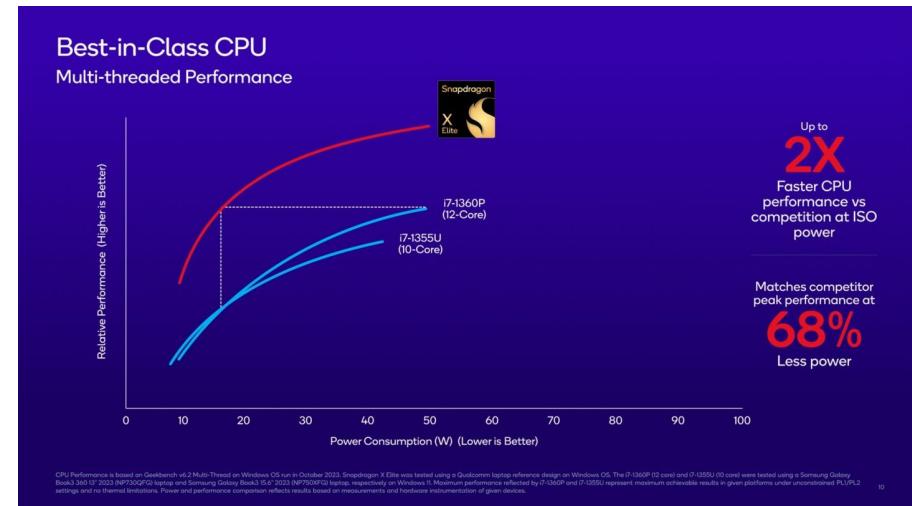
- First 5-nm PC chip
- 16 billion transistors
- “battery life up to 2x longer than previous-generation Macs”
- “Macs and PCs have traditionally used multiple chips for the CPU, I/O, security, and more”
- “these technologies are combined into a single SoC, delivering a whole new level of integration for greater performance and power efficiency”
- M2 is from enhanced 5 nm process



Ars Technica. URL:  
<https://arstechnica.com/gadgets/2020/11/apple-dishes-details-on-its-new-m1-chip/>

# SoC's Are a Big Deal: Qualcomm Snapdragon X Elite (2023)

“Nearly three years ago, **Qualcomm bought a** company called **Nuvia** for \$1.4 billion. Nuvia was mainly working on server processors, but the company's founders and many of its employees had also been **involved in developing the A- and M-series Apple Silicon** processors that have all enabled the iPhone, iPad, and Mac to achieve their enviable blend of performance and battery life. Today, **Qualcomm is formally announcing the fruit of the Nuvia acquisition:** the Qualcomm Snapdragon X Elite is a **12-core, 4 nm chip** that will compete directly with Intel's Core processors and AMD Ryzen chips in PCs—and, less directly, Apple's M2 and M3-series processors for Macs.”



# M3 Is Coming



3 nm

Left from comment by user randolorian on MacRumors. URL:  
<https://www.macrumors.com/2020/10/13/apple-magsafe-iphone-12/>

Middle from MacRumors. URL:  
<https://www.macrumors.com/2012/05/30/tim-cook-at-d10-loves-that-customer-rumor-sites-and-the-media-care-about-apple/>

Right from Imgflip. URL:  
<https://imgflip.com/memegenerator/78785463/Tim-Cook-Laughing>

# Why SoC's? Integration Benefits

- Power efficiency
  - “Usually 90% of power consumption is in data and bus address cabling. Since all the components are on the same chip and internally connected, and their size is also very small, the power consumption is hugely decreased.”
- Performance
- Smaller footprint
- Less weight

# Things Are Just Getting Started

**SIA** SEMICONDUCTOR INDUSTRY ASSOCIATION

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## Latest News

**Senate Passage of USICA Marks Major Step Toward Enacting Needed Semiconductor Investments**

Tuesday, Jun 08, 2021, 6:30pm  
by Semiconductor Industry Association

*United States Innovation and Competition Act would provide \$52 billion to fund the semiconductor research, design, and manufacturing initiatives in the CHIPS for America Act*

[https://www.semiconductors.org/senate-passage-of-usica-marks-major-step-towa  
rd-enacting-needed-semiconductor-investments/](https://www.semiconductors.org/senate-passage-of-usica-marks-major-step-toward-enacting-needed-semiconductor-investments/)

**CNBC**

MARKETS BUSINESS INVESTING TECH POLITICS CNBC TV WATCHLIST CRAMER PRO ▾

TECH

## Google is planning a new Silicon Valley campus with hardware hub, plans show

PUBLISHED FRI, AUG 6 2021 1:47 PM EDT

Jennifer Elias @JENN\_ELIAS

SHARE f t in e

**KEY POINTS**

- Google is planning another new Silicon Valley campus dubbed "Midpoint."
- The five-building office campus will sit adjacent to a large new center for Google's hardware business, according to preliminary plans.
- One large building in particular is getting an overhaul. 20% of that building is designated for office space and 80% for manufacturing (presumably prototype devices), storage, distribution, and other purposes, according to plans. The company began planning the site in 2018.

In this article GOOGL +4.08 (+0.14%)

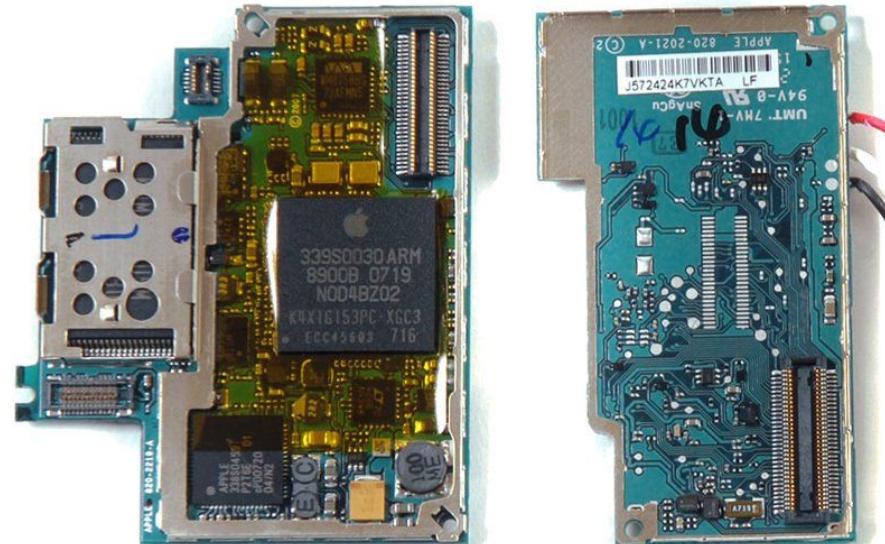


Google is asking the city for feedback on its early plans to transform a Silicon Valley office site with "sustainability" features.  
City of San Jose filing

Jennifer Elias, "Google is planning a new Silicon Valley campus with hardware hub, plans show". URL:  
[https://www.cnbc.com/2021/08/06/google-planning-silicon-valley  
-campus-hardware-lab.html](https://www.cnbc.com/2021/08/06/google-planning-silicon-valley-campus-hardware-lab.html)

# The Original iPhone (2007) Chip Wasn't Intel's Or AMD's

- Package on package (PoP) SoC
- **ARM** processor
- PowerVR GPU
- 412 MHz
- Chip manufacturer: Samsung
- iPhone 3G had same chip



“iPhone 1st Generation Teardown”. iFixit. URL:  
<https://www.ifixit.com/Teardown/iPhone+1st+Generation+Teardown/599>

# A Tale of Two Architectures



Arm logo from: <https://www.arm.com/company/policies/trademarks/guidelines-corporate-logo>

Intel logo from: <https://www.intel.com/content/www/us/en/company-overview/visual-brand-identity.html>

AMD logo from: <https://library.amd.com/media/?mediald=0FD2D9C6-DCC2-4ABF-97B3BC268FF0F2C2>

Meme from: <https://knowyourmeme.com/memes/woman-yelling-at-a-cat/photos/templates>

# The Game Is Afoot, Dear Watson

- “fourth quarter of 2020 alone, the Arm ecosystem shipped a record 6.7 billion Arm-based chips”
- “works out to an amazing production rate of 842 chips *per second*”
- “Arm outsells all other popular CPU instruction set architectures — x86, ARC, Power, and MIPS — combined”

tom'sHARDWARE

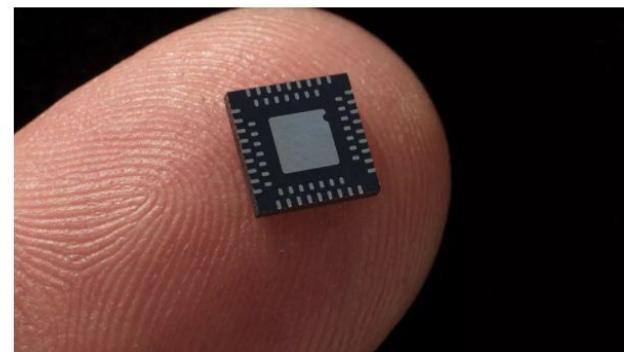
US Edition 

## 842 Chips Per Second: 6.7 Billion Arm-Based Chips Produced in Q4 2020

By Anton Shilov February 13, 2021

Arm-based chips surpass x86, ARC, Power, and MIPS-powered chips, combined

       Comments (2)



(Image credit: Arm)

# ARM May Take Over More Than Just Mobile

A screenshot of the Arm Newsroom website. The header features the "arm" logo. Below it is a large blue background image of a fingerprint. The word "NEWSROOM" is overlaid in white capital letters. The main headline reads "Arm Technology Powers the World's Fastest Supercomputer".

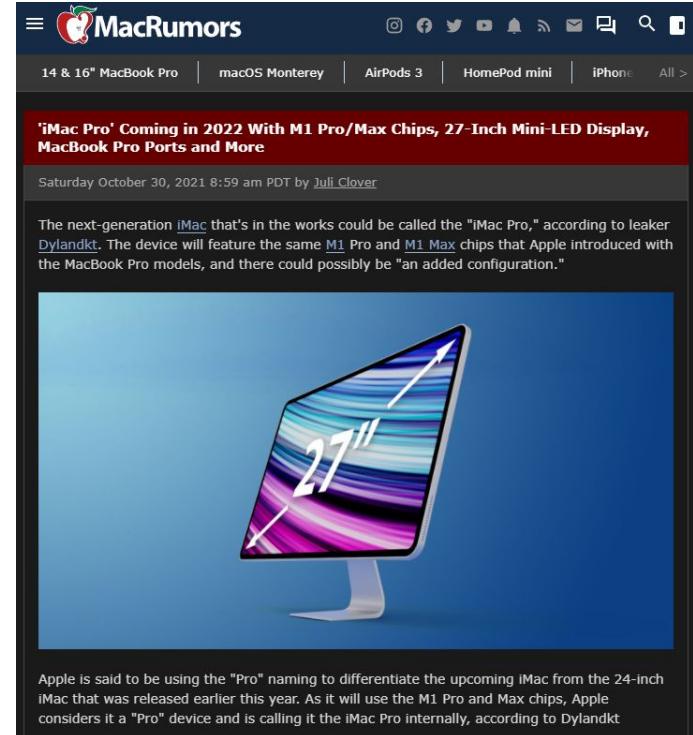
Arm Technology Powers the World's Fastest Supercomputer

June 22, 2020

Fugaku supercomputer, jointly developed by RIKEN and Fujitsu, is No.1 on the TOP500 list

**International Supercomputing Conference** – Today at the International Supercomputing Conference (ISC) it was announced that the Fugaku supercomputer, a system jointly developed by RIKEN and Fujitsu Limited, and based on Arm® technology, was awarded the number one spot of the TOP500 list. Having been crowned the world's most efficient supercomputer on the Green500 list in November 2019, Fugaku was today also given top honors on the [HPCG](#) list, a ranking of benchmarks across real-world applications, and the [HPL-AI](#), which rates performance on tasks used in artificial intelligence applications.

<https://www.arm.com/company/news/2020/06/powering-the-worlds-fastest-supercomputer>

A screenshot of a MacRumors article. The header includes the MacRumors logo and navigation links for "14 & 16" MacBook Pro", "macOS Monterey", "AirPods 3", "HomePod mini", "iPhone", and "All >". The main title is "'iMac Pro' Coming in 2022 With M1 Pro/Max Chips, 27-Inch Mini-LED Display, MacBook Pro Ports and More". The date is Saturday October 30, 2021 8:59 am PDT by Juli Clover. The text discusses the next-generation iMac featuring M1 Pro and M1 Max chips, a 27-inch Mini-LED display, and ports from the MacBook Pro. Below the text is an image of a 27-inch iMac with a colorful abstract screen.

'iMac Pro' Coming in 2022 With M1 Pro/Max Chips, 27-Inch Mini-LED Display, MacBook Pro Ports and More

Saturday October 30, 2021 8:59 am PDT by [Juli Clover](#)

The next-generation [iMac](#) that's in the works could be called the "iMac Pro," according to leaker [Dylandkt](#). The device will feature the same [M1 Pro](#) and [M1 Max](#) chips that Apple introduced with the MacBook Pro models, and there could possibly be "an added configuration."



<https://www.macrumors.com/2021/10/30/imac-pro-2022-rumors/>

# Player 3 Has Joined The Match



**RISC-V is a free and open ISA enabling a new era of processor innovation through open standard collaboration.**

**The RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.**

<https://riscv.org/about/>



TRENDING Alder Lake Apple M1 Pro and M1 Max Windows 11 ISO Bypass Windows 11 TPM

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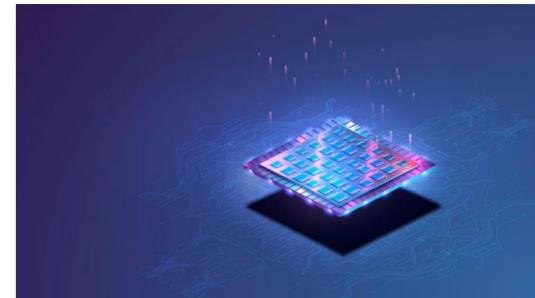
Home > News

**SiFive Envisions 128-Core RISC-V SoCs as Gap With x86 and Arm Closes**

By Anton Shilov 10 days ago

SiFive: RISC-V has no limits.

[Comments \(4\)](#)



(Image credit: OpenFive)

SiFive emerged from stealth mode as a developer of small, low-power cores for microcontrollers in 2016. By late 2020, the company had a chip that could run Linux and this week said that it developed a CPU core that is comparable to modern offerings designed by Intel and Arm. The company believes that such high-performance designs could be used for a wide variety of applications, including server-grade system-on-chips with 128-cores.

<https://www.tomshardware.com/news/sifive-develops-ultra-high-performance-risc-v-core>

# Fun Times

The image shows a screenshot of a news article from SiliconANGLE. At the top left is the SiliconANGLE logo. On the right side of the header are three icons: a person, a gear, and a menu. Below the header, there's a banner for an IBM event titled "Beyond Firewalls Resilience Strategies for All" with an "ON DEMAND" button. The main content area features a large image of a SiFive HiFive Unleashed RISC-V processor chip mounted on a printed circuit board. A red banner at the bottom left reads "INFRa". The main headline is "RISC-V startup SiFive reportedly lets go most of its engineers and executives". Below the headline is a byline "BY MARIA DEUTSCHER".

RISC-V startup SiFive reportedly lets go most of its engineers and executives

BY MARIA DEUTSCHER

SiFive Inc., a well-funded startup that develops RISC-V processors, has reportedly laid off many of its employees and discontinued its core product line.

Semiconductor industry journalist Ian Cutress [reported](#) the development today, citing people familiar with the matter. SiFive confirmed the high-level details of the report in a statement.

SiFive was founded in 2016 by the inventors of the RISC-V instruction set architecture. An instruction set architecture is a collection of technologies that can be used to build central processing units. Unlike Arm Holdings plc's market-leading CPU blueprints, RISC-V is free, which has helped it garner significant industry interest in recent years.

The company has developed a line of ready-to-use CPU cores based on RISC-V. Those cores are optimized for tasks such as running artificial intelligence applications and powering car subsystems. In addition to offering predesigned silicon, SiFive develops custom RISC-V chips for companies with more specialized requirements.

Between 2020 and 2022, the company also competed in the interconnect market. It operated a business unit called OpenFive that developed technologies for tasks such as linking together chiplets and adding USB support to processors. Last May, SiFive [sold](#) the unit to fellow chipmaker Alphawave IP Group plc for \$210 million.

According to today's report, SiFive has laid off most of its engineering, product and sales teams. Many executives are believed to have left as well. SiFive is now said to be led by its founders and Chief Executive Officer Patrick Little.

It's unclear exactly how many employees have been let go. The sources cited in today's report estimate the number ranges from 100 to more than 300. According to its [website](#), SiFive's engineering team included more than 180 staffers who comprised over 85% of its total workforce.

As part of the restructuring initiative, the company is also believed to have discontinued its line of predesigned RISC-V processor cores. From now on, it's expected to focus primarily on designing custom cores for customers.

# Potential NVIDIA Acquisition of ARM



Uniting the world leader in AI with Arm's vast ecosystem to drive innovation and launch a new wave of computing around the world.



## Driving the future of AI

AI is the most powerful technology force of our time. In the future, trillions of computers running AI will create a new internet-of-things all over the world – from smart retail, to manufacturing and service robots, to self-driving cars and smart cities – reinventing computing as we know it.

With its proposed acquisition of Arm, NVIDIA will be able to turn new AI possibilities into realities much faster. Together, we will be able to:

<https://arm.nvidia.com/>

The header of a CNBC news article. It features the NBC logo and the word "CNBC". Below the logo, there are navigation links for "MARKETS", "BUSINESS", "INVESTING", "TECH", "POLITICS", "CNBC TV", "WATCHLIST", "CRAMER", and "PRO".

## TECH

### Nvidia's \$40 billion takeover of Arm faces in-depth investigation from EU

PUBLISHED WED, OCT 27 2021 11:53 AM EDT | UPDATED WED, OCT 27 2021 12:09 PM EDT

Sam Shread  
@SAM\_L\_SHREAD

SHARE

- The probe, announced by the Commission on Wednesday, is the latest setback for the chip companies who have already said the deal is unlikely to be completed before the initial deadline of March 2022.
- The Commission said it is concerned that the merger could restrict access to Arm's "neutral" chip designs and that it could lead to higher prices, less choice and reduced innovation in the semiconductor industry.

In this article

NVDA -1.69 (-0.66%)



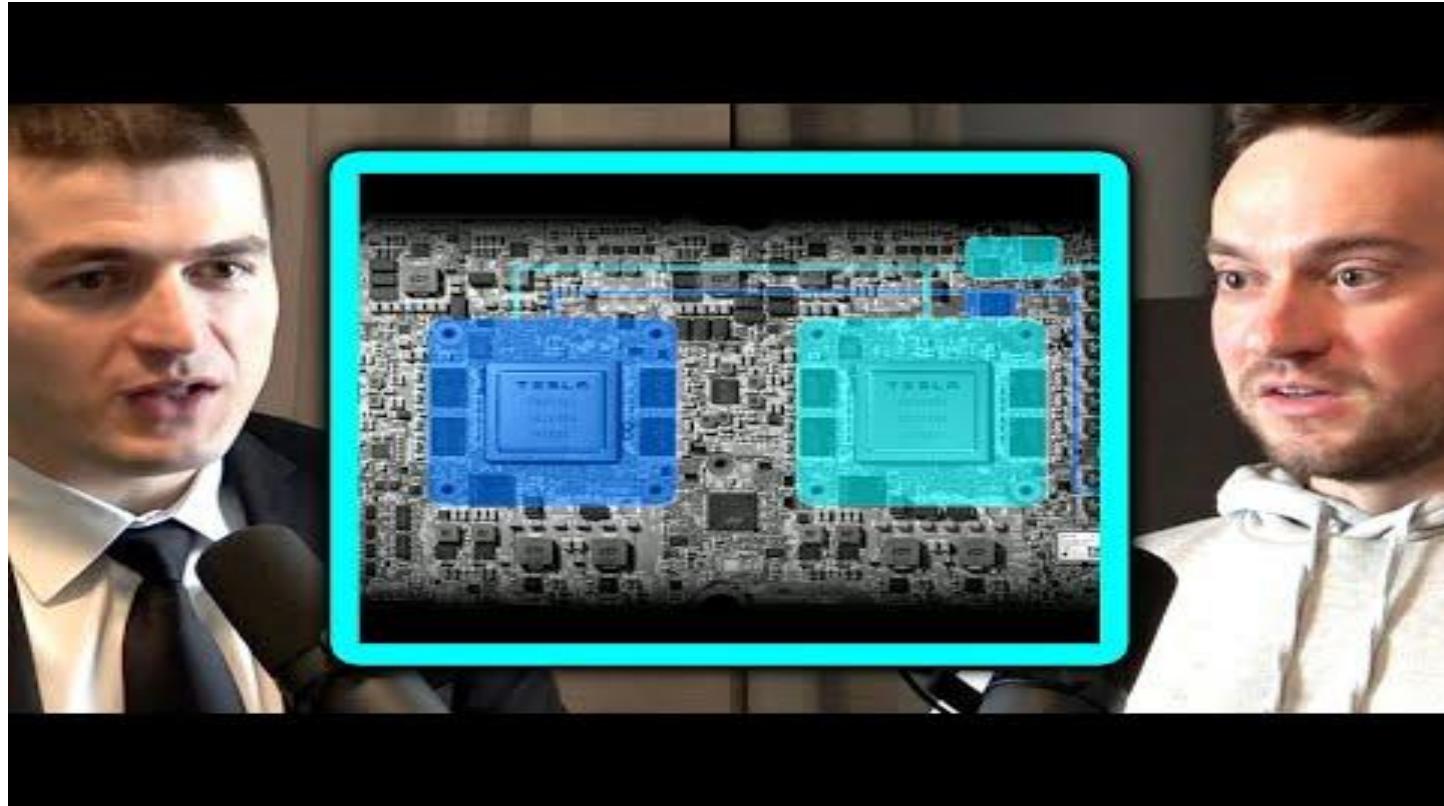
Nvidia CEO Jensen Huang speaks during a press conference at The MGM during CES 2018 in Las Vegas on January 7, 2018.

Mandel Ngan / AFP / Getty Images

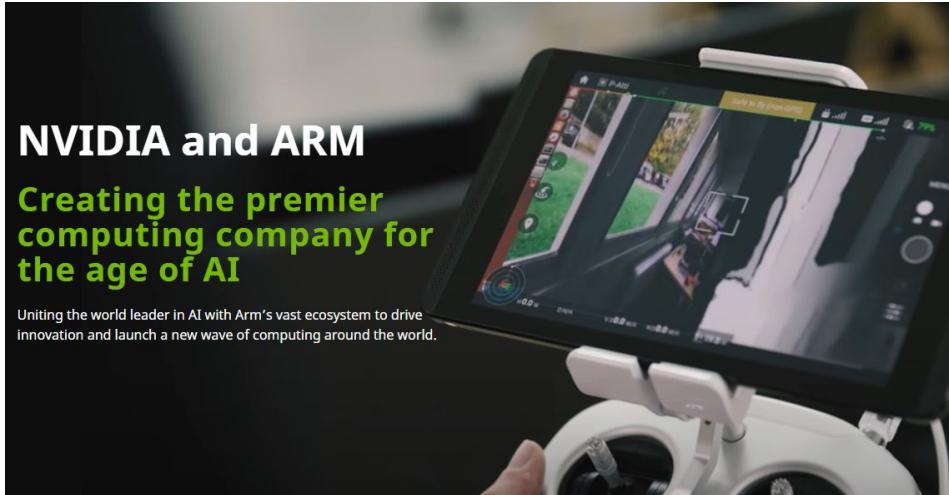
<https://www.cnbc.com/2021/10/27/nvidias-takeover-of-arm-faces-in-depth-investigation-in-europe.html>

**“NVIDIA could be the new Intel”**

(language warning)



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- KEY POINTS**
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Nvidia CEO Jensen Huang speaks during a press conference at The MGM during CES 2018 in Las Vegas on January 7, 2018.

Mandel Ngan / AFP / Getty Images

<https://www.cnbc.com/2021/10/27/nvidias-takeover-of-arm-faces-in-depth-investigation-in-europe.html>

# No Acquisition, But Relationship Continues

The screenshot shows a news article from the NVIDIA Newsroom. The header includes the NVIDIA logo and navigation links for 'Datasheet', 'Newsroom', 'Press Release', 'SHARE' (Twitter, LinkedIn, Facebook, Email), and a menu icon. The main title is 'NVIDIA and SoftBank Group Announce Termination of NVIDIA's Acquisition of Arm Limited'. Below the title is a sub-headline 'SoftBank to Explore Arm Public Offering'. The date 'February 7, 2022' is listed. The main content discusses the termination of the acquisition agreement between NVIDIA and SoftBank Group Corp. due to regulatory challenges, and how Arm will now start preparations for a public offering.

**NVIDIA and SoftBank Group Announce Termination of NVIDIA's Acquisition of Arm Limited**

SoftBank to Explore Arm Public Offering

February 7, 2022

SANTA CLARA, Calif., and TOKYO – Feb. 7, 2022 – NVIDIA and SoftBank Group Corp. ("SBG" or "SoftBank") today announced the termination of the previously announced transaction whereby NVIDIA would acquire Arm Limited ("Arm") from SBG. The parties agreed to terminate the Agreement because of significant regulatory challenges preventing the consummation of the transaction, despite good faith efforts by the parties. Arm will now start preparations for a public offering.

The screenshot shows the 'Datasheet' for the NVIDIA GH200 Grace Hopper Superchip. It features the NVIDIA logo and the product name 'NVIDIA GH200 Grace Hopper Superchip'. A photograph of the superchip is shown on the right. The page is divided into sections: 'Key Features' (listing 72-core Grace CPU, H100 Tensor Core GPU, NVLink-C2C, memory support, and fast-access memory), 'The World's Most Versatile Computing Platform' (describing the NVLink-C2C interconnect), and a detailed diagram of the superchip architecture. The diagram illustrates the central Grace CPU, two Hopper GPUs, and various memory and network components connected via NVLink-C2C and PCIe Gen5 interconnects.

**NVIDIA GH200 Grace Hopper Superchip**

**Key Features**

- > 72-core NVIDIA Grace CPU
- > NVIDIA H100 Tensor Core GPU
- > Up to 480GB of LPDDR5X memory with error-correction code (ECC)
- > Supports 96GB of HBM3 or 144GB of HBM3e
- > Up to 624GB of fast-access memory
- > NVLink-C2C: 900GB/s of coherent memory

**The World's Most Versatile Computing Platform**

The NVIDIA Grace Hopper™ architecture brings together the groundbreaking performance of the Hopper™ GPU with the versatility of the NVIDIA Grace™ CPU in a single superchip, connected with the high-bandwidth, memory-coherent NVIDIA® NVLink® Chip-to-Chip (C2C) interconnect.

NVIDIA NVLink-C2C is a memory-coherent, high-bandwidth, and low-latency interconnect for superchips. The heart of the GH200 Grace Hopper Superchip, it delivers up to 900 gigabytes per second (GB/s) of total bandwidth, which is 7X higher than PCIe Gen5 lanes commonly used in accelerated systems. NVLink-C2C enables applications to oversubscribe the GPU's memory and directly utilize NVIDIA Grace CPU's memory at high bandwidth. With up to 480GB of LPDDR5X CPU memory per GH200 Grace Hopper Superchip, the GPU has direct access to 7X more fast memory than HBM3 or almost 8X more fast memory with HBM3e. GH200 can be easily deployed in standard servers to run a variety of inference, data analytics, and other compute and memory-intensive workloads. GH200 can also be combined with the NVIDIA NVLink Switch System, with all GPU threads running on up to 256 NVLink-connected GPUs and able to access up to 144 terabytes (TB) of memory at high bandwidth.

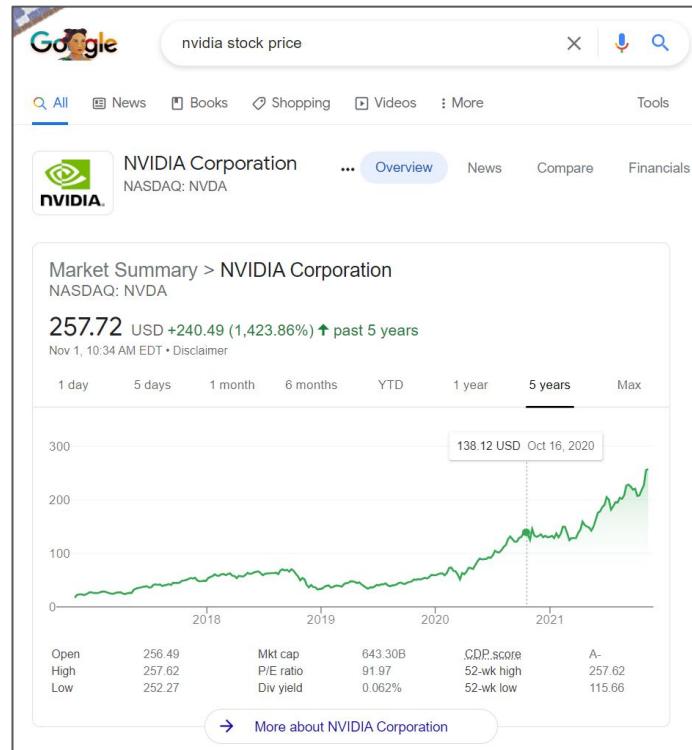
**NVIDIA GH200 Grace Hopper Superchip**

The diagram shows the internal structure of the GH200 superchip. It features a central Grace CPU (LPDDR5X 480GB) connected to two Hopper GPUs (LPDDR5 144GB). Both the CPU and GPUs are connected to a NVLink-C2C interconnect. The diagram also shows PCIe Gen5 lanes (16x) and memory modules (16Gb, 32Gb, 64Gb) connected to the chip. Network interfaces (NVLink 4x, NVLink 2x, PCIe Gen5 2x) are also depicted.

# NVIDIA Stock Price

Hardware is a  
big deal

How do we  
boot up  
hardware?



Middle and right screenshots from Googling “nvidia stock price”, middle is from 2021 and right is from 2023. URL for 2023:

[https://www.google.com/search?q=nvidia+stock+price&og=nvidia+stock+price&gs\\_lcp=EgZjaHJvbWUyDwgAEFUYORIDArAxjABDIINCAEQABiDARjAxjABDIHCIAQABiABDIHCAQQABiABDIHCAUQABiABDIHCAYQABiABDIHCACQABiABDIHCABQABiABDIHCABCDMwNTBqMWo3qAisAIA&sourceid=chrome&ie=UTF-8](https://www.google.com/search?q=nvidia+stock+price&og=nvidia+stock+price&gs_lcp=EgZjaHJvbWUyDwgAEFUYORIDArAxjABDIINCAEQABiDARjAxjABDIHCIAQABiABDIHCAQQABiABDIHCAUQABiABDIHCAYQABiABDIHCACQABiABDIHCABQABiABDIHCABCDMwNTBqMWo3qAisAIA&sourceid=chrome&ie=UTF-8)

# Back To Our Cute Beagle

**“How do I turn this thing on?”**



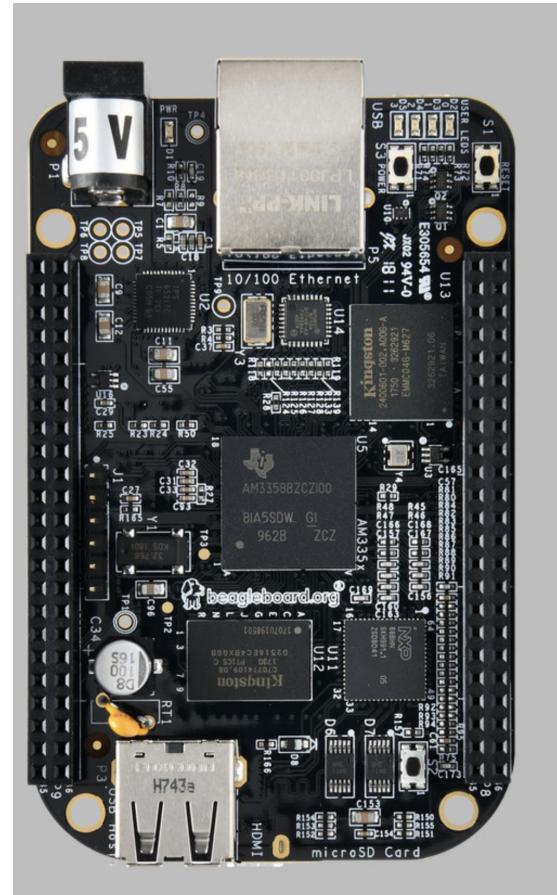
[https://store.steampowered.com/app/813780/Age\\_of\\_Empires\\_II\\_Definitive\\_Edition/](https://store.steampowered.com/app/813780/Age_of_Empires_II_Definitive_Edition/)



<https://www.liveabout.com/age-of-empires-2-cheats-pc-4688586>



<https://www.deviantart.com/trebuxet/art/How-do-you-turn-this-on-346449804>



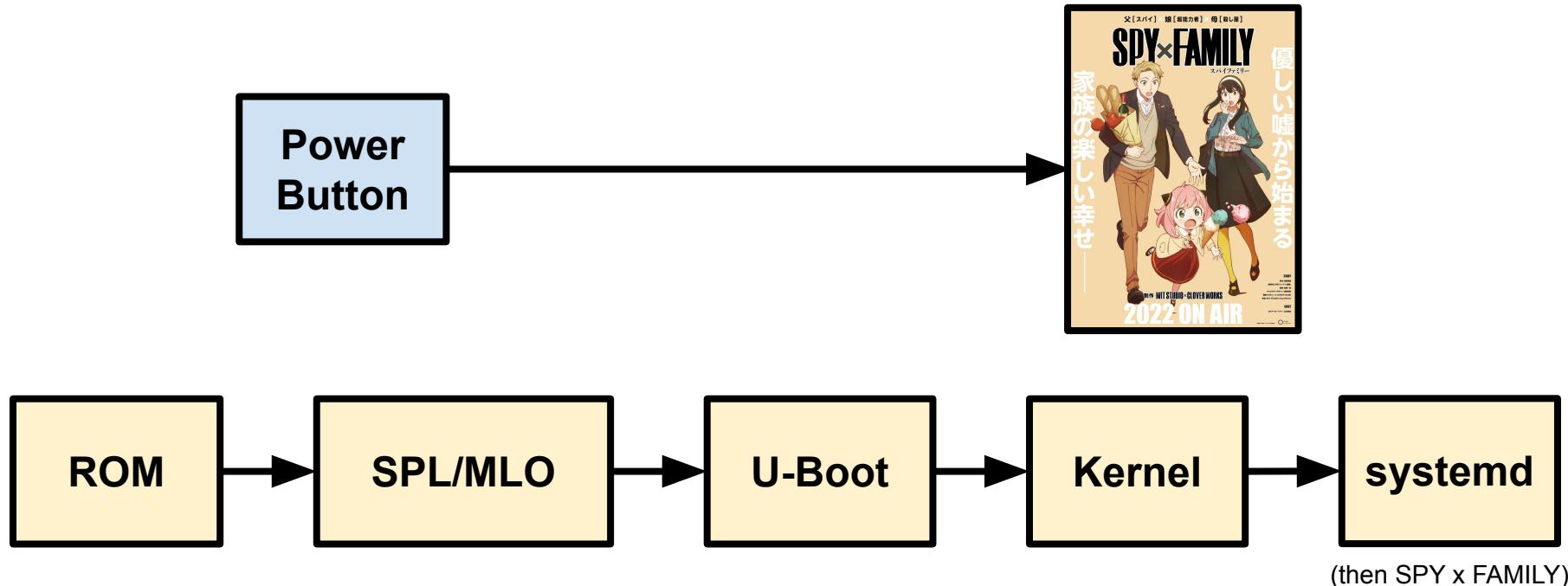
<https://beagleboard.org/black>

# Goal Of Boot Process (2023 Edition)

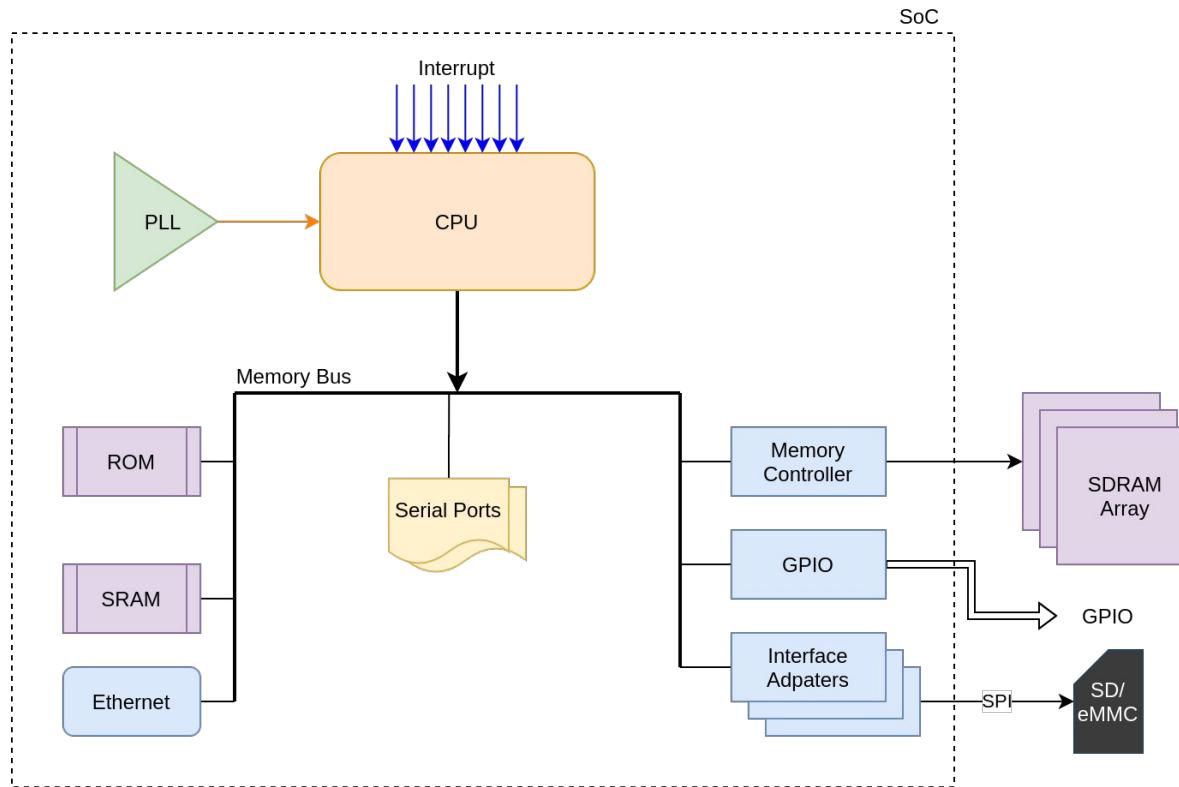


(season 3)

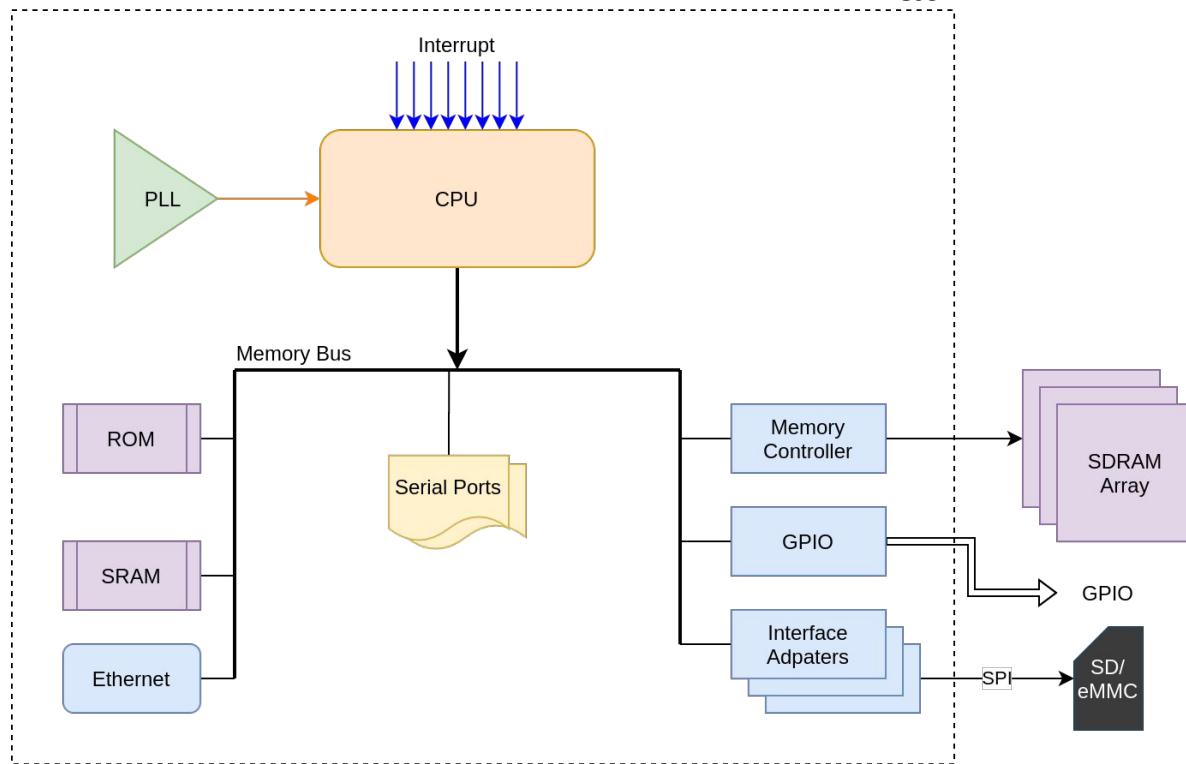
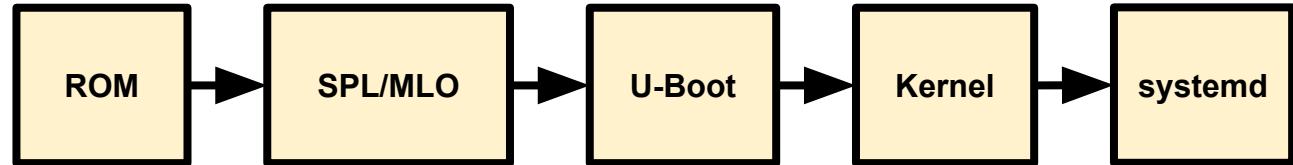
# Actual Boot Process



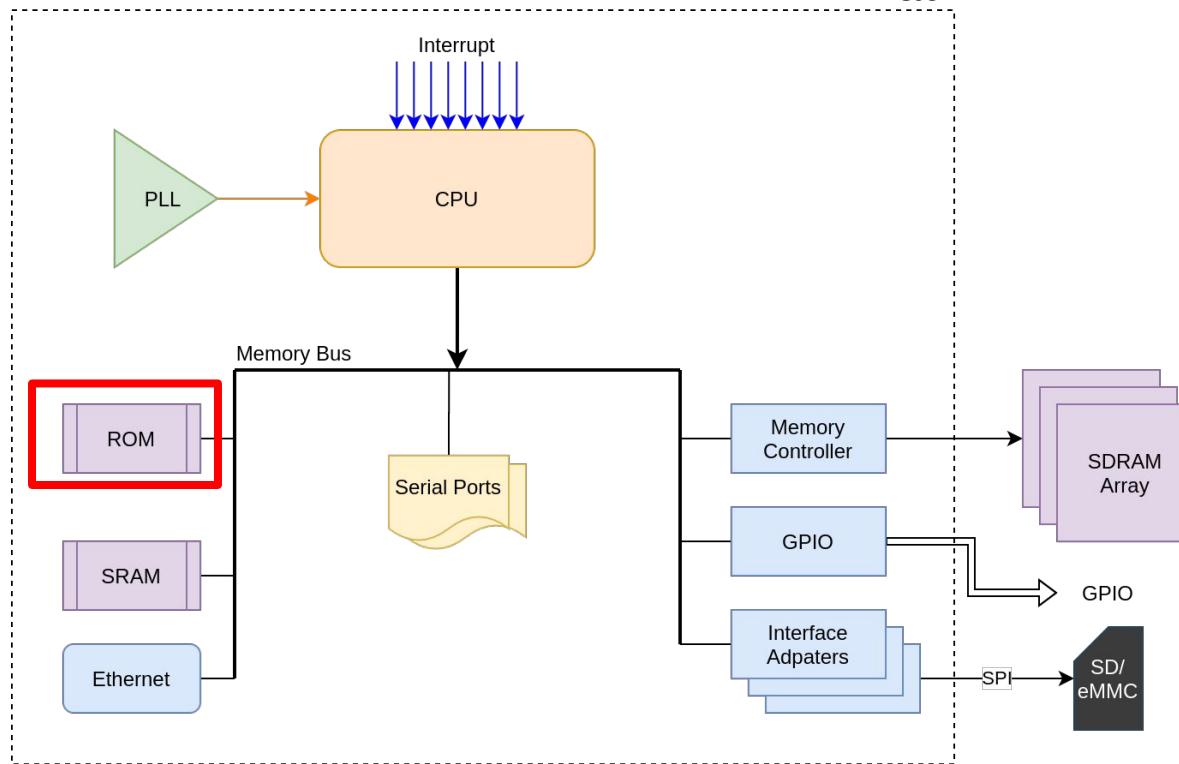
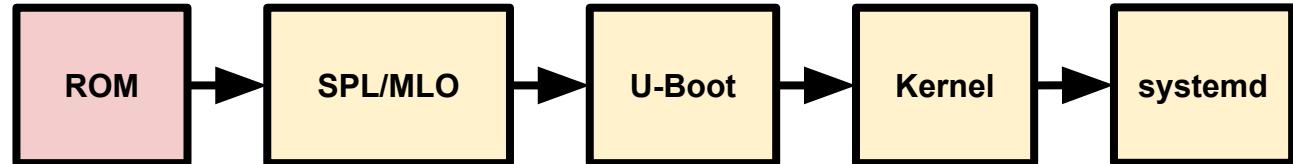
# SoC & Boot-Up



# SoC & Boot-Up



# SoC & Boot-Up



# 1. ROM (Firmware) [ZSBL]

- ROM: Read-only memory
- ZSBL: Zeroth stage bootloader
  - This is sometimes called the first stage 
- Stores first software that processor runs
- Configures clocks

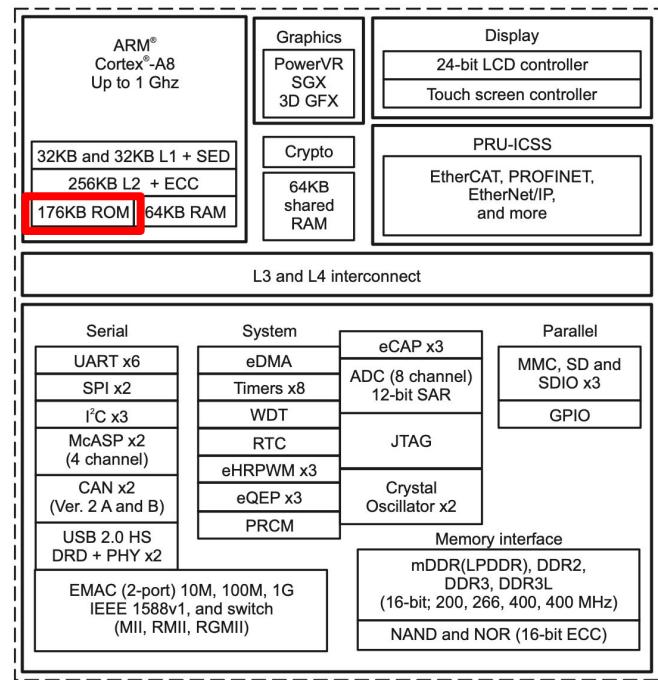
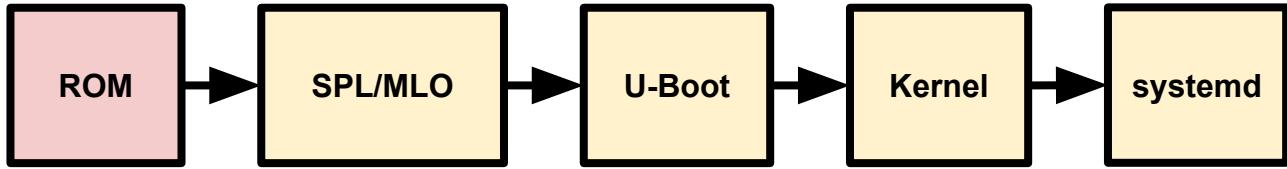
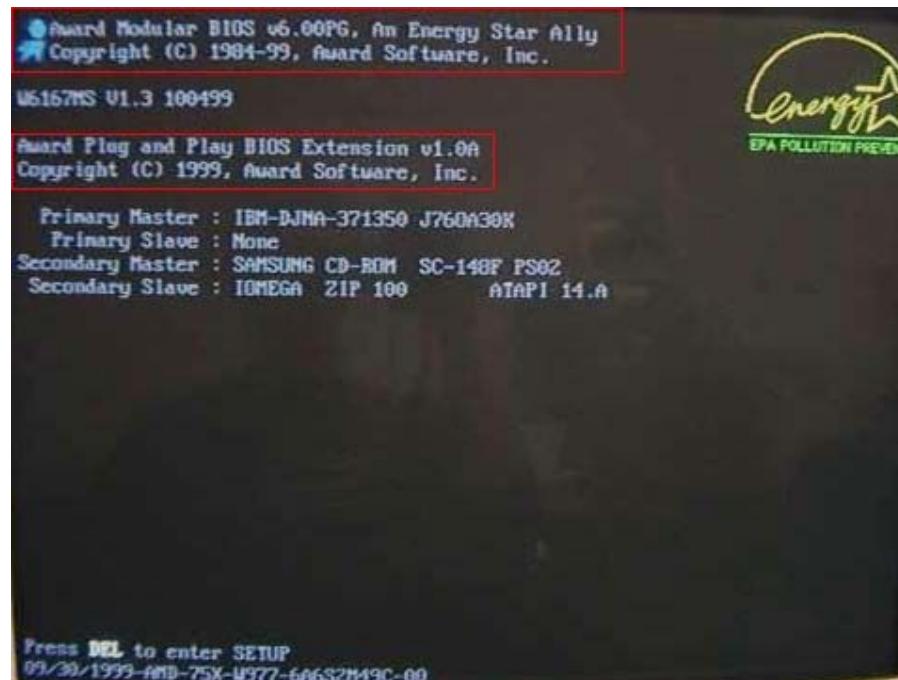


Figure 1-1. AM335x Functional Block Diagram

# BIOS - PC Equivalent of OMAP ROM

- Basic input output system
- On ROM
- Not tied to an OS
- POST
  - Power-on self-test



POST screen. From Computer Hope. URL:  
<https://www.computerhope.com/issues/ch000234.htm>

# 1. OMAP ROM

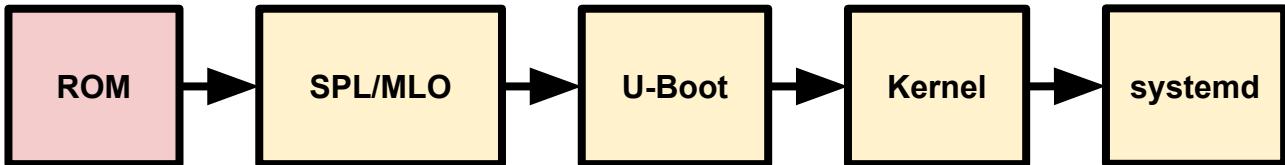
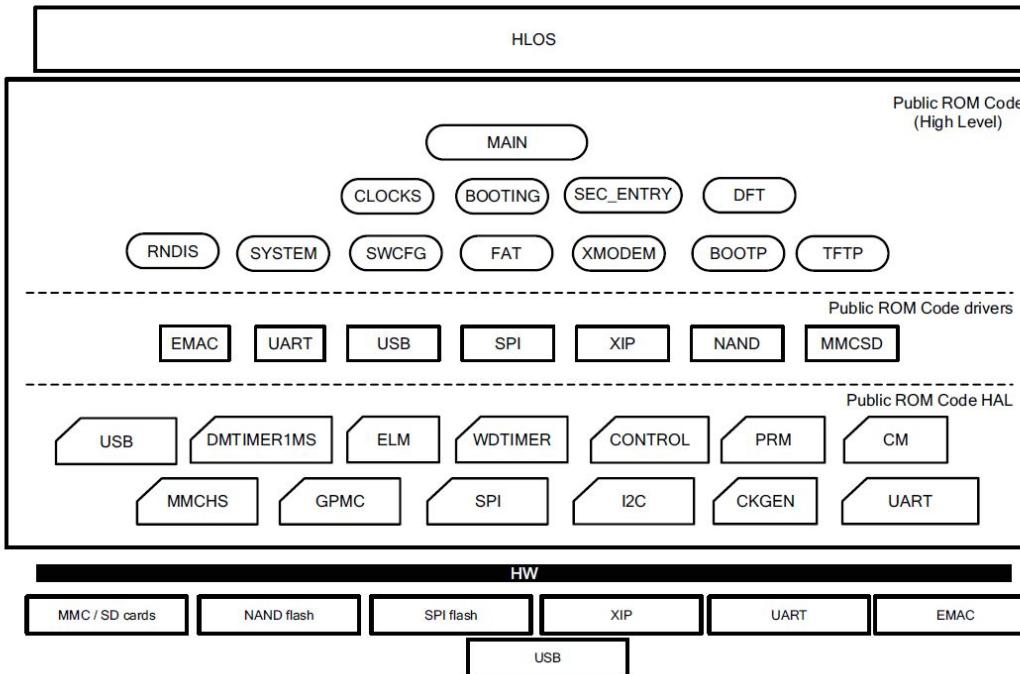


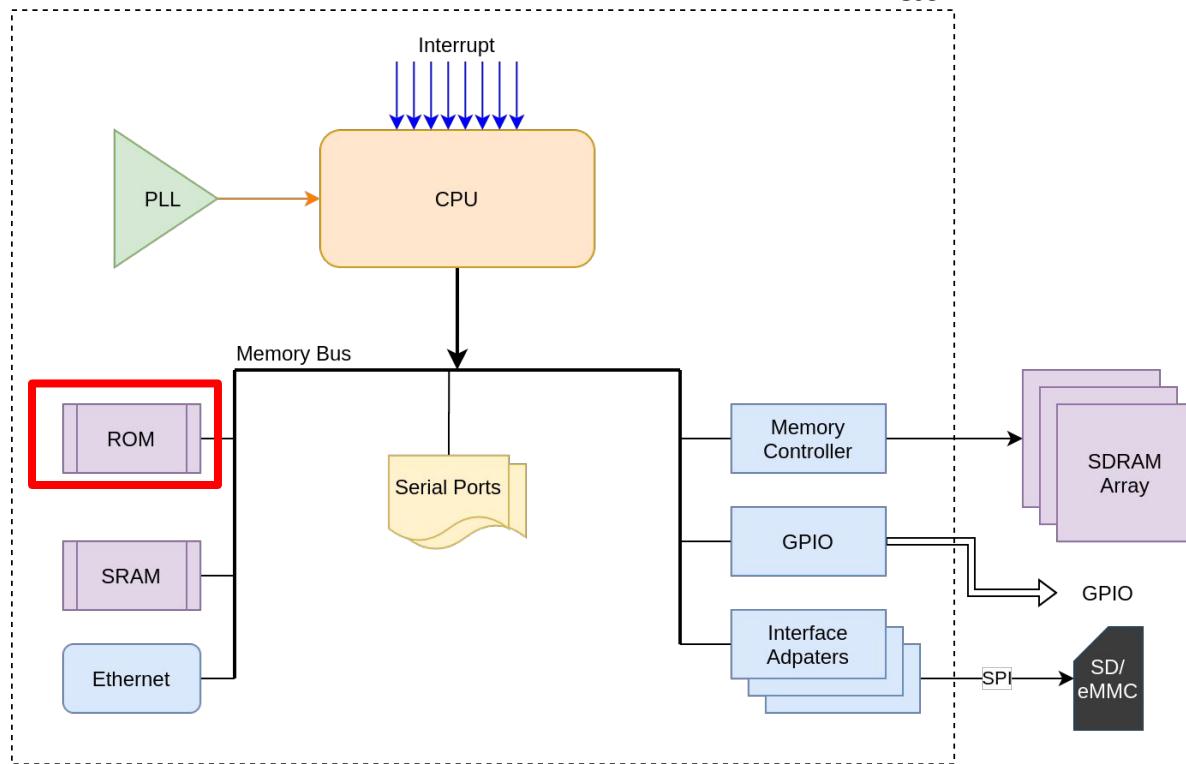
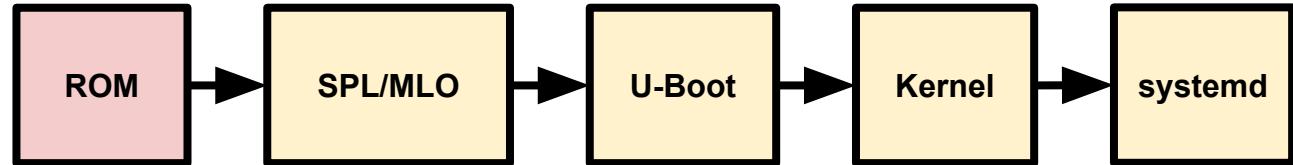
Figure 26-1. Public ROM Code Architecture



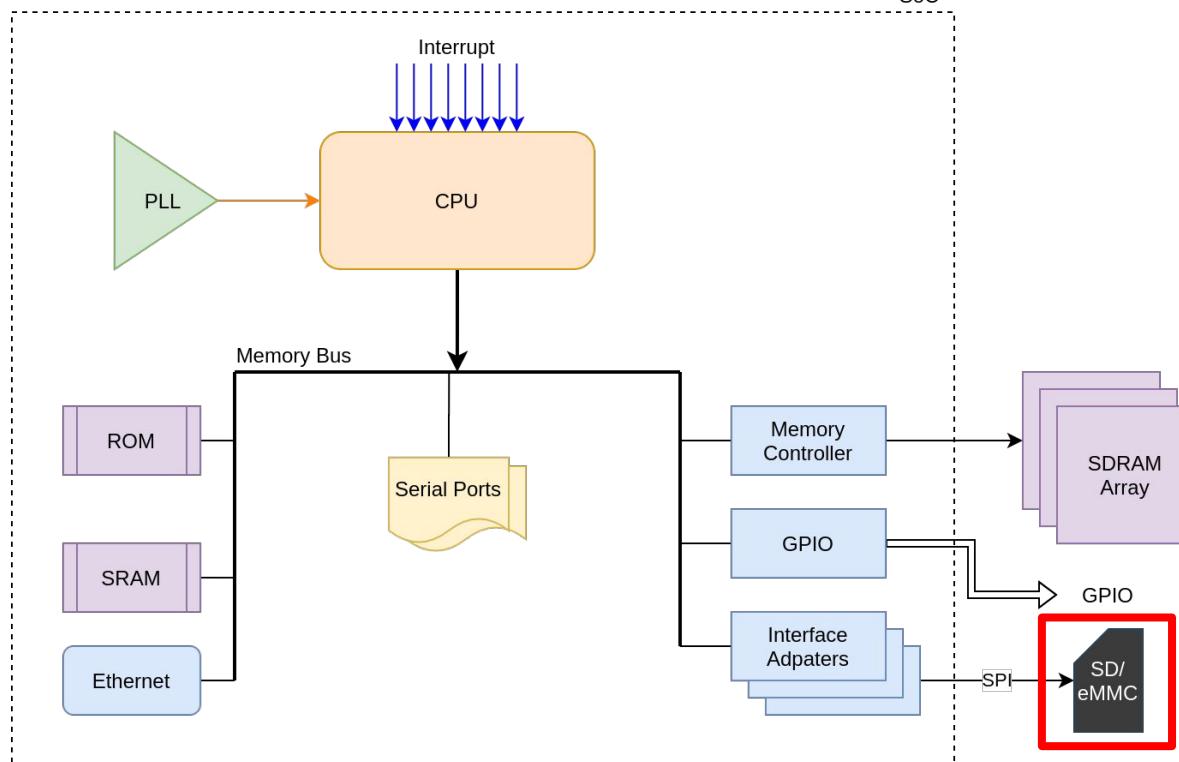
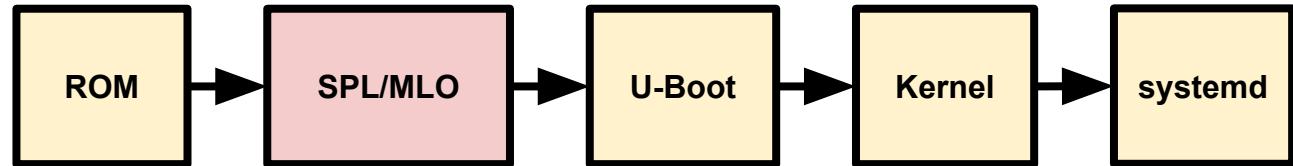
From page 5019 of TI's AM335x and AMIC110 Sitara™ Processors Technical Reference Manual.

URL: [https://www.ti.com/lit/ug/spruh73q/spruh73q.pdf?ts=1635782166289&ref\\_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FAM3358](https://www.ti.com/lit/ug/spruh73q/spruh73q.pdf?ts=1635782166289&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FAM3358)

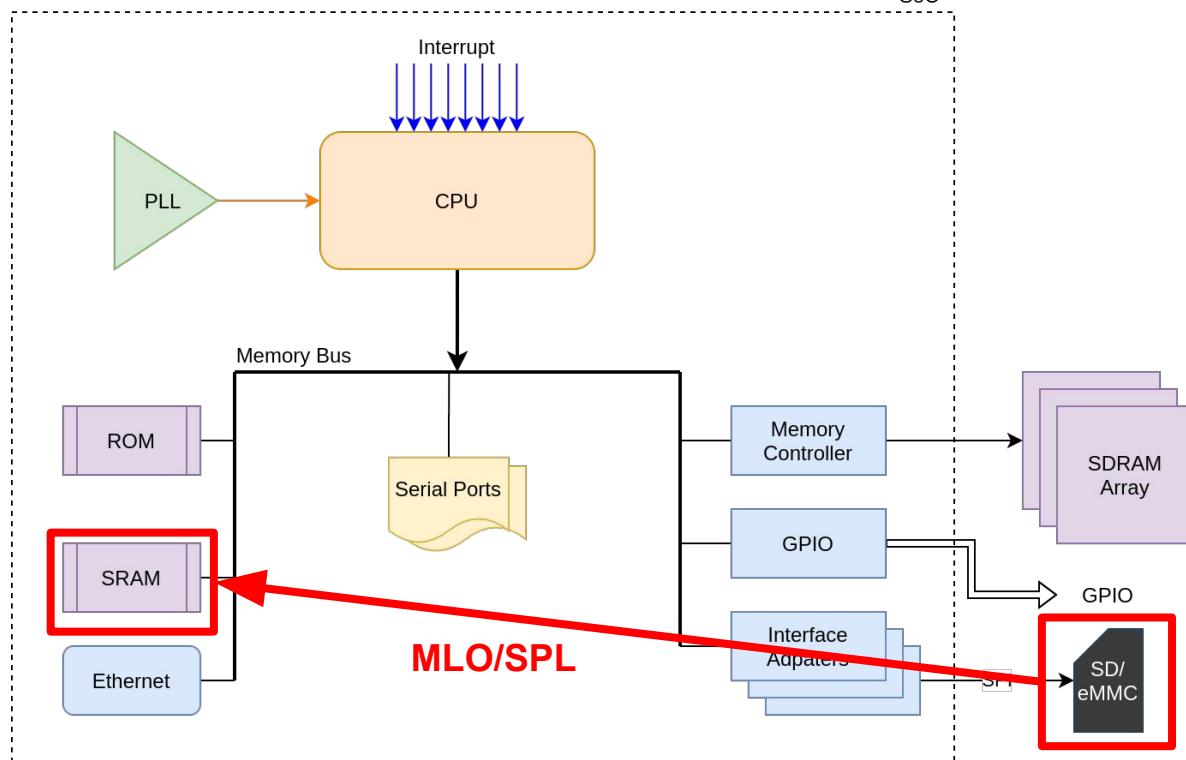
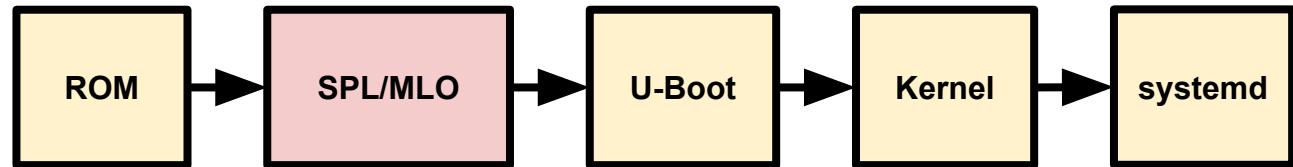
# SoC & Boot-Up



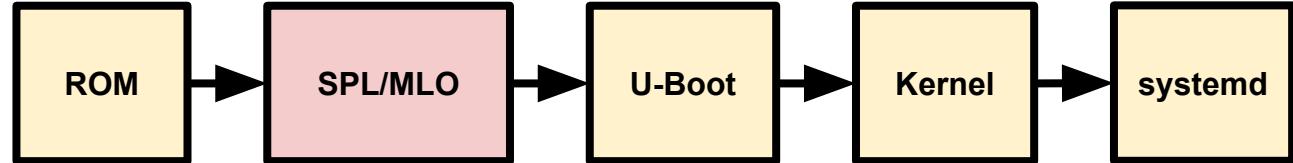
# SoC & Boot-Up



# SoC & Boot-Up

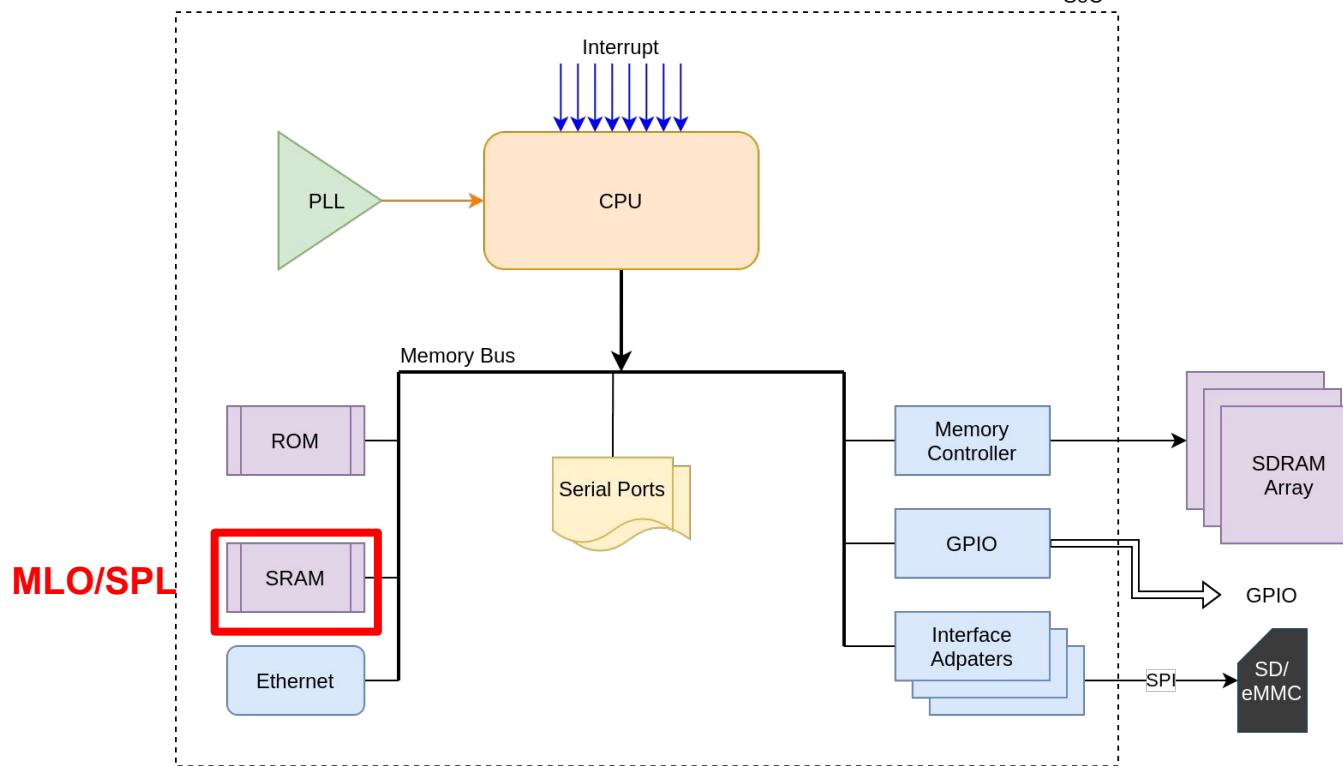
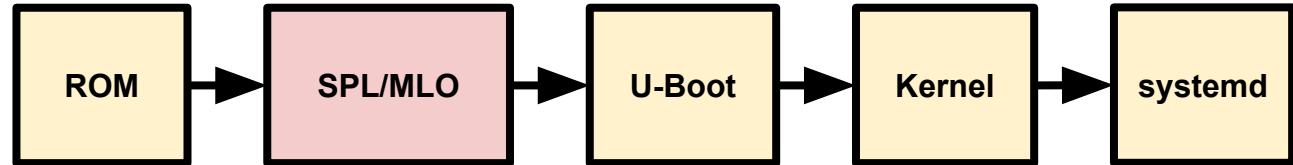


## 2. Loader (SPL) [FSBL]

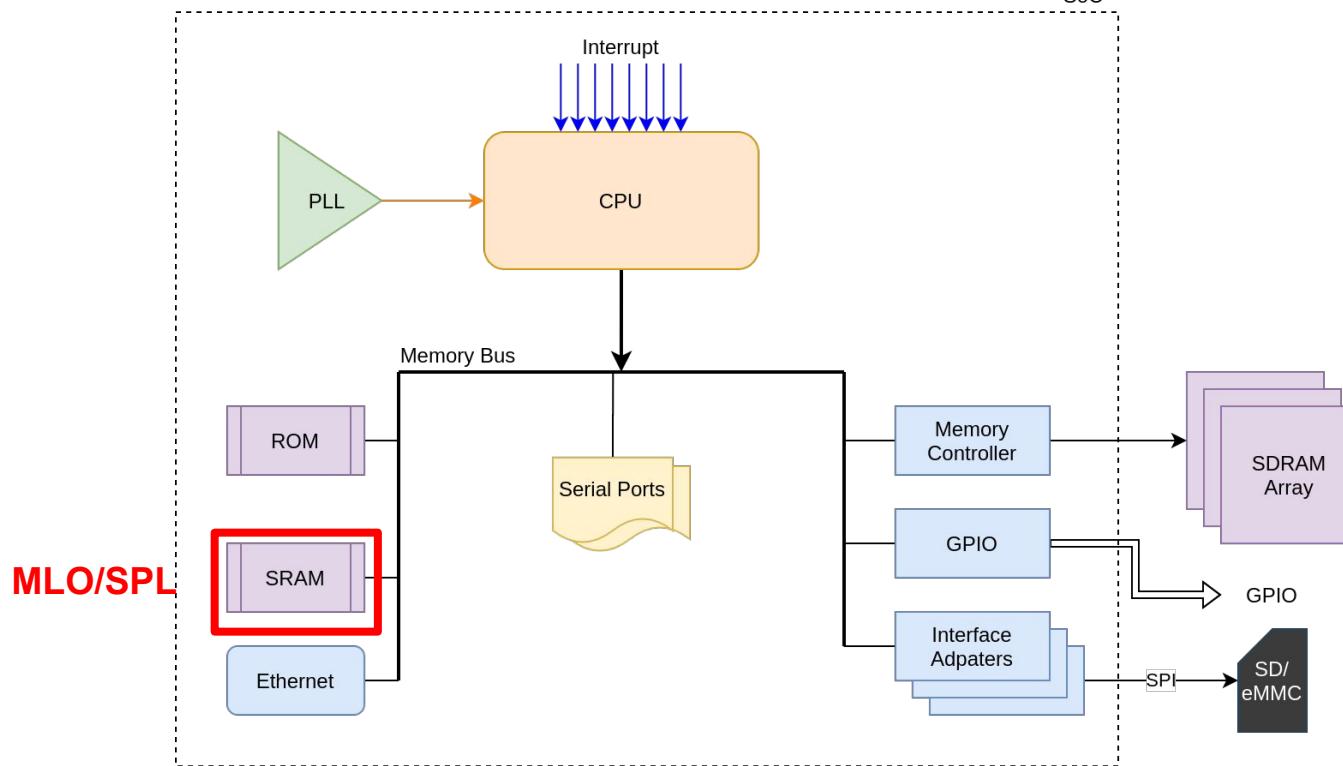
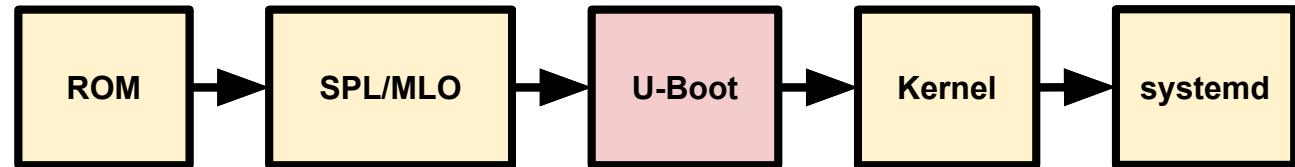


- SPL: Secondary program loader
- FSBL: First stage bootloader
  - This is sometimes called the second stage :)
- MLO: MMC loader
  - MMC - MultiMediaCard
  - BeagleBone has eMMC - embedded MMC (4GB)
- Program that can load next program (U-Boot) into off-SoC RAM

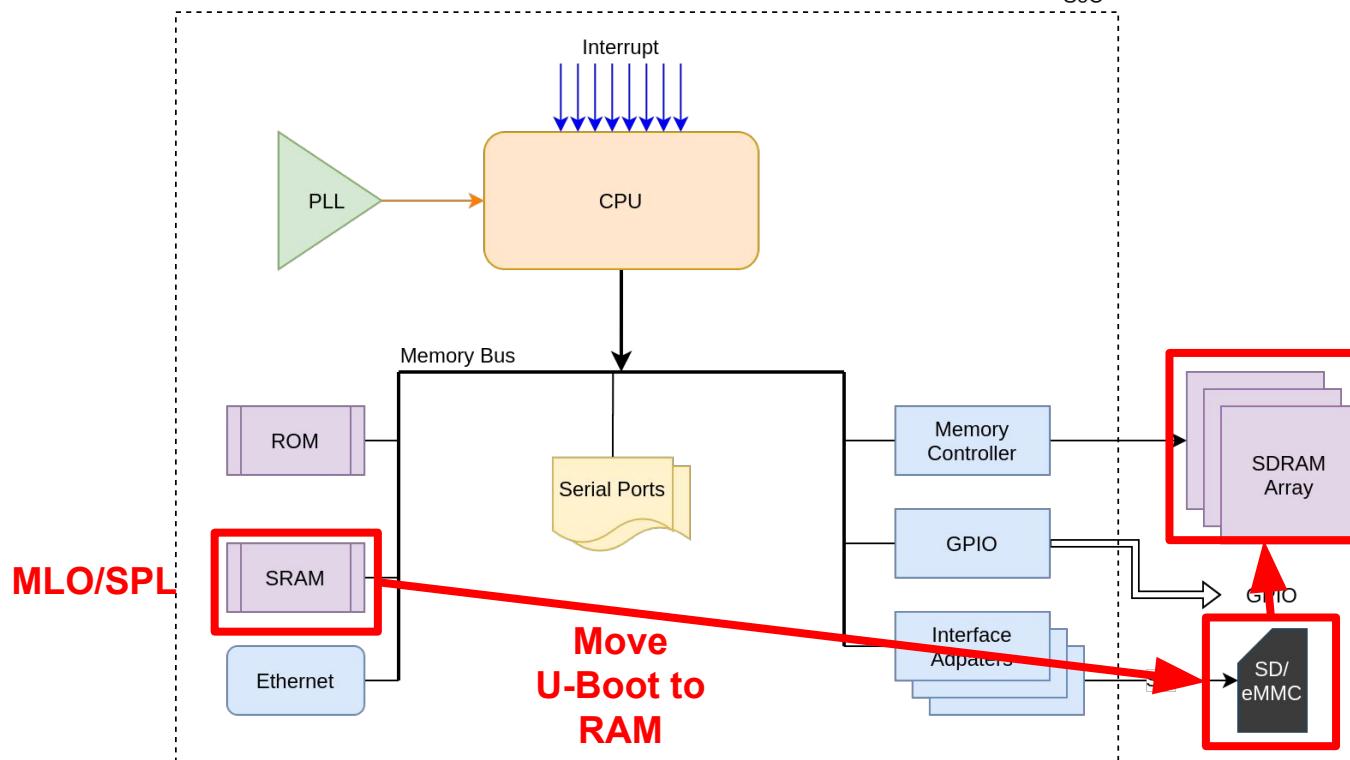
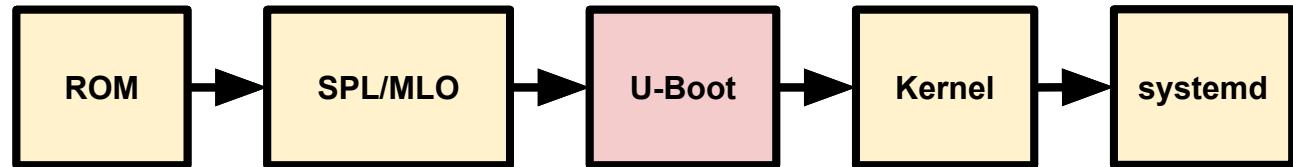
# SoC & Boot-Up



# SoC & Boot-Up

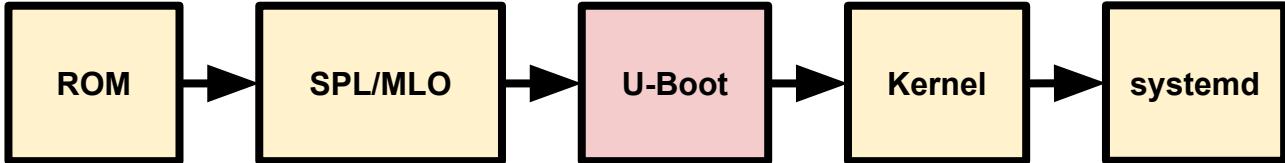


# SoC & Boot-Up



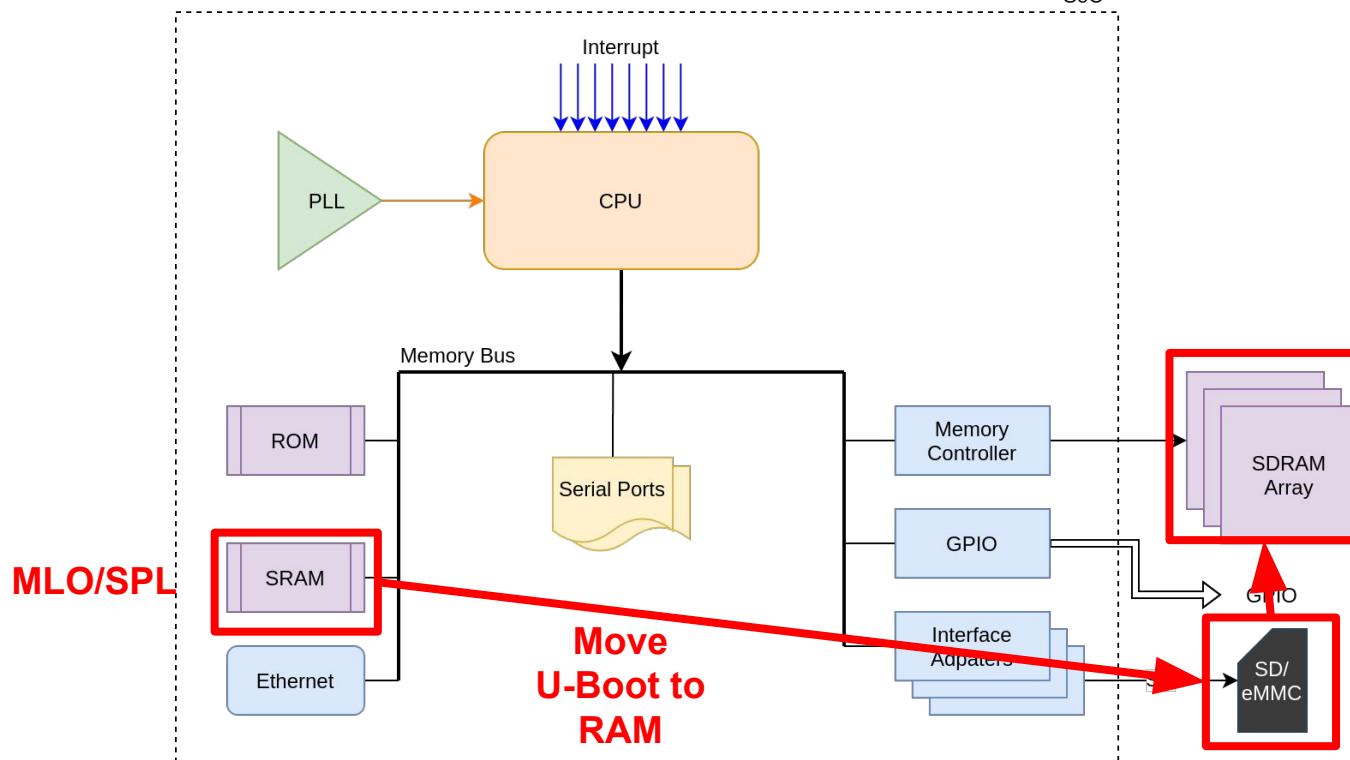
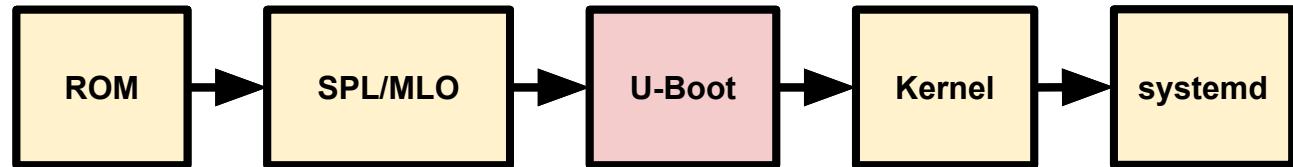
Move  
U-Boot to  
RAM

### 3. U-Boot

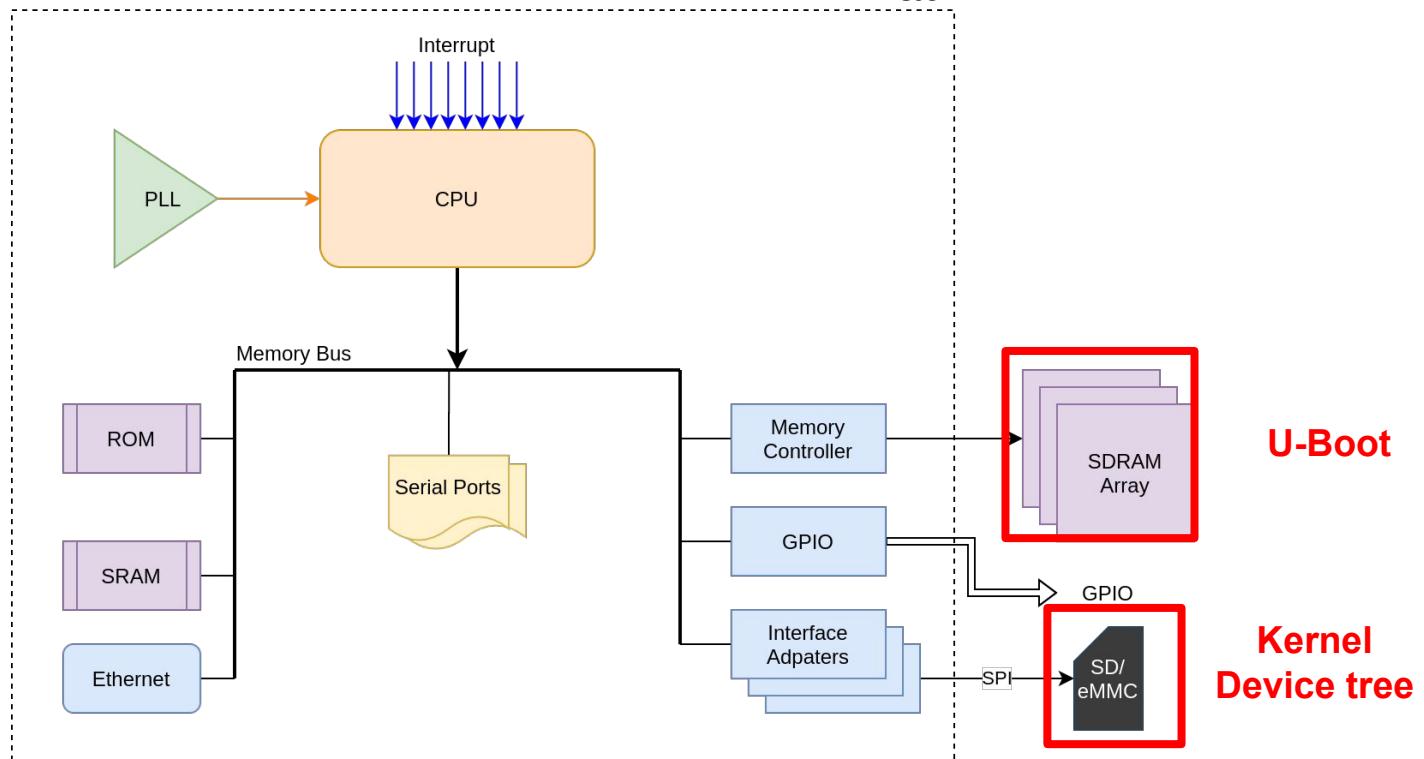
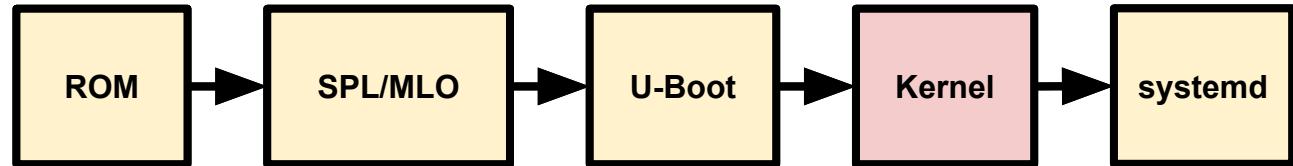


- Universal Boot Loader
- Puts kernel in RAM
- Check out `/boot/vmlinuz`
- Compressed
- `ulmage/zImage`
- Starts kernel
- Provides kernel with device tree
- Configuration file: `/boot/uEnv.txt`
- Note: MLO is actually ‘U-Boot SPL’
  - I.e. MLO is barebones version of U-Boot

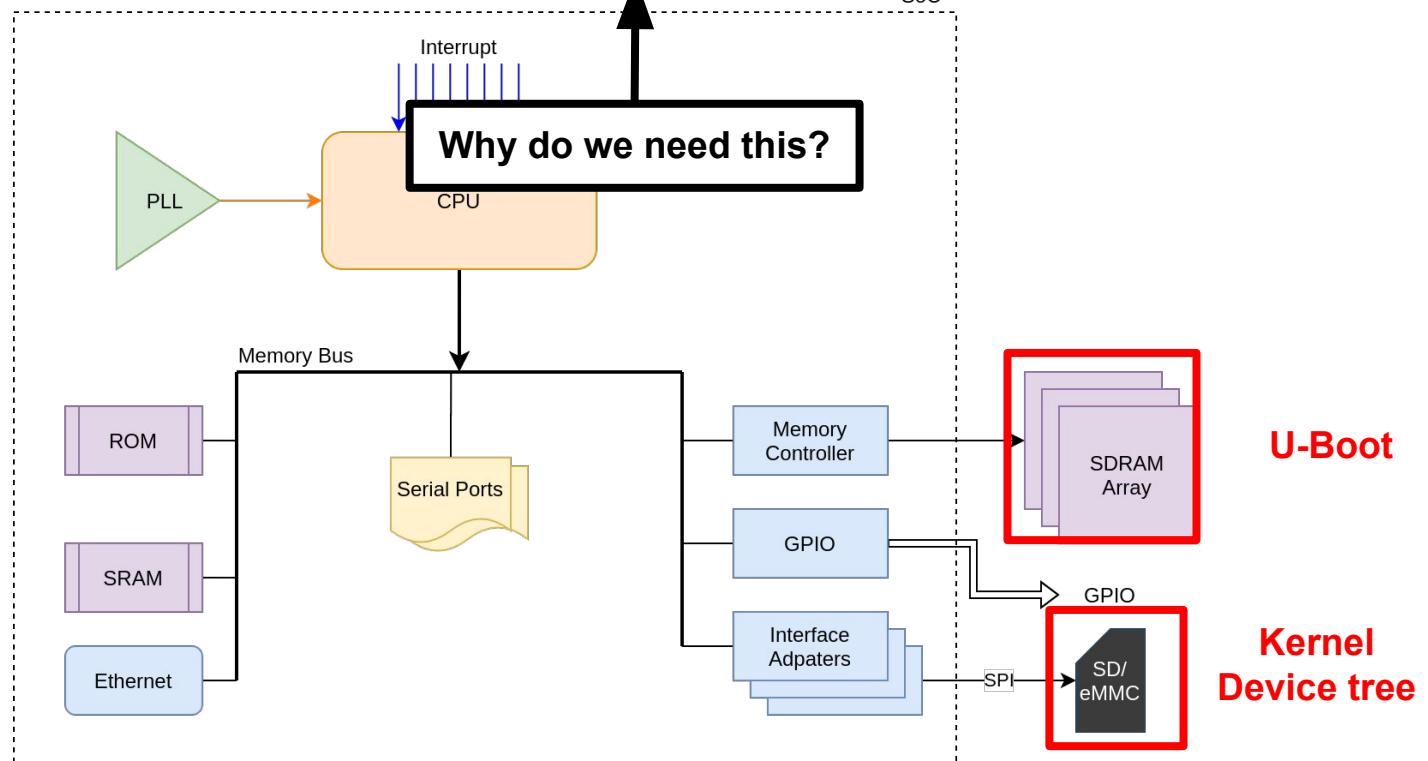
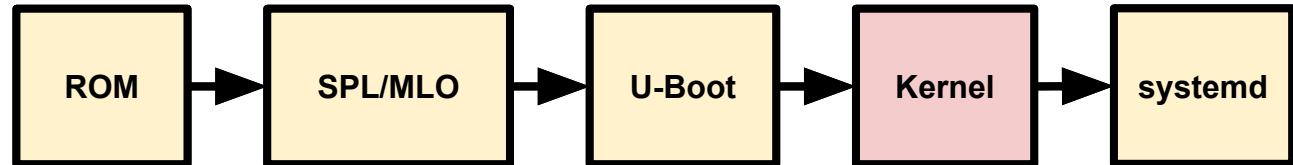
# SoC & Boot-Up



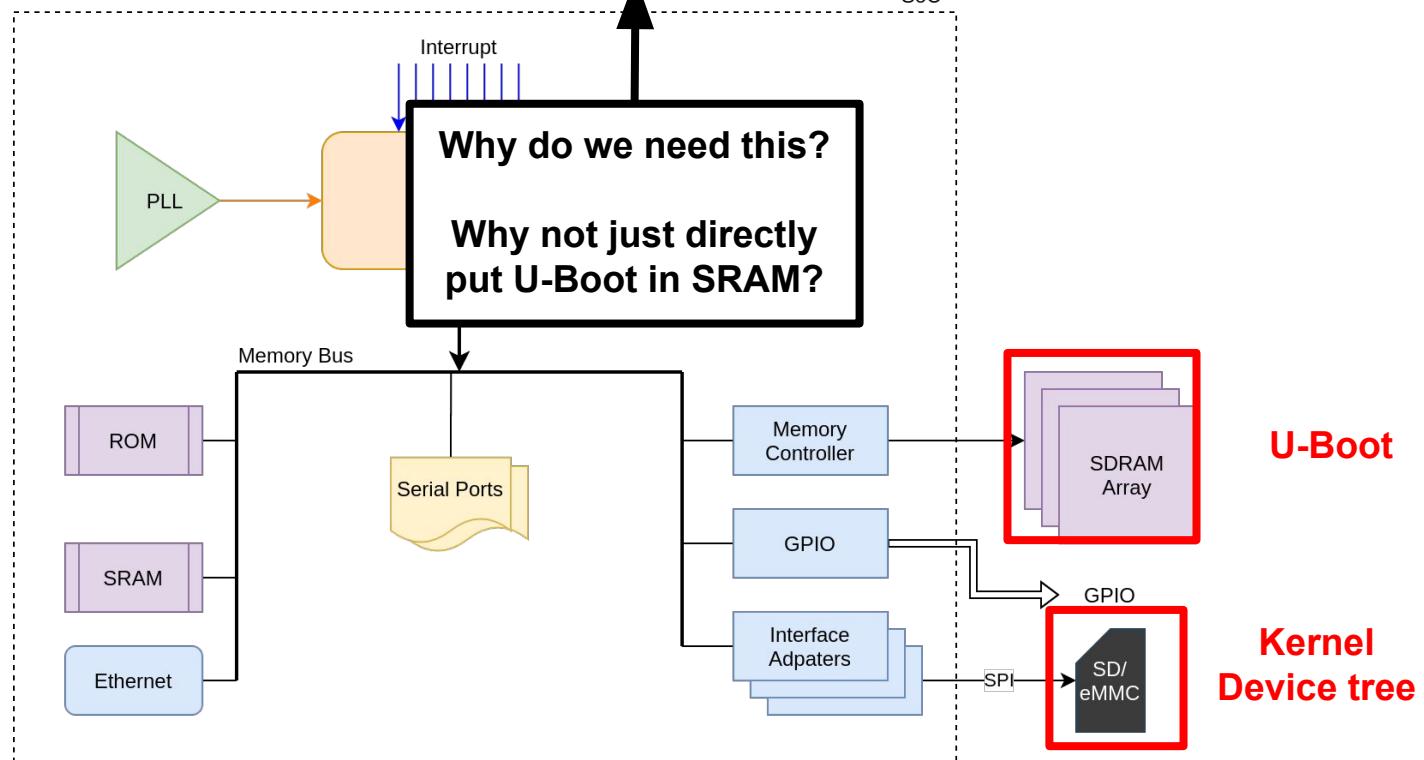
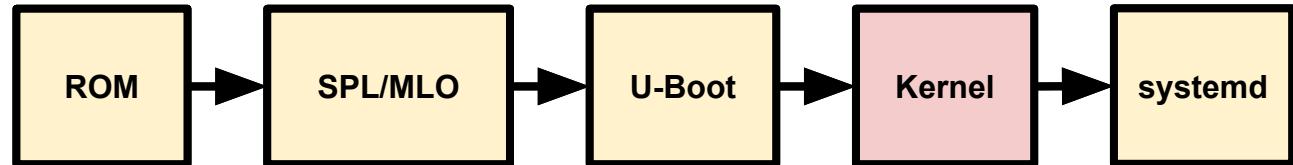
# SoC & Boot-Up



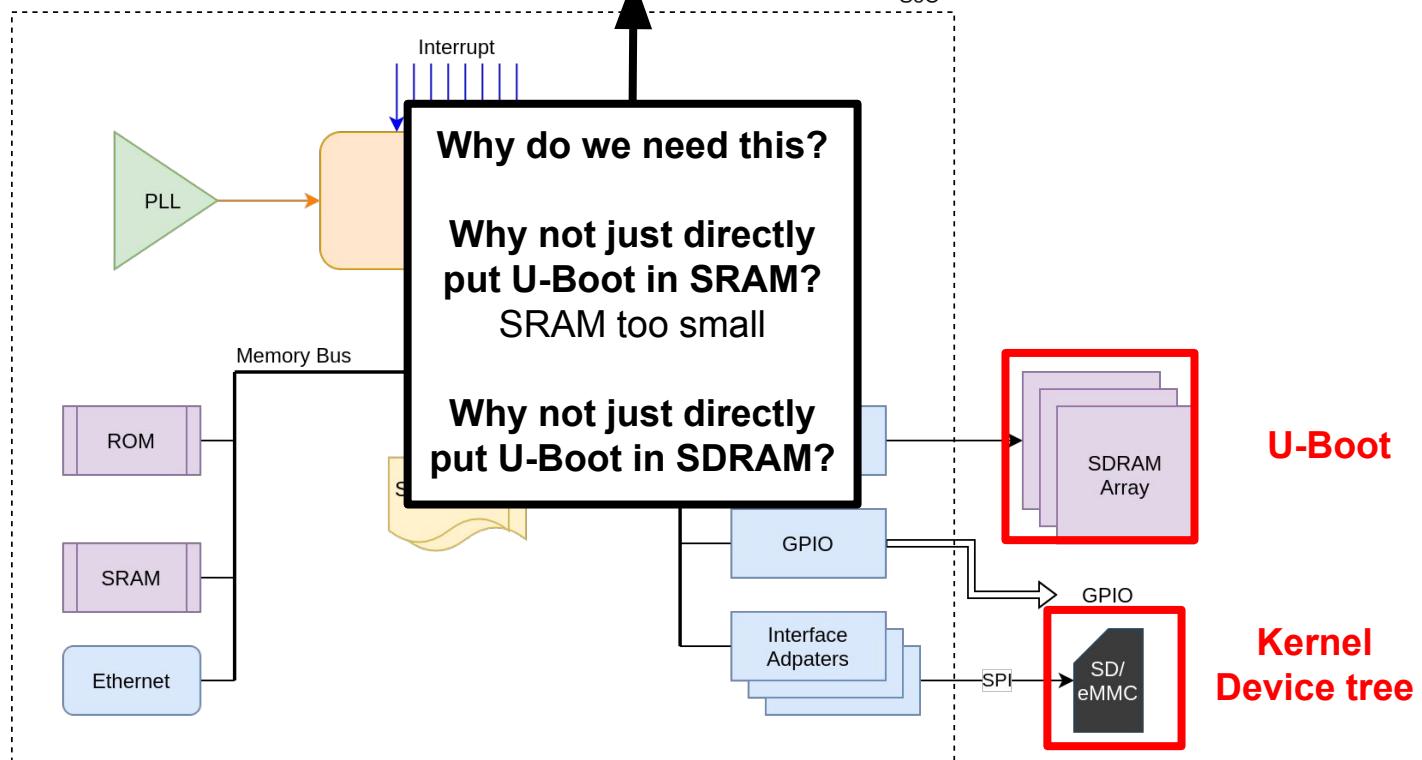
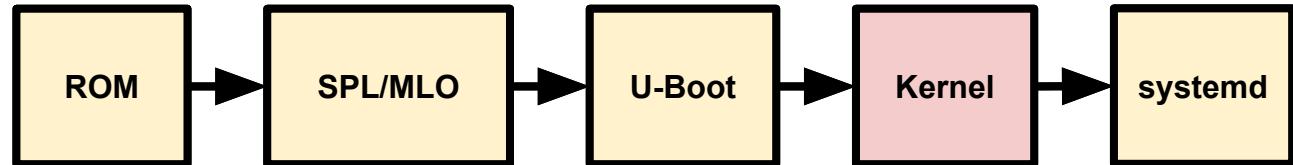
# SoC & Boot-Up



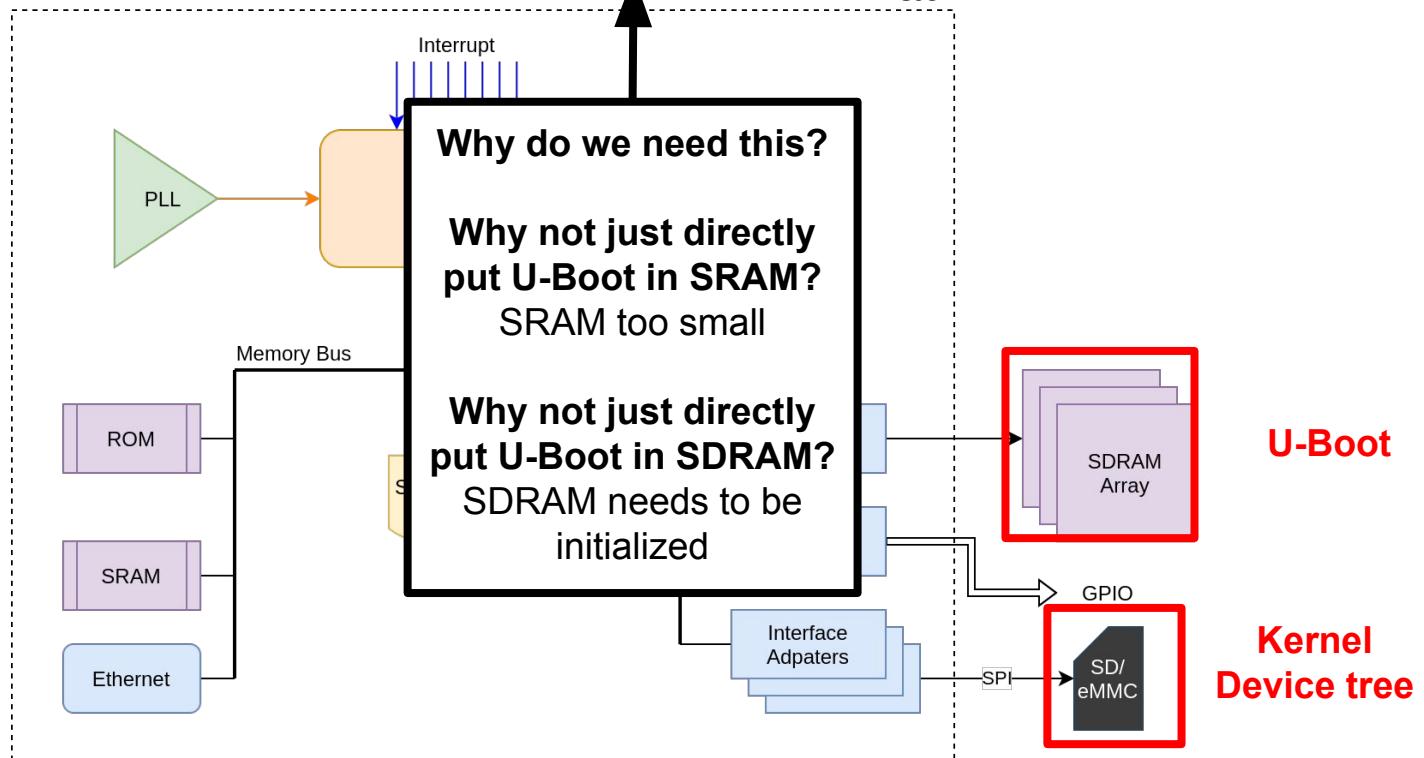
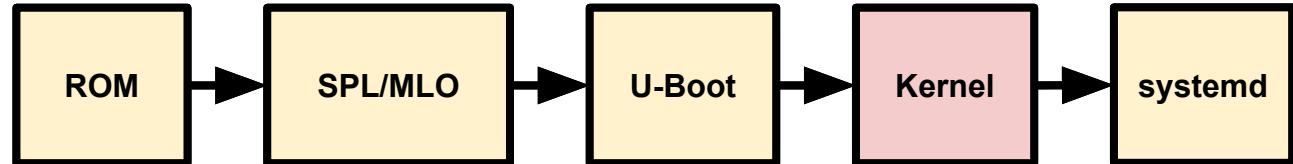
# SoC & Boot-Up



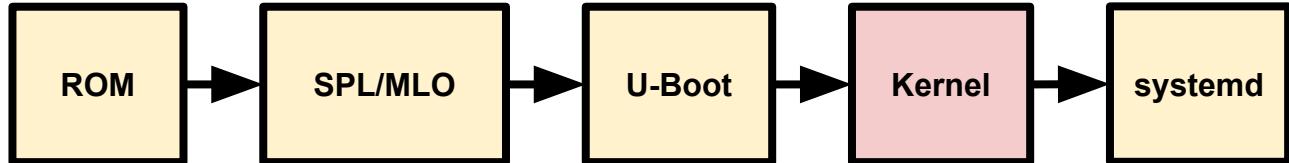
# SoC & Boot-Up



# SoC & Boot-Up

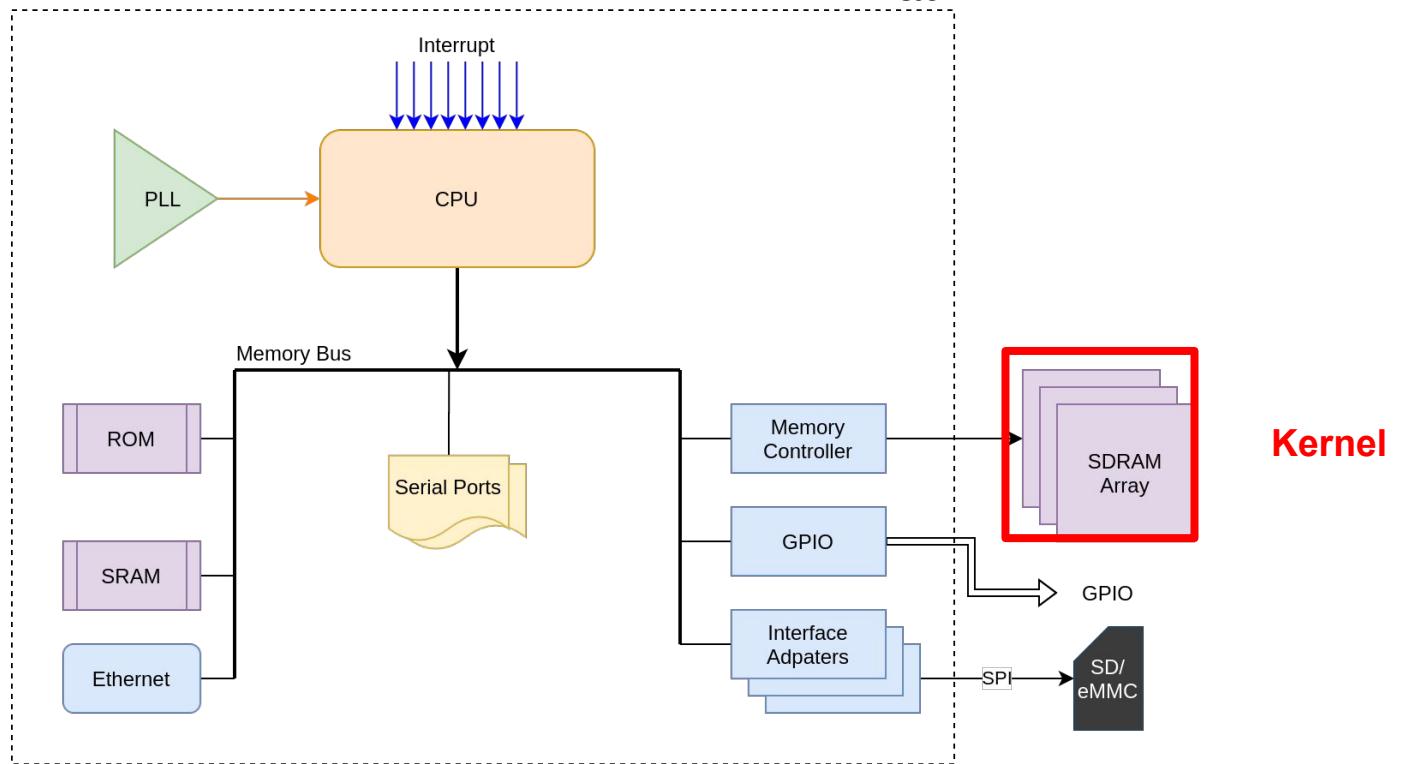
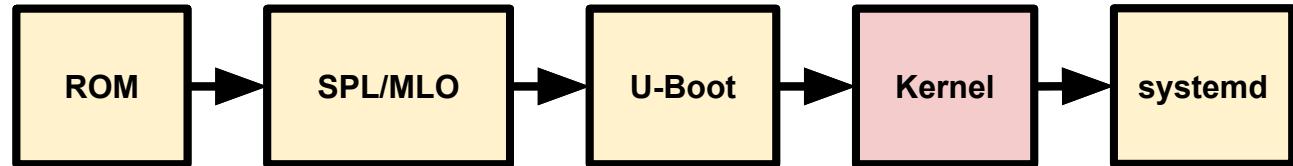


## 4. Kernel

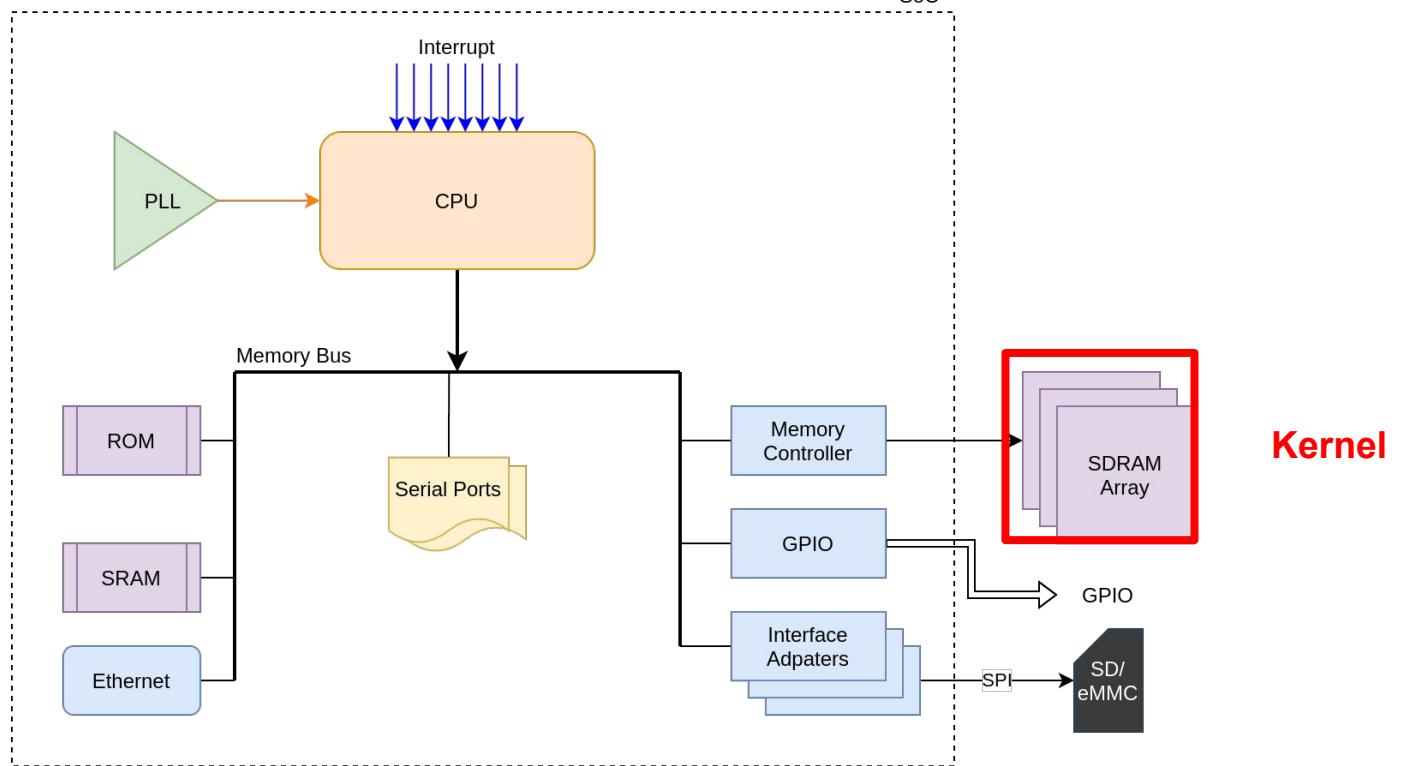
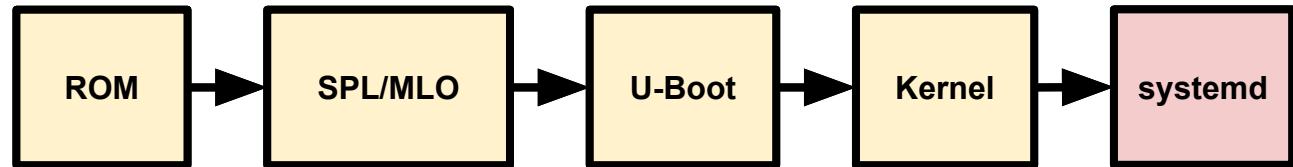


- Automatically decompresses (if needed)
- Receives device tree
  - Loads drivers
  - Activates devices
- Mount root fs
- U-Boot does not *\*call\** the kernel, *\*passes\** control to it

# SoC & Boot-Up

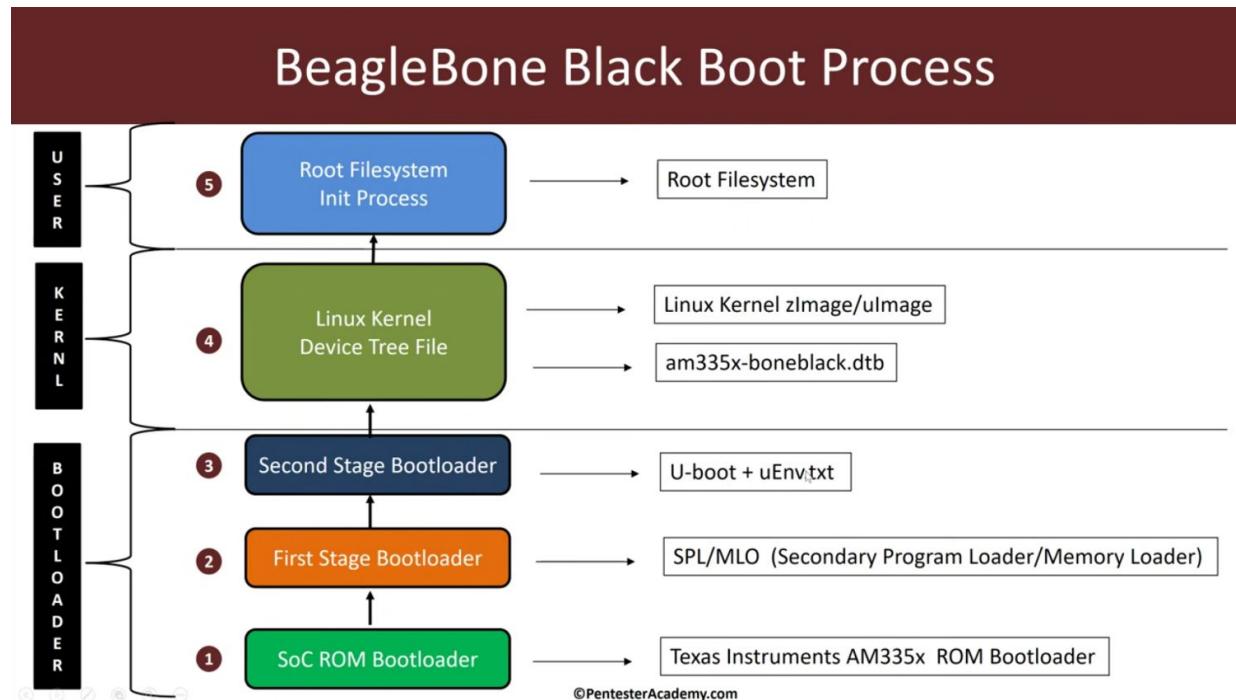


# SoC & Boot-Up

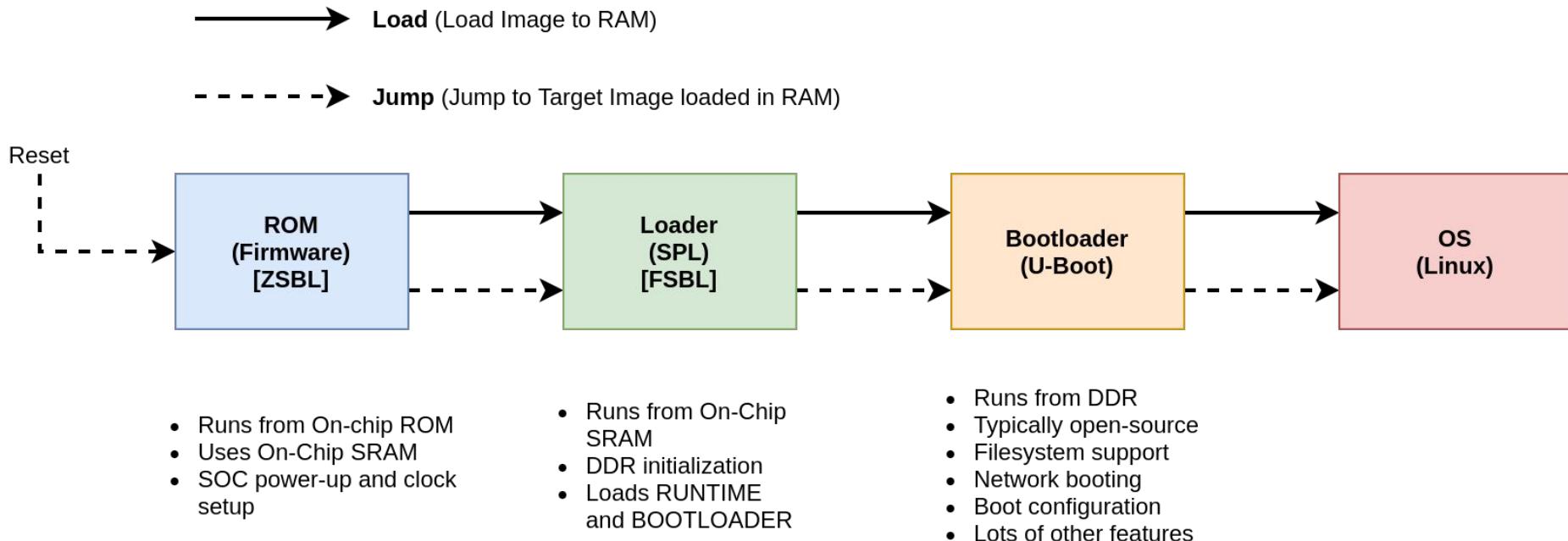


Kernel

# BBB Boot Process (Slide From Pentester Academy TV)



# Boot Process For BeagleBone Black (OMAP)

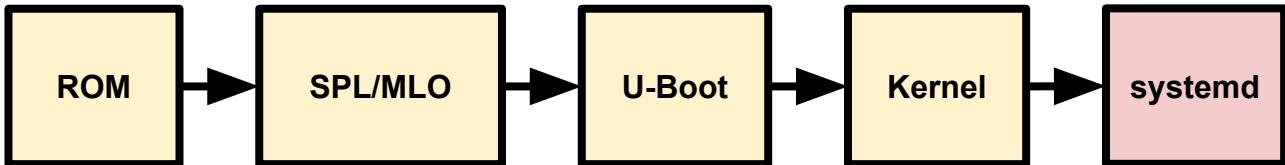


# **init process: systemd**

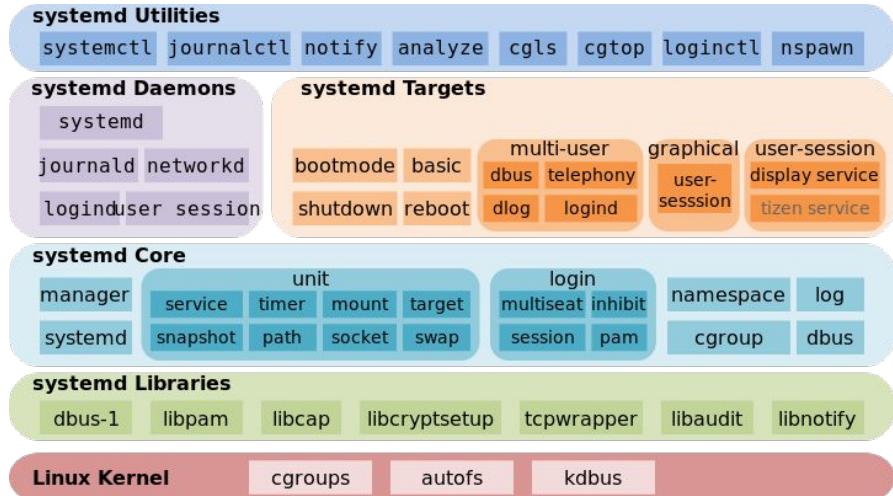
# Daemons

- Processes
- Run in the background
- Non-interactive
- **Service** - daemon superset

## [ ⏪ ] systemd

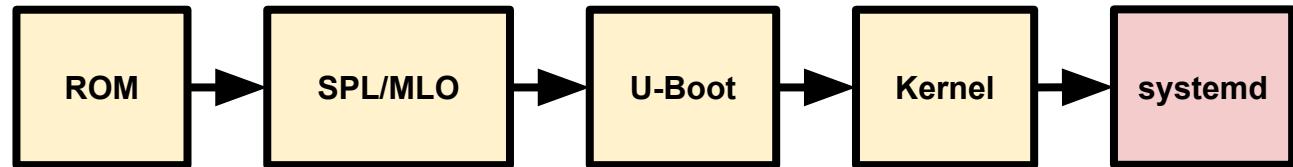


- System & service manager
- d stands for daemon (in Unix fashion)
- Init process (daemon) PID 1
  - Universal common ancestor of all processes
- Parallelism
- *Controversial*

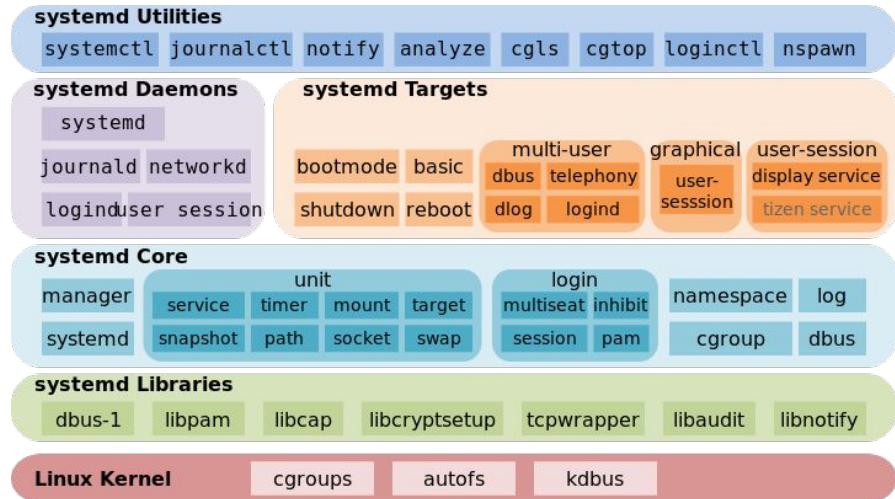


Carla Schroder, "Understanding and Using Systemd". URL:  
<https://www.linux.com/training-tutorials/understanding-and-using-systemd/>

[ ⟲ ] **systemd**



“**systemd** is a Linux **initialization system** and **service manager** that includes features like **on-demand starting of daemons**, mount and automount point maintenance, snapshot support, and **processes tracking** using Linux **control groups**. **systemd** provides a **logging daemon** and **other tools** and **utilities** to help with common system administration tasks.”



Carla Schroder, “Understanding and Using Systemd”. URL:  
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# **Lennart Poettering: One Objective of systemd**

[Lennart is the initial author of systemd]

“Unifying pointless differences between distributions”

*More to come...*