Xiao Wei

SCU-3155, 500 El Camino Real (612)-212-1825 shawnweix@gmail.com
Santa Clara, CA 95053 http://django-website.herokuapp.com

OBJECTIVE:

Looking for internship that can involve ASIC/FPGA test &verification or VLSI design &test.

TAKEN COURSES:

- Linear Control System, Communication, information Security Management
- **VLSI Design I, VLSI Design II**, VLSI Physical Design
- **Design For Testability**, **Modern Time Analysis**

SKILLS:

- Solid understanding of VLSI fundamentals (**CMOS integrated circuit, Combinational Logic, Sequential Logic, RTL, Memory**)
- Solid understanding of Circuit Analysis (**Static Timing Analysis, SSTA, Timing Analysis Algorithm, Placement and Routing Algorithm, DFT, ATPG, BIST, memBIST, Scan Test, Memory Test**)
- Good understanding of Circuit Design (Combinational Logic circuit design, Sequential Logic circuit design, Static Logic circuit design, Dynamic Logic circuit design, LFSR, **Memory Design**)
- Software: **Mentor Graphics IC studio**, **Synopsys VCS**, **Matlab**, eclipse, Visual C++, Multisim, Prote199, Altium Designer, Auto CAD, Lattice Diamond.
- Programming language: **Verilog HDL**(proficient), **C++**(proficient), **Matlab** (proficient), C (prior experience), Java (prior experience), and Assembly (prior experience).

PROJECTS:

- 0.35um Gate-level COMS logic circuit design, testing &simulation &layout
  Designed 4bit Dynamic CLA Adder & 4bit 6T SRAM including surrounding circuitry.
  Sizing transistors and implemented circuits of certain function.
  Given test patterns, verify its functionality. Based on Signal Waveform to do circuit analysis. Using schematic to do layout under software Mentor Graphics IC studio.
- RISC ALU design
  Based on ALU architecture and specification to design, implement, test and verify using Verilog HDL complier VCS. Routing analysis and timing analysis using Lattice Diamond.
- Linear system analysis (including controllability, observability, stability and feedback control laws design)
  Based on system states equations to solve the system under Matlab.

EDUCATION:

Sep.2007 – Jun. 2011: Nanjing University of Science & Technology in P. R. of China

- Received BS Degree in Electronics

Jan.2013 – now: Santa Clara University

- Major: Electrical Engineering, focusing on Digital VLSI Design & Test
- Expecting a Master's Degree in Electronics in 2014