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Microprocessors and Assembly Language
CSE 311

8086 Pin Configuration

8086 works in two operating modes. These are

1. Minimum Mode
2. Maximum Mode

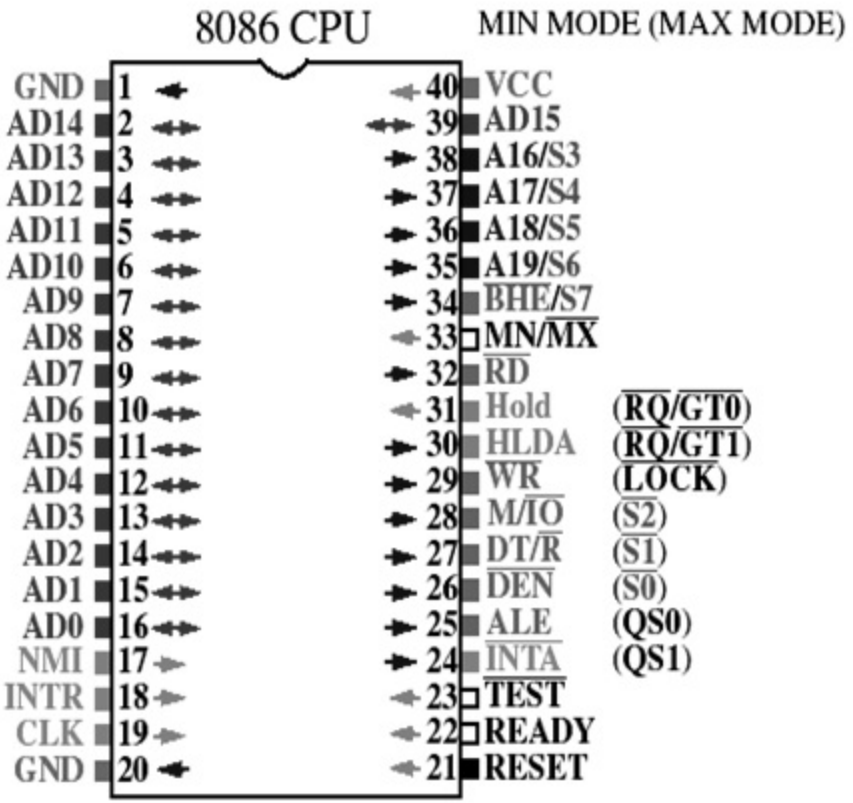
The requirements for supporting minimum and maximum 8086 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the 8086 is equipped with a pin (MN/$\overline{MX}$) which defines the system configuration.

The definition of a certain subset of the pins changes dependent on the condition of the pin. When MN/MX pin is strapped to GND, the 8086 treats pins 24 through 31 in maximum mode. An 8288 bus controller interprets status information coded into S0, S2, S2 to generate bus timing and control signals compatible with the MULTIBUS architecture. When the MN/MX pin is strapped to VCC, the 8086 generates bus control signals itself on pins 24 through 31

Minimum mode is cheaper since all control signals for memory and I/O are generated by the microprocessor. This mode is also called uniprocessor mode.

Maximum mode is designed to be used when a coprocessor (8087) exists in the system. This requires an external bus controller: The 8288 Bus Controller. This is multiprocessor mode.

8086/88 Pinout



Pin Configuration in Maximum Mode

$\overline{\text{MN}}/\text{MX}$: CPU works in minimum mode when this pin is tied to VCC when connected to GND then it is will work in maximum mode.

AD15-AD0: Multiplexed address/data bus. During first clock of a bus cycle this multiplexed bus acts as address bus and for the rest of the periods of bus cycle acts as data bus.

A19/S6-A16/S3: High order 4 bits of the 20-bit address are multiplexed with status bits S6-S3.

S3, S4: These lines are decoded as follows as selector of a particular segment.

A17/S4	A16/S3	Function
0	0	Extra segment
0	1	Stack Segment
1	0	Code or no segment
1	1	Data Segment

S5: This gives the current status of IF flag.

S6: This indicates that 8086 has control on bus. During hold acknowledgement 8086 tri-states this pin allowing another bus master to get control on system bus.

BHE/S7: BHE (Bus High Enable) is active during the first clock cycle of an instruction execution and for the rest of the periods S7 status is given but this has not been assigned any meaning.

INTR: This pin receives maskable interrupt request.

NMI: This is nonmaskable interrupt input pin.

RESET: This pin is system reset signal. This signal must be high at least for four clock cycles. It causes 8086 to initialize its internal registers DS, SS, ES, and IP and flags to zero and CS to FFFFh. Thus after a reset 8086 starts to fetch instruction from FFFF0h.

CLK: This pin provides the basic timing of 8086. This receives clock pulses from 8284 external clock generator.

Ready: This is an input pin and CPU receives an acknowledgment from memory or I/O device that it can complete the current bus cycle. The activation of ready pin depends on the operating speed of the peripherals.

$\overline{\text{TEST}}$: This pin is used in conjunction with the WAIT instruction causing CPU to enter in a idle state until a low is seen on this pin.

$\overline{\text{RD}}$ (READ): Activates read operation from memory or an I/O device.

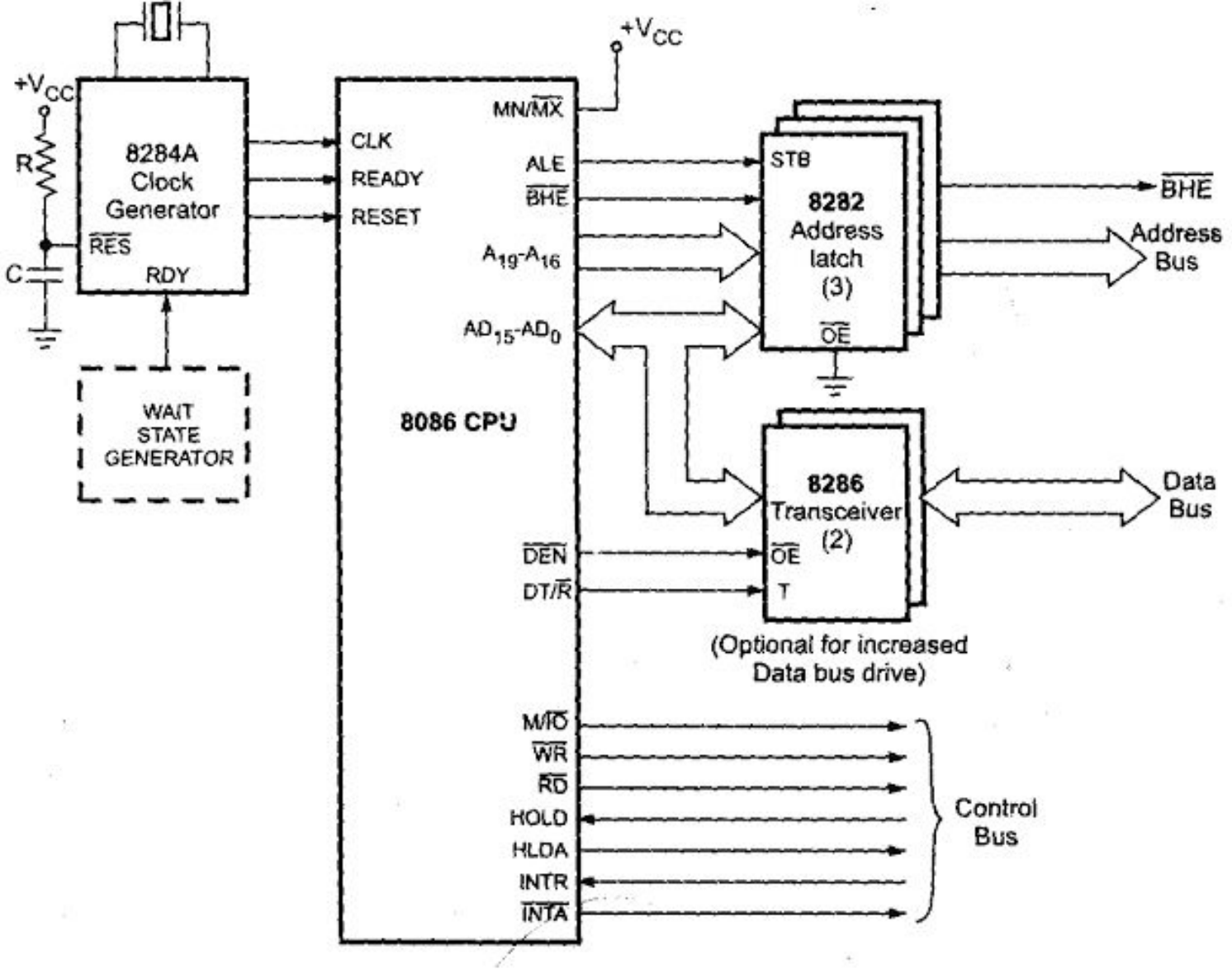
Pins 24-31 in minimum mode

$\overline{DT}/R$ (Data Transmit/Receive): 8086 outputs on this pin to give the direction of data flow for data bus transceiver 8286 transmitting/receiving data.

$\overline{DEN}$ (Data bus Enable): Activates data bus transceiver 8286 to inform that CPU is ready to send or receive data.

ALE (Address latch enable): This pin is used to enable the address latch 8282. When 1, address data bus contains a memory or I/O address.

M/$\overline{IO}$ (Memory/Input/Output): Indicates if address is a Memory or IO address.



8086 Minimum Mode Configuration

$\overline{WR}$ (Write): When 0 then microprocessor is driving data bus to memory or an I/O device. This pin is used in conjunction with M/IO and $\overline{RD}$ pins to specify the type of transfer.

INTA (Interrupt Acknowledgement): Acknowledges the interrupt request.

HOLD: This is an input pin used to receive the bus request from bus master. 8086 will not gain the control of bus until this signal is dropped.

HLDA (Hold Acknowledgement): Processor outputs a bus grant signal to the requesting bus master.

Pins 24-31 in maximum mode:

$\overline{INTA}$ ……	QS1
ALE ……	QS0
$\overline{DEN}$ ……	$\overline{S0}$
DT/$\overline{R}$ ……	$\overline{S1}$
M/$\overline{IO}$ ……	$\overline{S2}$
$\overline{WR}$ ……	LOCK
HLDA ……	$\overline{RQ/GT1}$
HOLD ……	$\overline{RQ/GT0}$

QS1, QS0 (Queue Status): Reflects the statue of instruction queue. This status indicates the activity in queue during the previous clock cycle.

QS1	QS0	Function
0	0	No operation
0	1	First byte from queue
1	0	Reset queue
1	1	Subsequent bytes from queue

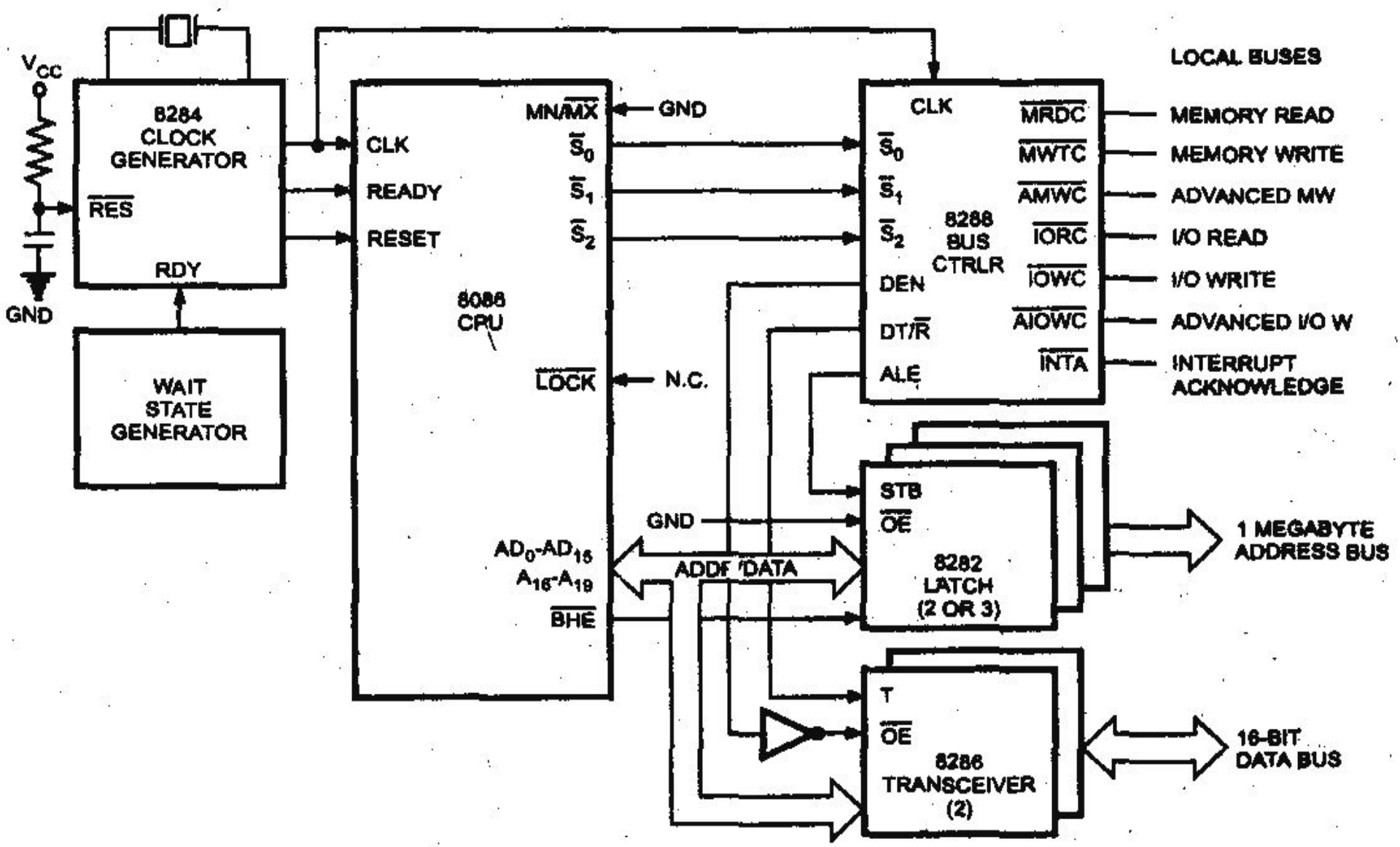
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$(Status): Indicates the type of transfer to take place during a bus cycle. These signals will be decoded by bus controller 8288 as

S2	S1	S0	Decoded O/P
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Memory
1	1	0	Write Memory
1	1	1	Inactive

LOCK: Bus is locked by CPU preventing other bus master from getting control.

RQ/GT0 (Request/Grant): For inputting bus request and outputting bus grants.

RQ/GT1 (Request/Grant): For inputting bus request and outputting bus
grants. RQ/GT0 has higher priority.



8086 in Maximum Mode Configuration