

Class Test 3

Date : 21.03.2021

Time : class hour (start of
class)
(12:30)

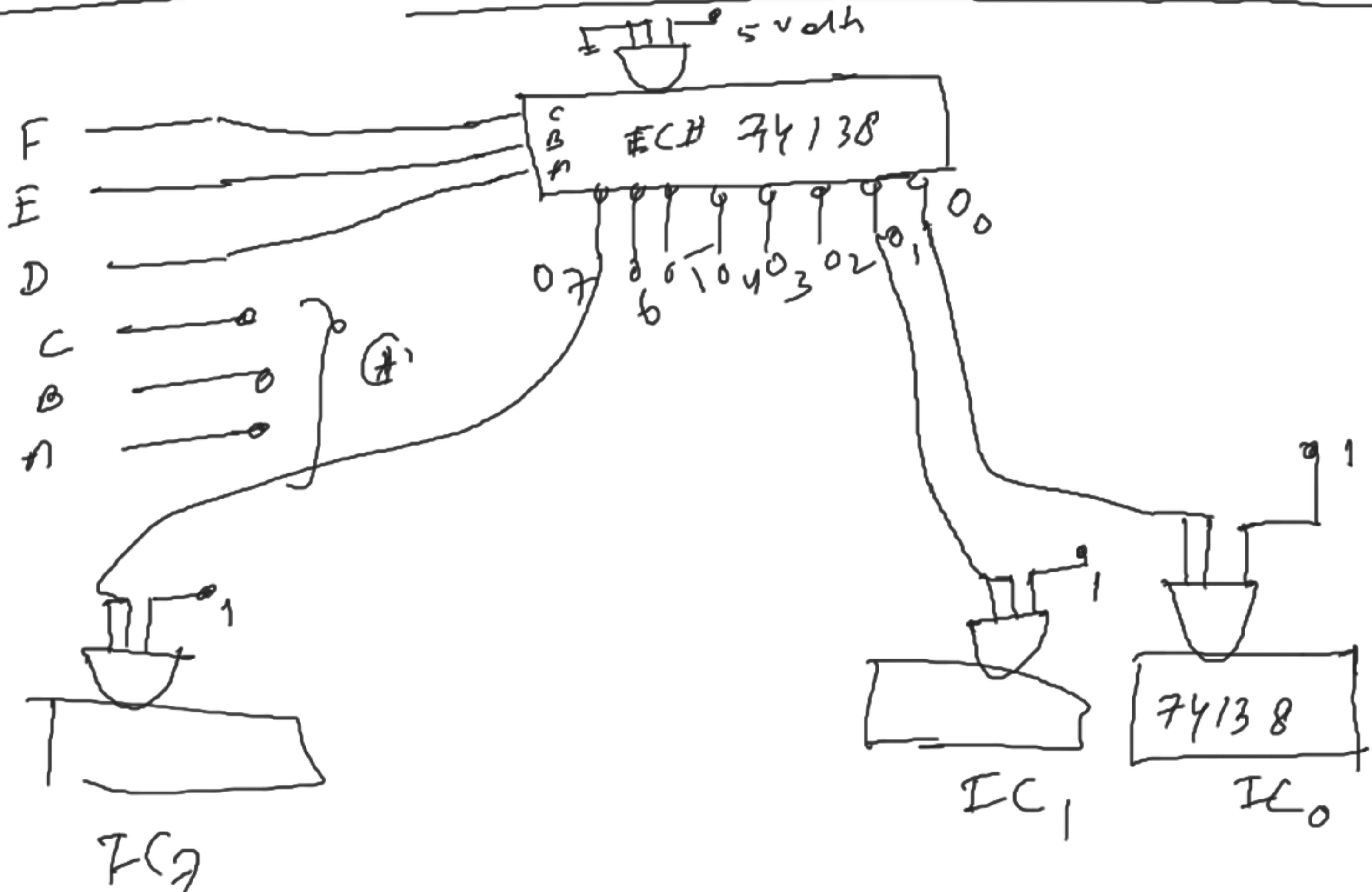
Syllabus : chapter 9 : All

chapter 7:

- synchronous counter
- I C# 74293 # #
- shift counter
 - ring • Johnson

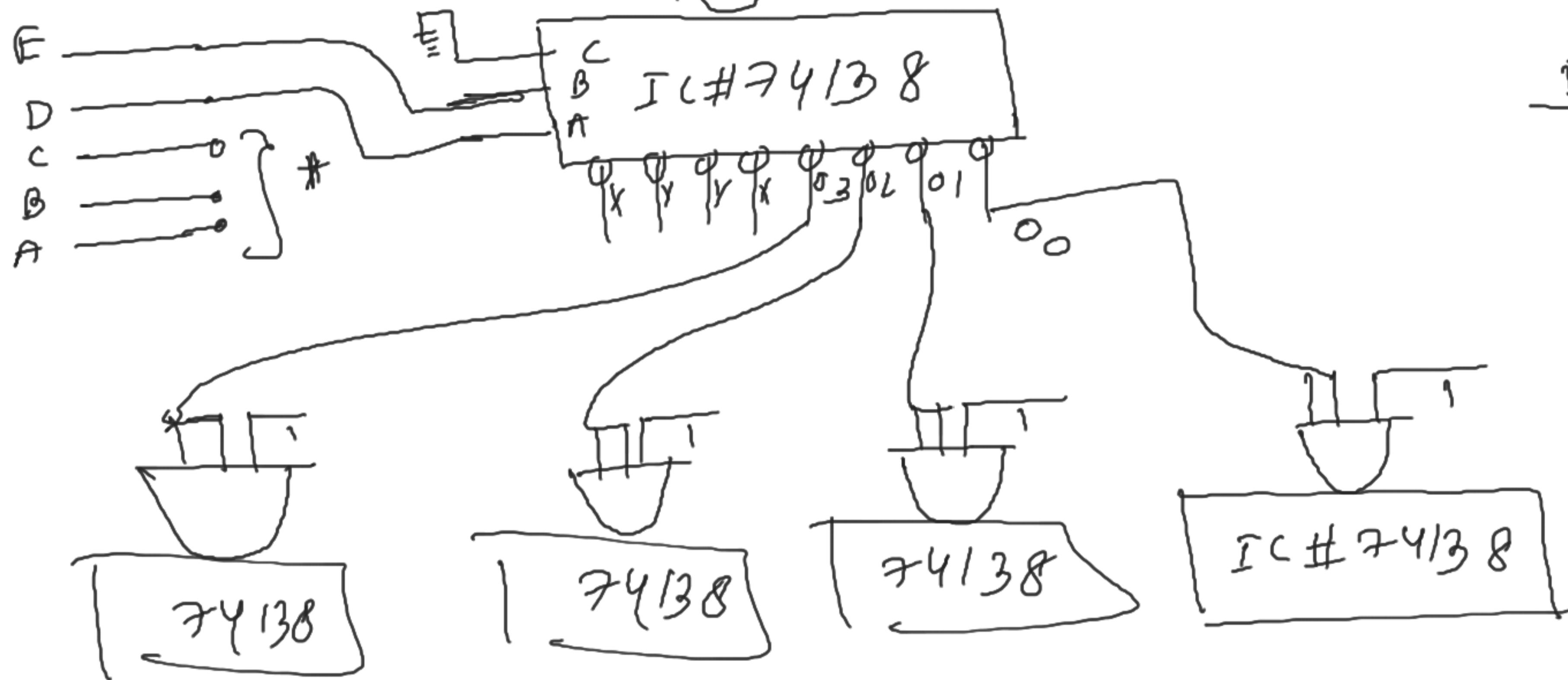
Decoder :

6 lines to 64 lines Decoder



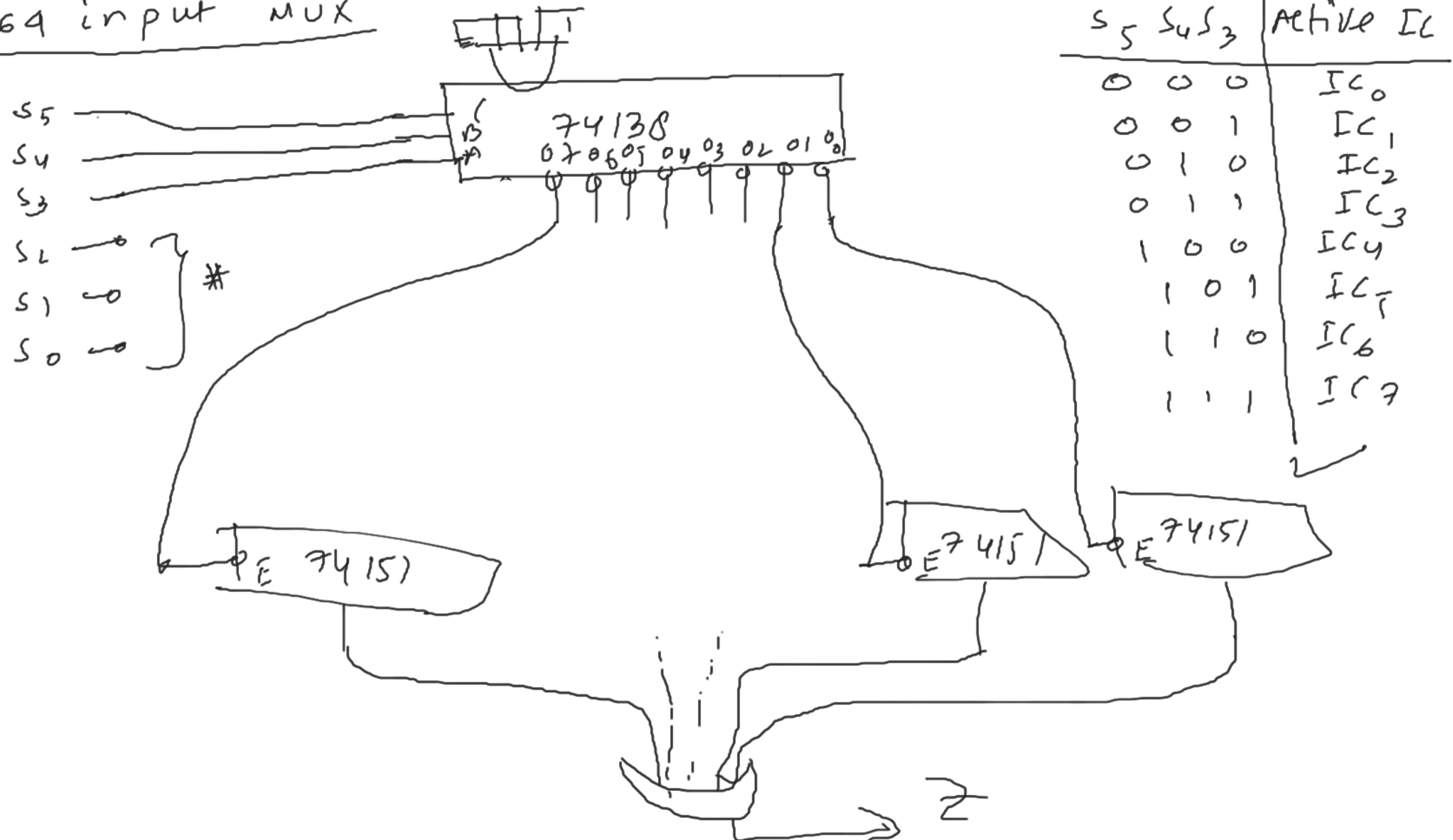
FED	Active IC
0 0 0	IC_0
0 0 1	IC_1
0 1 0	IC_2
0 1 1	IC_3
1 0 0	IC_4
1 0 1	IC_5
1 1 0	IC_6
1 1 1	IC_7

5 lines to 32 lines Decoder

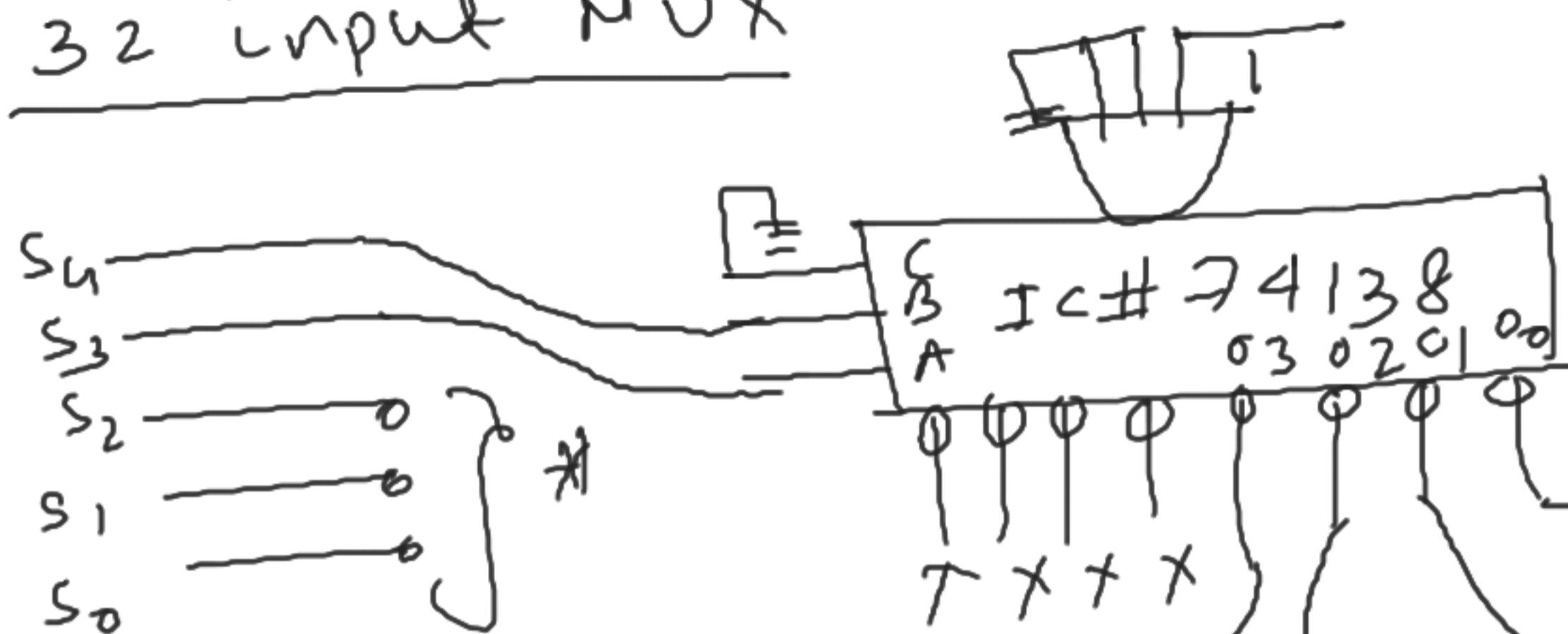


E	D	Active IC
0	0	IC ₀
0	1	IC ₁
1	0	IC ₂
1	1	IC ₃

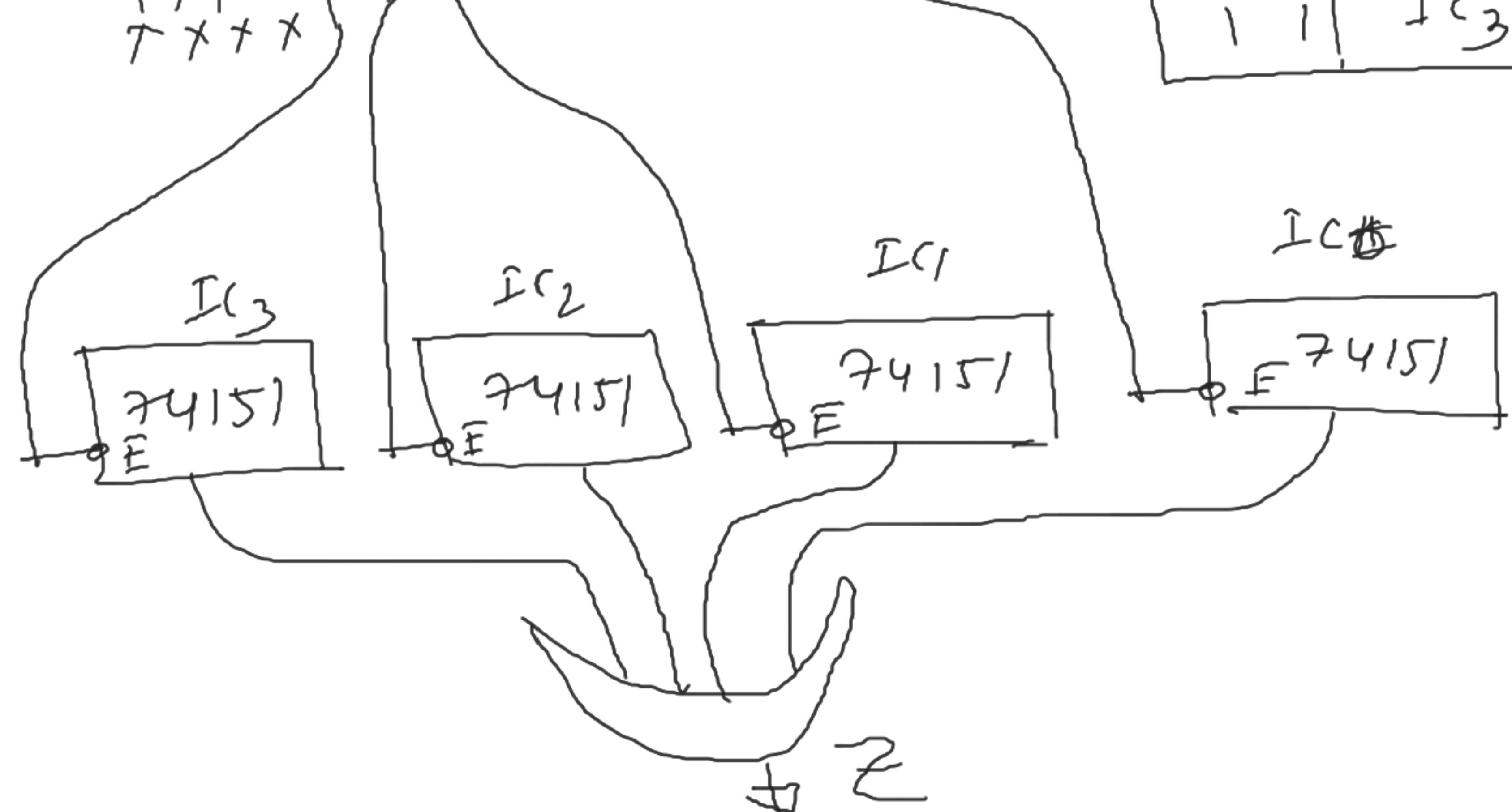
64 input MUX



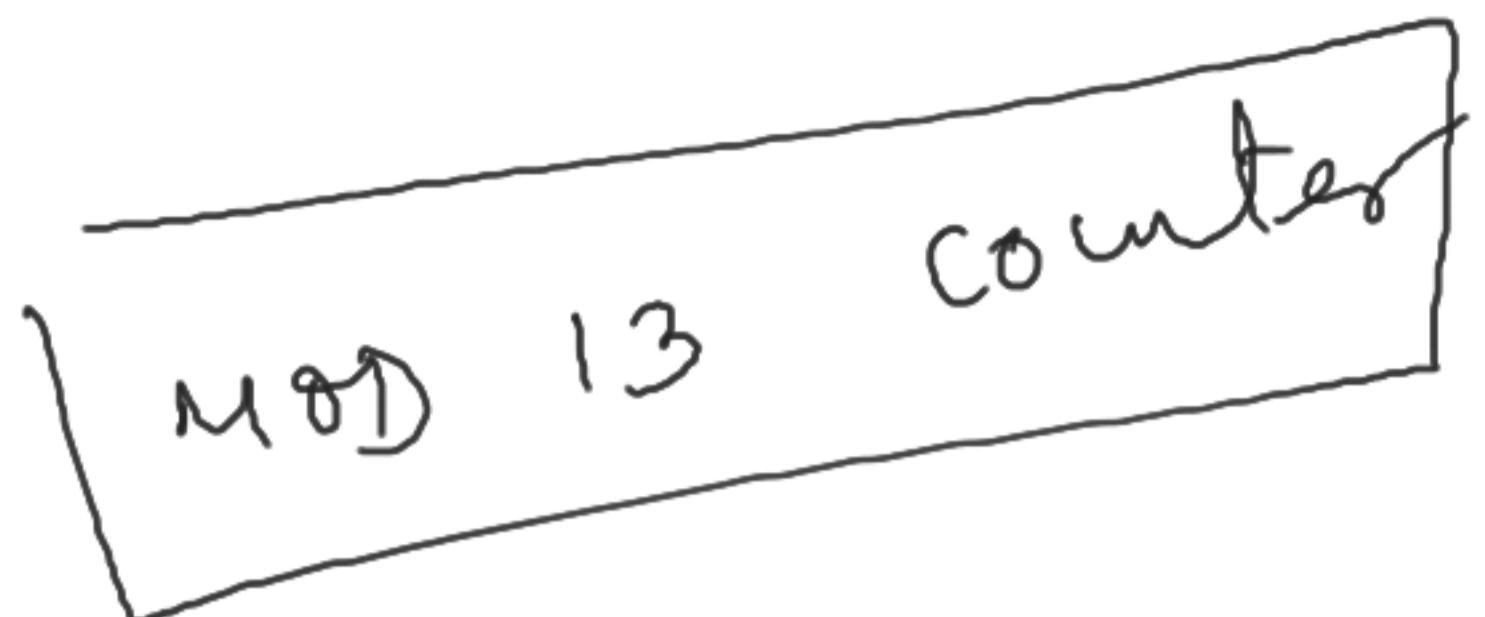
32 input MUX



S_4	S_3	Active IC
0	0	IC ₀
0	1	IC ₁
1	0	IC ₂
1	1	IC ₃

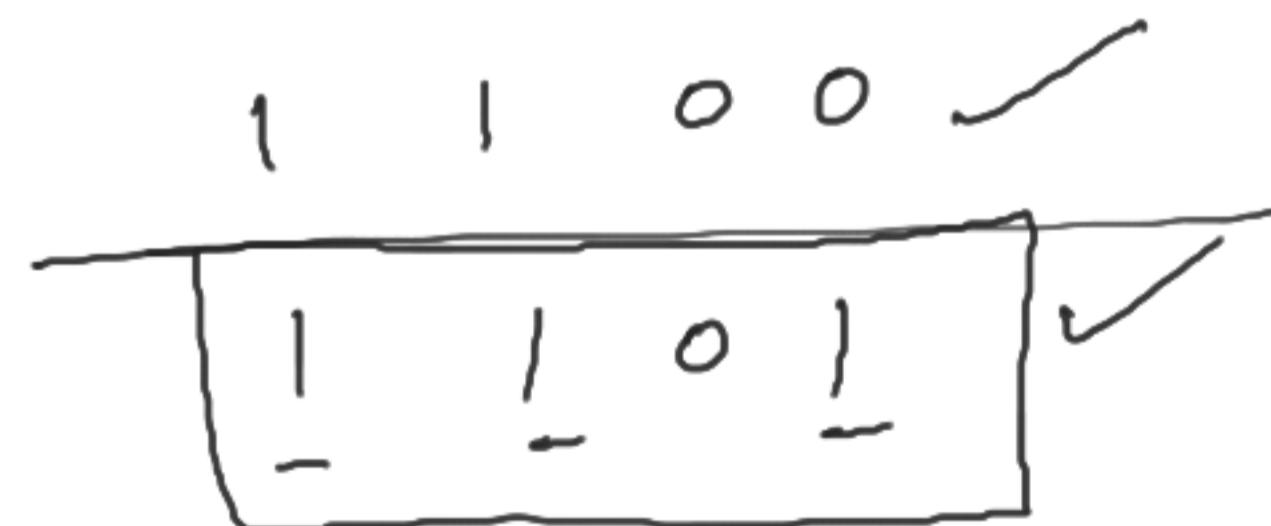
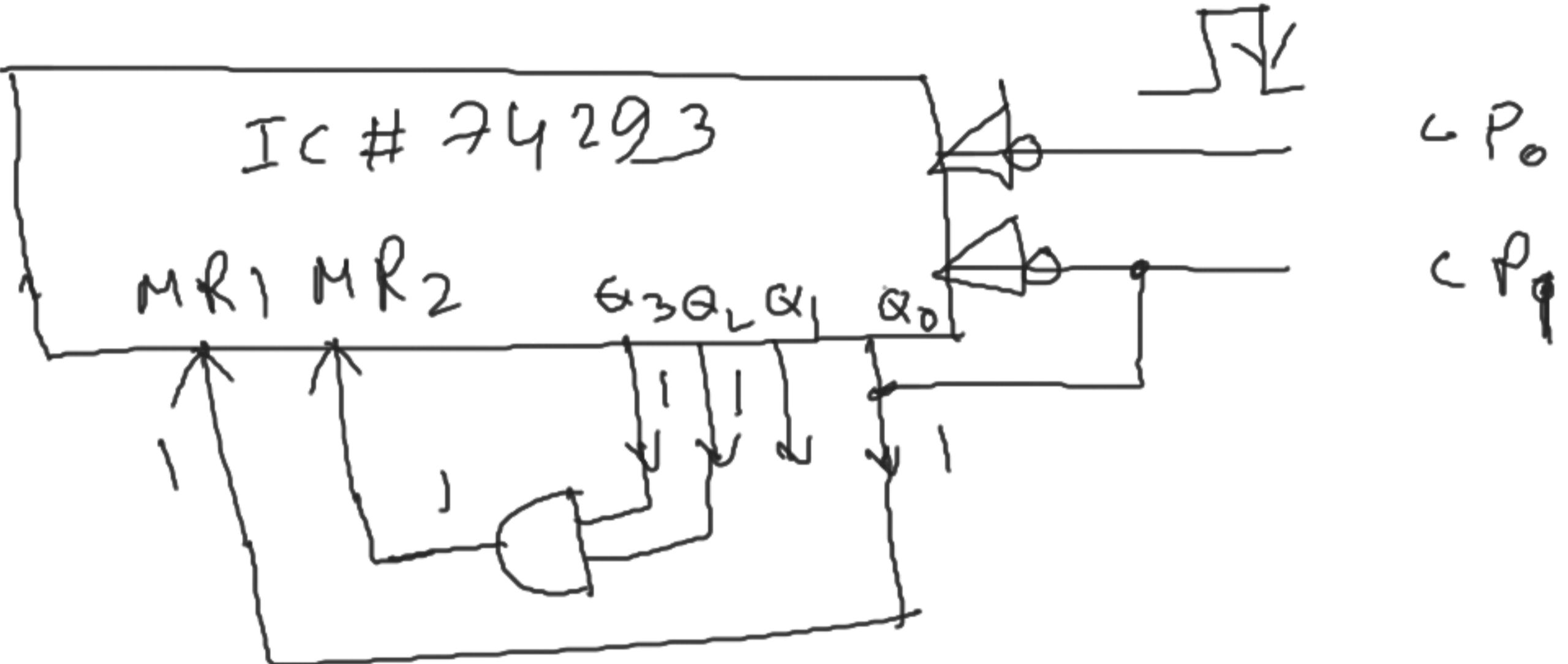


IC # 74293 : (Counter) ✓ PRE = 1



$Q_3 Q_2 Q_1 Q_0$

0 0 0 0

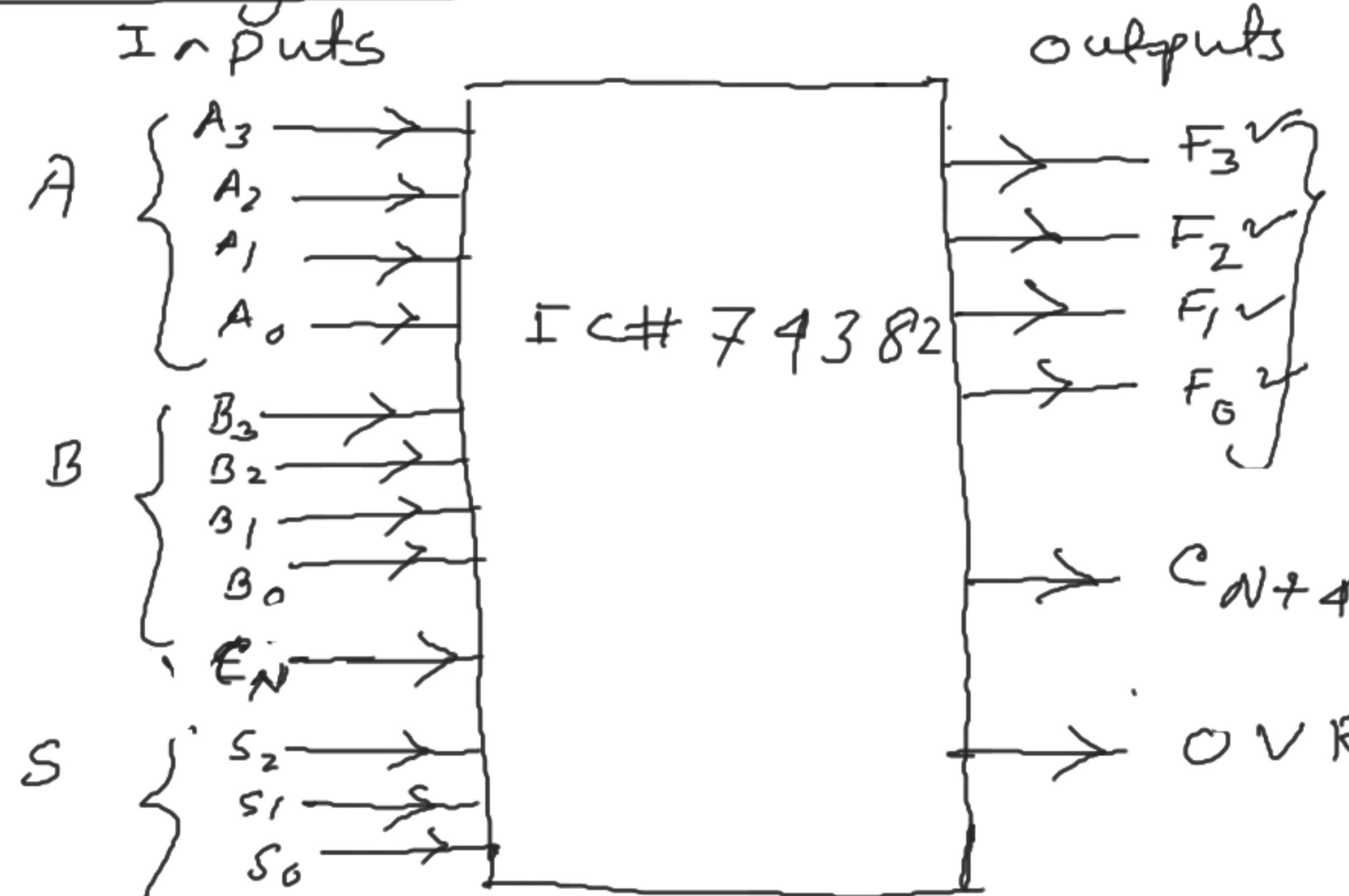


Chapter 6 : ALU Integrated Circuit

4-bit ALU:

IC # 74382 (ALU) : (8 operation)

Block diagram :



Function Table

S ₂ S ₁ S ₀	Operation	Comment
0 0 0	CLEAR	0 0 0 0
0 0 1	B - A	C _N = 1
0 1 0	A - B	C _N = 1
0 1 1	A + B	C _N = 0
1 0 0	A ⊕ B	Ex-OR
1 0 1	A OR B	OR
1 1 0	A AND B	AND
1 1 1	PRESET	1 1 1 1

$A \Rightarrow$ 4-bit input Number | $S \Rightarrow$ Select input
 $B \Rightarrow$ 4-bit input Number | $C_{N+4} \Rightarrow$ carry output
 $c_N =$ carry input | $OVR \Rightarrow$ Overflow

$$S_2 = 0, S_1 = 1, S_0 = 1$$

$$\begin{array}{c} \textcircled{A+B} \\ A = 1001 \\ B = 1110 \\ \hline F = \boxed{0\ 111} \end{array}$$

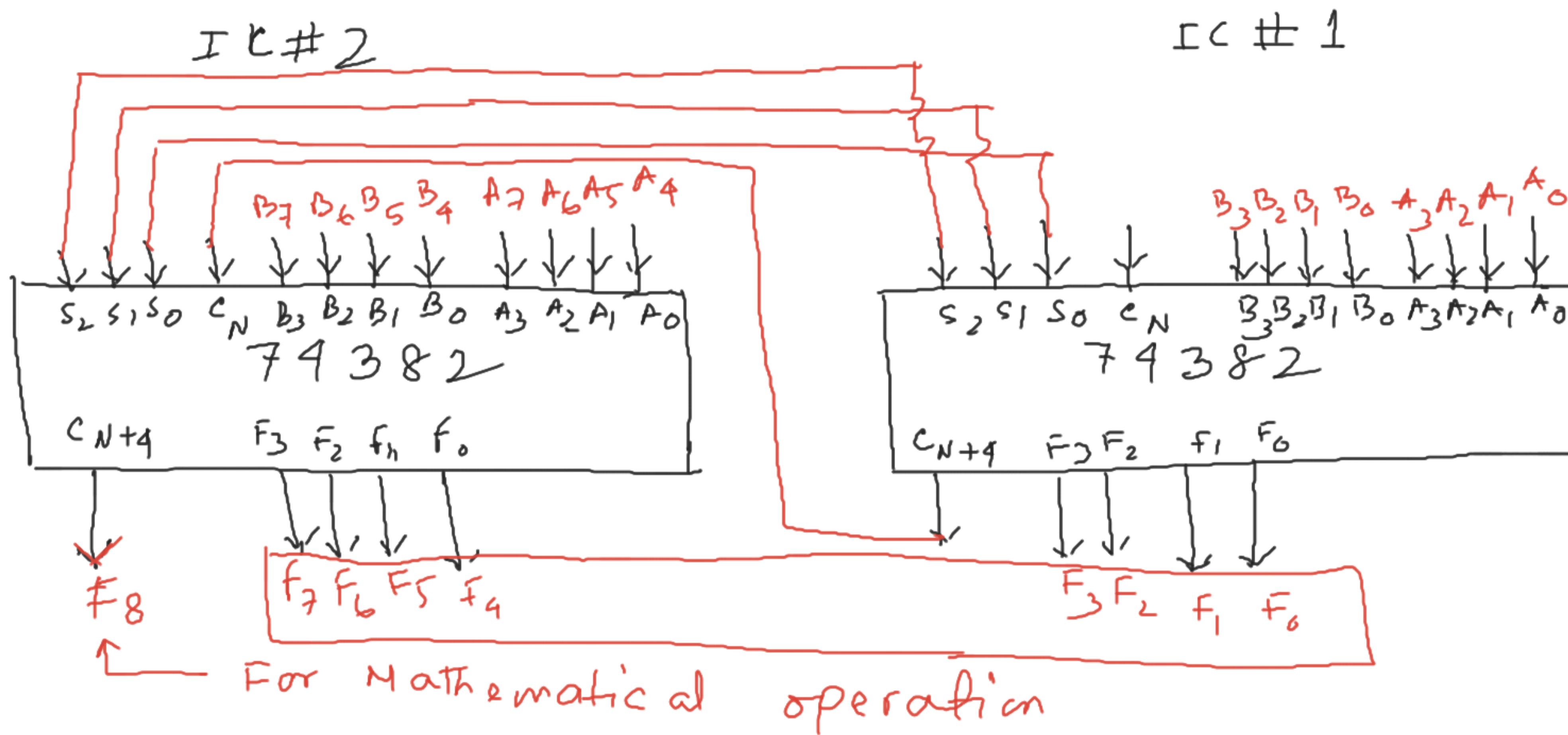
$$C_{N+4} = 1$$

$$S_2 = 1, S_1 = 0, S_0 = 0$$

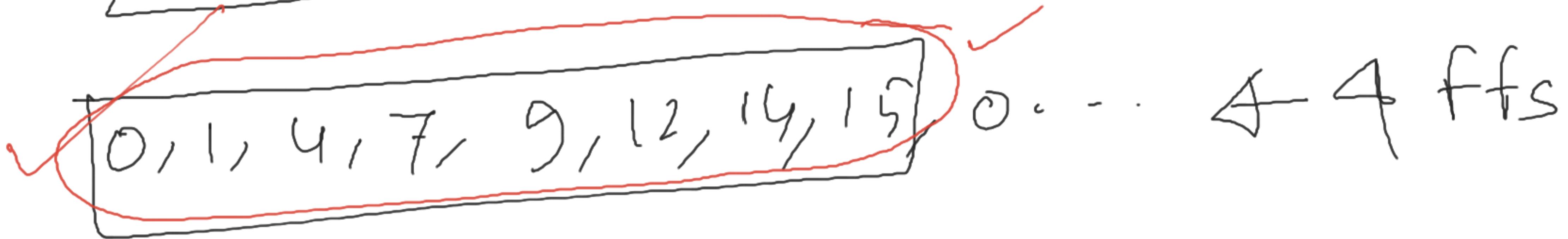
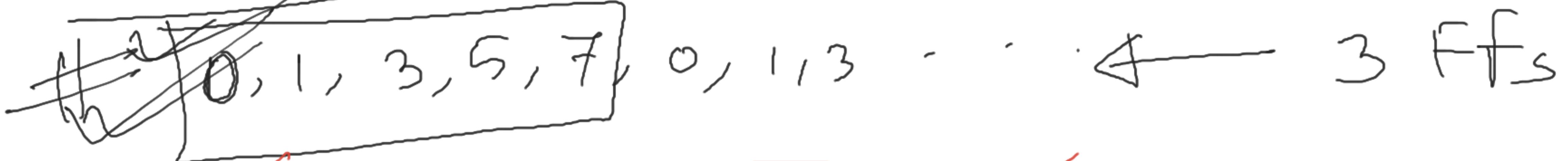
1 0 1 1 1 \Rightarrow 23

$$\begin{array}{c} A \oplus B \\ A = 1101 \\ B = 1010 \\ \hline F = 0111 \end{array}$$

Design 8-bit ALU using IC# 74382



counter : Any sequence



SAP₁ : (Programming position)

Synchronous Counter Design (Any sequence)

Diagram showing the design of a synchronous counter for any sequence using 3 JK flip-flops.

Step 1: * → Undesired state * Circuit Excitation Table

The circuit uses 3 JK flip-flops (J_B, K_B; J_A, K_A) and a clock input (CLK). The output Q is shown for each state transition.

Circuit Excitation Table:

D ₃	D ₂	D ₁	D ₀	J _B	K _B	J _A	K _A	Q
0	0	0	0	0	1	0	0	No change
1	*	0	1	0	0	x	1	0 ✓
2	0	1	0	1	0	x	0	1 ✓
3	*	0	1	0	0	x	1	0 ✓
4	1	0	0	1	0	1	0	0 ✓
5	*	1	0	0	0	0	1	0 ✓
6	1	1	0	1	1	0	1	1 ✓
7	1	1	1	0	0	1	1	1 ✓

State Table:

State	J	K	J	K
0 → 0	0	0	0	0
0 → 1	1	1	1	0
1 → 1	1	1	1	1
1 → 0	0	1	0	0
0 → 0	0	0	0	0
0 → 1	1	1	1	1
1 → 0	0	1	0	0
1 → 1	1	1	1	1

Step 2 : Simplification (K-map)

	$\bar{A}\bar{B}$	$A\bar{B}$	$A\bar{B}$	$\bar{A}B$
\bar{C}	0	1	3	2
C	4	5	7	6

✓ $J_C = \bar{A}B$

$K_C = A$

✓ $J_B = \bar{A}$

✓ $K_B = \bar{C} + A$

✓ $J_A = BC$

✓ $K_A = 1$

0	0	0	1
x	x	x	x

x	x	x	x
x	1	1	0
0	1	1	0

1	0	x	x
1	0	x	x

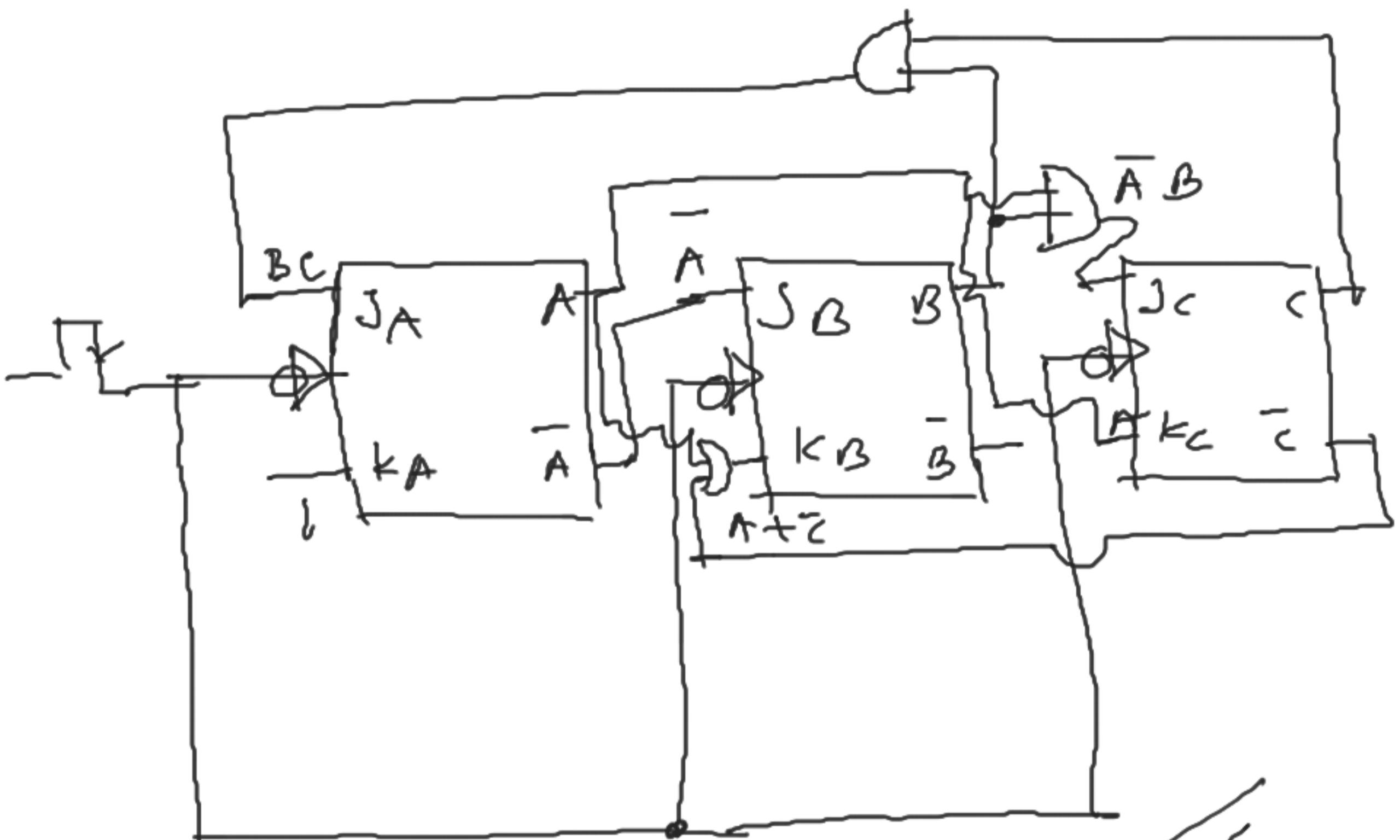
x	x	1	1
x	x	1	0

0	x	x	0
0	x	x	1

x	1	1	x
x	1	1	x

Step 3 : Circuit

$$\left. \begin{array}{l} J_A = K_A = 1 \\ J_B = K_B = A \\ J_C = K_C = AB \end{array} \right\}$$



20

Step 1 →

8 ✓

Step 2 →

6 ||

Step 3 →

4

~~0, 1, 4, 7, 9, 12, 14, 15, 0~~

Step 1: Circuit Excitation Table

		B after pulse		A after pulse										
D	C	B̄A	D	C	S A	J _D	K _D	J _C	K _C	J _B	K _B	J _A	K _A	
0	0	0 0	0	0	0 1	0	x	0	x	0 x	1	2x		
0	0	0 1	0	1	0 0	0	x	1	2x	0 2x	x 1			
0	0	1 0	0	0	0 0	0	x	0	x	x 1	0 x			
0	0	1 1	0	0	0 0	0	x	0	x	x 1	x 1			
0	1	0 0	0	1 1	1	x		x 0	1	2x	1	2x		
0	1	0 1	0	0 0	0 0	x		x 1	0	2x	x 1			
0	1	1 0	0	0 0	0 0	x		x 1	x 1	x 1	0 2x			
0	1	1 1	1	0 0 1	1	x		x 1	x 1	x 1	x 1			
1	0	0 0	0	0 0 0	x	1		0 x	0 x	0 x	0 x			
1	0	0 1	1	1 0 0	x	0		1 x	0 x	x 1	0 x			
1	0	1 0	0	0 0 0	x	1		0 x	1 x	x 1	x 1			
1	0	1 1	0	0 0 0	x	1		0 x	1 x	x 1	x 1			
1	1	0 0	1	1 1 0	x	0		x 0	1 x	0 x	0 x			
1	1	0 1	0	0 0 0	x	1		x 1	0 x	x 1	x 1			
1	1	1 0	1	1 1 1	x	0		x 0	x 0	1 x	x 1			
1	1	1 1	0	0 0 0	x	1		x 1	x 1	x 1	x 1			

Step 2: Simplification

	$\bar{A}\bar{B}$	$A\bar{B}$	AB	$\bar{A}B$
$\bar{C}\bar{D}$	0	1	3	2
$\bar{C}D$	4	5	7	6
$C\bar{D}$	12	13	15	14
CD	8	9	11	10

$$J_D = ABC$$

0	0	0	0
0	0	0	0
x	x	x	x
x	x	x	x

$$K_B = \bar{D} + A + C$$

$\bar{A}\bar{C}$	x	x	x
$AB + AC$	x	x	x
$= AB + \bar{A}\bar{C}$	x	x	x
	x	x	x

$\bar{B}\bar{D}$	1	x	x
$+ BCD$	1	x	x
	0	x	x
	0	x	x

$$J_C = \bar{A}\bar{B}$$

0	1	0	0
x	x	x	x
x	x	x	x
0	1	0	0

$$K_A = \bar{C} + B + D$$

\bar{C}	1	x	x
$B + D$	1	x	x
	x	x	x
	x	x	x

$$K_C = A + \bar{B}\bar{D}$$

x	x	x	x
0	1	1	1
0	1	1	0
x	x	x	x

Step 3: Draw The circuit.

CT 9% Sunday

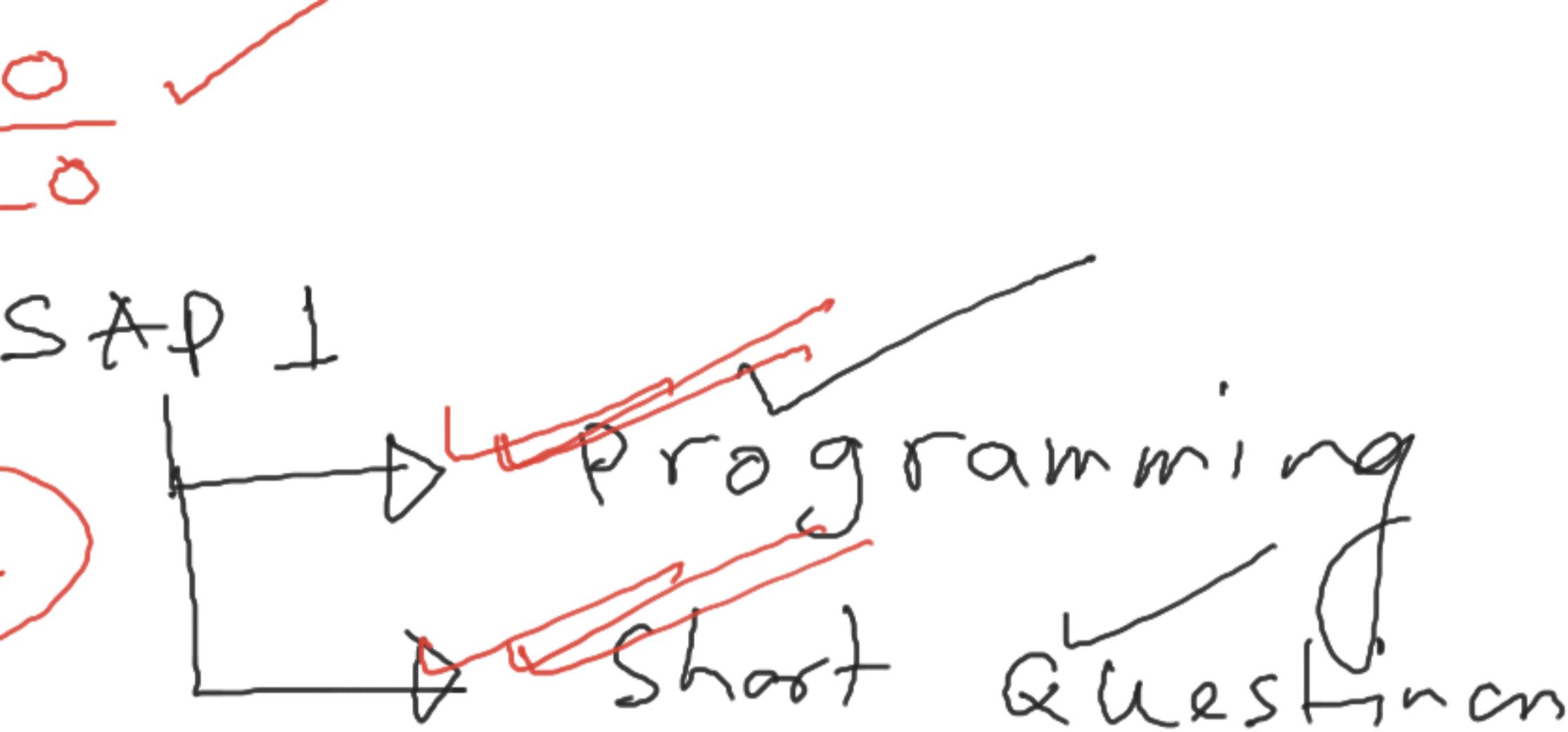
$$\frac{20}{20}$$

syllabus \Rightarrow

15

12

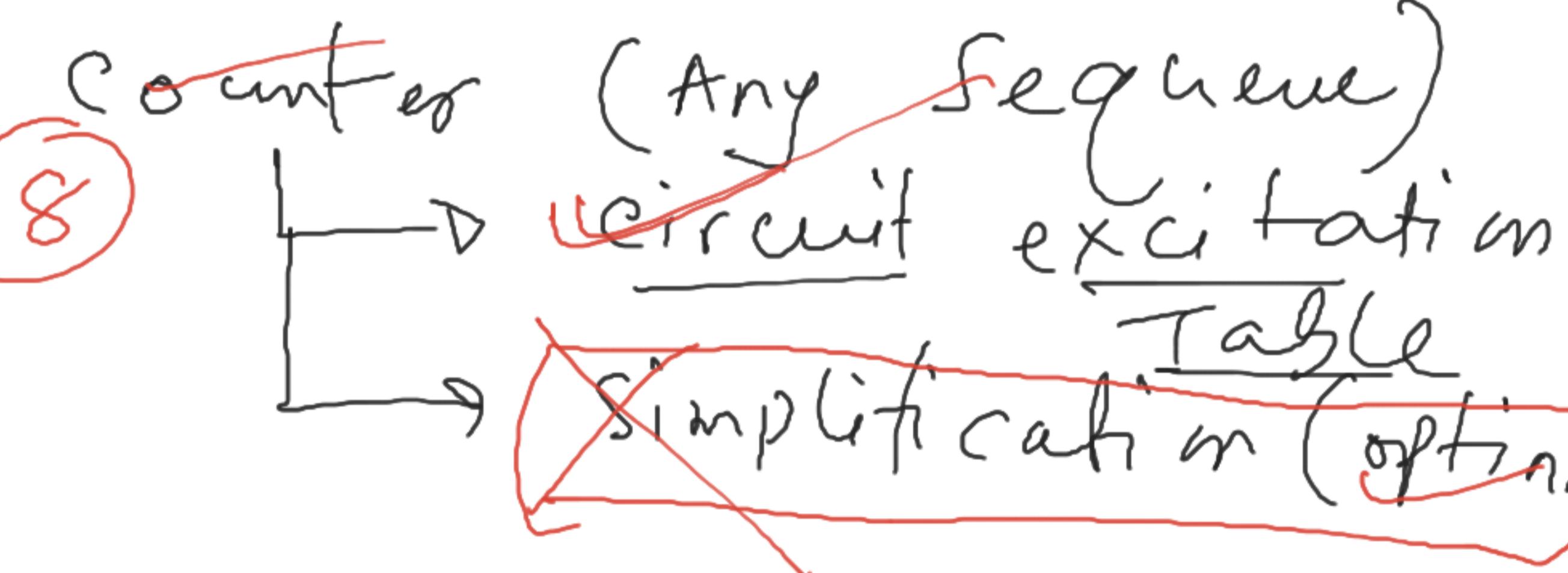
SAP 1



GT

5

8



Instruction Set

LDA ← Load a value in accumulator
(0000)

ADD ← RAM + Accumulation
(0001)

SUB ← Accumulator - RAM
(0010)

OUT ← Accumulation : display to
the output
(1110)

HLT ← stop the program
(1111)

~~D~~ \rightarrow ~~20~~ + $40 - 18 + 7 - 25$ ✓
 All are decimal figure
~~H~~ \rightarrow $14 + 28 - 12 + 07 = 19$

$$\begin{array}{r}
 16 \bigg| 20 \\
 \underline{-16} \\
 \hline
 4 \\
 + 14 \\
 \hline
 14
 \end{array}$$

$$\begin{array}{r}
 16 \bigg| 40 \bigg| 2 \\
 \underline{-32} \\
 \hline
 8 \\
 \boxed{28}
 \end{array}$$

OUT
HLT

$$\begin{aligned}
 16 - 2 &= 14 \\
 \frac{14}{2} &= 7
 \end{aligned}$$

$$H \Rightarrow 14 + 28 - 12 + 7 - 19$$

8 bit

Address	contents	Address	Contents in Binary	Contents in HEX
0 H	LDA F H	0 0 0 0	0 0 0 0 1 1 1 1	OF
1 H	ADD E H	0 0 0 1	0 0 0 1 1 1 0	1 E
2 H	SUB D H	0 0 1 0	0 0 1 0 1 1 0 1	2 C
3 H	ADD C H	0 0 1 1	0 0 0 1 1 1 0 0	1 D
4 H	SUB B H	0 1 0 0	0 0 1 0 1 0 1 1	2 C
5 H	OUT	0 1 0 1	1 1 1 0 1 1 1 1	FF
6 H	HLT	0 1 1 0	1 1 1 1 1 1 1 1	FF
7 H	FFH	0 1 1 1	1 1 1 1 1 1 1 1	FF
8 H	FFH	1 0 0 0	1 1 1 1 1 1 1 1	FF
9 H	FFH	1 0 0 1	1 1 1 1 1 1 1 1	FF
A H	FFH	1 0 1 0	1 1 1 1 1 1 1 1	FF
B H	19 H	1 0 1 1	0 0 0 1 1 0 0 1	19
C H	07 H	1 1 0 0	0 0 0 0 0 1 1 1	07
D H	12 H	1 1 0 1	0 0 0 1 0 0 1 0	12
E H	28 H	1 1 1 0	0 0 1 0 1 0 0 0	28
F+1	14 H	1 1 1 1	0 0 0 1 0 1 0 0	14

Before final Exam (50%)



$$CT \Rightarrow 20$$

$$\text{Assignment} \Rightarrow 10 \quad (5 \times 2)$$

$$\text{mid term} = 20$$

$$\text{Total} \Rightarrow 50$$

Final \Rightarrow 150 3 hrs

written Exam (2 hrs) \Rightarrow 120 \Rightarrow [40]

Viva \Rightarrow 30 ✓

3rd day after Last Exam

{ (10 AM to onward)

1 \rightarrow 10 ()

11 \rightarrow 20 ()

(C01 & C02)

Before final ??

7

Final Exam: 2 hours

4 question

($4 \times 30 = 120$ Marks)

problem
2v

1. SAP 1

JK FF

Any Sequence

50

3v

20

2. Counter

5

7

(1 or More)

74293

OR

4

6

(A, B, C)
Logic circuit

3. MSI

chap 9

Application

74151

IC # 74382

4. ALU

chap 6

→

3 & 4

Logic,

Boolean

K-map

3 & 4

slide = [3, 4, 5, 6]

CO4, CO5

CO4, CO5

CO4, CO5

A, B, C, D
1 74151
6 input
NOT