Assignment-5
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Instruction Set :

* The SAP-1 instruction set follows:-

SAP-1 Instruction SET		
Memonies	Operation	Description
LDA	ACC ← RAM[MAR]	Load RAM data into accumulator
ADD	ACC ← ACC + B	Add RAM data to accumulator
SUB	ACC ← ACC - B	subtract RAM data from accumulator.
OUT	OUT ← ACC	Load accumulator data into output register
HLT	clk ← 0	stop processing;

⇒ To load instruction and data words, into the SAP-1 memory, we have to use some kind of code that the computer can interpret.

* Assembly language involves working with mnemonies when writing a program.

* Machine language involves working with strings of Os and 1s,

SAP-1 OP CODES.	
Mnemonies	Op Code
LDA	0000
ADD	0001
SUB	0010
OUT	1110
HLT	1111

Control bit:

SAP-1 has 6-cycle controller with 12-bit microinstruction word. The 12-bits coming out of the Controller ~~sequency~~ sequencer from a word that controls the rest of the computer, Before each operation a clear (CLR) signal resets the computer

Macro Inst	T-state	Micro Operation	Active	COIN
LDA	T_4	MAR ← IR(3....0)	L'_M, E'_1	1A3H
	T_5	ACC ← RAM[MAR]	CE', L'_A	2C3H
	T_6	None	None	3E3H
ADD	T_4	MAR ← IR(3....0)	L'_M, E'_1	1A3H
	T_5	B ← RAM[MAR]	CE'_5, L'_B	2E1H
	T_6	ACC ← ACC+B	L'_A, E_u	3C7H
OUT	T_4	OUT ← ACC	E_A, L'_O	3F2H
	T_5	None	None	3E3H
	T_6	None	None	3E3H

* RAM state:-

For an operation:- 5 + 3 =

Address:	Content	
0H	LDA 4H	⟶ 0000 0100
1H	ADD 5H	⟶ 0001 0101
2H	OUT	⟶ 1110 1111
3H	HLT	
4H	5H	
5H	3H	
6H	FFH	
7H	FFH	
8H	FFH	
9H	FFH	
AH	FFH	
BH	FFH	
CH	FFH	
DH	FFH	
EH	FFH	
FH	FFH	

* Timing Diagram:-

Instruction	T_1	T_2	T_3	T_4	T_5	T_6
LDA	Ep Lm'	CP	Ce' Li'	Ei' Lm'	Ce' Le'	X
ADD	Ep Lm'	CP	Ce' Li'	Ei' Lm'	Ce' Lb'	Eu La'
OUT	Ep Lm'	CP	Ce' Li'	Ea Lo'	X	X