Department of Computer Science & Engineering

University of Asia Pacific (UAP)

Program: B.Sc. in Computer Science and Engineering

Final Examination	**Spring 2020**	**2nd Year 2nd Semester**
Course Code: CSE 209	**Course Title: Digital Logic & System Design**	**Credits: 4**
Full Marks: 120* (Written)		**Duration: 2 Hours**

* Total Marks of Final Examination: 150 (Written: 120 + Viva: 30)

Instructions:

1. There are **Four (4)** Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins.
2. Non-programmable calculators are allowed.

1. **a)** What are the difference between arithmetic and logical operation? What types of operation are possible in SAP-1 Computer? 04

b) Write down the instruction set and the corresponding op-code of SAP-1 Computer. 05

c) How many operations are possible in SAP-1 computer? Explain your answer. 05

d) Create a SAP-1 assembly language program and then generate the machine code for the expression of 18 - 20 + 35 – 52 + 8. These numbers are in decimal form. 16

2. **a)** Design a synchronous counter using J-K FFs that has the following sequence: 000, 010, 101, 110, and repeat. The undesired (unused) states 001, 011, 100, and 111 must always go to 000 on the next clock pulse. 20

b) A photo detector circuit is being used to generate a pulse each time a customer walks into a certain establishment. The pulses are fed to a seven-bit counter. The counter is used to count these pulses as a means for determining how many customers have entered the store. After closing the store, the proprietor checks the counter and finds that it shows a count of $0001100_2=12_{10}$. He knows that this is incorrect because there were many more than twelve people in his store. Assuming that the counter circuit is working properly. 05

(i) What could be the reason for the discrepancy?

(ii) How can you overcome from the discrepancy?

c) Consider a counter circuit that contains eight JK flip-flops wired in the arrangement of 05

$Q_7Q_6Q_5Q_4Q_3Q_2Q_1Q_0$.

(i) Determine the counter's MOD number.

(ii) Determine the output frequency in KHz when the input clock frequency is 8 MHz.

(iii) What is the range of counting states for this counter?

(iv) Assume a starting state (count) of 00100111. What will be the counter's state after 1325 pulses?

3. **a)** Implement the function F(A, B, C, D) = ∑(0, 1, 2, 6, 7, 11, 12, 14, 15) using only one IC# 74151(Multiplexer). You can use other logic gates, if necessary. 12

b) Show how IC# 74151 can be used to generate the logic function Z = AB + BC + CA. 08

c) For each item, indicate whether it is referring to a decoder, a MUX, or a DEMUX. 06

(i) Has more inputs than outputs.

(ii) Uses SELECT inputs.

(iii) Can be used in parallel-to-serial conversion.

(iv) Only one of its outputs can be active at one time.

(v) Can be used to route an input signal to one of several possible outputs.

(vi) Can be used to generate arbitrary logic functions.

d) For IC# 74138 (Decoder), what input conditions will produce the following outputs: 04
(i) LOW at O_6
(ii) LOW at O_4
(iii) LOW at O2
(iv) All outputs are HIGH.

4. **a)** Implement the following function using K-map. 10

$$F (A, B, C, D) = \sum(0, 1, 2, 3, 7, 8, 10, 11, 13, 14, 15)$$

b) Design a logic circuit that follows the following requirements: 10

(i) Output X will be logical equivalent to (C AND D) when A and B are the same.

(ii) X will remain HIGH when A and B are different.

c) Draw the block diagram of 4 bit ALU chip (IC# 74382) and label the all inputs & outputs. Describe 8(Eight) operations of the 4 bit ALU chip that perform by select input. 10

OR

a) Draw the block diagram of IC# 74293(Counter). Using this implement MOD 500 counter. 10

b) Design MOD 12 Johnson counter using JK flip-flop and describe its operation. 10

c) Describe the basic operation of IC# 7483(4-bit parallel adder). Using this draw a 4-bit parallel adder/subtractor. You can use other logic gates if necessary. Briefly describe the operation of your diagram. 10