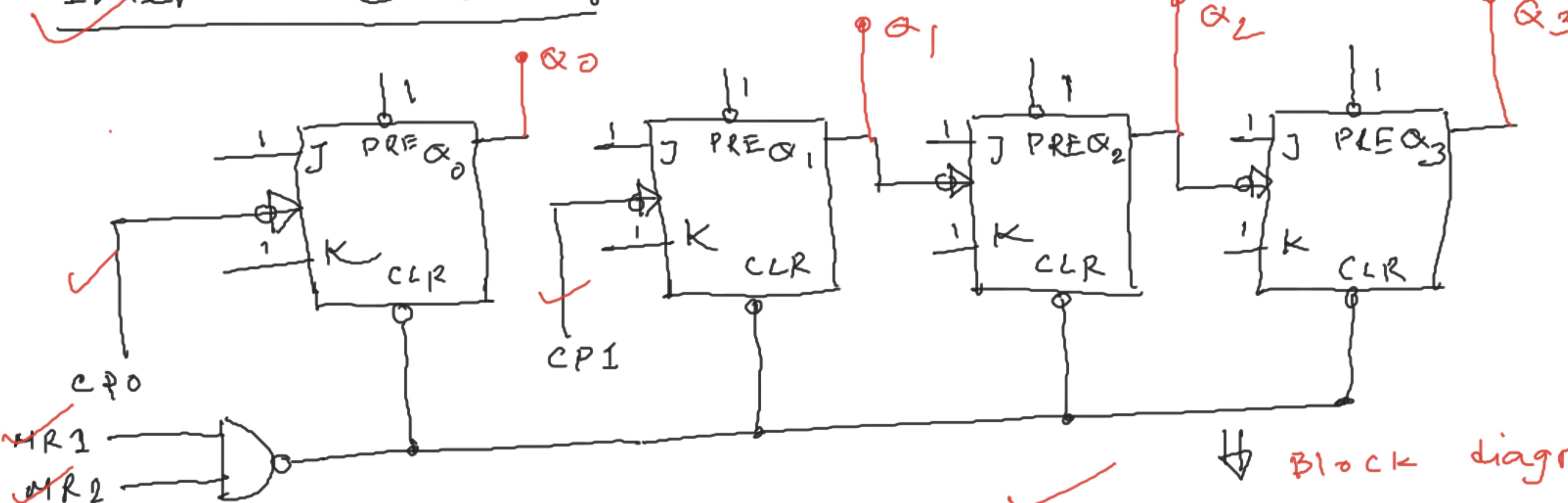


IC # 74293 (counter):

Internal circuit:



{ CP<sub>0</sub> → Clock pulse 0

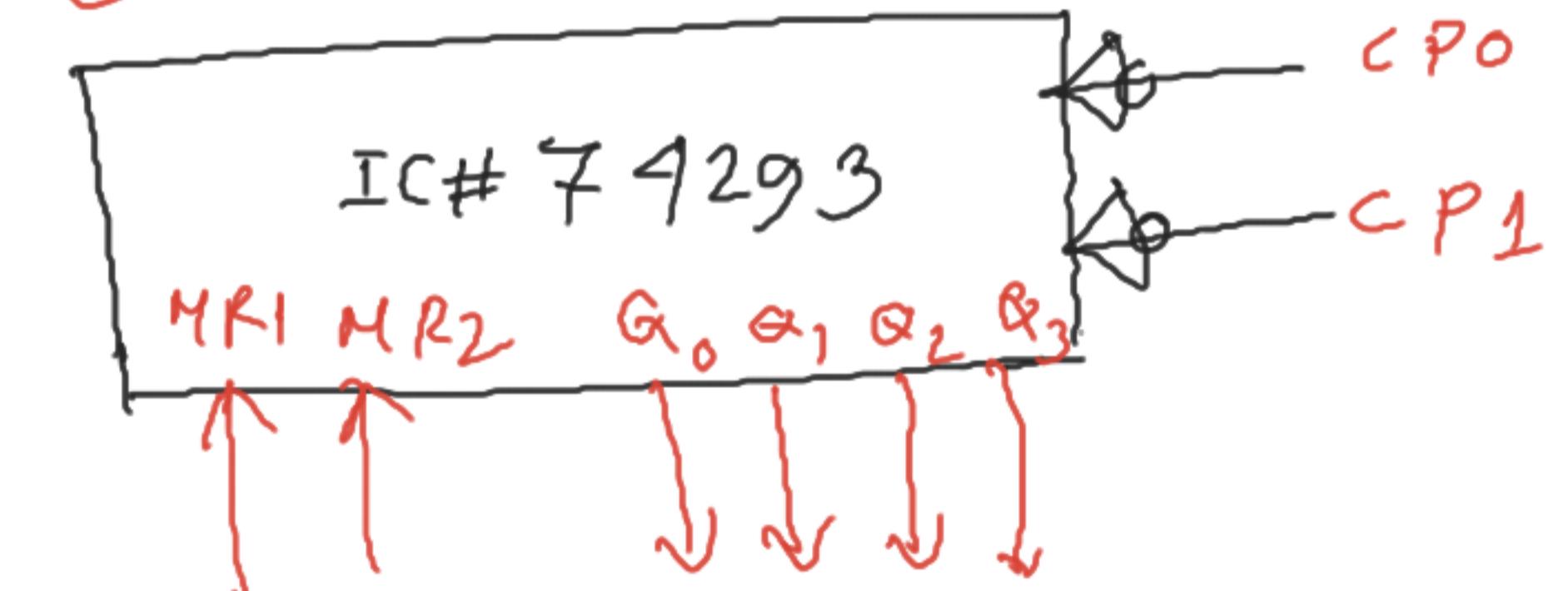
{ CP<sub>1</sub> → Clock pulse 1

{ MR<sub>1</sub> → Master Reset 1

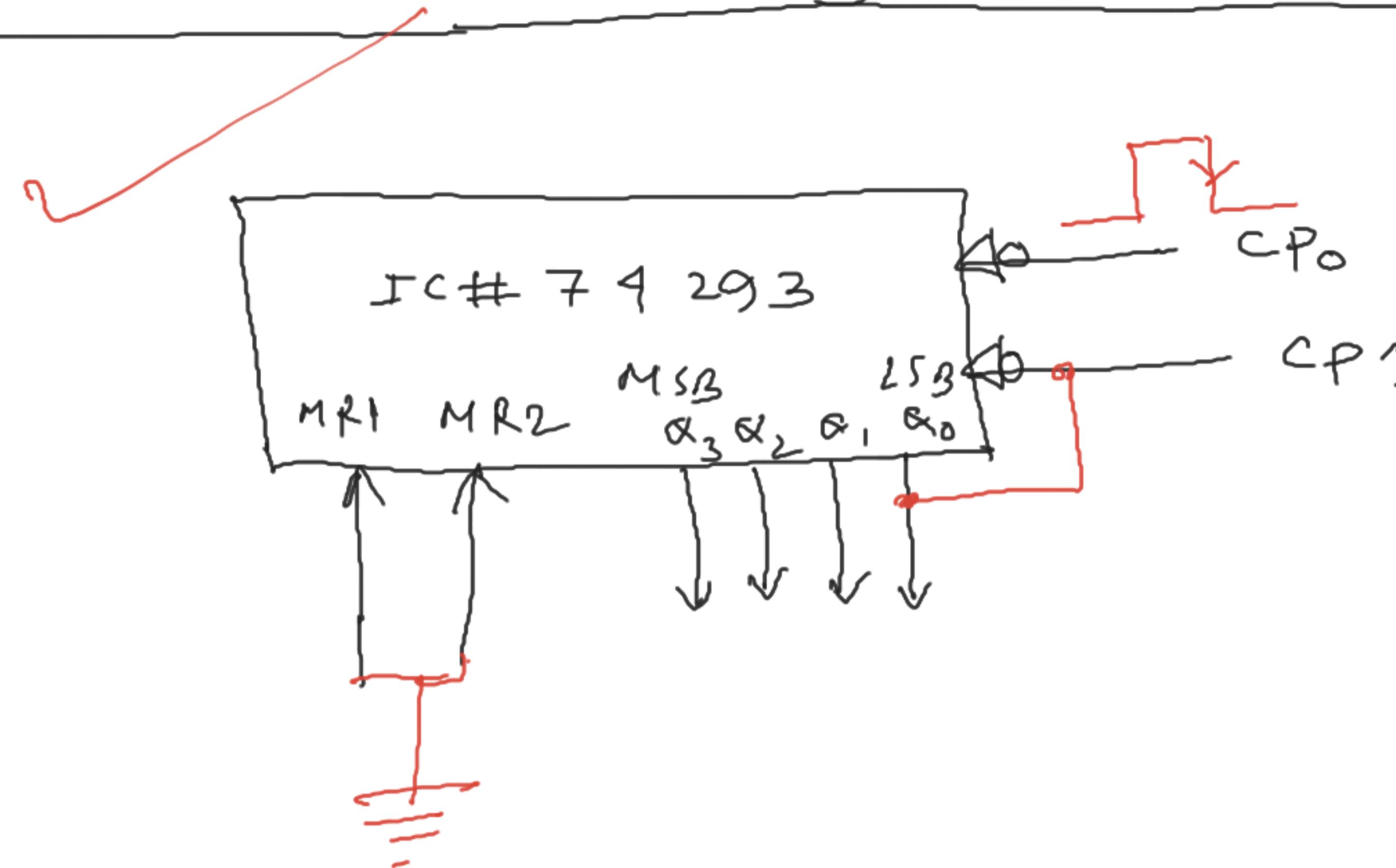
{ MR<sub>2</sub> → Master Reset 2

2<sup>W</sup> counter

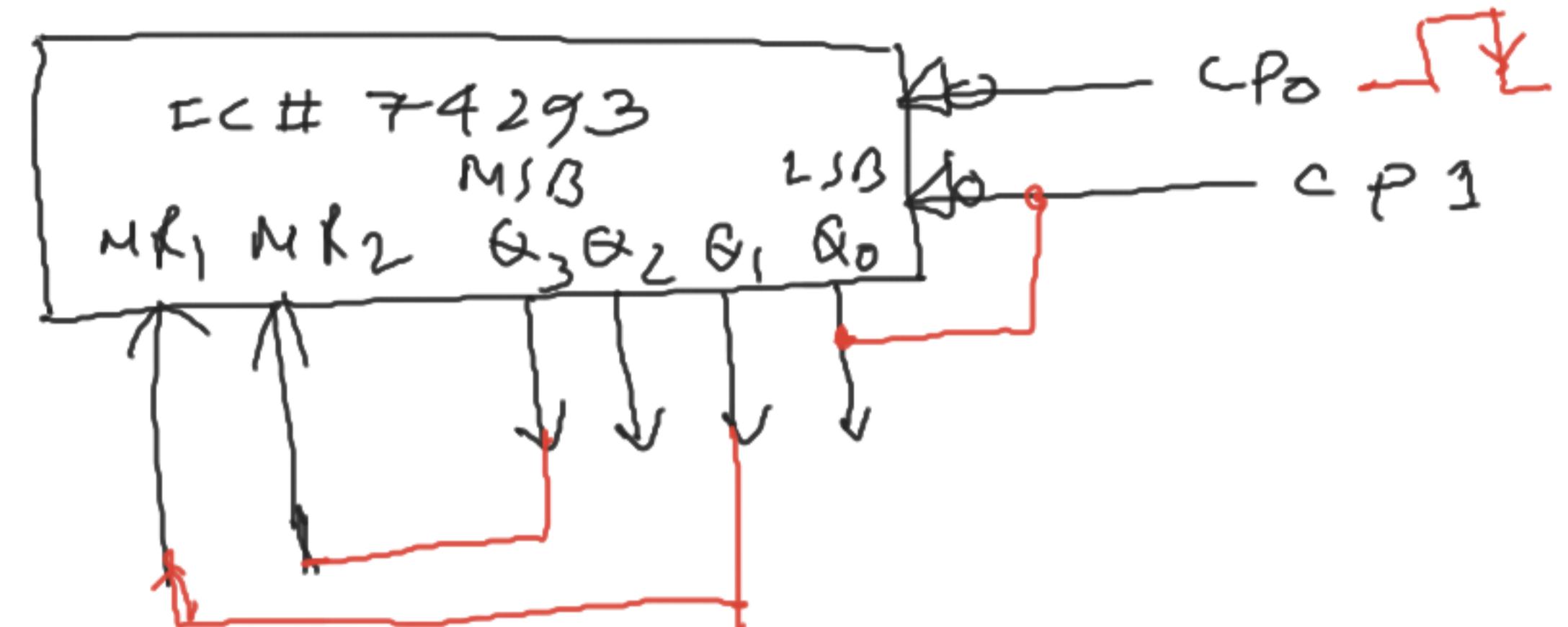
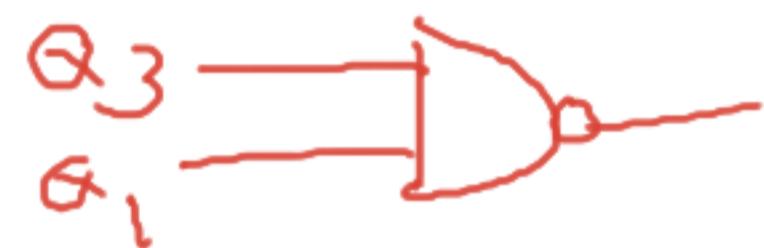
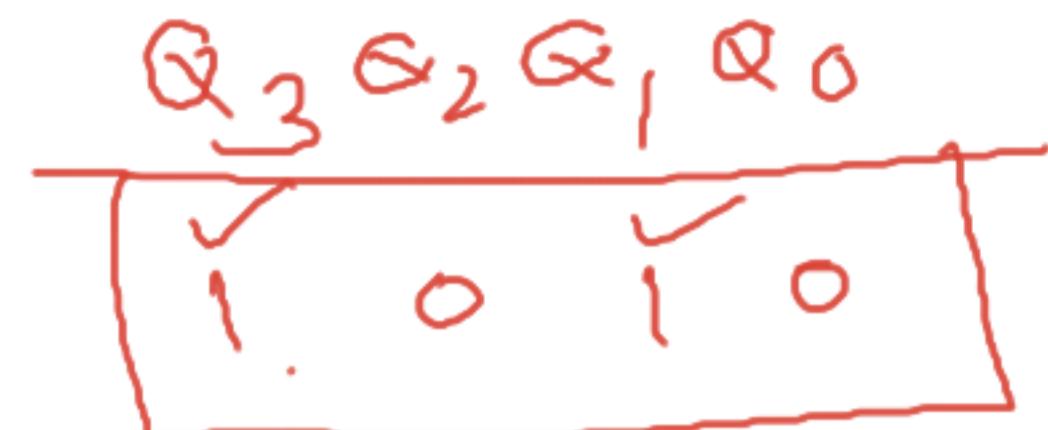
Block diagram



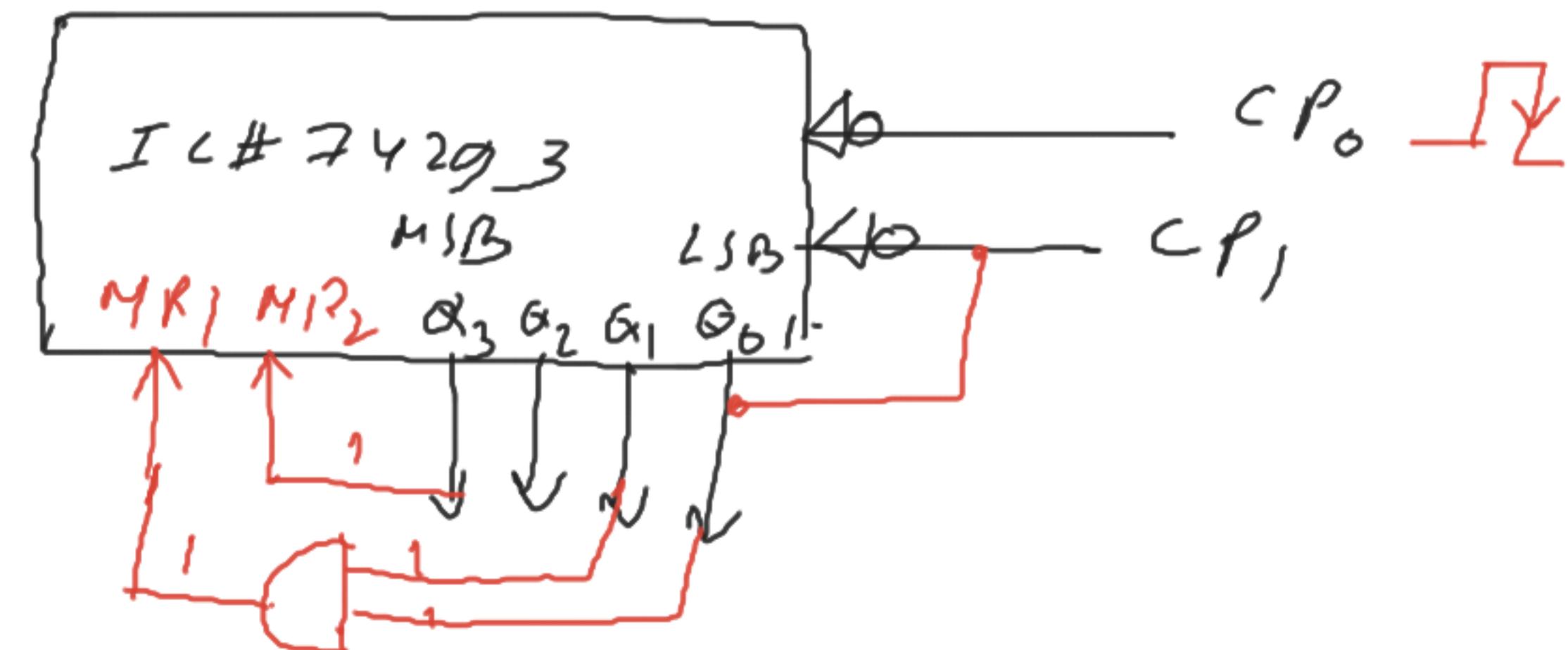
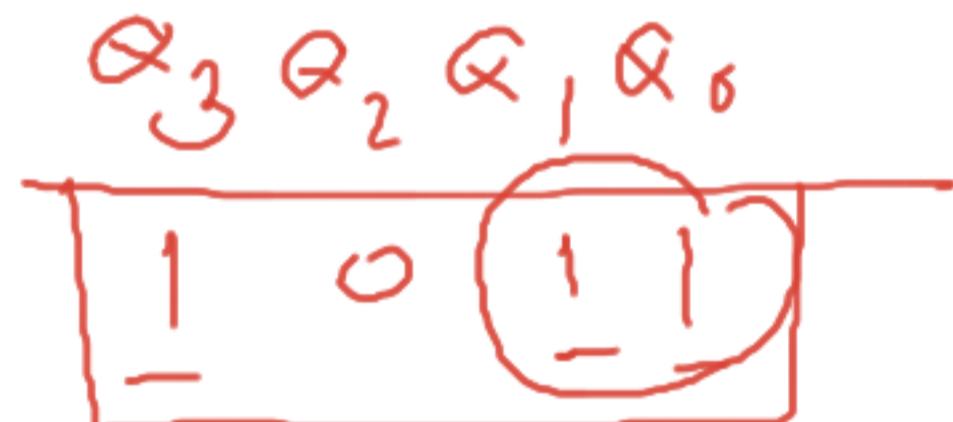
Design MOD 16 counter using IC# 74293 :



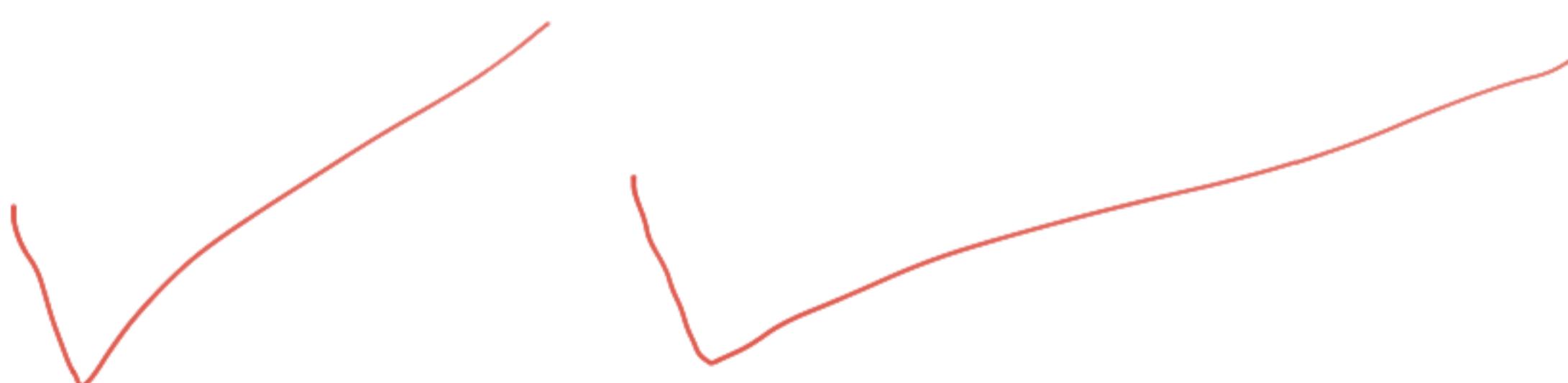
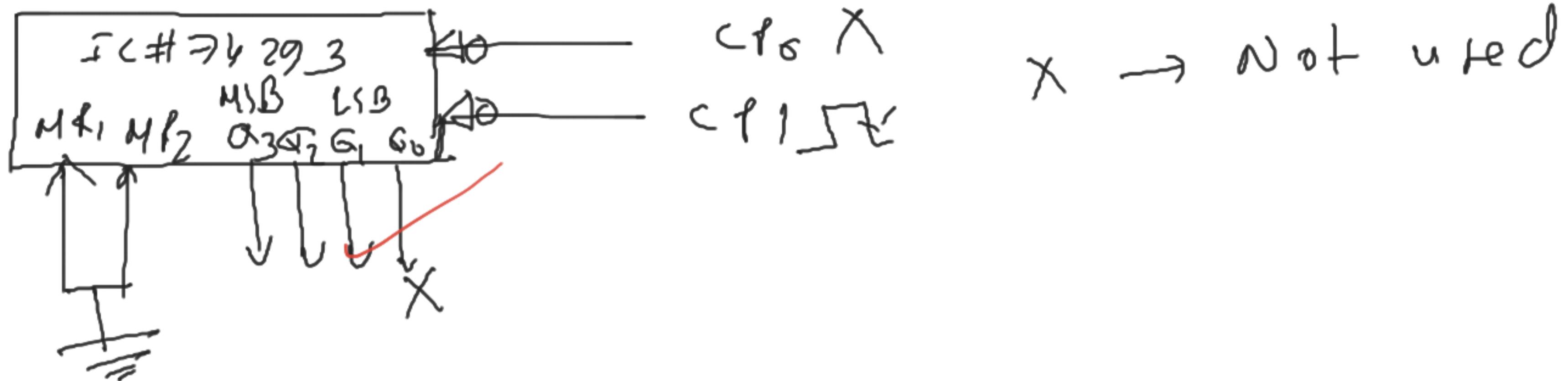
Design mod 10 counter using IC # 74293



Design mod 11 counter using IC# 74293



Design mod 8 counter using IC# 74293

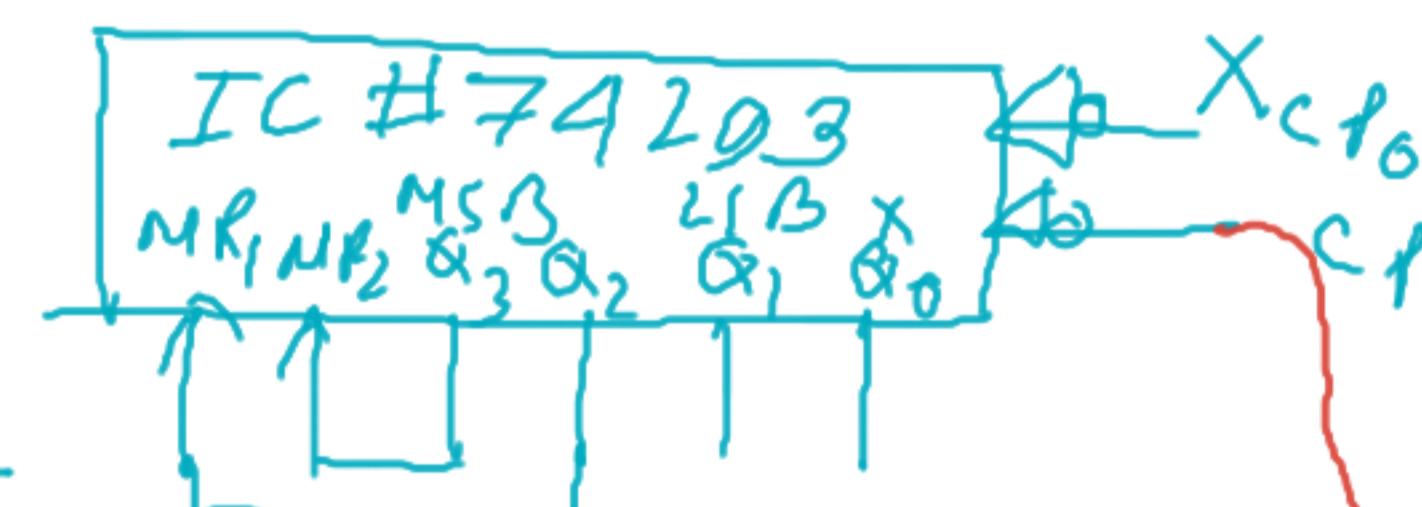




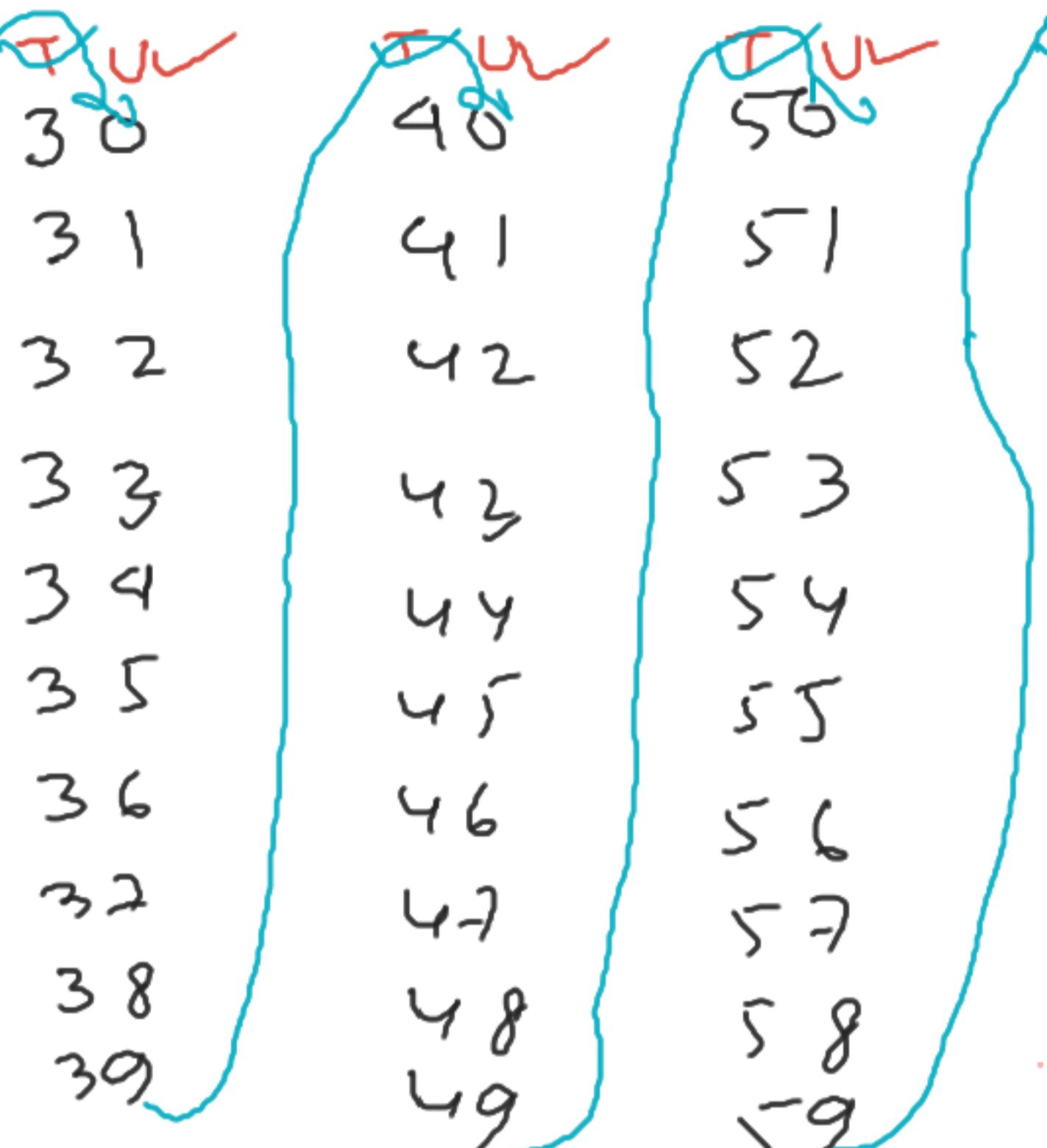
Unit  
Q<sub>3</sub> Q<sub>2</sub> Q<sub>1</sub>, Q<sub>0</sub>

0 0 0 0

1 0 0 0  
1 0 0 1  
0 0 0 0



X → Not use      MOD 10



N → MOD 10 counter

T → MOD 6 counter



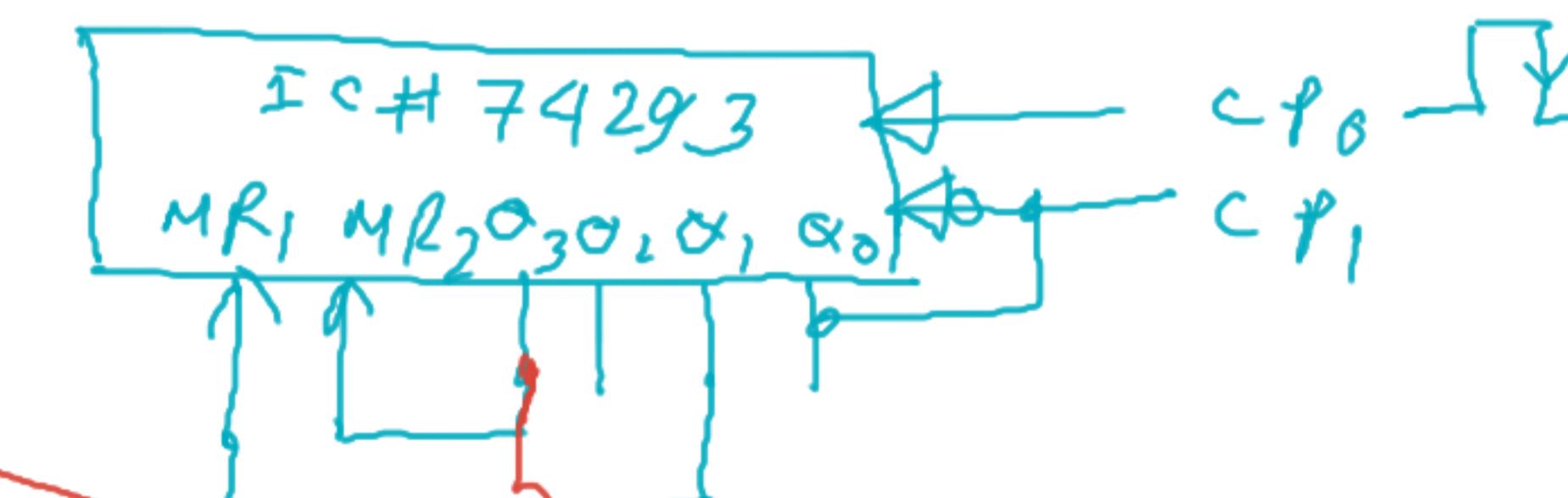
0 0 0 0  
0 0 0 1  
0 0 1 0  
0 0 1 1  
0 1 0 0  
0 1 0 1  
0 1 1 0  
0 1 1 1  
1 0 0 0

0 0 0 1  
0 0 1 0  
0 0 1 1  
0 1 0 0  
0 1 0 1  
0 1 1 0  
0 1 1 1  
1 0 0 0

0 0 0 1  
0 0 1 0  
0 0 1 1  
0 1 0 0  
0 1 0 1  
0 1 1 0  
0 1 1 1  
1 0 0 0

0 0 0 1  
0 0 1 0  
0 0 1 1  
0 1 0 0  
0 1 0 1  
0 1 1 0  
0 1 1 1  
1 0 0 0

0 0 0 1  
0 0 1 0  
0 0 1 1  
0 1 0 0  
0 1 0 1  
0 1 1 0  
0 1 1 1  
1 0 0 0



~~MOD~~ 100 :

0 0  
.

9 9

~~MOD~~ 1000

✓ VV  
0 0 0



~~MOD~~ 8060

9 9 9

✓ VVV  
0 0 0

4 IC

~~MOD~~ 500

✓ VV  
0 0 0

7 9 9

4 9 9

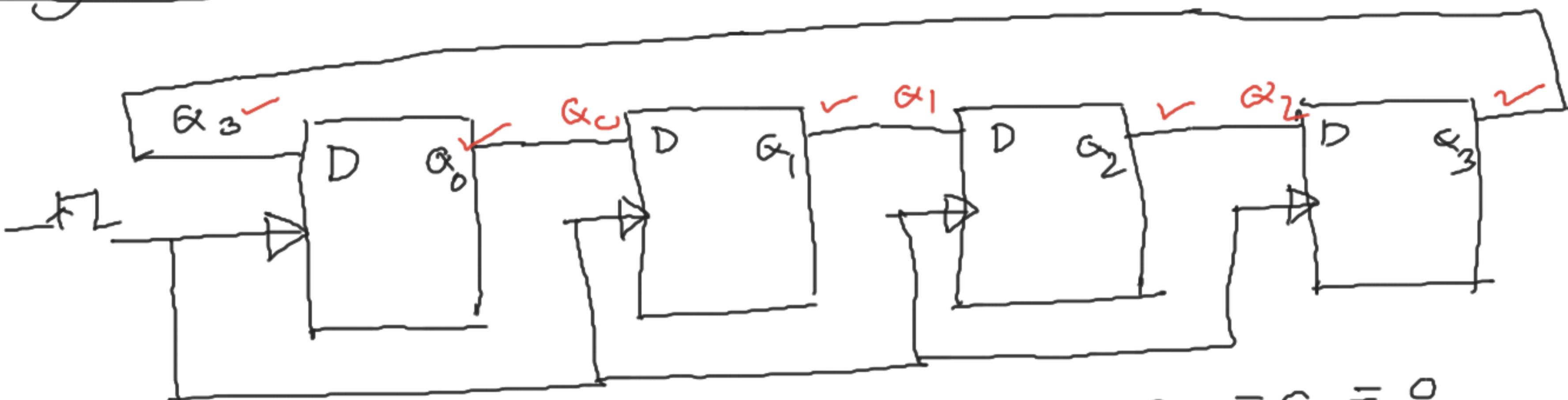
- ~~Shift counter~~: 1) Ring counter 2) Johnson counter
- D Ring counter:

D Ring counter:

MOD 4

Ring Counter

D	CLK	Q
0	P	0
1	P	1



Initially  $Q_0 = 1, Q_1 = Q_2 = Q_3 = 0$

operation:

After giving the pulse

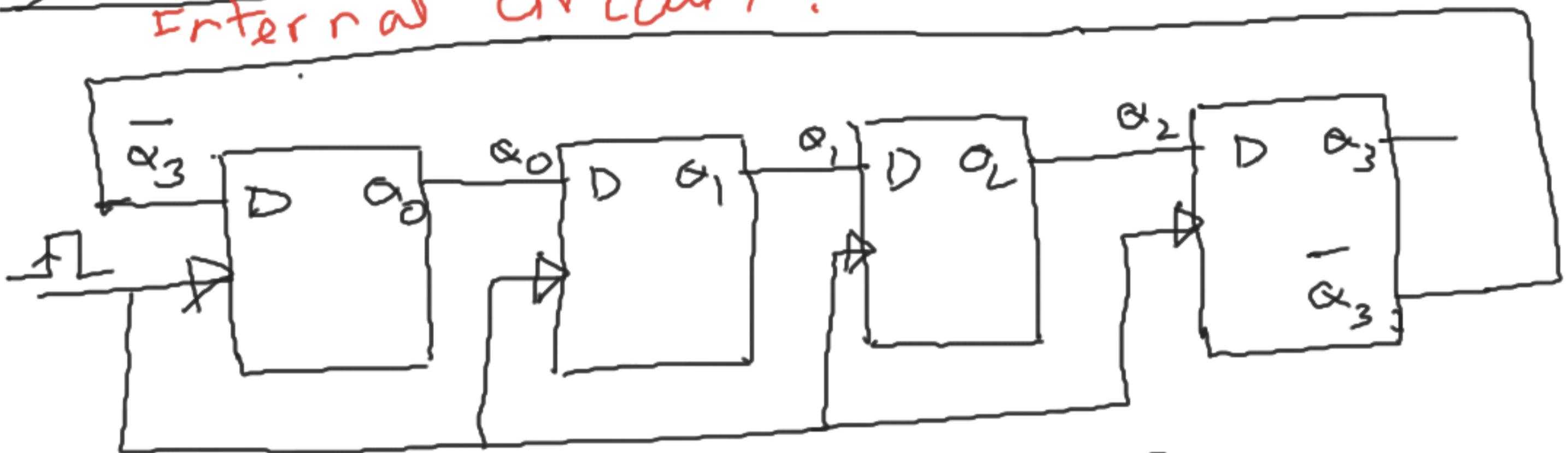
$$\begin{cases} Q_0 = Q_3 \\ Q_1 = Q_0 \\ Q_2 = Q_1 \\ Q_3 = Q_2 \end{cases}$$

For ring counter

MOD number = Number of flip flop

	$Q_0$	$Q_1$	$Q_2$	$Q_3$
# 1	1	0	0	0
# 2	0	1	0	0
# 3	0	0	1	0
# 4	1	0	0	0

2) Johnson counter : Mod 8 Johnson Counter  
 Internal circuit : Truth Table



Initially  $Q_0 = Q_1 = Q_2 = Q_3 = 0$

Operation :

After giving the pulse

For Johnson  
Counter,

$$\left\{ \begin{array}{l} Q_0 = \bar{Q}_3 \\ Q_1 = Q_0 \\ Q_2 = Q_1 \\ Q_3 = Q_2 \end{array} \right.$$

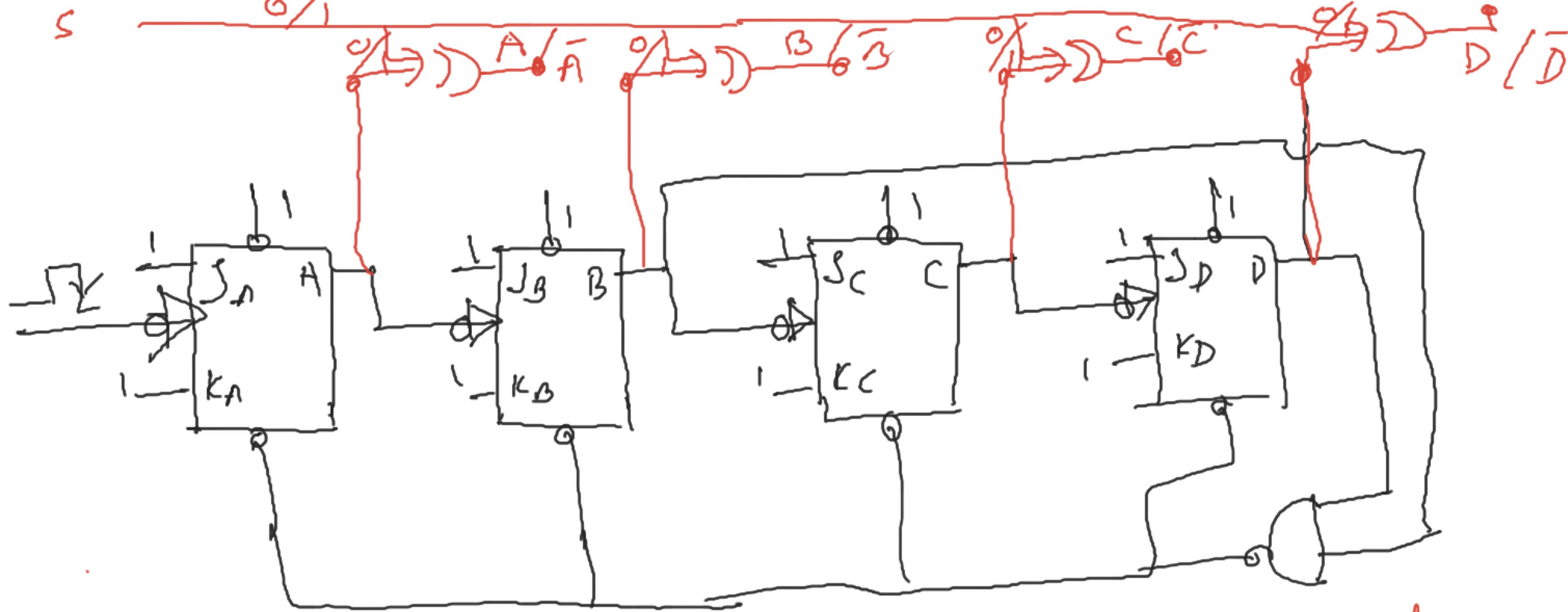
#

Mod number =  
 $2 \times \text{Number of}$   
 Flip flop

	$Q_0$	$Q_1$	$Q_2$	$Q_3$
#1	0	0	0	0
#2	1	0	0	0
#3	1	1	1	0
#4	1	1	1	1
#5	0	1	1	1
#6	0	0	1	1
#7	0	0	0	1
#8	0	0	0	0

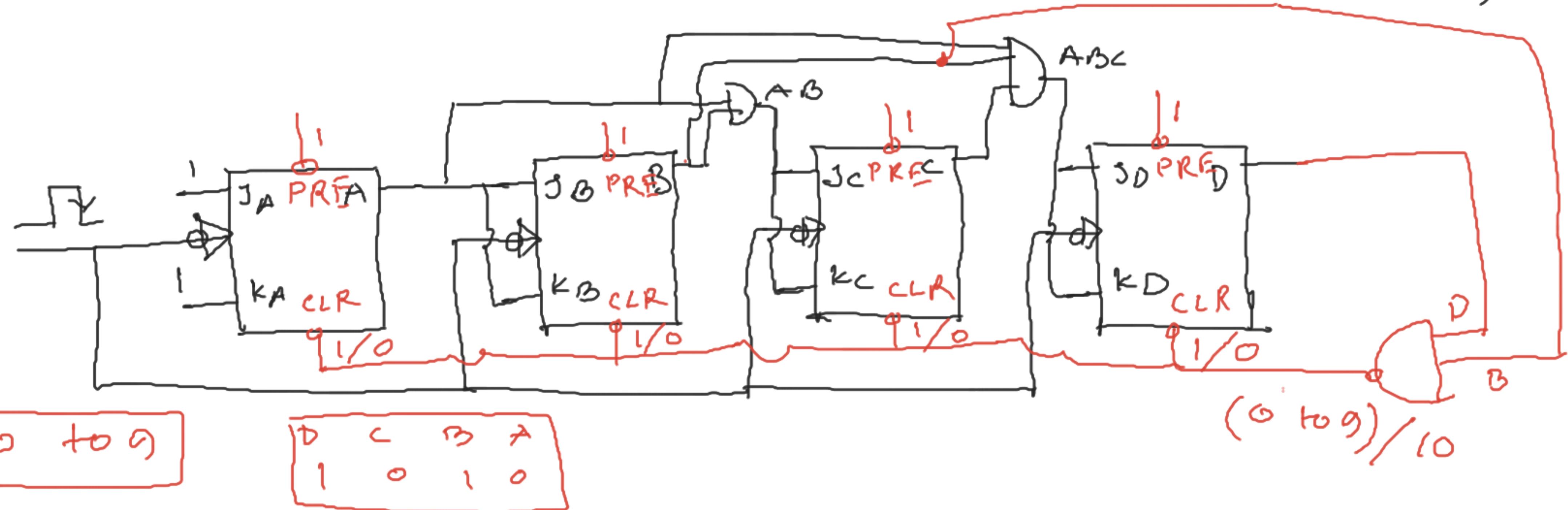
MOD 10 asynchronous up/down counter

MOD 10 UP				MOD 10 Down			
D	C	B	A	D	C	B	A
0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	0
0	0	1	0	1	1	0	1
0	0	1	1	1	1	0	0
0	1	0	0	1	0	1	1
-	0	1	0	1	0	1	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	0	0
1	0	0	0	0	1	1	1
1	0	0	1	0	1	1	0



Operation: If  $S = 0$  Then outputs are  $A, B, C, D$   
 If  $S = 1$  Then  $\Rightarrow$  Up counter outputs are  $\bar{A}, \bar{B}, \bar{C}, \bar{D}$   
 $\Rightarrow$  Down counter

MOD 10 synchronous up counter: ( $\leq 2^N$  synchronous counter)



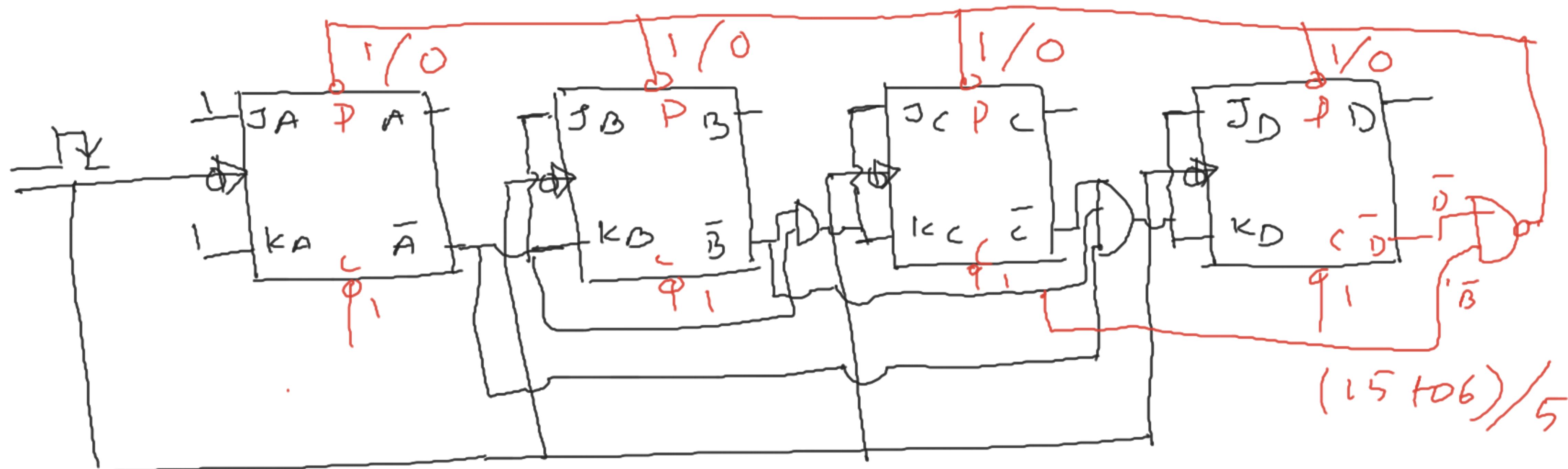
Operation: From 0 to 9  $\Rightarrow$  PRE = 1, CLR = 0  
 $\therefore$  Normal clock operation

At 10  $\Rightarrow$  PRE = 1, CLR = 0

$\therefore A = B = C = D = 0$

$\therefore$  It counts from 0 to 9.

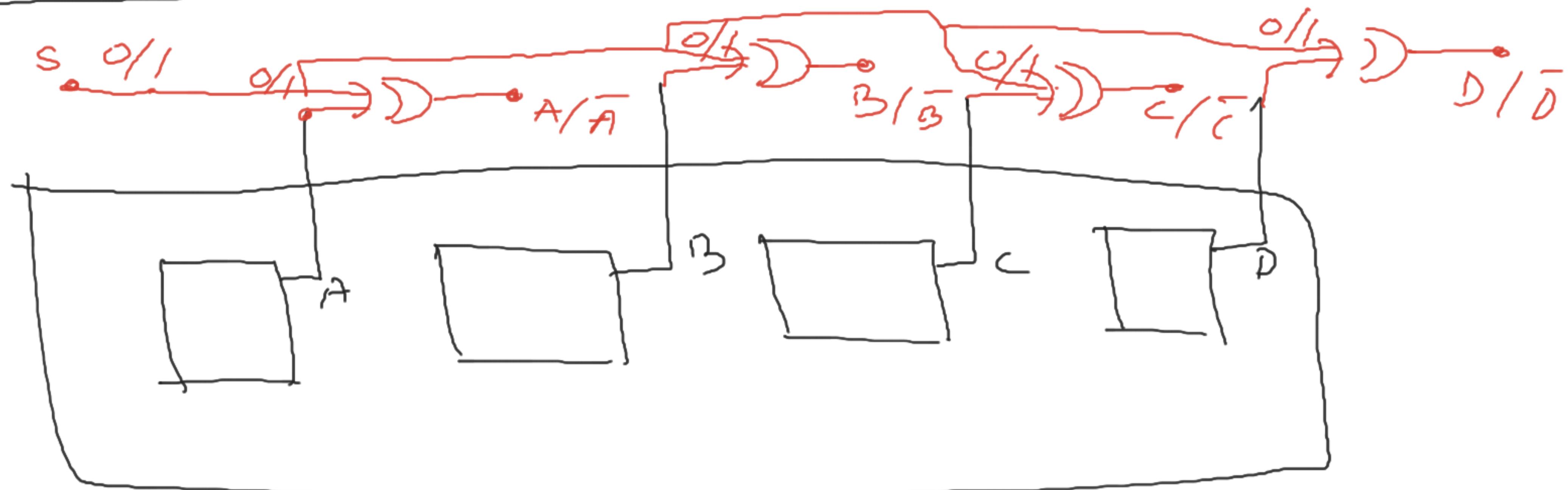
MOD 10 synchronous Down counter : (15 to 6)



operation: From 15 to 6  $\Rightarrow$  PRE = 1 ; CLR = 1  
 $\therefore$  Normal clock operation

At 5  $\Rightarrow$  PRE = 0 ; CLR = 1  
 $\therefore$  It counts from 15 to 6.

mod 10 synchronous up/down counter

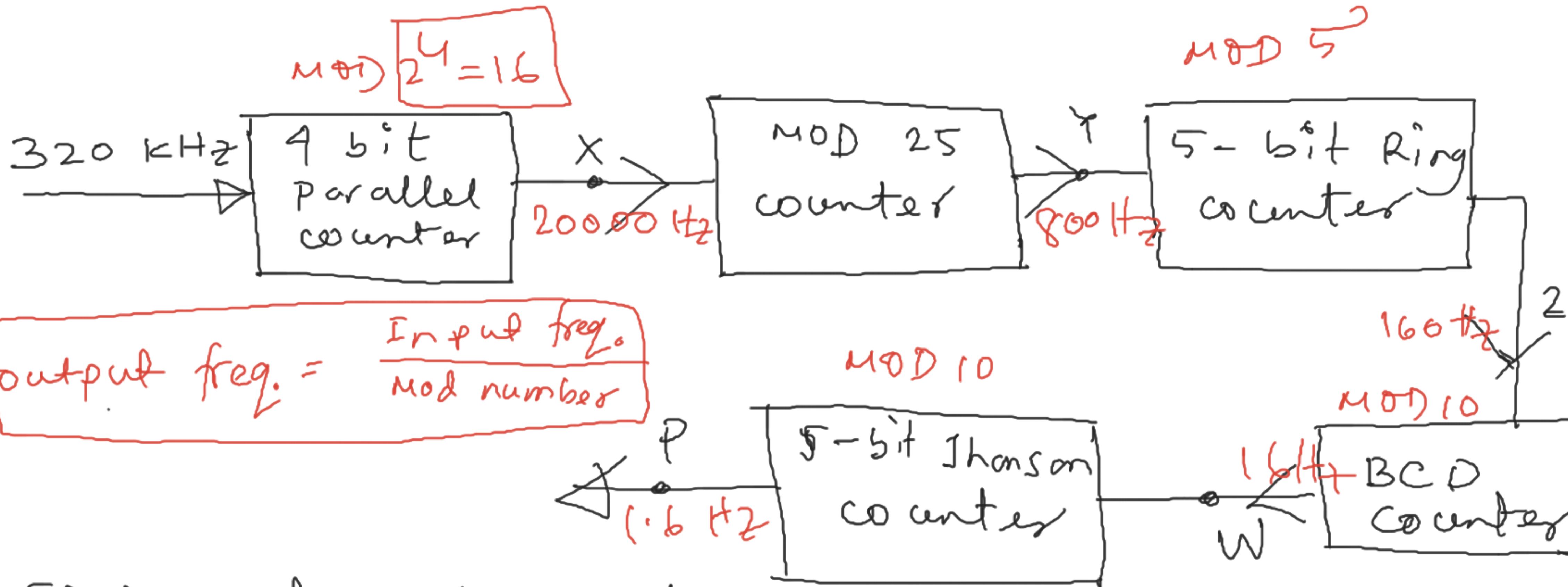


→ mod 10 synchronous  
up counter

For each of the following statements, indicate the type(s) of counter.

- 1) Each flip flop is clocked at the same time.  
↳ synchronous/parallel counter.
- 2) Each flip flop divides its <sup>input</sup> frequency by 2.  
↳ synchronous or asynchronous counter
- 3) The counting states are 111, 110, 101, 100, 011, 010, 001, 000, ... → MOD 8 Down counter.
- 4) The counter has 10 distinct states.  
↳ MOD 10 / BCD counter / Decade counter
- 5) The total delay is sum of individual ffs delay. → Asynchronous/Ripple counter,

- 6) The mod number is twice the number of flip flop.  $\rightarrow$  Johnson counter.
- 7) The counter can count in either direction.  $\rightarrow$  Up/Down counter.
- 8) The counter counts from 0 to 99  $\rightarrow$  MOD 100 up counter.
- 9) The mod number is equal to number of flip flop.  $\rightarrow$  Ring counter
- 10) The total delay is the sum of one FF's delay and one AND gate's delay.  
 $\rightarrow$  synchronous counter.

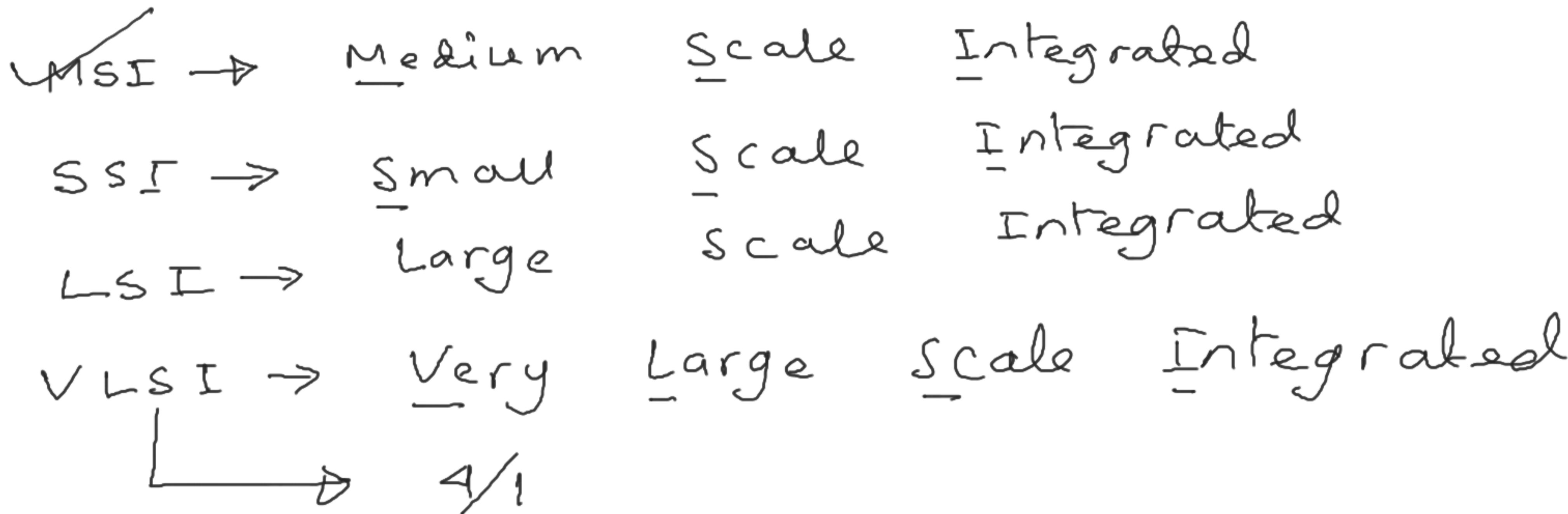


Find out values of  $x, y, z, w$  and  $p$  in Hz.

$$x = \frac{320 \times 1000}{16} = 20000 \text{ Hz}; y = \frac{20000}{25} = 800 \text{ Hz}$$

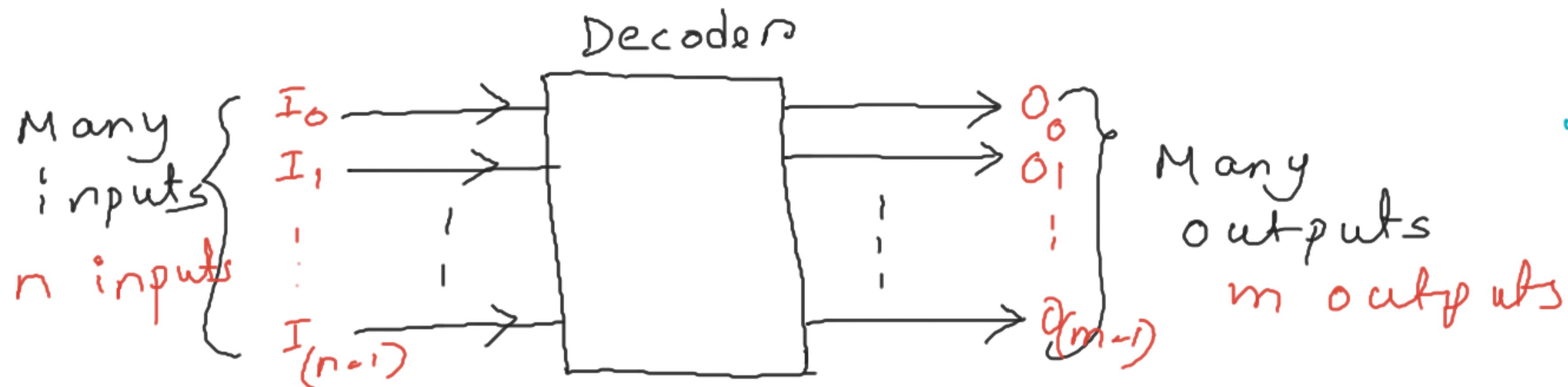
$$z = \frac{800}{5} = 160 \text{ Hz}, w = \frac{160}{10} = 16 \text{ Hz}; p = \frac{16}{10} = 1.6 \text{ Hz}$$

## Chapter 9: MSI Logic Circuits



- ✓ Decoder
- ✓ Multiplexer (MUX)
- ✓ Demultiplexer (DEMUX)

## 1) Decoder :-



No. of inputs	No. of outputs
2	$4 = 2^2$
3	$8 = 2^3$
4	$16 = 2^4$
5	$32 = 2^5$

{ At a time one of the output will be active according to corresponding combination of inputs.  
 (Number of inputs)

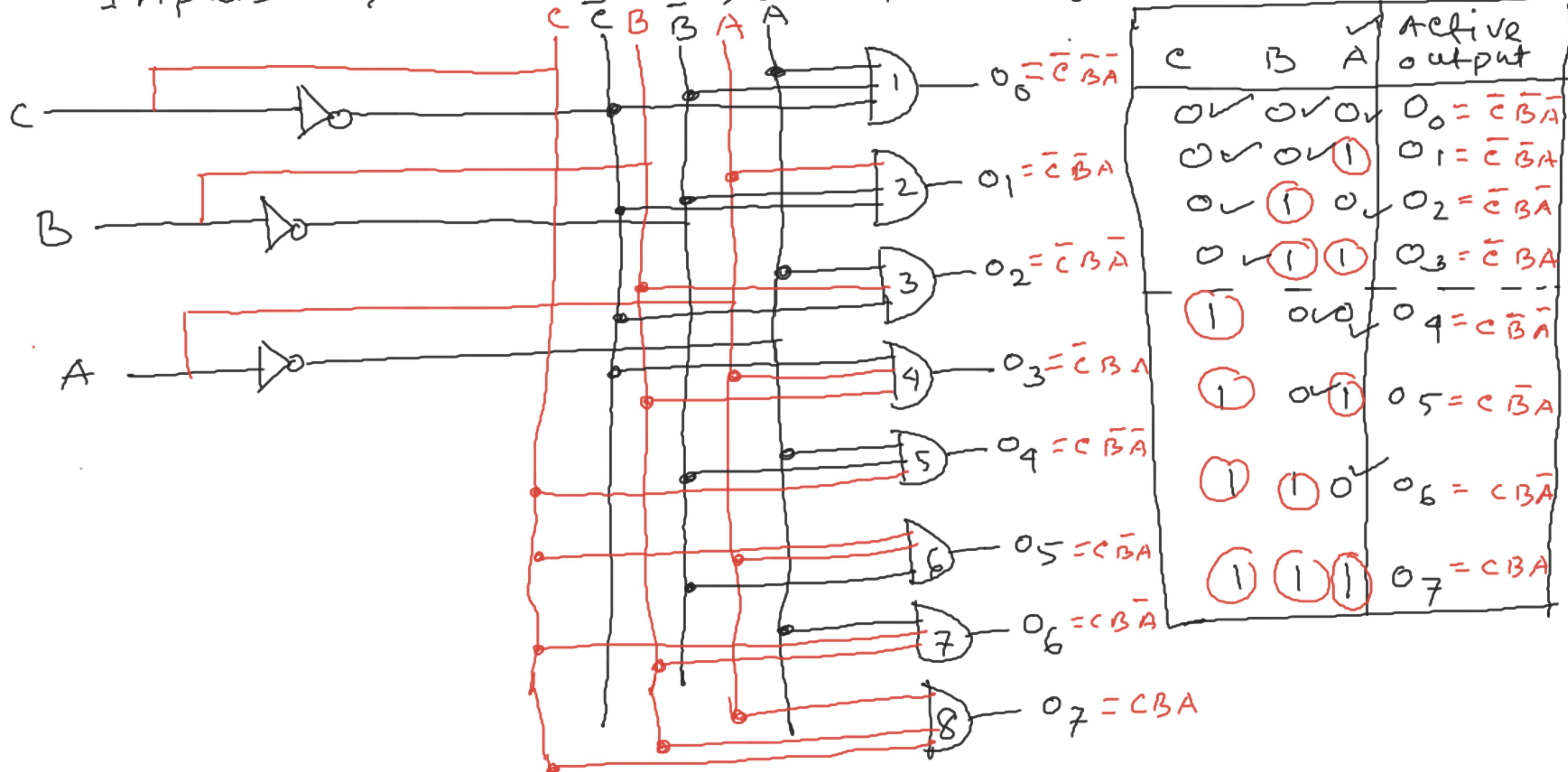
∴ Number of outputs = 2

∴

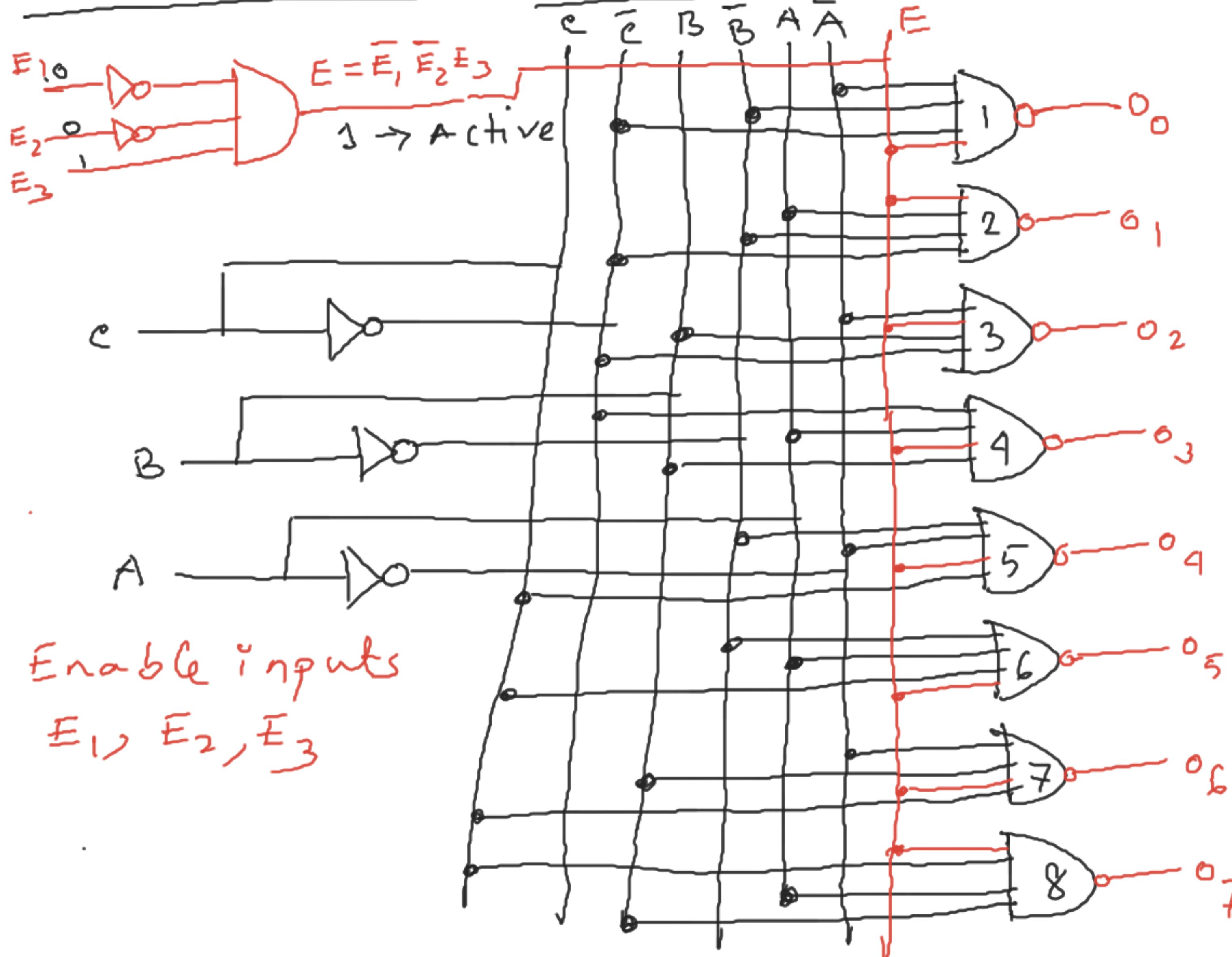
$$m = 2^n$$

# 3 lines to 8 lines Decoder: Internal Circuit

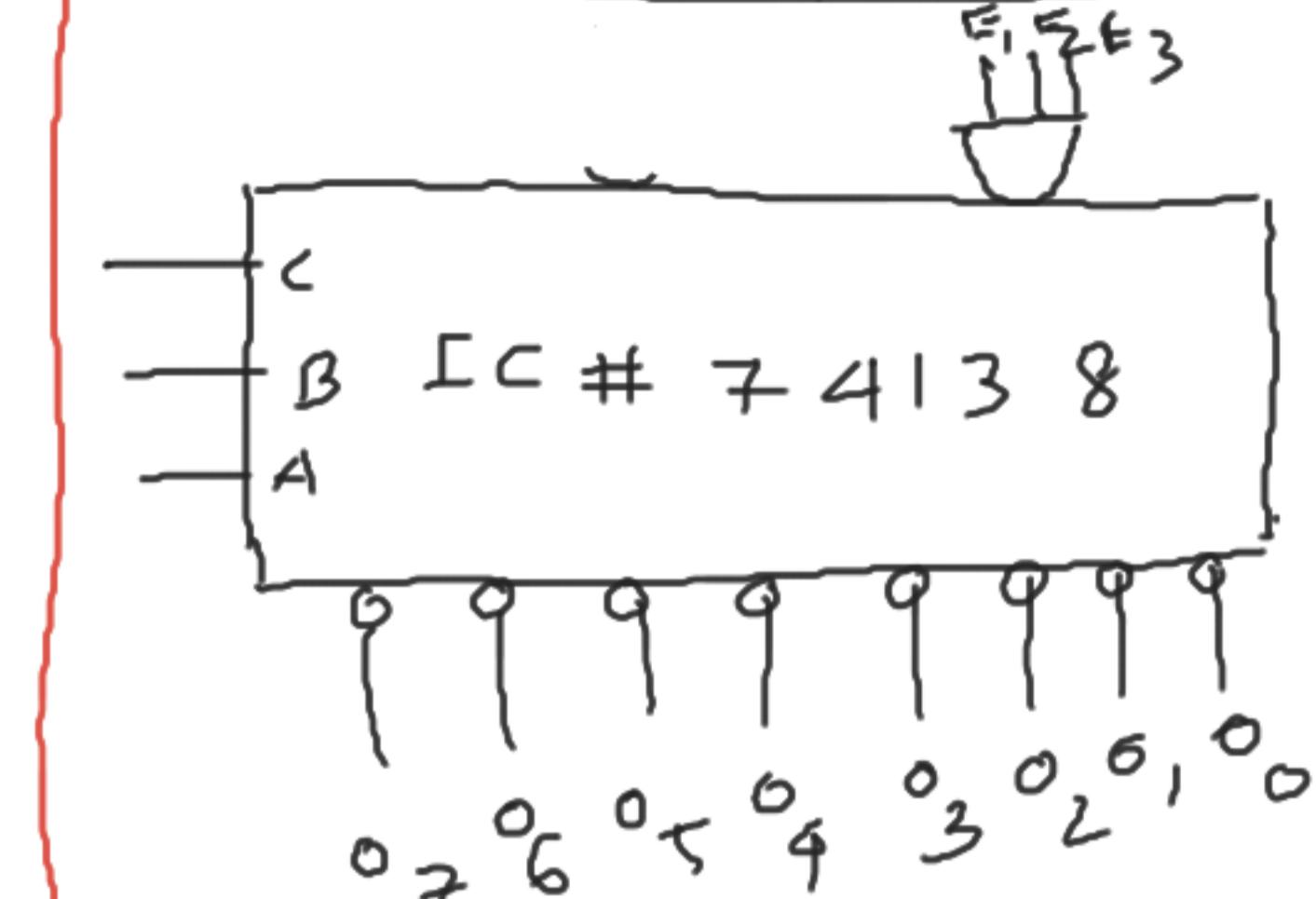
Inputs → A, B, C ; Outputs → O<sub>0</sub> to O<sub>7</sub>



IC # 74138 : Internal circuit:



Block diagram



✓ Active mode:  $E_1 = E_2 = 0, E_3 = 1$

✓ Other combination

↳ Inactive mode

$\{E_1 = 0, E_2 = 0, E_3 = 1\}$

$\{A = 1, B = 1, C = 0\}$

which output will be active?  $\rightarrow O_3$  is active

$\{E_1 = 0, E_2 = 1, E_3 = 0\}$  No one

$\{A = 0, B = 1, C = 1\}$  is active