PIPELINING CONCEPT IN 8086

Shaila Rahman

Assistant Professor

PIPELINING IN 8086

Pipelining is a concept according to which the processor is divided into some segments which can work in parallel and the instruction get partially processed during its journey through the pipe.

| T1 | T2 |

Fetch I1

Fetch I2 Execute I1

BIU and EU forms the instruction pipelining in 8086.

For N functional units the pipe get full speed at Nth clock period.

PIPELINING IN 8086

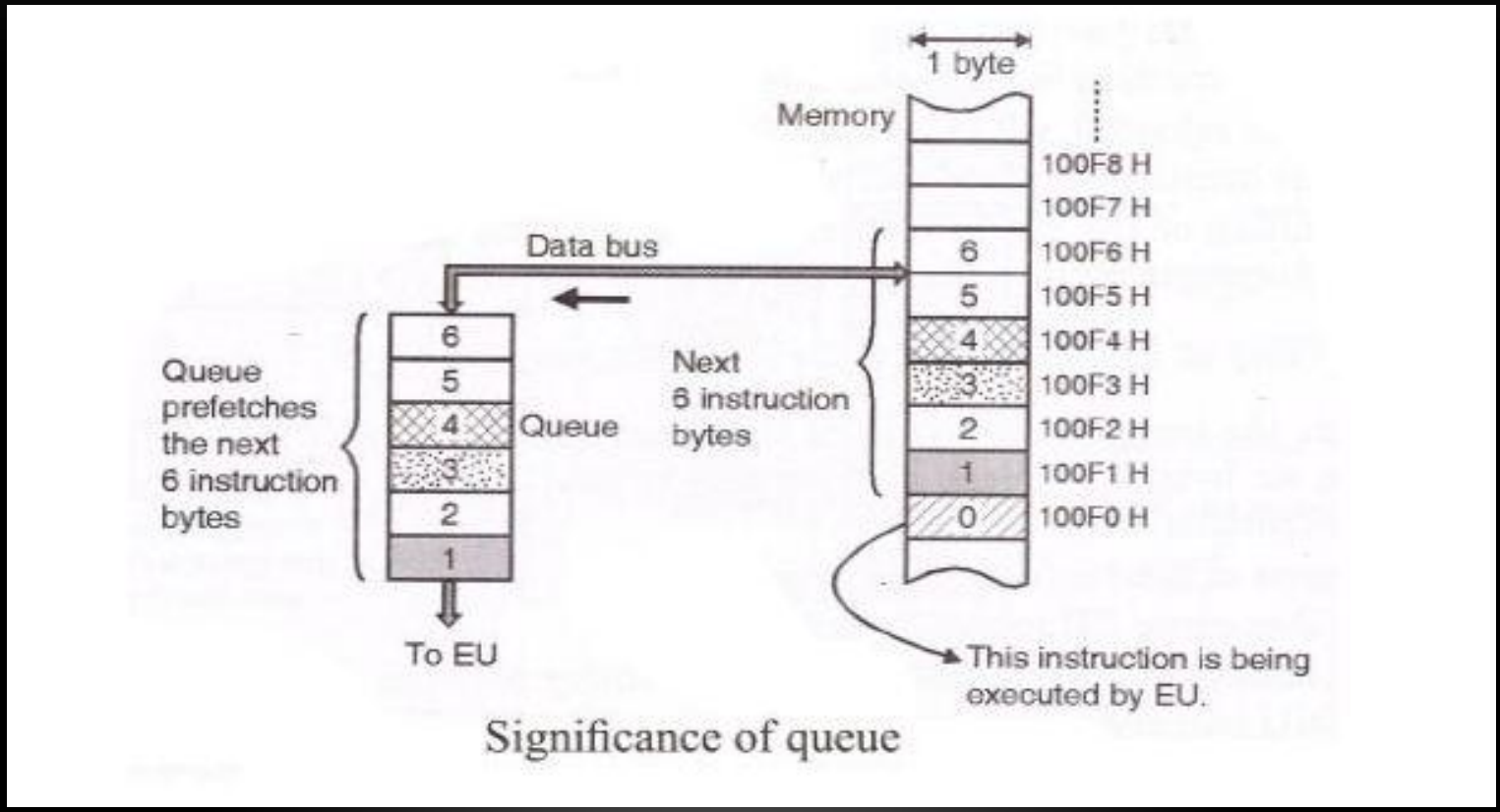
The process of fetching the next instruction when the present instruction is being executed is called as pipelining. Pipelining has become possible due to the use of queue. BIU (Bus Interfacing Unit) fills in the queue until the entire queue is full. BIU restarts filling in the queue when at least two locations of queue are vacant. Thus BIU needs at least two bytes empty space in queue for prefetching.

Except in the case of JMP and CALL instructions, where the queue must be dumped and then reloaded starting

ADVANTAGES OF PIPELINING

- The execution unit always reads the next instruction byte from the queue in BIU. This is faster than sending out an address to the memory and waiting for the next instruction byte to come.
- In short pipelining eliminates the waiting time of EU and speeds up the processing.

THE FOLLOWING DIAGRAM DEMONSTRATE THE PIPELINED FEATURE



Significance of queue

EXPLANATION

- As shown in the above figure, while the EU is busy in decoding the instruction corresponding to memory location 100F0, the BIU fetches the next six instruction bytes from locations 100F1 to 100F6 numbered as 1 to 6.
- These instruction bytes are stored in the 6 bytes queue on the first in first out (FIFO) basis.
- When EU completes the execution of the existing instruction and becomes ready for the next instruction,
- Thus the Queue will always hold the instruction bytes of the next instructions to be executed by the EU.

PROBLEM OF PIPELINING IN 8086

- During JMP instructions there is a problem related to pipeline. Any Jump calls non sequential instruction as BIU fetches sequentially.
- Queue needs to reset and refill with the branch reference instructions this time EU has to sit idle until one instruction is fetched.