



UNIVERSITY OF ASIA PACIFIC

Department of Computer Science & Engineering

Course Title – Digital Logic & System Design Lab

Course Code – CSE 210

Experiment No. – 04 (part - ii)

Experiment name – Adder & Sub-tractor with #IC-7483 & Full Adder.

SUBMITTED BY

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Date of Performance – 09-01-2021

Date of Submission – 16-02-2021

PROBLEM STATEMENT:

- d. Design 4-bit Adder- Subtractor using #IC-7483
- e. Design a 4-bit Full Adder with Logic gate.

OBJECTIVE: The objective of the experiment is to design Adder & Subtractor at a time using #IC-7483 and design Adder & Subtractor with Full Adder.

APPARATUS:

- IC-7408(AND Gate)
- IC-7432(OR Gate)
- IC-7404(NOT Gate)
- IC-7486(X-OR)
- IC-7483(4-bit Parallel Adder)
- Logic Display
- Logic Switch

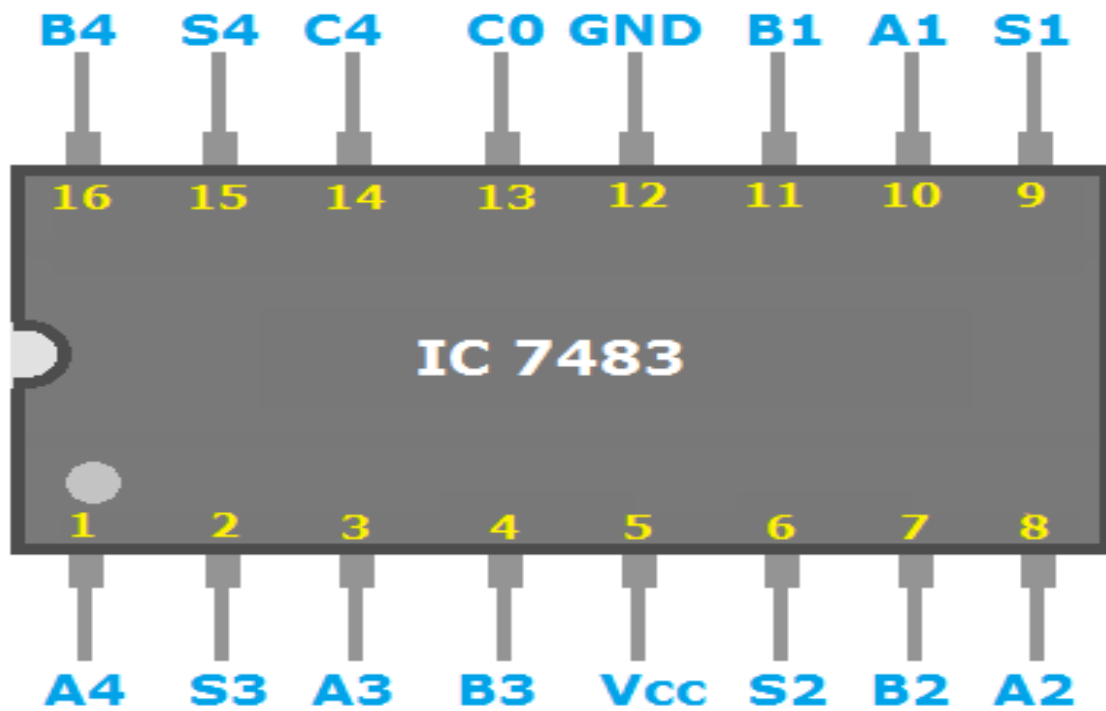
INTRODUCTION:

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units or ALU.

To use IC-7483 as an Adder & Subtractor at a time, we have to use XOR gate. We just have to connect the inputs of B with XOR gate as 1st input of XOR gate, and the 2nd input of those XOR gate will be 1 and Carry-in will be 1. In subtractor the S₄ or the Carry-out will count as Carry Bit. IC 7483 is a 4 bit parallel adder which consists of four interconnected full adders along with the look ahead carry circuit.

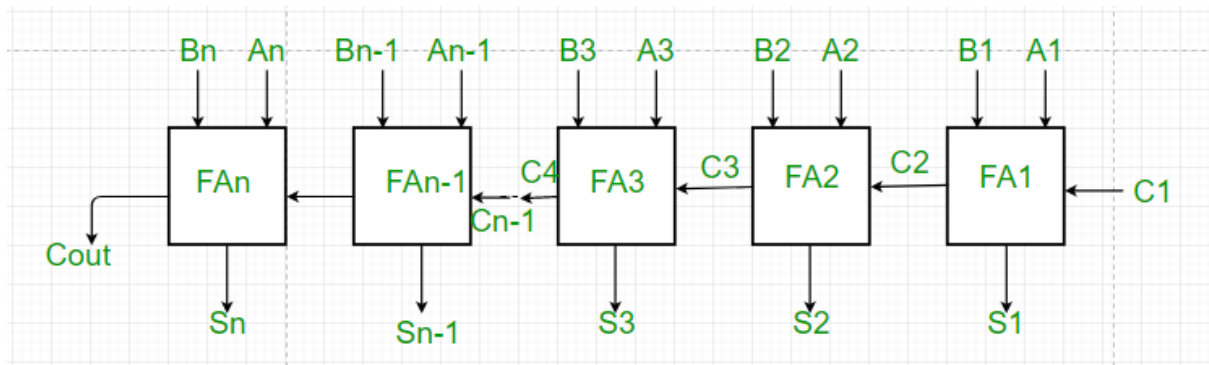
We will design adder-subtractor with full adders.

PIN CONFIGURATION:



IC 7483 Pin Diagram

BLOCK DIAGRAM:



OPERATION:

ADDER

C ₅	C ₄	C ₃	C ₂	C ₁
	A ₄	A ₃	A ₂	A ₁
+	B ₄	B ₃	B ₂	B ₁
<hr/>				
S ₅	S ₄	S ₃	S ₂	S ₁

SUBTRACTOR

C ₅	C ₄	C ₃	C ₂	C ₁
	A ₄	A ₃	A ₂	A ₁
+	$\overline{B_4}$	$\overline{B_3}$	$\overline{B_2}$	$\overline{B_1}$
+				1
<hr/>				
S ₅	S ₄	S ₃	S ₂	S ₁

❖ ADDER + SUBTRACTOR

Addition Operation: $C_{in} = 0$.

$$\begin{array}{r}
 A = 14 \rightarrow 1 \ 1 \ 1 \ 0 \\
 B = 11 \rightarrow 1 \ 0 \ 1 \ 1 \\
 \hline
 1 \ 1 \ 1 \ 0 \\
 + 1 \ 0 \ 1 \ 1 \\
 \hline
 1 \ 1 \ 0 \ 0 \ 1
 \end{array}$$

$14 + 11 = 25$

$(1 \ 1 \ 0 \ 0 \ 1)_2 = (25)_{10}$

Subtraction Operation: $C_{in} = 1$.

$$\begin{array}{r}
 A = 15 \rightarrow 1 \ 1 \ 1 \ 1 \\
 B = 10 \rightarrow 1 \ 0 \ 1 \ 0
 \end{array}$$

Binary of 10	1	0	1	0		1	1	1	1	
One's complement	0	1	0	1		+	0	1	1	0
Two's complement			+	1						
	0	1	1	0						

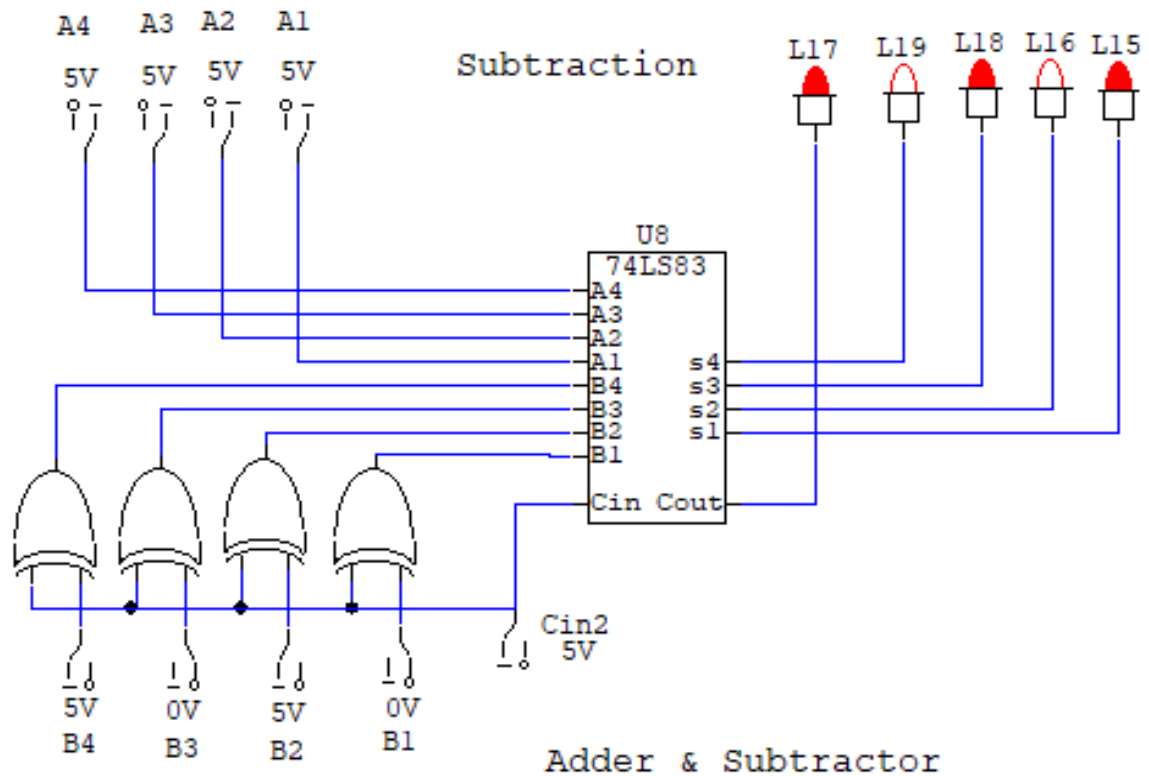
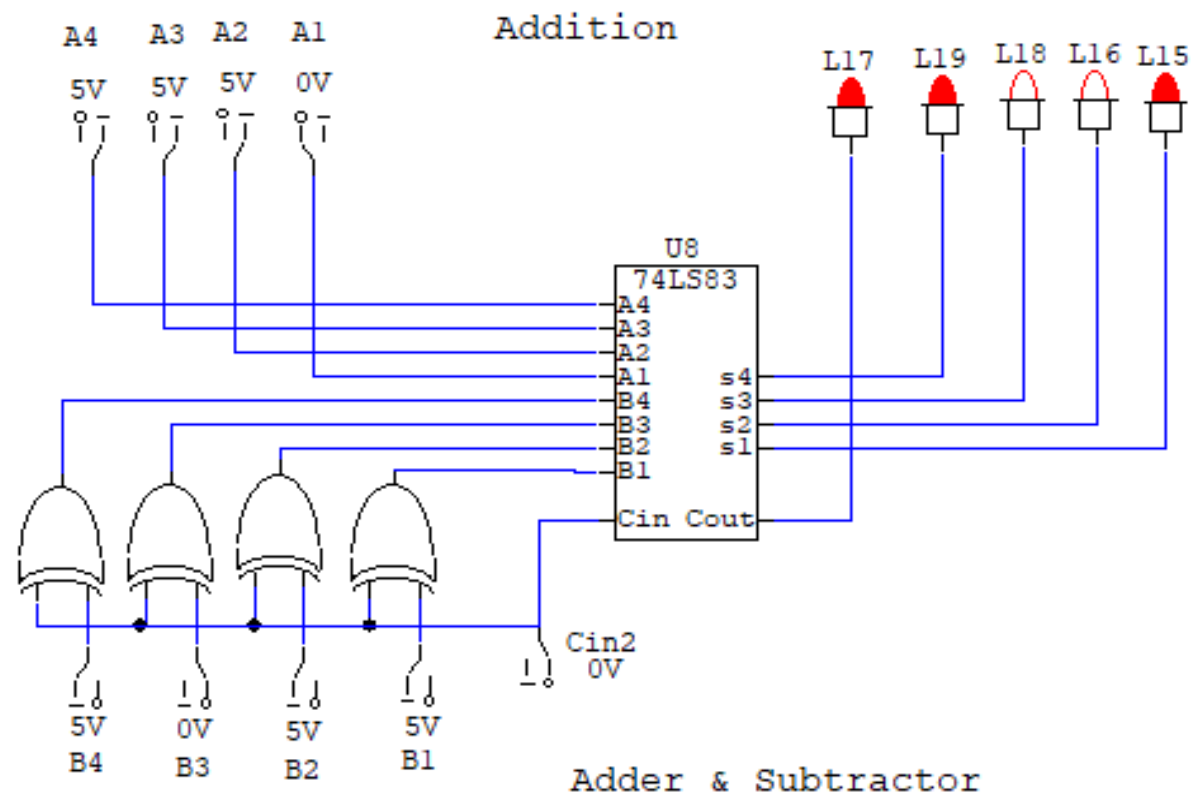
Carry Bit

In subtraction the carry bit will not be counted. So the output will be

$(0 \ 1 \ 0 \ 1)_2 = (5)_{10}$

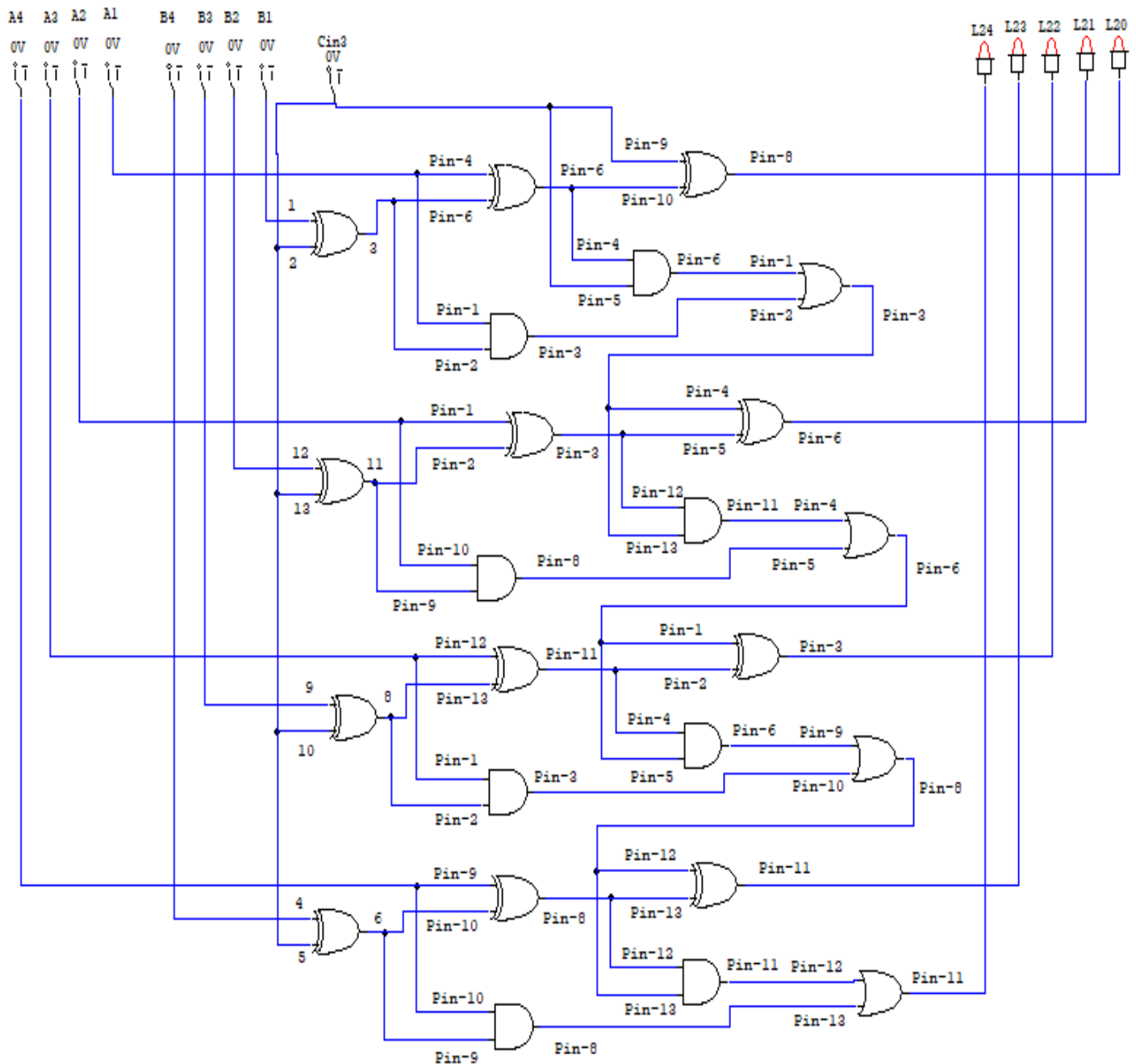
$A - B = 15 - 10 = 5$

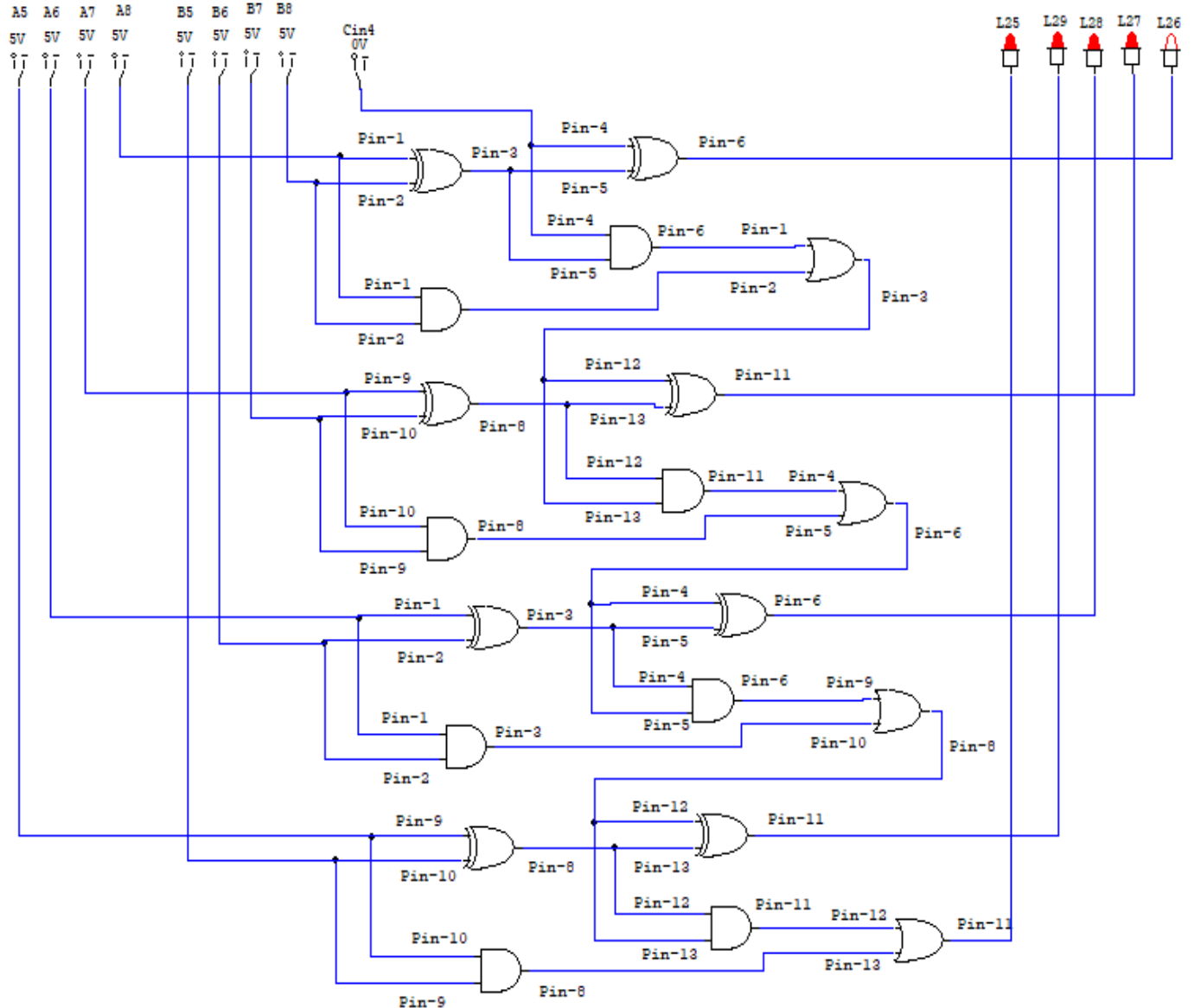
CIRCUIT DIAGRAM:



❖ DESIGNING 4-BITS FULL ADDER WITH LOGIC GATES

CIRCUIT DIAGRAM:





DISCUSSION: In this experiment discussed about 4 bit parallel adder. We have used 4-bit parallel adder IC#7483 for Addition and Subtraction at a time. We also designed 4-bit parallel adder-subtractor with full adder.