Department of Computer Science & Engineering

University of Asia Pacific (UAP)

Program: B.Sc. in Computer Science and Engineering

Final Examination	**Fall 2020**	**2nd Year 2nd Semester**
Course Code: CSE 209	**Course Title: Digital Logic & System Design**	**Credits: 4**
Full Marks: 120* (Written)		**Duration: 2 Hours**

* Total Marks of Final Examination: 150 (Written: 120 + Viva: 30)

Instructions:

1. There are **Four (4)** Questions. Answer all of them. All questions are of equal value. Part marks are shown in the margins.
2. Non-programmable calculators are allowed.

1. a) Implement the following function using K-map.

$$F(A, B, C, D) = \sum(0, 1, 2, 5, 7, 9, 10, 12, 13, 14, 15)$$ 10

b) Design a logic circuit that follows the following requirements:
(i) Output X will be logical equivalent to (A AND D) when B and C are different. 10
(ii) X will remain HIGH when B and C are the same.

c) Draw the block diagram of 4 bit ALU chip (IC# 74382) and label the all inputs & outputs. Describe 8(Eight) operations of the 4 bit ALU chip that perform by select input. 10

OR

a) Draw the block diagram of IC# 74293(Counter). Using this implement MOD 700 counter. 10

b) Design MOD 12 Johnson counter using JK flip-flop and describe its operation. 10

c) Design a BCD adder using IC # 7483 (4-bit parallel adder) and NAND gates only. Briefly describe its operation. 10

2. a) What are the difference between arithmetic and logical operation? What types of operation are possible in SAP-1 Computer? 4

b) Write down the instruction set and the corresponding op-code of SAP-1 Computer. 5

c) How many operations are possible in SAP-1 computer? Explain your answer. 5

d) Create a SAP-1 assembly language program and then generate the machine code for the expression of 52 + 28 - 38 + 72 - 12. These numbers are in decimal form. 16

3. **a)** Design a synchronous counter using J-K FFs that has the following sequence: 000, 010, 100, 110, 111 and repeat. The undesired (unused) states 001, 011 and 101 must always go to 000 on the next clock pulse. 20

b) i) What are the values of J and K so that the J-K flip-flop can operate as a toggle FF (changes states on each clock pulse)? Then apply a 10-kHz clock signal to its CLK input and determine the frequency of the waveform at Q (output of J-K flip-flop). 05

ii) Connect Q from this FF to the CLK input of a second J-K FF that also has same value of J and K of the first FF. Determine the frequency of the signal at this FF's output.

c) Consider a counter circuit that contains five FFs wired in the arrangement Q_4, Q_3, Q_2, Q_1, Q_0. 05

i) Determine the counter's MOD number.

ii) Determine the output frequency in Hz when the input clock frequency is 10-kHz.

iii) What is the range of counting states for this counter?

iv) Assume a starting state (count) of 01011. What will be the counter's state after 243 pulses?

4. **a)** Implement the function F(A, B, C, D) = ∑(0, 1, 2, 5, 7, 8, 10, 12, 14, 15) using only one IC# 74151(Multiplexer). You can use other universal logic gate, if necessary. 12

b) Show how IC# 74151 can be used to generate the logic function y = AC` + A`B + B`C. 08

c) In the figure below, the signal Sub and some XOR gates alter the 4-bit parallel adder (IC # 7483) inputs. 10

i) Describe the operation of the circuit when Sub = 1.

ii) Describe the operation of the circuit when Sub = 0.