
# UNIVERSITY OF ASIA PACIFIC

## Department of Computer Science & Engineering

**Course Title** – Digital Logic & System Design

**Course Code** – CSE 209

**Assignment** – 02

**Topic** – Designing MOD-10 asynchronous UP/DOWN counter using JK Flip Flop. Use other logic gates if necessary. . Briefly explain the operation.

**Submitted by:**

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**Section** – A

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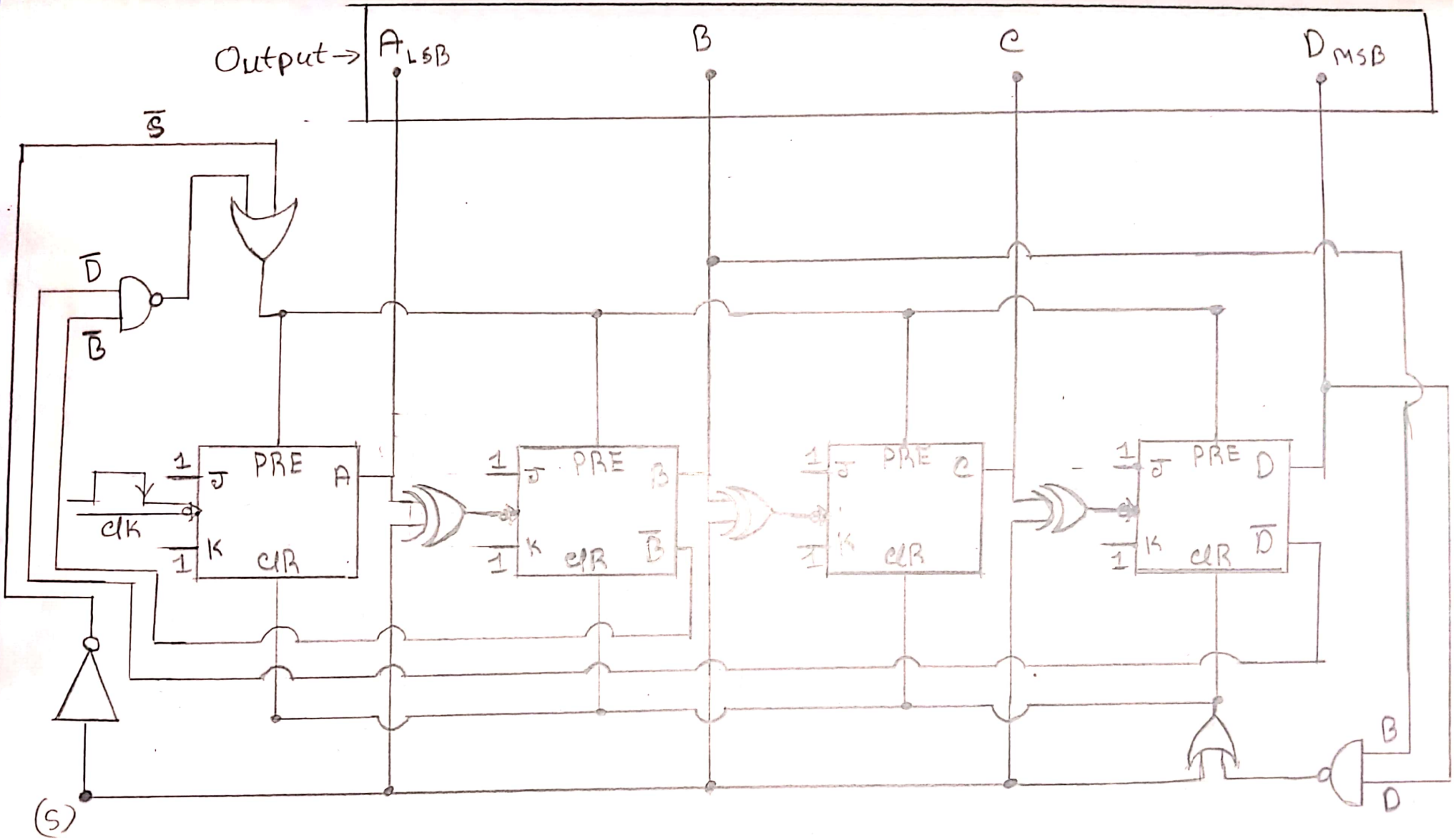


Initially A=B=C=D=0

| D | C | B | A | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | |
| 0 | 0 | 0 | 1 | PRE=1 |
| 0 | 0 | 1 | 0 | |
| 0 | 0 | 1 | 1 | clR=1 |
| 0 | 1 | 0 | 0 | |
| 0 | 1 | 0 | 1 | |
| 0 | 1 | 1 | 0 | |
| 0 | 1 | 1 | 1 | |
| 1 | 0 | 0 | 0 | |
| 1 | 0 | 0 | 1 | |
| 1 | 0 | 1 | 0 | PRE=1 clR=0 |

operation:

If S=0, then 2nd pulse = A

3rd pulse = B

4th pulse = C

For S=0, PRE = 1.

So, For (0 to 9) PRE=1, As either B or D is 0, so clR=1

∴ Normal clock operation.

At 10, PRE = 1 and as B=D=1, clR=

∴ A=B=C=D=0

so it comes 0 0 0 0

∴ It count from 0 to 9

so it is Mod-10 upcounter.

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| D | C | B | A | |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | |
| 1 | 1 | 1 | 0 | PRE=1 |
| 1 | 1 | 0 | 1 | |
| 1 | 1 | 0 | 0 | clR=1 |
| 1 | 0 | 1 | 1 | |
| 1 | 0 | 1 | 0 | |
| 1 | 0 | 0 | 1 | |
| 1 | 0 | 0 | 0 | |
| 0 | 1 | 1 | 1 | |
| 0 | 1 | 1 | 0 | |
| ⋮ | | | | PRE=0 |
| 0 | 1 | 0 | 1 | clR=1 |

If S=1, then 2nd pulse = $\overline{A}$

3rd pulse = $\overline{B}$

4th pulse = $\overline{C}$

For S=1, clR=1.

From (15 to 6) clR=1, As either B or D is 1, PRE = 1

For 5 : B=D=0, so, PRE=0

clR=1

∴ All outputs are 1

so A=B=C=D ⇒ 1

so, it counts from (15 to 6)

So it is Mod-10 down-counter.