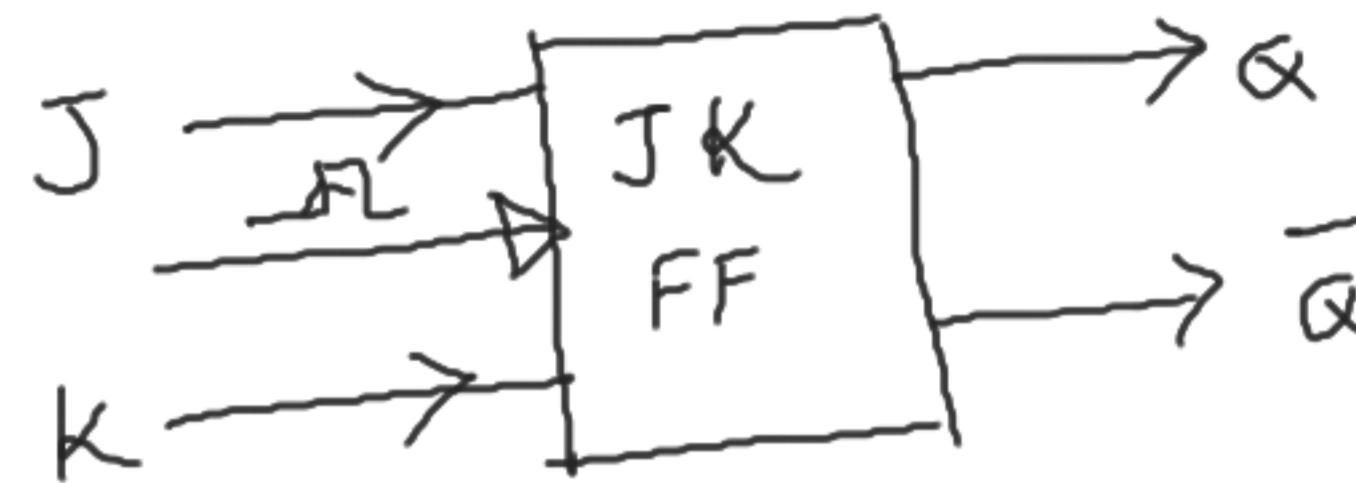
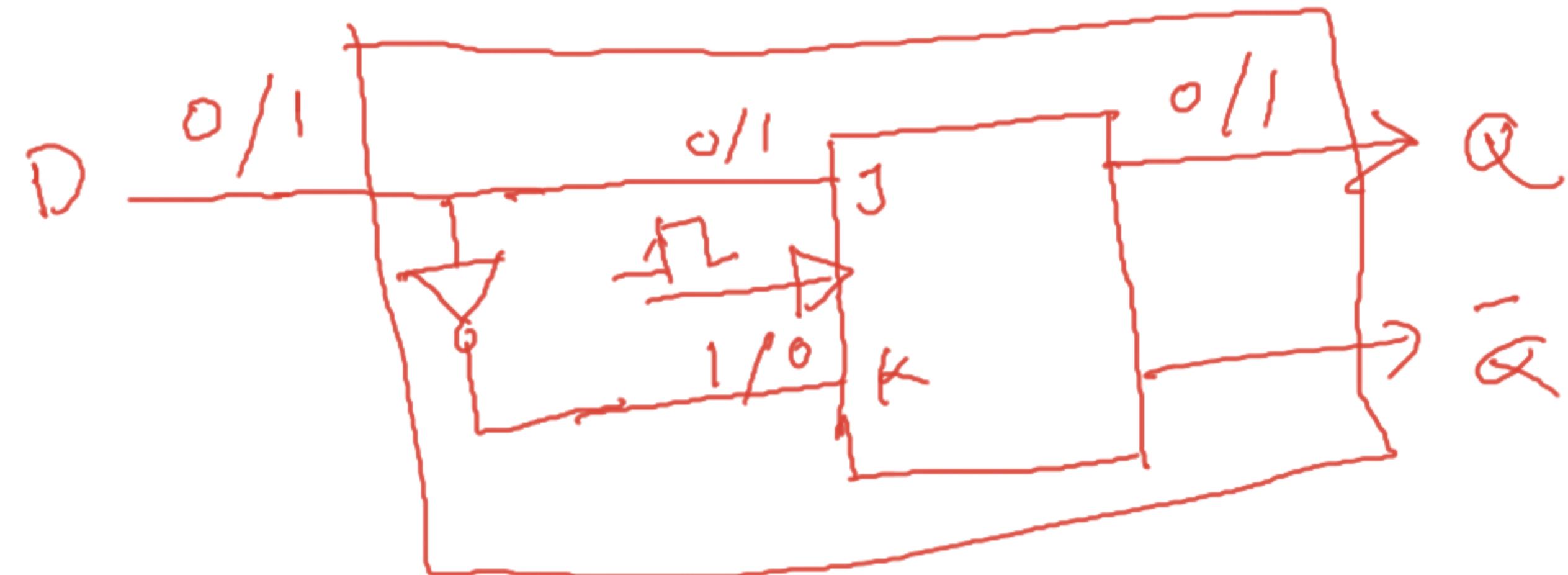
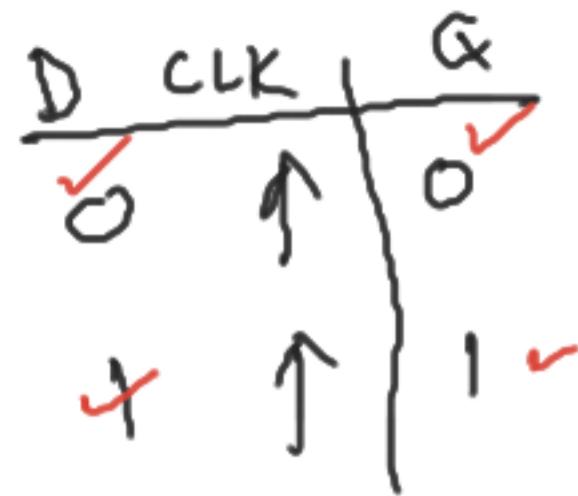


How to convert JK Flip Flop to D Flip Flop:

JK Flip Flop:



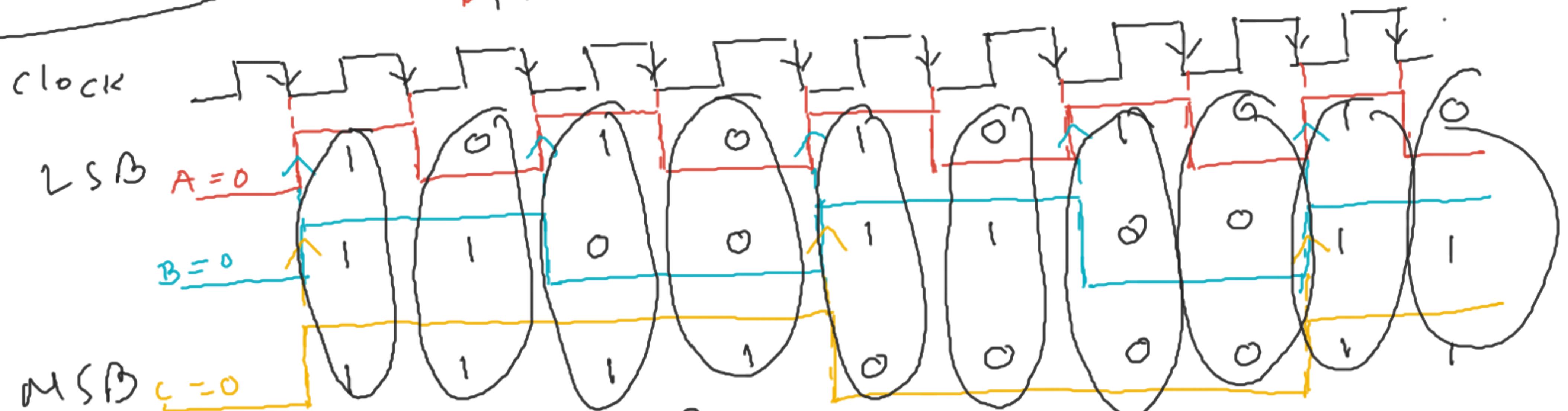
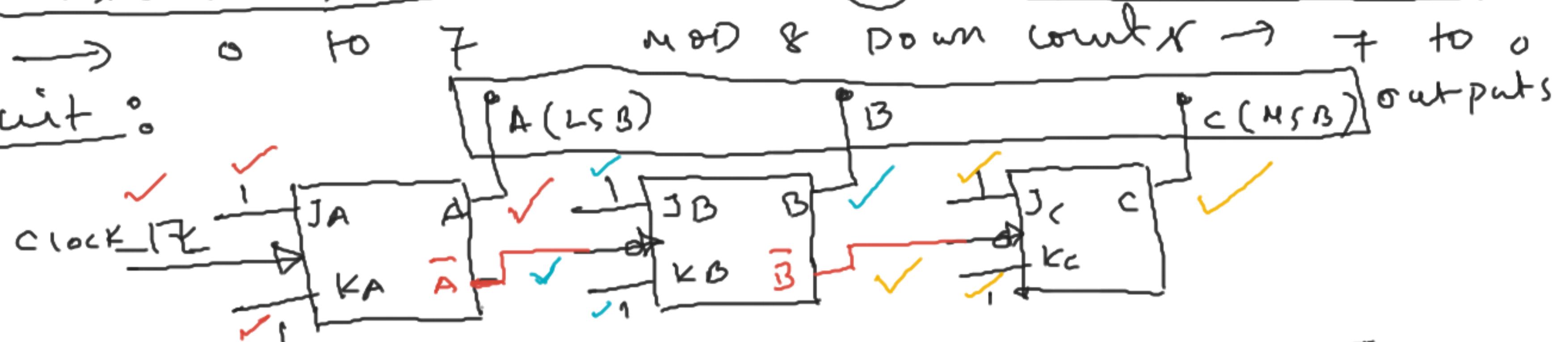
D Flip Flop:



Design MOD 8 Down asynchronous counter using JK Flip Flop:

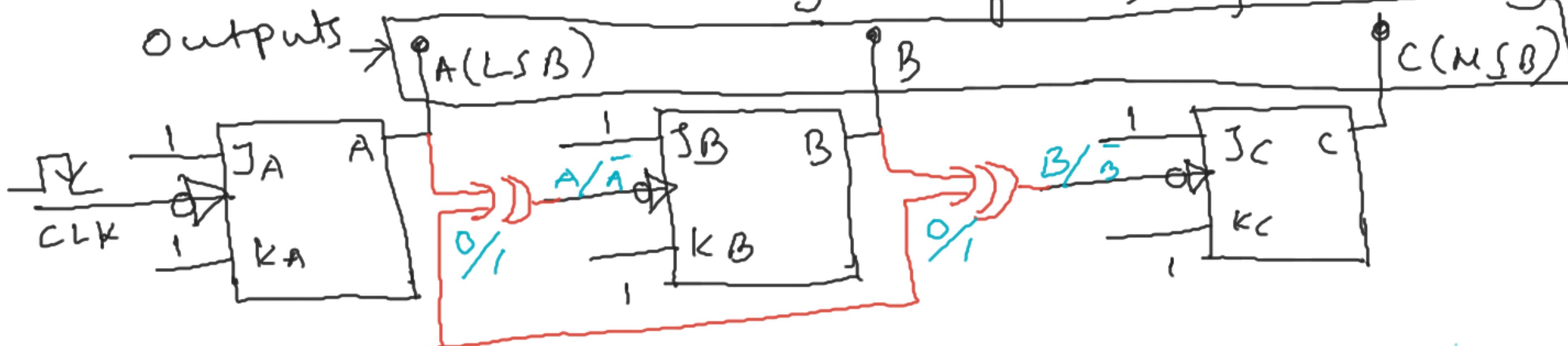
MOD 8 Up counter \rightarrow 0 to 7
 Internal circuit:

Initially
 $A = B = C = 0$



It counts from 7 to 0
 ∴ This is MOD 8 Down counter

Design MOD 8 UP/DOWN N counter using JK Flip Flop.
 You can use other logic gates, if necessary.



O/I
switch(s)

operations :-

{ If $S = 0$

Then 2nd pulse = A
 3rd " = B

∴ This is mod 8 up counter

If $S = 1$

Then 2nd pulse = \bar{A}
 3rd " = \bar{B}

∴ This is mod 8 down counter

Q5)

$$\text{Input frequency} = 256 \text{ kHz}$$

" " = 2 kHz

a) Output frequency = $\frac{\text{Input frequency}}{\text{Mod numbers}}$

$2 = \frac{256}{\text{Mod number}}$

$\therefore \text{Mod numbers} = \frac{256}{2}$
 $= \underline{\underline{128}}$

b) Range = 0 to 127

Q 6)

0 to 1023

a) $1024 = 2^N$
 $2^{10} = 2^N$

$N = 10$
Number of ffs = 10

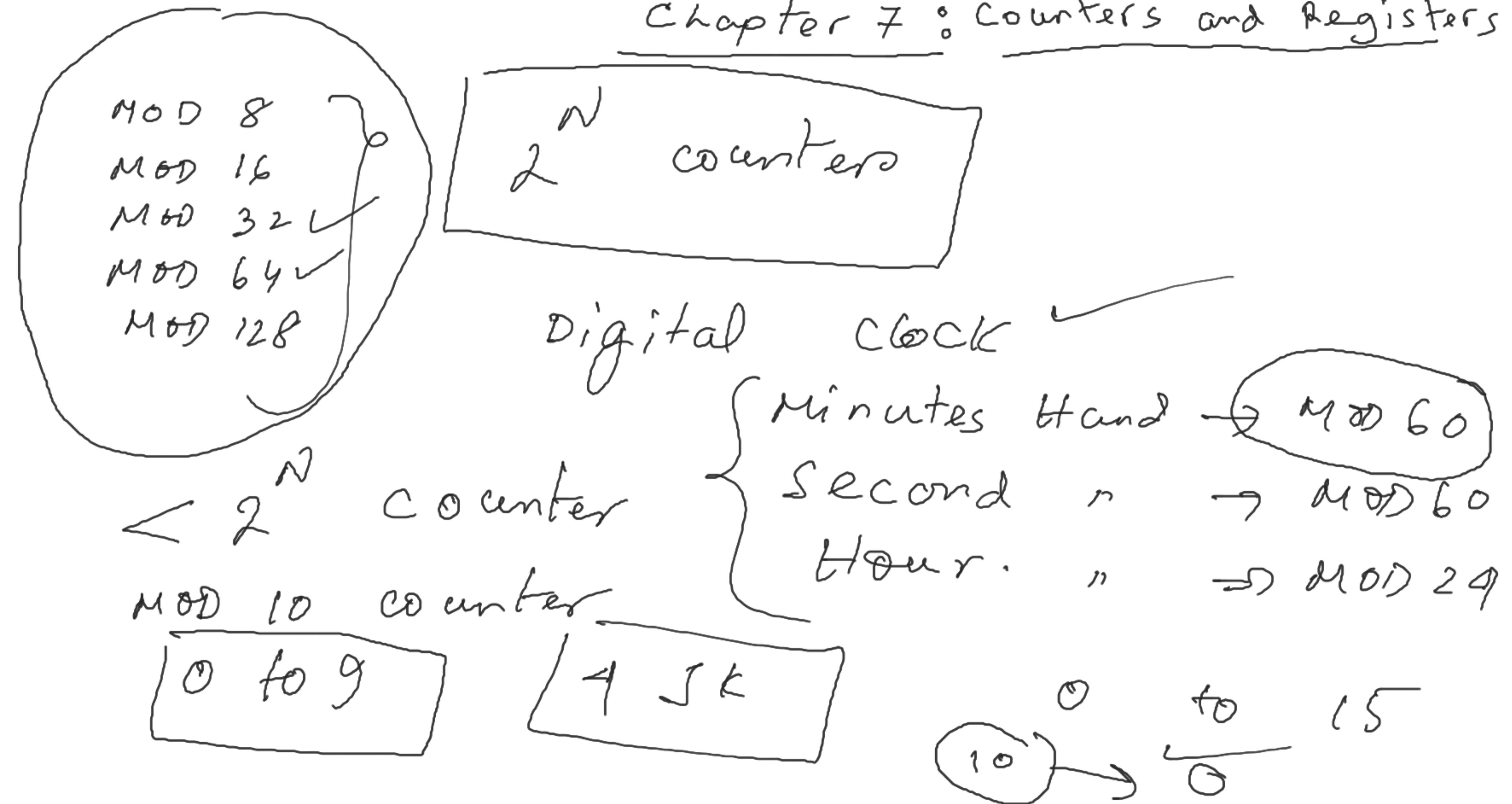
c) Mod number = 1024

d) $2060 \div 1024$
 $= [000000100]$ ✓

b) Output frequency = $\frac{2 \times 10^6 \text{ Hz}}{1024}$
= 1953.125
Hz

004 | 2060 | 2
2048 |
12

Chapter 7 : Counters and Registers

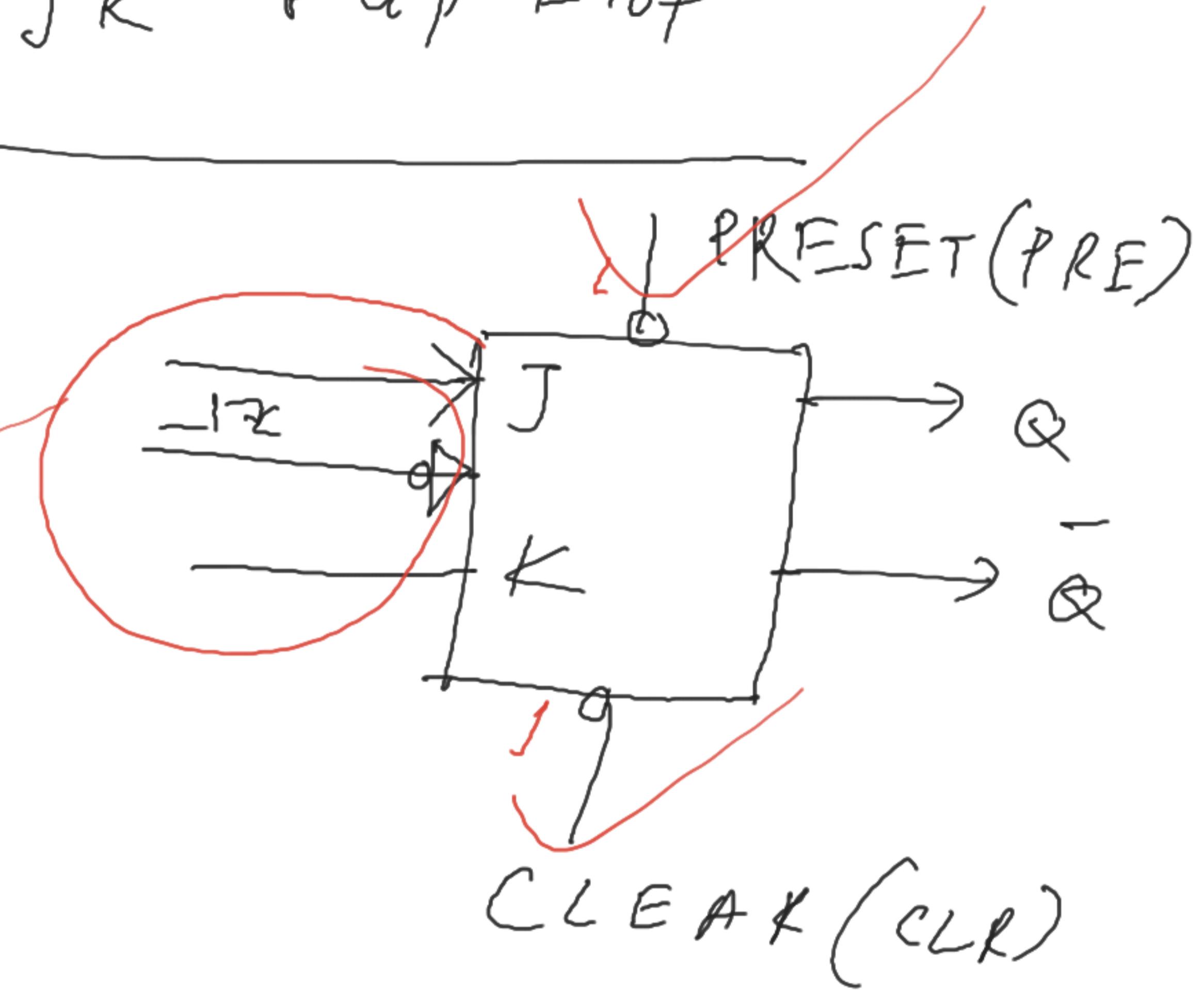


Asynchronous inputs JK Flip Flop

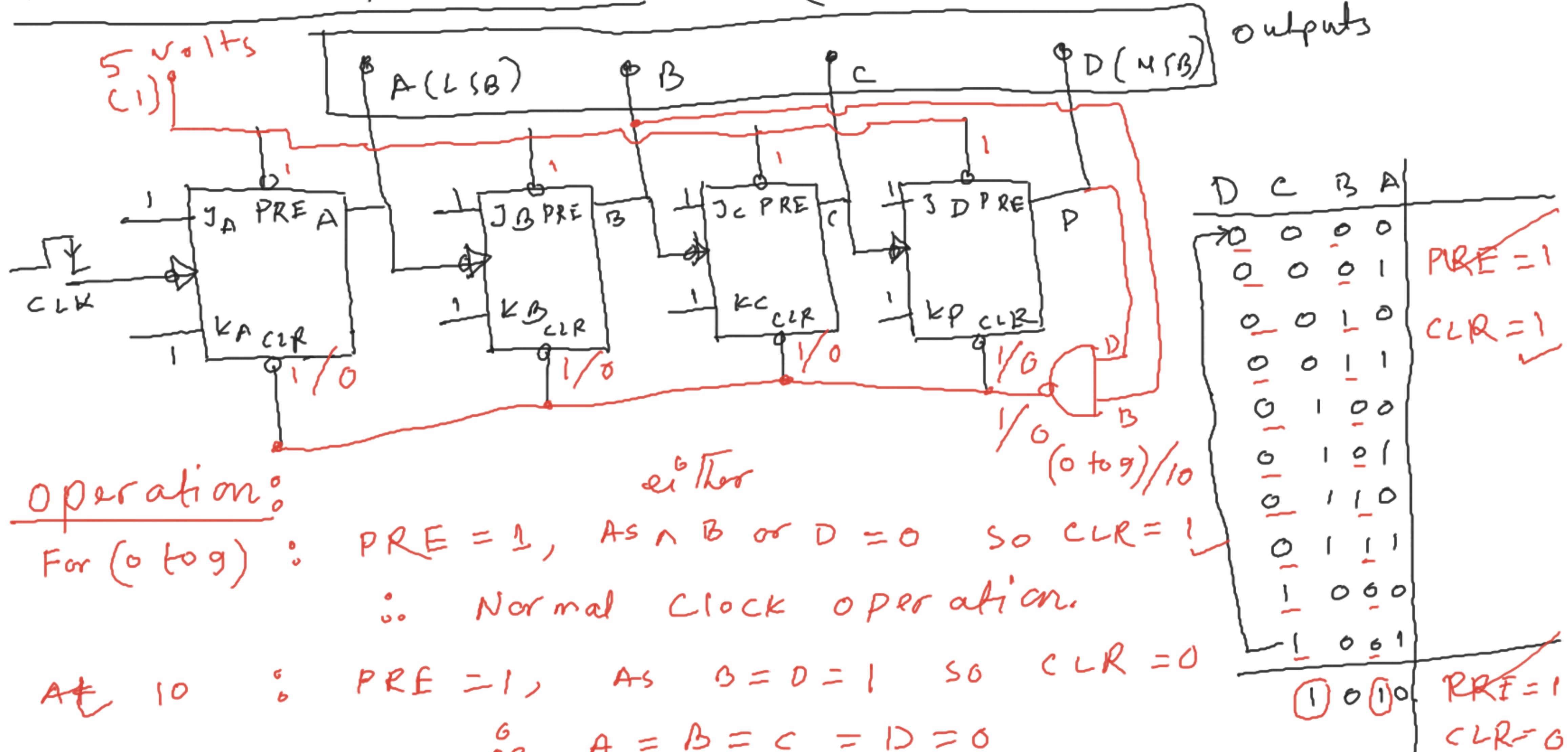
Truth Table

<u>PRE</u>	<u>CLR</u>	<u>Q</u>
0	0	Not used
0	1	$Q = 1$
1	0	$Q = 0$

Normal clock operation



MOD 10 Asynchronous Up Counter : (0 to 9)



Operation:

For (0 to 9) : PRE = 1, AS \wedge B or D = 0 so CLR = 1
 \therefore Normal CLOCK operation.

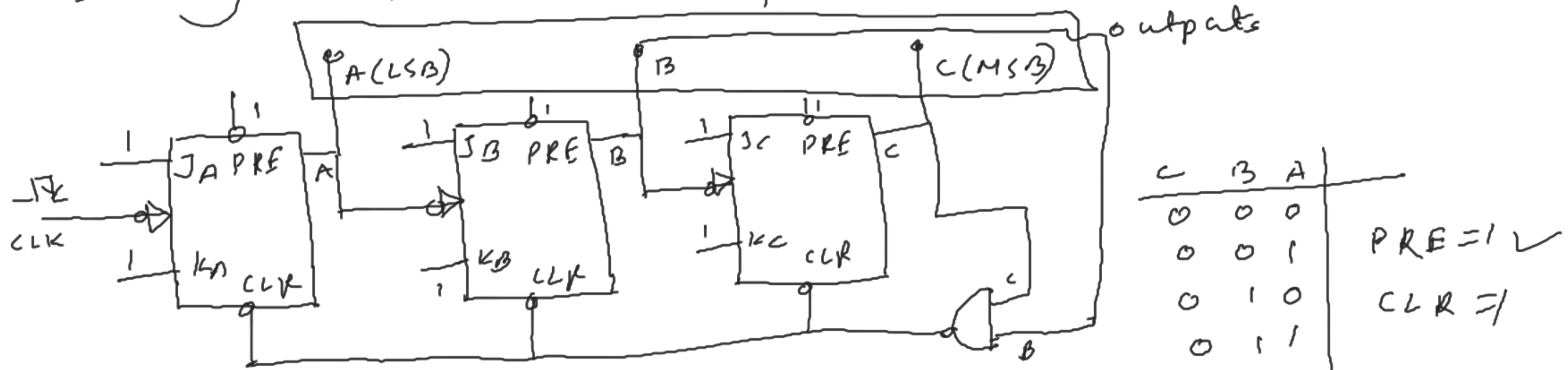
At 10 : PRE = 1, AS B = D = 1 so CLR = 0

\therefore A = B = C = D = 0
 so if comes 0000

\therefore The counter counts from 0 to 9.

D	C	B	A	RRF = 1
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	
1	0	0	1	RRF = 1
1	0	1	0	CLR = 0

Design MOD 6 ^{asynch} Up counter using JK Flip Flop.
 You can use other logic gates, if necessary.
 Briefly explain the operation.



operation:

From 0 to 5 \Rightarrow $PRE = 1$; as either
 B or $C = 0$, so $CLR = 1$

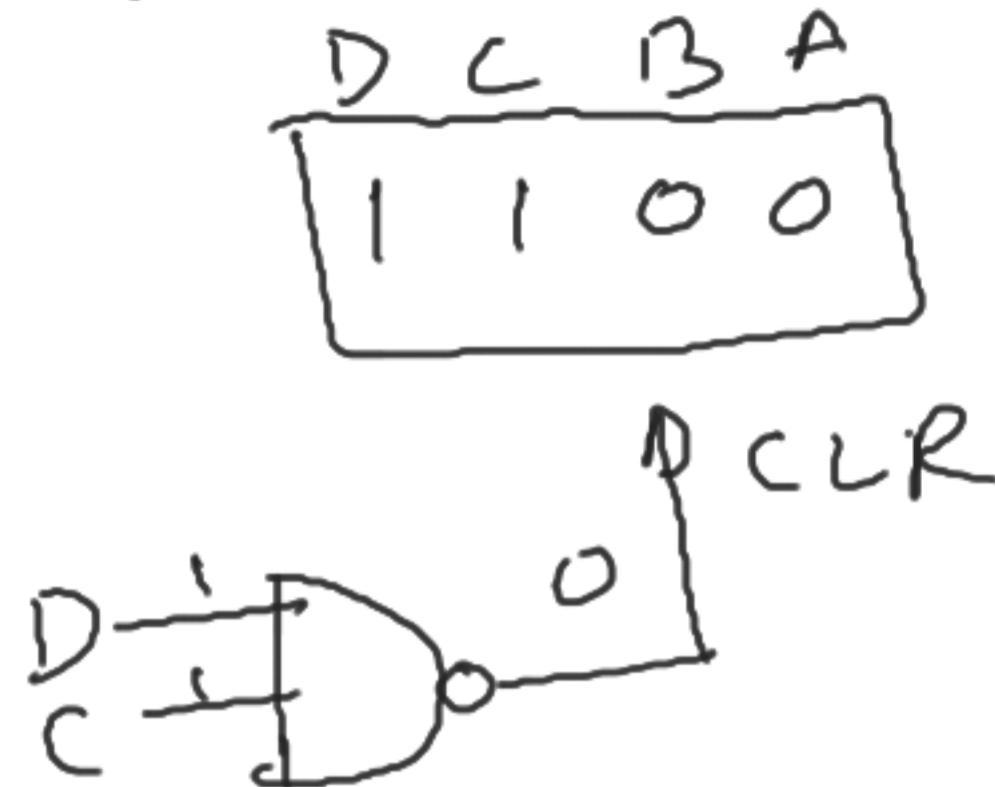
\therefore Normal clock operation

For 6 \Rightarrow $PRE = 1$; as $B = C = 1 \therefore CLR = 0$
 $\therefore A = B = C = 0 \therefore$ it counts 000
 \therefore This counts from 0 to 5.

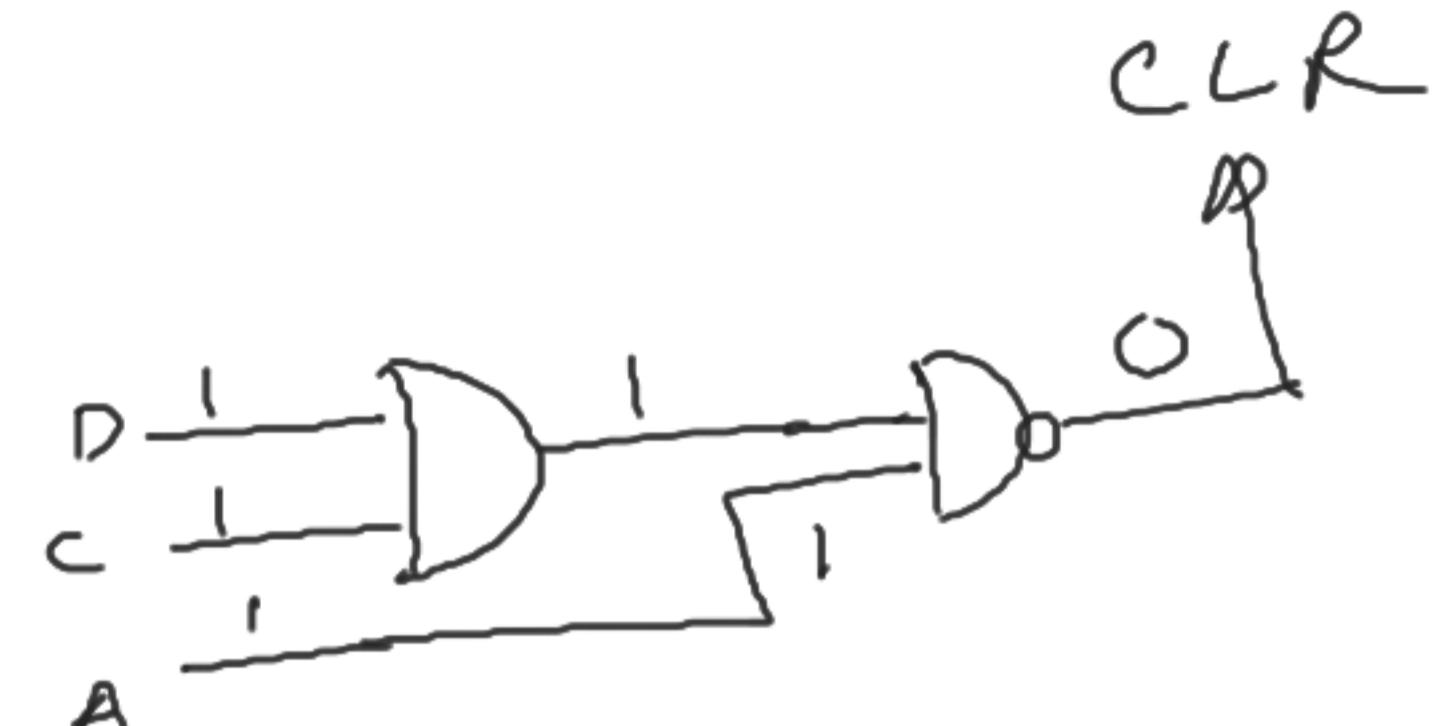
C	B	A	
0	0	0	$PRE = 1$
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	$CLR = 1$

1	0	1	$PRE = 1$
1	1	0	$CLR = 0$

MOD 12

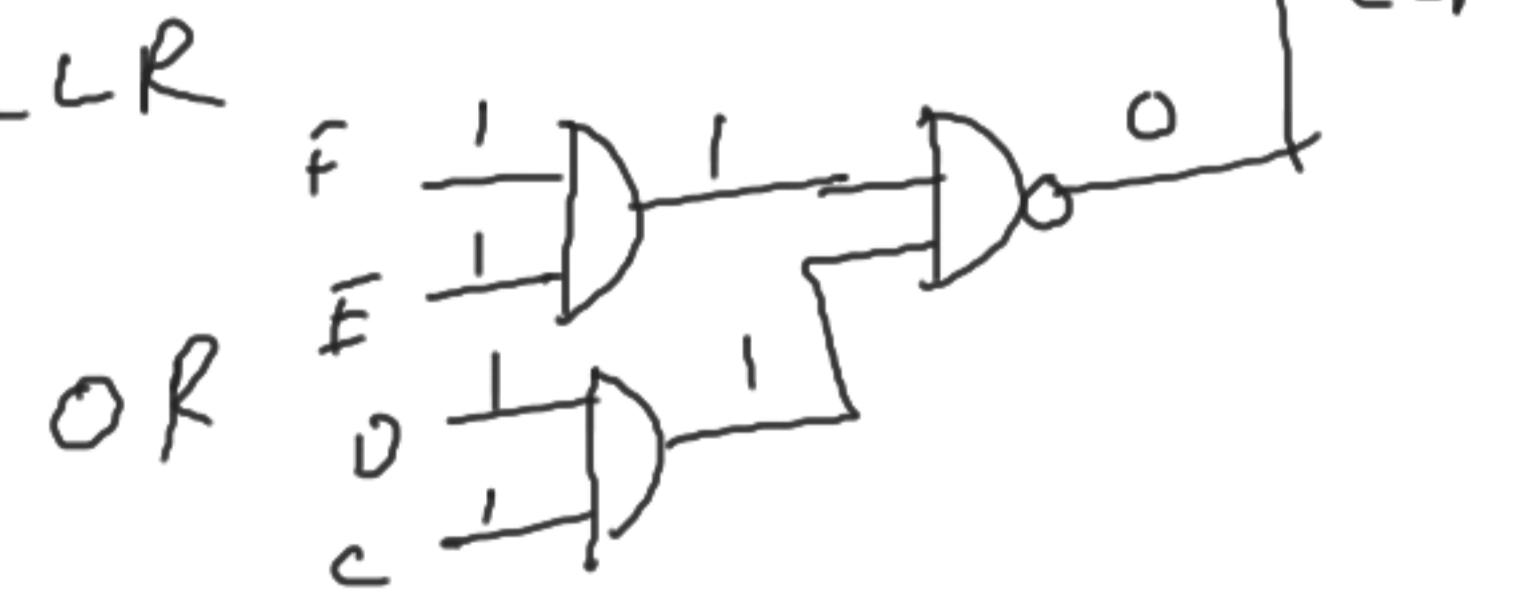
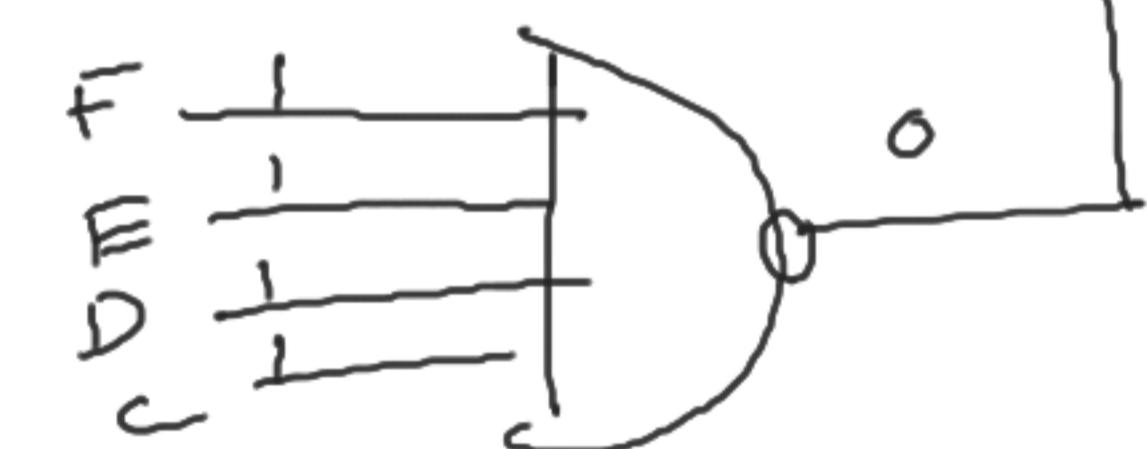


MOD 13
DCBA
1101

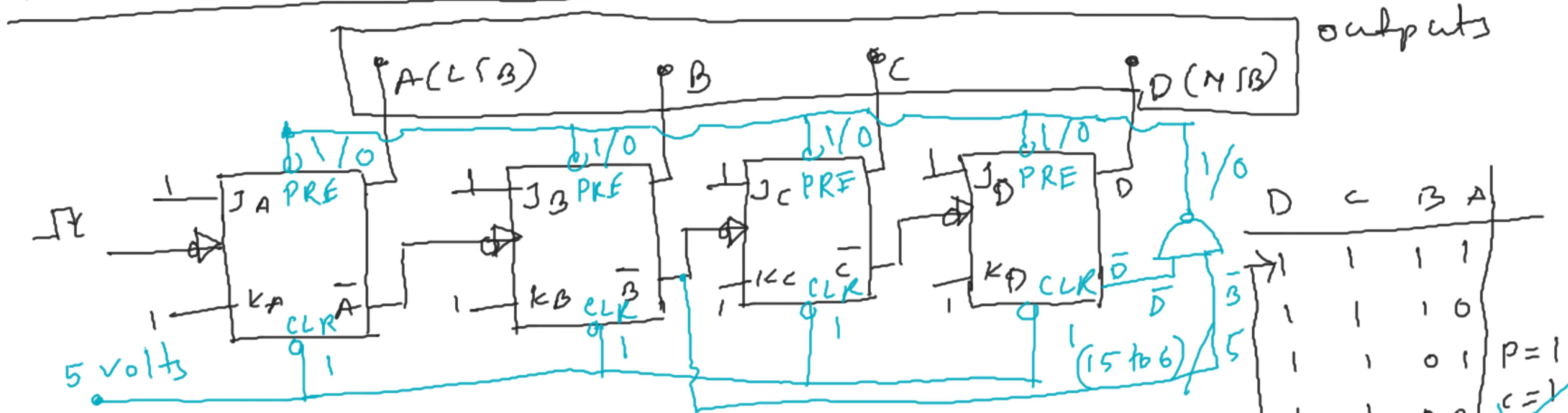


MOD 60

F E D C B A
1 1 1 1 0 0



Mod 10^4 down counter:



operation:

From 15 to 6: either B or D comes 1 $\therefore \text{PRE} = 1$
and $\text{CLR} = 1$

\therefore This is normal clock operation

For 5: $B = D = 0 \therefore \text{PRE} = 0, \text{CLR} = 1$

\therefore All outputs are 1
 $A = B = C = D = 1$

\therefore It counts from 15 to 6 \therefore It is a mod 10 down counter

Assignment 2: Design MOD 10 ^{asynchronous} a UP/Down counter using JK Flip Flop. You can use other logic gates, if necessary. Briefly explain the operation.

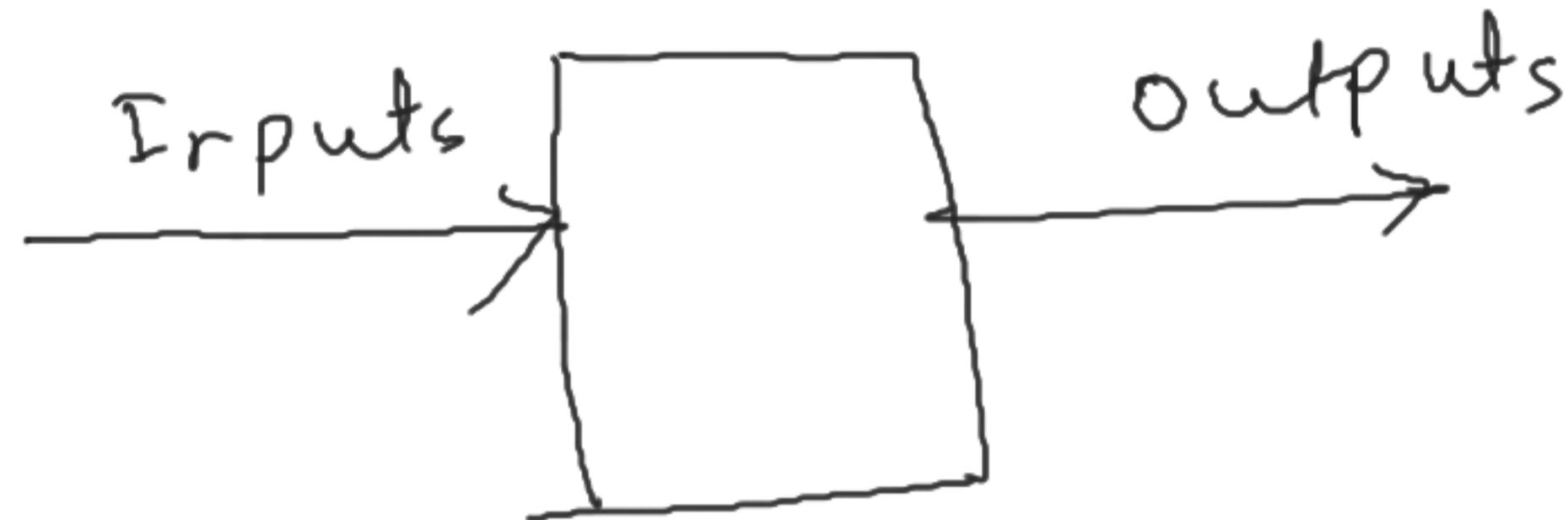
within

16.02.2021 (11:59 pm)

switch(s)

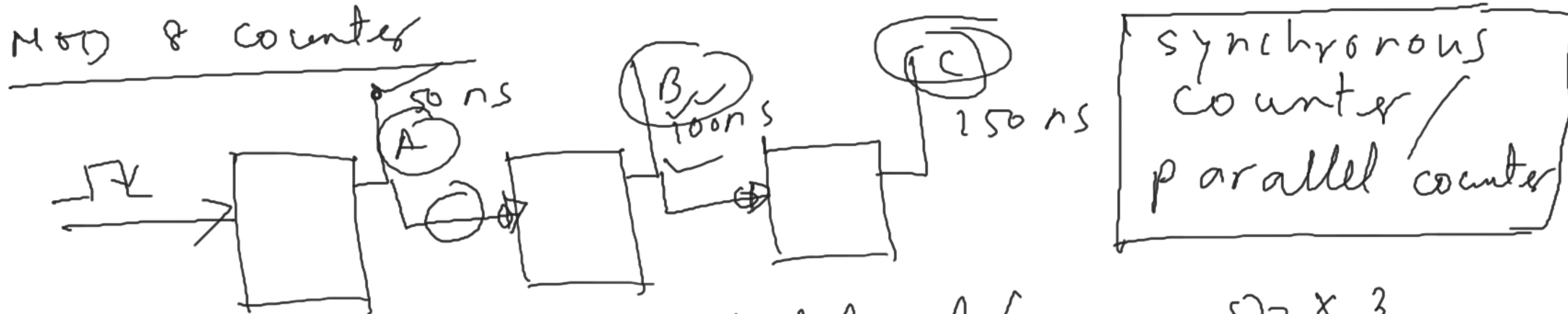
{
 |
 |
 $s = 0$ UP Counter
 $s = 1$ Down Counter

Propagation delay (t_{pd}) : For any device to give the inputs and response for outputs, it takes some time. This time is called propagation delay.



AND gate $\Rightarrow t_{pd} = 20 \text{ ns}$
 $= 20 \times 10^{-9} \text{ sec}$ & it is denoted

JK flip flop $\Rightarrow t_{pd} = 50 \text{ ns}$ by t_{pd}
 $= 50 \times 10^{-9} \text{ sec}$

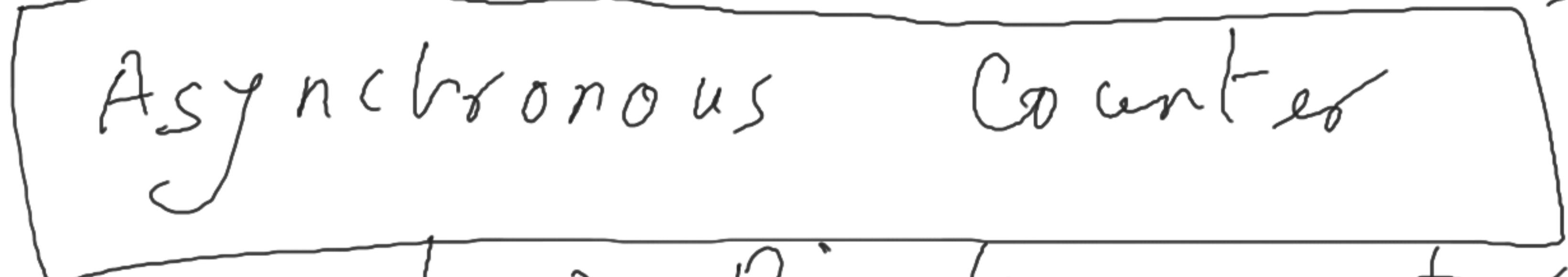


Mod 8 counts \Rightarrow

$$\begin{aligned} \text{total delay} &= 50 \times 3 \\ &= 150 \text{ ns} \end{aligned}$$

mod 16 counts \Rightarrow

$$\begin{aligned} &\quad \text{11} \quad \text{17} \\ &= 50 \times 4 \\ &= 200 \text{ ns} \end{aligned}$$



In general:

For asynchronous counter

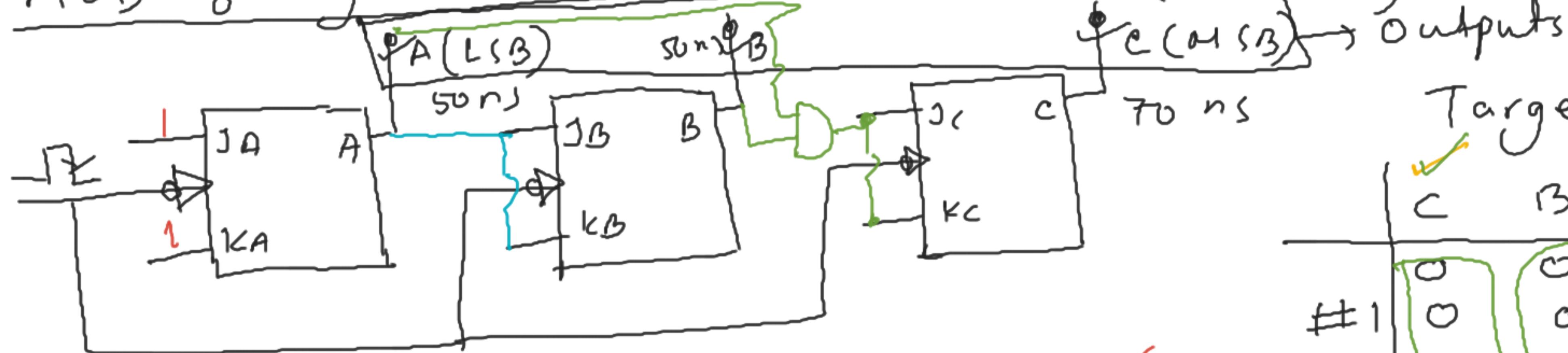
Total delay = (t_{pd} for one JK Flip Flop) \times
Number of flip flop

For MOD 1024 counter

Total delay = 50 ns \times 10
= 50 ns

Synchronous / Parallel counter:

MOD 8 synchronous up counter: (0 to 7)



operation: Initially $A = B = C = 0$

#1 : A is always Toggle. $J_A = k_A = 1$

#2 : At $A = 0$ Then

At $A = 1$ Then

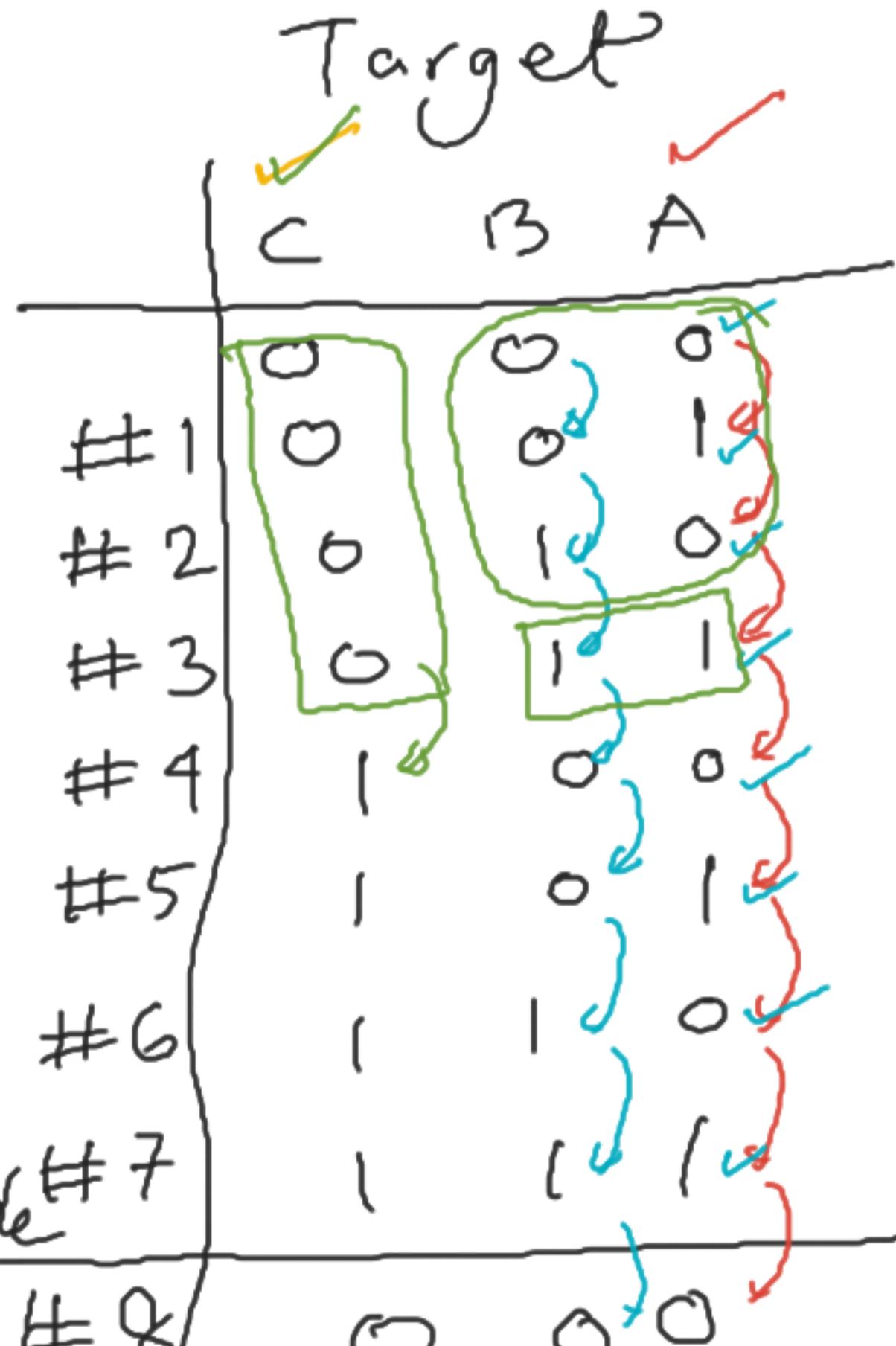
$\therefore J_B = k_B = A$

#3 : If $A = B = 1$ Then
otherwise Then

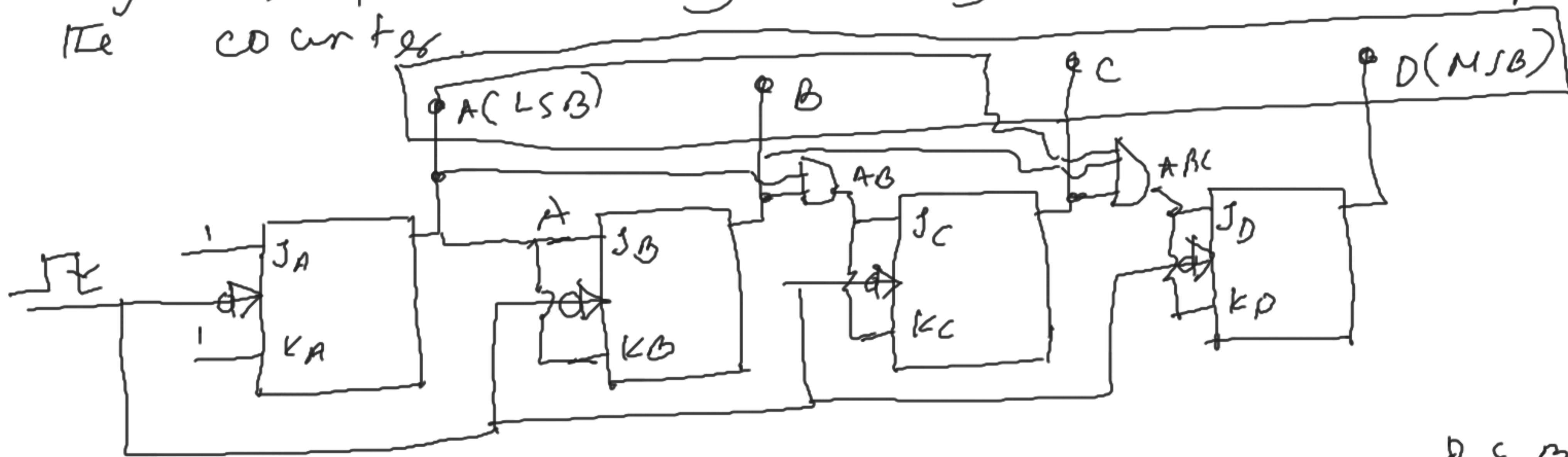


	J	K	clk	Q
#1	0	0	↑	NC
#2	0	1	↓	0
#3	0	0	↑	1
#4	1	0	↓	1
#5	1	0	↑	0
#6	1	1	↓	1
#7	1	1	↑	0
#8	0	0	↓	0

Toggle



Draw the circuit diagram of mod 16 synchronous up counter using JK flip flop. You can use other logic gates, if necessary. Briefly describe the operation of the counter.

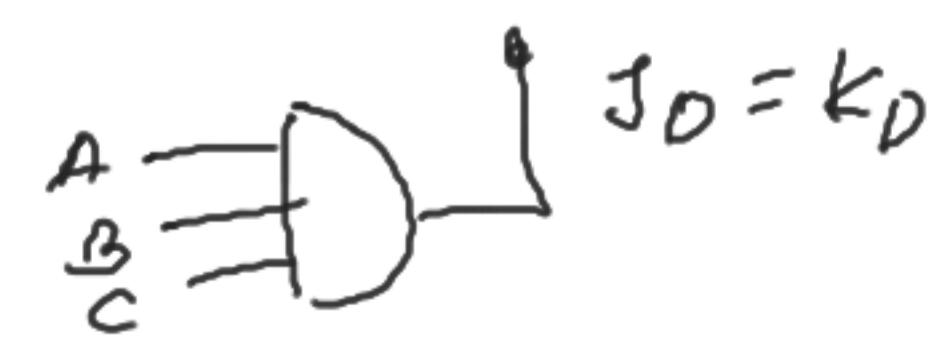


D C B A

D⁰: when $A = B = C = 1$ Then $J_D = K_D$

otherwise

$$J_D = K_D = ABC$$



Propagation delay of synchronous counter:

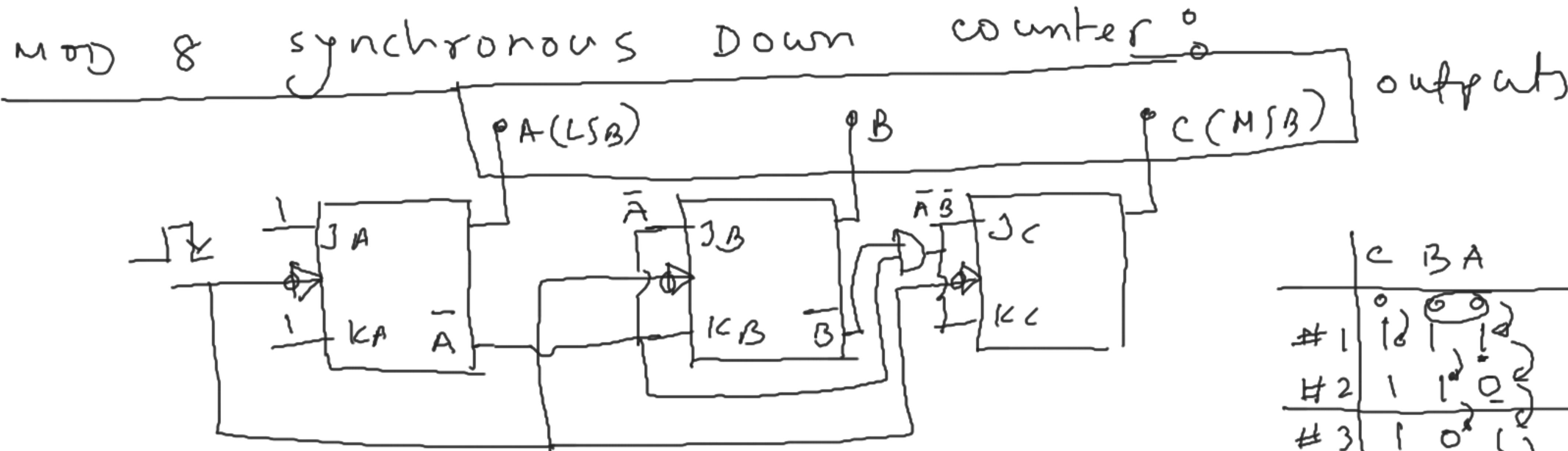
For MOD 8 counter: Total delay = $50 + 20 = 70 \text{ ns}$

for MOD 16 " : Total delay = $50 + 20 = 70 \text{ ns}$

In general:

For synchronous counter

Total delay = t_{pd} for one JK + t_{pd}
for one AND gate



Initially $A = B = C = 0$

operation

$A \Rightarrow A$ is always toggle $\therefore J_A = K_A = 1$

$B \Rightarrow \begin{cases} \text{when } A = 1 & J_B = K_B = 0 \\ \text{, } & A = 0 & J_B = K_B = 1 \end{cases}$

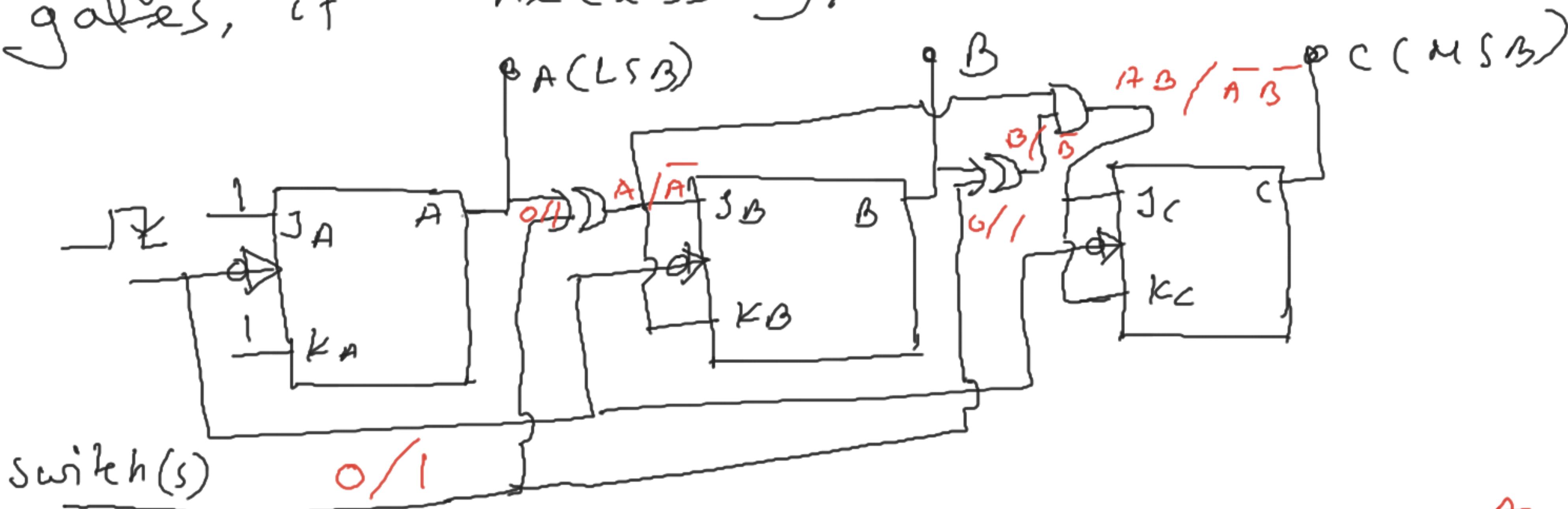
$C \Rightarrow \text{when } A = B = 0$

or otherwise

$J_C = K_C = \bar{A} \bar{B}$

	C	B	A
#1	0	0	0
#2	1	1	0
#3	1	0	1
#4	0	0	0
#5	0	1	1
#6	0	1	0
#7	0	0	1
#8	0	0	0

Design MOD 8 synchronous up/Down counter using JK flip flop. You can use other logic gates, if necessary.



operation: If $S = 0$ Then $J_B = K_B = A$
 $J_C = K_C = A\bar{B}$
so it is up counter

If $S = 1$ Then $J_B = K_B = \bar{A}$
 $J_C = K_C = \bar{A}\bar{B}$
∴ This is down counter.