INTEL 8086 MICROPROCESSR ARCHITECTURE

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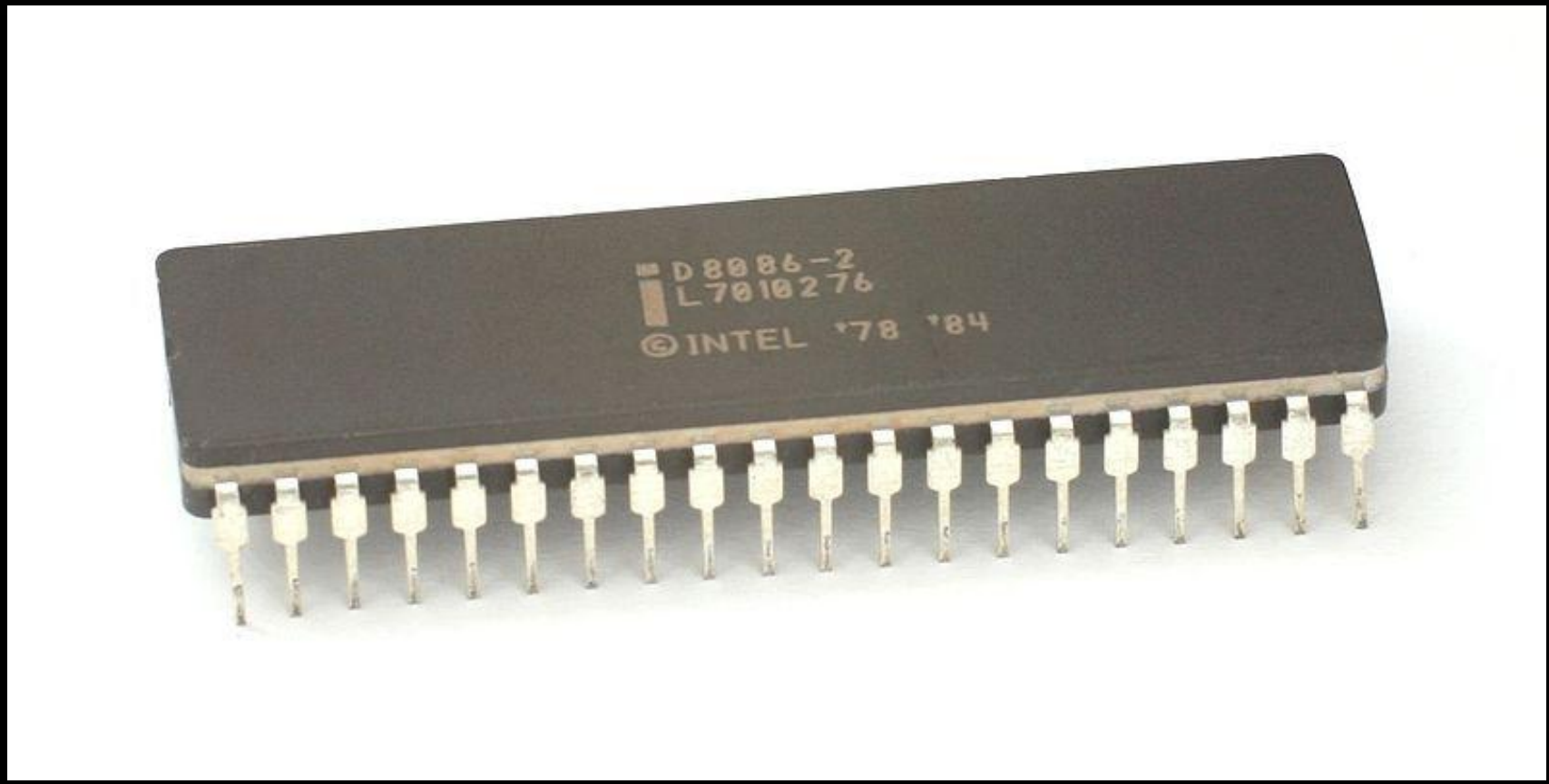
INTEL 8086 MICROPROCESSORS

The **8086** is a 16-bit microprocessor chip designed by Intel between early 1976 and mid-1978, when it was released. The 8086 gave rise to the x86 architecture of Intel's future processors.

INTEGRATED CHIP- 8086



8086 FEATURES

1. 8086 microprocessor usually the 16-bit version of 8080 microprocessor.
2. ALU and internal register set all are 16-bit.
3. Data bus is 16-bit .
4. Address bus is 20-bit.
5. Direct Addressing Capability 1 MB (2^{20}) of Memory.
6. **It can support up to 64K (2^{16}) I/O ports**
7. **It provides 14, 16 -bit registers**
8. **It has multiplexed address and data bus AD0- AD15 and A16 – A19.**
9. Memory is organized as an array of bytes.
10. Memory is segmented.

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11. Architecture Designed for Powerful Assembly Language and Efficient High Level Languages.
12. 8 and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal is applicable including multiplication and division.
13. Power supply is 5v.
14. External clock signal generator 8284 is used.
15. **Word size is 16 bits and double word size is 4 bytes.**

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16. Range of clock Rates:
    5 MHz for 8086,
    8 MHz for 8086-2,
    10 MHz for 8086-1
17. MULTIBUS System Compatible Interface.
18. The CPU is implemented in N-Channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin DIP or plastic package.
19. The 8086 operates in both single processor and multiple processor configurations to achieve high performance levels
20. **8086 is designed to operate in two modes, Minimum and Maximum.**

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21. **It can Prefetches up to 6 instruction bytes from memory and queues them in order to speed up instruction execution.**
22. **A 40 pin dual in line package.**
23. **Address ranges from 00000H to FFFFFH**

INTEL 8086 INTERNAL ARCHITECTURE

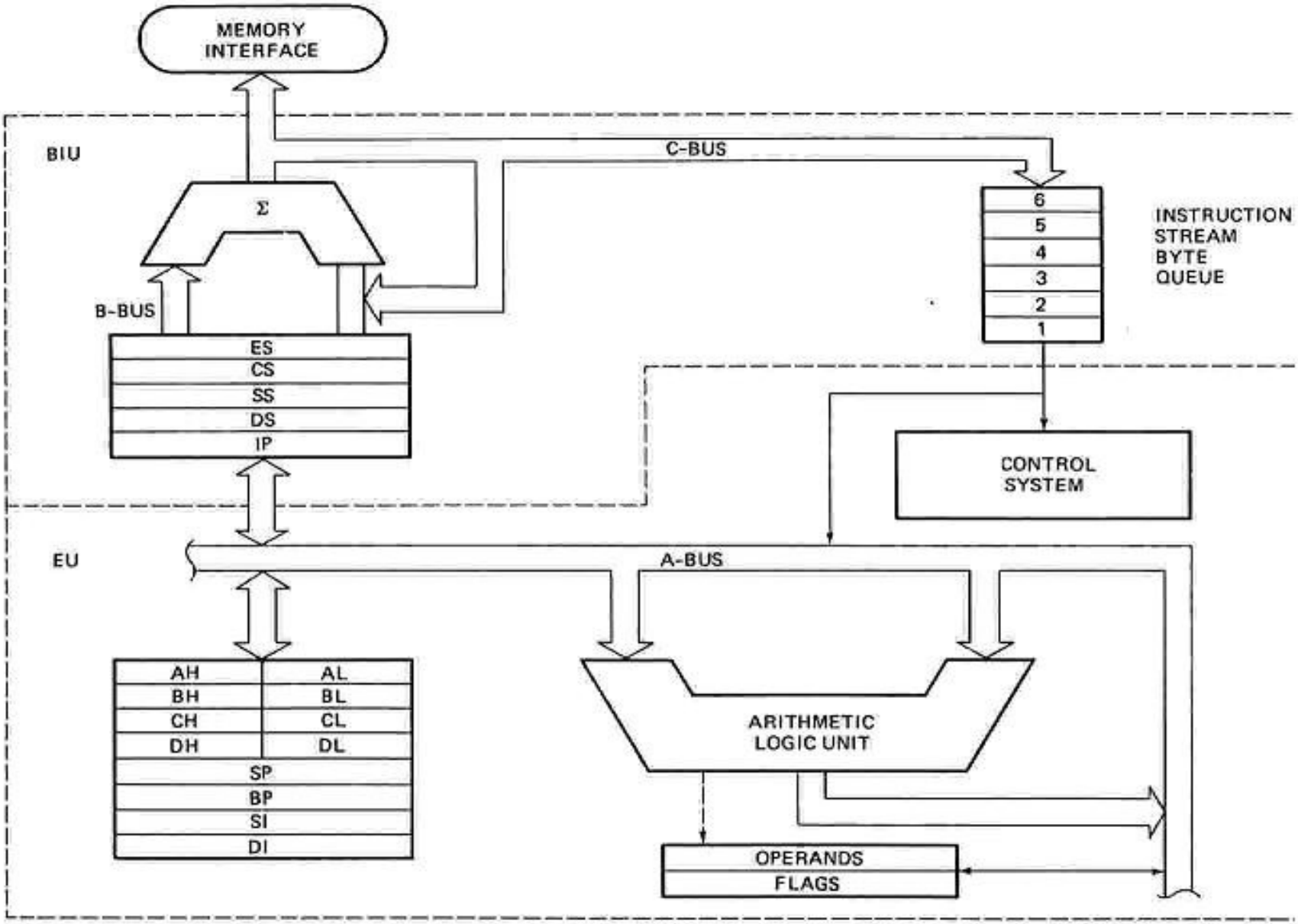


FIGURE 8086 internal block diagram. (*Intel Corp.*)

8086 ARCHITECTURE

8086 has two blocks BIU and EU.

Bus Interface Unit (BIU)

Execution Unit (EU)

BIU

1. The BIU handles all transactions with memory and I/O devices. Thus transferring data and addresses on the buses to load/store instruction and variables.
2. It fetches instructions, also Prefetches for empty space in queue.
3. Calculates 20-bit PA(Physical Address)
4. Generates the bus control signals to execute bus cycle.

BIU ELEMENTS

I. Instruction queue
II. Segment registers
III. Instruction pointer
IV. Address adder
V. Bus control Logic

EU

EU does the following

1. Decodes the instruction fetched by BIU
2. Generates the control signals for execution
3. Executes the instructions
4. Reflect the processor status on flag

EU ELEMENTS

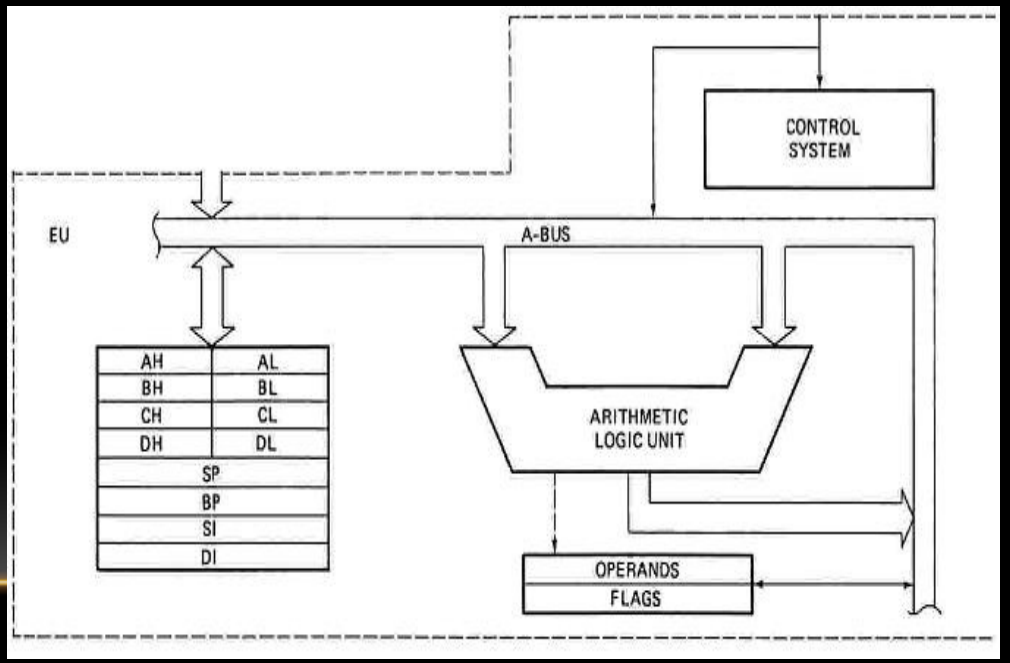
i. Control circuitry
ii. Instruction decoder
iii. ALU
iv. General purpose registers
v. Pointer and Index register
vi. Flag register.

EXECUTION UNIT

- Decodes instructions fetched by the BIU
- Generate control signals,
- Executes instructions.

The main parts are:

- Control Circuitry
- Instruction decoder
- ALU
- Registers



BUS INTERFACE UNIT (BIU)

Contains

- 6-byte Instruction Queue (Q)
- The Segment Registers (CS, DS, ES, SS). The Instruction Pointer (IP).
- The Address Summing block (Σ)
- Bus control logic