CT#4 A **CSE 317** **Fall 2021** **MARK: 20** **TIME: 40MIN**

1. **a)** CPU request the following Block addresses (x+15), (x+25) and (x+12). **10**
There are 16 one-word blocks in cache. Design and Show the memory mapping for the following cache configurations.

I. Direct mapped.

II. 4-way ,8-way and 16- way set associative mapped. (use LRU replacement policy) *
Where X= last two digits of your ID.

b) **10**

For the following configuration Determine the number of bits required for physical address, tag, index and block offset.

i) Consider 32 words cache and 512 words main memory. Block size 4 words. Determine the number of memory blocks and cache lines.
ii) Consider 16 words cache and 64 words main memory. Block size 4 words.
iii) Consider 16 words cache and 128 words main memory. Block size 4 words.
iv) Consider 32 words cache and 1024 words main memory. Block size 4 words.
v) Consider 8 words cache and 32words main memory. Block size 2 words
Also draw the required block for direct mapping cache.