2023 Digital IC Design Homework 4

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Simulation Result

Functional simulation	Score	Gate-level simulation	Score

```
# ----------------------------------------------------
#
# START!!! Simulation Start .....
#
# ----------------------------------------------------
#
# Layer 0 output is correct !
# Layer 1 output is correct!
#
# ----------------------------------------------------
#
# --------------------- S U M M A R Y ----------------
#
# Congratulations! Layer 0 data have been generated successfully! The result is PASS!!
#
# Congratulations! Layer 1 data have been generated successfully! The result is PASS!!
#
# terminate at      57350 cycle
# ----------------------------------------------------
#
# ** Note: $finish    : D:/NCKUCollege/111-2/DIC/HW4/file/testfixture.v(175)
#    Time: 2867500 ns  Iteration: 0  Instance: /testfixture
```

```
# ----------------------------------------------------
#
# START!!! Simulation Start .....
#
# ----------------------------------------------------
#
# Layer 0 output is correct !
# Layer 1 output is correct!
#
# ----------------------------------------------------
#
# --------------------- S U M M A R Y ----------------
#
# Congratulations! Layer 0 data have been generated successfully! The result is PASS!!
#
# Congratulations! Layer 1 data have been generated successfully! The result is PASS!!
#
# terminate at      57350 cycle
# ----------------------------------------------------
#
# ** Note: $finish    : D:/NCKUCollege/111-2/DIC/HW4/file/testfixture.v(175)
#    Time: 2867508150 ps  Iteration: 0  Instance: /testfixture
```

Synthesis Result

Total logic elements	661
Total memory bits	0
Embedded multiplier 9-bit elements	0
Total cycle used	57350

Flow Status	Successful - Mon May 22 18:34:19 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	ATCONV
Top-level Entity Name	ATCONV
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	661 / 55,856 (1 %)
Total registers	324
Total pins	82 / 325 (25 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	0 / 308 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

使用了 INPUT 將每個 kernel 的數值抓出來存到 k1-k9 暫存器，這邊判斷若 kenel 在 64*64 的 column 和 row 超過 0, address 就等於 0, 超過 63 就等於 63，並使用 blocking 的寫法可以減少 cycle。之後進到 CONV 的 state 進行運算，由於 kernel 的數值都可以用 shift 完成，因此直接使用 shift 做乘法，小數點在哪裡並不會影響加減法，使用這個方法克服小數點問題，做完 CONV 在下一個 state 寫入 L0。下一個 state 讀 L0 的值，一次讀 4 個存到 k1-k4，下一個 state 進行 maxpooling 寫到 L1，進位的問題用右移 4 將最右邊 4 為溢出並 +1，之後再左移 4 位。

*Scoring = (Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements) X Total cycle used*

*** Total logic elements must not exceed 1000.**