SystemC and Electronic System Level Design Methodology

Assignment 2, 2024-03-11

Abstract

Remodel the Assignment 1 timer module with `SC_CTHREAD`.

Please read carefully. All outputs required are described in the text. Five (5) points will be taken for each bug, missing the required output and behavior.

The `SC_CTHREAD` timer module

Description

1. Remodel the Exercise 1 timer module with `SC_CTHREAD`, where `clock` pin is a positive-triggered clock port, and `start` pin is a synchronous active-high reset port.
2. Use `SC_HAS_PROCESS` to configure the down-counting value at module instantiation, where the default down-counting value is 5.

sc_main

Description

1. Modify the `main.cpp` implemented in Assignment 1 to instantiate 3 timer modules. The first timer uses the default down-counting value. The other 2 timers use different down-counting values.
2. Create a trace file named `RESULT.vcd`. For each timer, trace ports and the register `count` as follows:
   - `clock`
   - `count`
   - `start`
   - `timeout`

makefile

Description

1. A `makefile` must be provided, with proper modifications to your environment.

Please turn in the source codes and `makefile` only. Do not turn in the executable.

Due date
2:00 PM, March 18, 2024

Score weight (towards the final grade) 5%