Jianxiao Cai

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Education

UNIVERSITY OF CALIFORNIA, SAN DIEGO — La Jolla, CA
M.S. in Computer Engineering — Sep 2024 – Exp. Jun 2026

- **GPA:** 3.62/4.0
- **Coursework:** VLSI Integrated Computing Circuitry, Fundamentals of Digital Image Processing, ML: Learning Algorithms

SHANGHAI NORMAL UNIVERSITY — Shanghai, China
B.Eng. in Electronic Information Engineering — Sep 2020 – Jun 2024

- **GPA**: 3.77/4.0
- **Coursework:** Logic Circuits & Application of FPGA, Digital Electronics and Integrated Parts, C Programming Language
- **Award**: Outstanding Graduate (University Level) for academic excellence and leadership, 2024

Work Experience

FORVIA HELLA, Advanced Engineering Intern — Shanghai | Jan 2024 – May 2024

- Implemented Model-Based Design in Simulink to build a BLDC motor controller, reducing coding complexity significantly.
- Designed motor driver circuits and validated motor operations via Arduino IDE, confirming firmware-hardware compatibility.
- Developed Simulink components for control behavior and motor parameters targeting Arduino deployment environment.
- Established a team-wide MBD workflow that cut low-level coding time by 40% and improved development consistency.
- Collaborated with teams to verify control logic, achieving stable system performance in test environments.

Projects

Intelligent Health Monitoring & Personalized Recommendation System - System Design | Edge AI

- Developed an offline health system on Jetson Nano, integrating five sensors and voice interaction to ensure data privacy.
- Deployed TinyLLM model under 4GB RAM, achieving 90% voice recognition accuracy in low-resource environments.
- Compressed the language model by 60% and replaced three libraries to enable stable real-time inference on device.
- Built a Python pipeline synchronizing sensor input and voice processing with latency consistently below 200 milliseconds.
- Delivered a complete prototype tested by 10+ users, receiving 90% positive feedback on usability and responsiveness.

Dual-Core Machine Learning Accelerator Based on Attention Mechanism - Chip Design | Verilog

- Executed gate-to-GDSII implementation of a dual-core accelerator using Cadence Innovus on TSMC 65nm process node.
- Achieved 0 DRC violations and 95% routing completion during physical verification by coordinating with the front-end team.
- Delivered final GDSII layout and power report, optimizing area by 12% under timing and silicon manufacturing constraints.

Global Warming Trend Forecasting and Causal Modeling - Python | Excel

- Built ARIMA and multi-regression models to measure how human activity influences long-term temperature shifts globally.
- Cleaned and standardized over 200,000 entries from five sources, resolving 15% missing values for consistent model input.
- Produced 50+ heatmaps and trend visualizations, revealing climate patterns and supporting data-driven decision-making.

RFID-Enabled Integrated Elderly ID and Health Code System - RFID | Circuit Design

- Designed features for an RFID-based system integrating identity verification and health code display for 100+ elderly users.
- Simulated and validated circuit behavior using Proteus; debugged embedded code across three interaction modules.
- Supported team presentations by preparing system diagrams and use-case demos for academic evaluation panels.

Skills

- Programming Languages: C/C++, Python, MATLAB, Java, Shell, Tcl, Verilog
- Software: Cadence Innovus, Synopsys DC, Xilinx Vivado, Simulink, Keil, Visual Studio Code, Excel, MATLAB, Stata
- Tools: Git, Linux, Docker, RESTful APIs
- Skills: Embedded Systems, Data Analysis, Hardware Prototyping, Technical Communication, Cross-Functional Collaboration