

North South University Department of Electrical & Computer Engineering LAB REPORT- 02

Course Code: CSE 231

Course Title: Digital Logic

Section: 09

Lab Number: 02

Experiment Name:

Combinational Logic Design

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Submitted by Group Number: 02

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Experiment Name: Combinational Logic Dosign

- Objectives: · Becoming familiaize with the analysis of combinational logic network
 - · hearning the implementation of networks using two canonical forms.
 - · Devise combination circuit using universal logic
 - · Acquirt with basic binary anithmatic circuits

Appenatus: Trainer Board, 1x1C 7411 Tripple 3-in put AND gates, 1x1e 7432 Tripple 3-input OR gates, 1x1e2404 Hex Inverters

Theory

- ; Minterm for each combination of the variables that produce a 1 in the function and taking the 'OR' of all those terms.
- · minterm in variables = product of nliterals in which each variable appears exactly once either in Tor F form.
- · Each minterm has value 1 for exactly one combination values of variables. example: ABC (111) => m7.
- · A function can be written as a sum of minterms, referred +, as a minterm expansion on a standard sum of products.

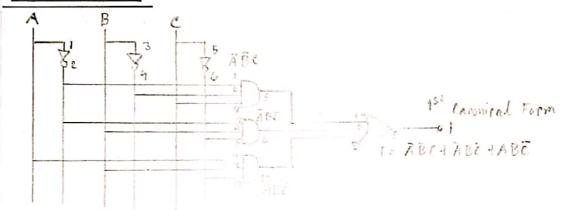
Maxtem for each combination of variables that produces a O in the function and then taking the AND of all those terms -maxterm of n variables = sum of n literals in which each variable appears exactly one in T or F foon, but not in both · Each maxterm has a value of 0 for exactly one combination of values of variables, example: A+B+e'(00)=> M1 (value is 0)

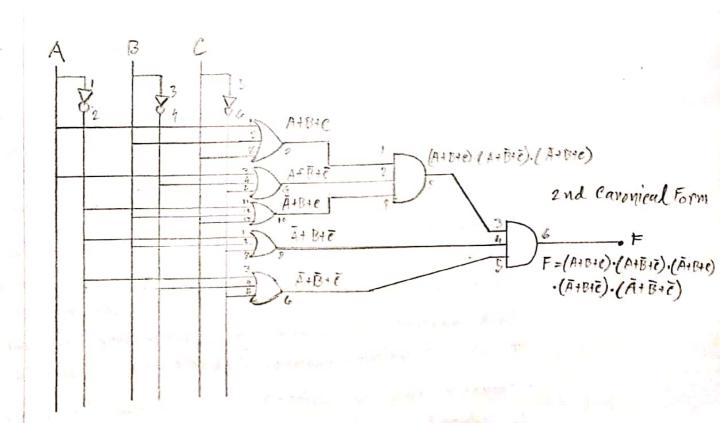
· Function can be written as a product of maxterns, which is referred to as a maxterm expansion or standard productof sen

Canonical forms: The technique that is used to .

Trepresent the mathematical entities on matrix in it's standard form is termed as canonical form. The term canonicalization is also known as standardization or normalization with respect to the equivalence reclation.

Circuit Diagram:





Experimental Procedure: All the minterms of three inpots ABC:

ABC(M) ABC(M), ABC(M), ABC(M), ABC(M), ABC(M), ABC(M), ABC(M).

All the Maxterms for three input ABC:

A+B+c(Mo), A+B+c(Mi), A+B+c(Me), A+B+c(Mg), A+B+c(Mg),

Experimental Data Table:

Input Reference ABC		F	Mintern	Men term	
0	000	0	ABE MAG	A+B+e Mo)	
1	001	1	ABC Mi	A+ B+ 6 (M)	
2.	010]	ABE IND	A+B+C M	
3	0 11	. 0	\$ BC (mg)	4+ B40 (M.	
4	100	0	FRE (re)	ATBIE (MA)	
5	101	Ó	ABC (ms)	A+B+E (ME)	
6	110	1	ABC (ma)	. A = B+C (Mo)	
7	111	0	ABC (Ma)	A+ B+E (M7)	

Truth table to a combinational circuit

	Shorthand Notation	Function
1st Canonical Form	F= [(M1/M2, M6)	F= ABE+ ABE+ ABE
2rd Ennonieal Form	F= TT (Mo, M3, M4, M5, M7)	F= (A+B+c)·(A+B+c)·(A+B+c)·(A+B+c)·(A+B+c)

¹st and 2nd canonical forms of the combinational Circuit

Discussion: In this experiment we learned abot the two canonical forms and how they work. We also learned that two differen eincuit can give same result if arranged properly For this experiment we had 11C 7464 Her Inverter (16tgat 11C with three input AND gate 744 4073 and two 10 with three input Orgate 4075. For minterm we didn't face any problem as it only required one AND and one or and a Her Inverter. But in Maxterm we had to use two OR Ic gate and the circuit was very complex for that yeason it took more time than expected.

while using two OR gates we used 1 or 1e tom three maxterm them connected output to AND gate input while the two other OR output from the other ORIC we connected these inputs to second AND input and got the expected output.

Wining the circuit in maxterm was quite challenging because we needed to comment a lot of gates. We also needed to use a lot of swires and Alhamdulillah the the experiment was working out. All our equipment were working perfectly. We did it on first try and did not face that much trouble in this experiment.

North South University

Department of Electrical and Computer Engineering

CSE 231L: Digital Logic Design Lab

Lab 02: Combinational Logic Design

A. Objectives

- Familiarize with the analysis of combinational logic network.
- Learn the implementation of networks using the two canonical forms.
- Devise combinational circuits using universal logic.
- Acquaint with basic binary arithmetic circuits –the half and full adders.

B. Theory

Concise theory pertinent to lab experiments to go here to aid students in performing experiments with minimal supervision. For example, topics for this lab should include definition and steps to:

Analysis of combinational logic design Min terms and max terms

Canonical Forms

Universal gates - bubble pushing, De Morgan's theorem.

C. Experiment 1: Analysis of a Combinational Logic Circuit

C.1. Equipments:

- Trainer Board
- 1 x IC 7411 Triple 3-input AND gates
- 1 x IC 7432 Quadruple 2-input OR gates
- 1 x IC 7404 Hex Inverters (NOT gates)

C.2. Procedure

Input Reference	A B C	F	Min term	Max term
0	000	0	19 ((s.)	A-B-C (M)
1	001	1	Mi hij	A+8+2 (M)
2	010	1	P = 11 -	(+13+0 (M2)
3	011	0	16 1 (Mg)	A + D + 7 (Ma)
4	100	0	ART (ma)	A+D+C (Ma)
5	101	0	AB: (ms)	A+8+0 (Ma)
6	110	1	AEC (10)	7+B+C (M6)
7	111	0	ABCV(m7)	A+B+C (1/2)

Table C.1 Truth table to a combinational circuit

- 1. Write down all the min terms and max terms of three inputs ABC in Table C.1.
- 2. Write down the function F in 1st and 2nd Canonical Forms in Table C.2.

e!	Shorthand Notation	Function	4
	$F = \Sigma \left(m_1, m_2, m_6 \right)$	F = ABC + ABC + ABC	
2 nd Canonical Form	$F = \Pi \left(M_{\bullet}, M_{3}, M_{4}, M_{5}, M_{7} \right)$	F = (A+B+c). (A+B+c). (A+B+c). (A+B+	c) (A+B

Table C.2 1st and 2nd canonical forms of the combinational circuit of Table C.1

3. Draw the circuits in the space provided below, clearly indicating the pin numbers corresponding to the relevant

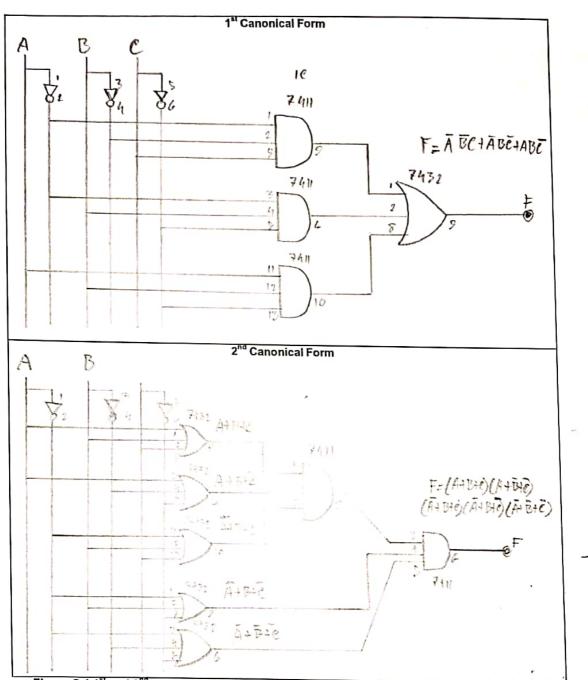


Figure C.1 1st and 2nd canonical circuit diagrams of the combinational circuit of Table C.1

- 4. Construct the 1st canonical form of the circuit and test it with the truth table.
 - Connect one min term at a time and check its output.
 - ii. Once all min terms have been connected and verified, OR the min terms for the function output.

C.3. Report

Simulate above two circuits (1st and 2nd canonical forms) in Logisim.

Prittika 13/3/24