North South University
Department of Electrical and Computer Engineering
CSE 231L: Digital Logic Design Lab
Lab 04: Combinational Logic Design

A. Objectives

- Design a complete minimal combinational logic system from specification to implementation.
- Minimize combinational logic circuits using Karnaugh maps.
- Learn various numerical representation systems.
- Implement circuits using 1st and 2nd canonical minimal forms.

B. Apparatus

- Trainer board
- Logic gate ICs: 2- and 3-input AND, OR, NAND

C. Procedure

Design of BCD to Excess-3 converter: Design, minimize and implement a digital logic system where an input in binary coded decimal (BCD) in converted and displayed in Excess-3.

1. Complete the truth table (Table E1, Section E) for the BCD to Excess-3 converter.
2. Identify the inputs and outputs from the truth table and complete the system analysis (Table E2, Section E).
3. Complete the K-maps (Figure E1, Section E) to find the minimal 1st canonical functions of each output variable.
4. Draw the minimal circuit showing the pin configurations (Figure E2, Section E).
5. Implement and test the circuit on the trainer board.
   Connect the 4 inputs to the BCD inputs on the trainer board to display the input digits on the seven-segment display.
6. Convert, implement and test the circuit in the suitable universal gate format. Show the circuit with pin configurations (Figure E3, Section E).

D. Report

1. Design and simulate the minimal NOR logic implementation of Excess-3 to BCD converter.

E. Experimental Data

Binary Coded Decimal (BCD)				Excess-3			
A	B	C	D	W	X	Y	Z

Table E1: Truth table - BCD to Excess-3

Number of inputs bits:		**Input variables:**	
Number of outputs bits:		**Output variables:**	

Table E2: System analysis

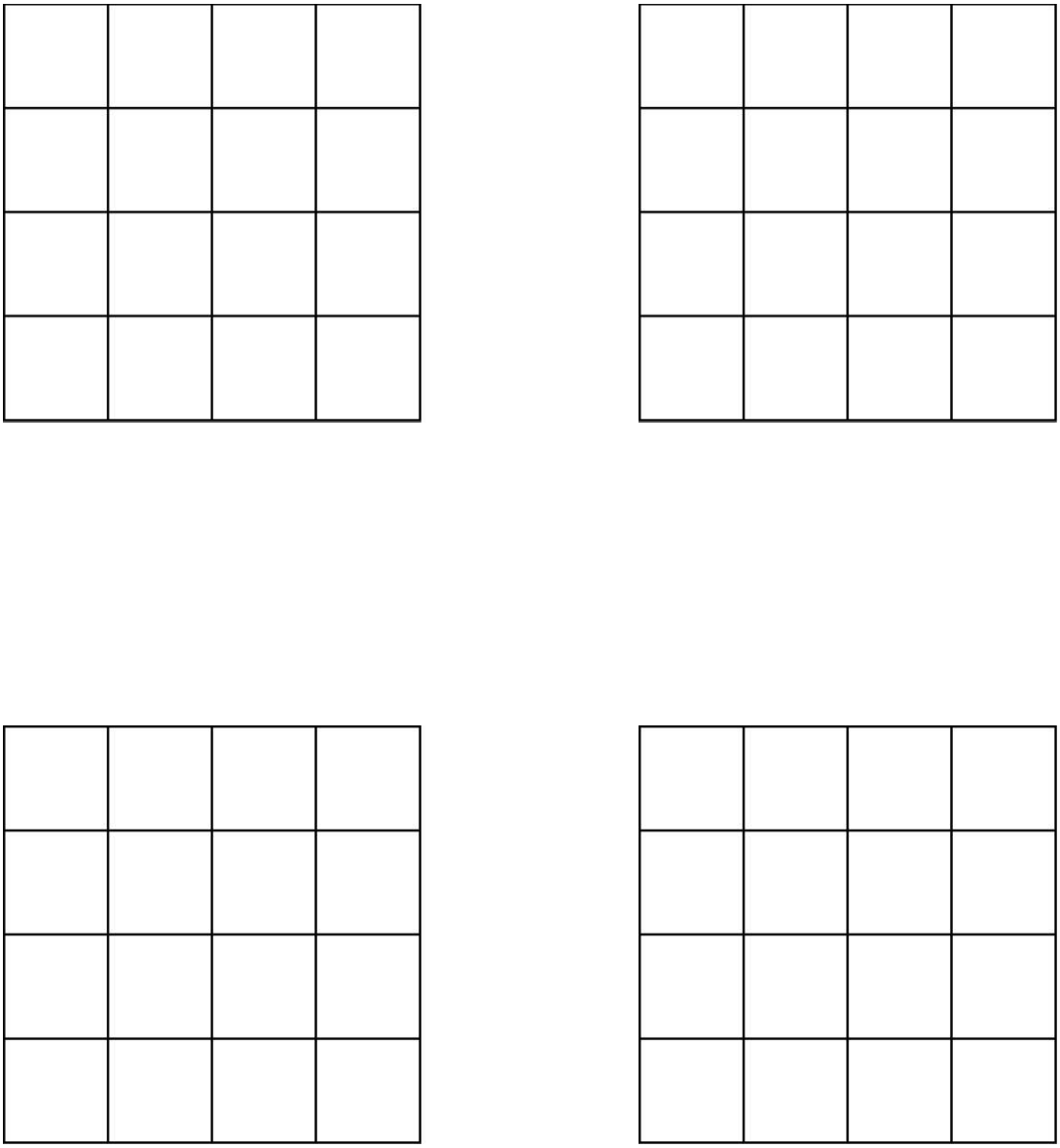

Figure E1: K-M

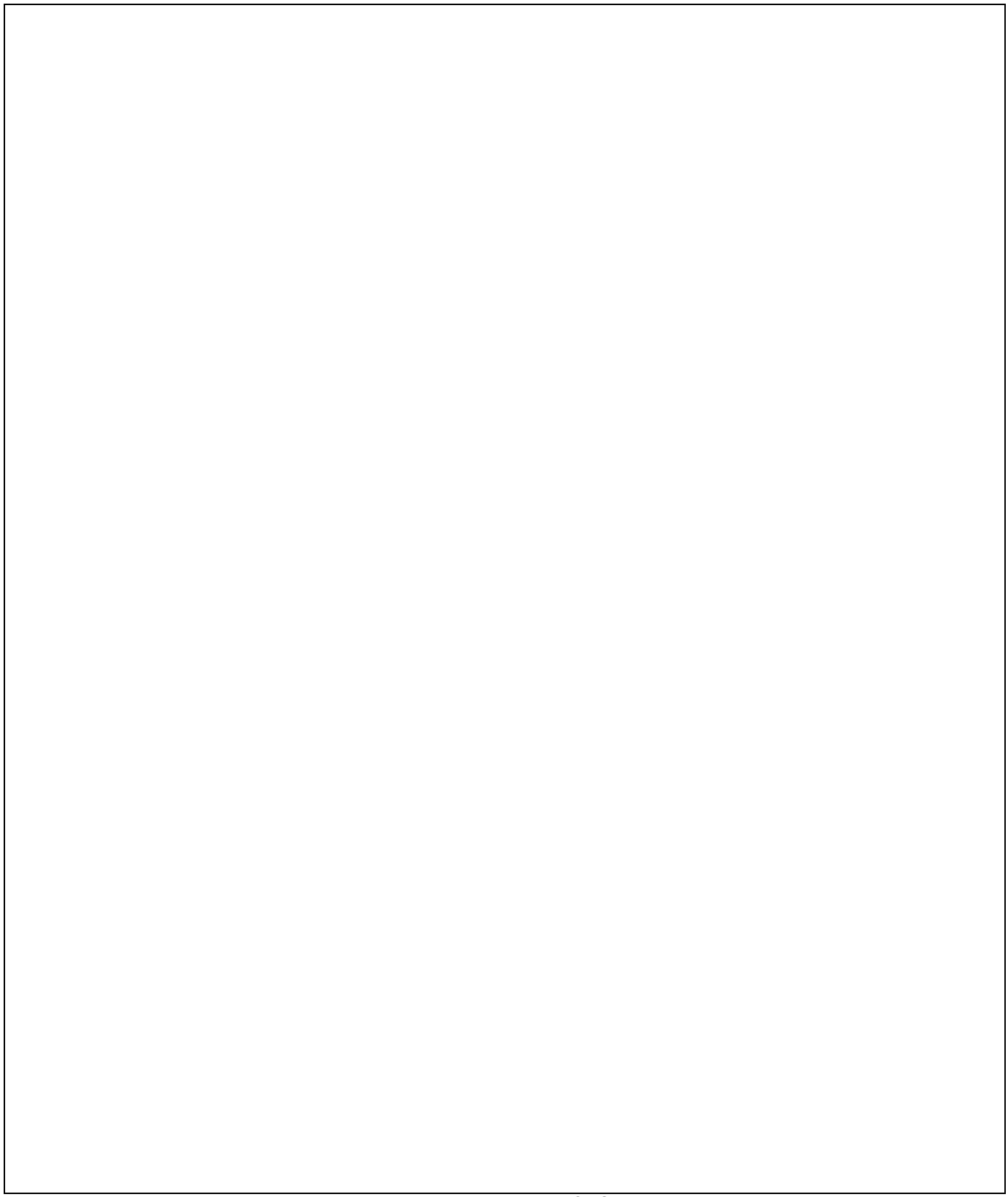

Figure E2: Minimal 1st canonical circuit of BCD to Excess-3 converter

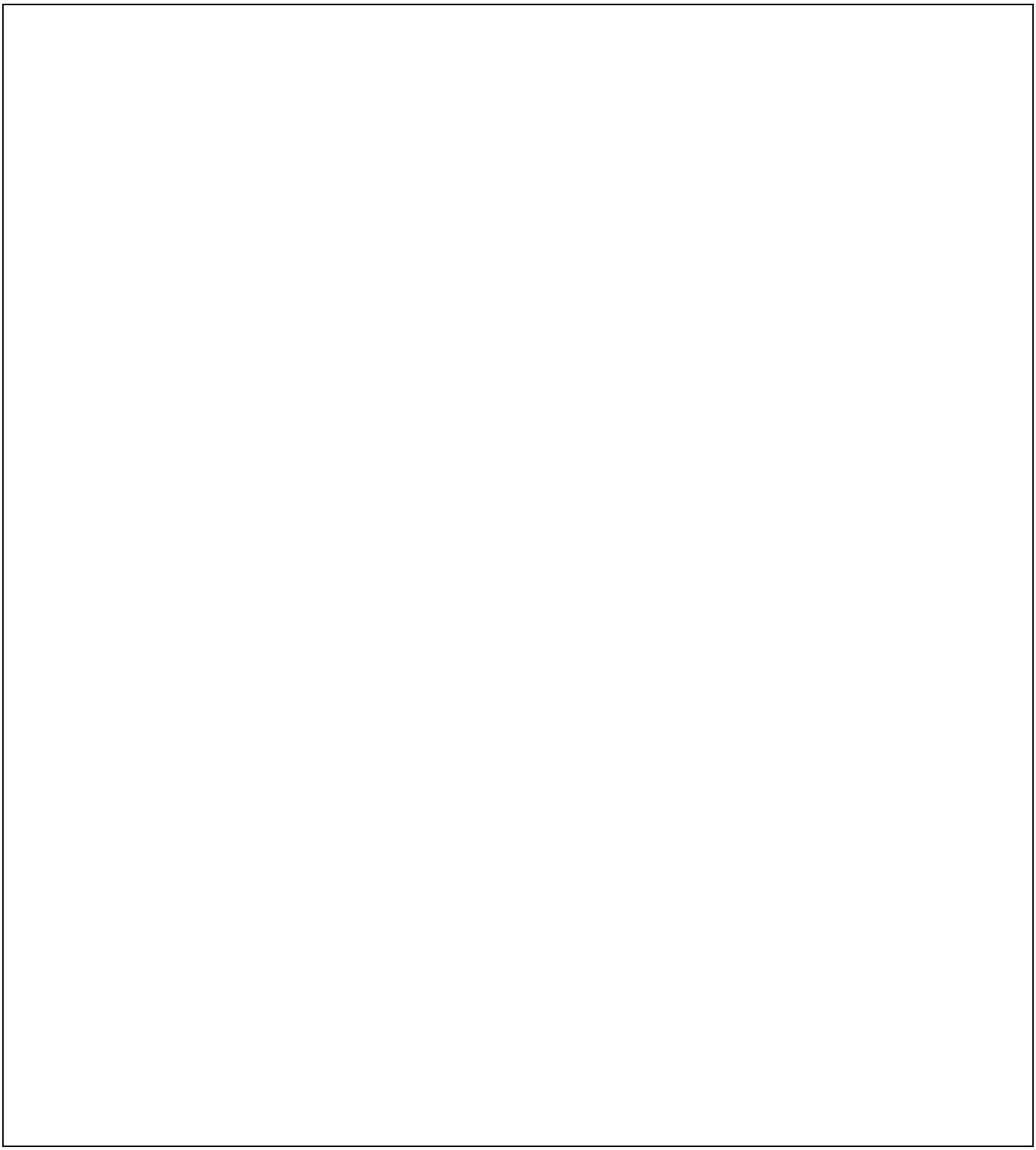

Figure E3: Minimal universal gate implementation of BCD to Excess-3 converter