

North South University Department of Electrical & Computer Engineering LAB REPORT-

Course Code:	CSE231L	
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Course Title: Digital Logic Design

Section: 09

Lab Number: 01

Experiment Name:

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Experiment Date: 06th Morch, 2024

Date of Submission: 13th March, 2024

Submitted by Group Number: 02

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- 1. Experiment Name: Digital Logic Grates and Boolean Functions
- 2. Objects & One of the major goals of this lab is to Pamillarize the students with the proper equipment and techniques and become familliarized with combinational logic circuits.
 - * To study the basic logic gates such as AND, OR, NOT, NAND, NOR, and X-OR.
 - To get acquainted with the description of boolean functions using truth tables, logic digrams and Boolean Algebra.
 - 3. Apparatus: IC 7404 Hex Inverter (NOT gates),

 IC 7432 Quadruple 2-input OR gates,

 IC 7486 Quadruple 2-input XOR gates,

 Traine Board, IC 7400 Quadruple 2-input

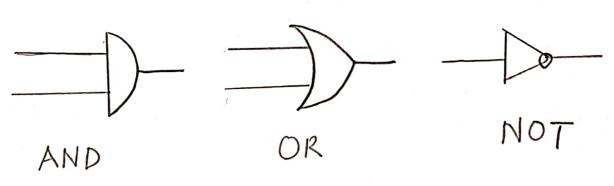
 NAND gate
 - 4. Theory: We know logic getter are the elementary building blocks of digital circuits. By performing one or more logical inputs, it produces a single output Pigital logic gates operate at two discrete voltage levels representings the binary values o (Logical Low) and I (Logical High). Now the true and fulse statements, off state will be considered False and On State

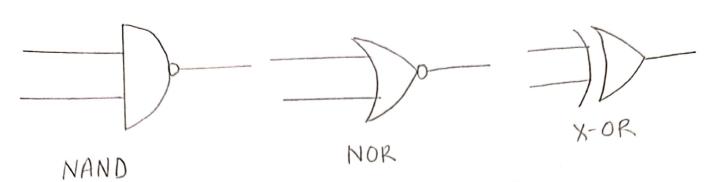
will be considered true.

$$0 \longrightarrow off \longrightarrow F \longrightarrow 0 \lor$$

$$1 \longrightarrow 0n \longrightarrow T \longrightarrow 5 \lor$$

Experiment - 1: Our first experiment was to check and verify the fundamental logic gates and also Universal gate like NAND gate, NOR gate and a special gate X-OR gate. To verify their truth table we use a traine board. In this board we took connection from the power house and one is a voltage which also implies off state and another was 5 V Which implies as On State. We also connect the IC to the trainer board and for input we took two wire and connect them with two switch. For our output section, to check whether we get our expected output or not. We took one wire connecto the Ic occording to the logic gate and another end connect to the output LED section.





1	-						
	Α	В	F=A·B	F=A+B	F=(AB)	F = ADB	F=(AtB)
	0	0	0	0	1	0	1
	0	1	0	١	1	- 1	0
	1	0	0		١	1	0
-	١	1	1	1	0	0	0

A	F=A'
0	1
1	0

Table: Truth table of logic gates

Experiment 02: In this second experiment we tried

3 input AND gate and 3 input OR gate. As we

3 input AND gate and 3 input OR gate, if one input

Know in the truth table of AND gate, if one input

is 0 then the output will also be a so, to

is 0 then the output will also be a so, to

show output 1, the three-input must be 1. Again

Show output 1, the three-input must be 1. Again

In the OR gate thruth table, we know that

if any one input is 1, then the final output

if entry one input is 1, then the final output

three input is 0, only then the final output

three input is 0, only then the final output

three input is 0, only then the final output

three input is 0, only then the final output

three input is 0, only then the final output

three input is 0, only then the final output

will show zero. But to perform we need to two

will show zero. But to perform we need to two

and AND gate because our Ic has two input gate.

For that first we put IC 7408 to the traine board.

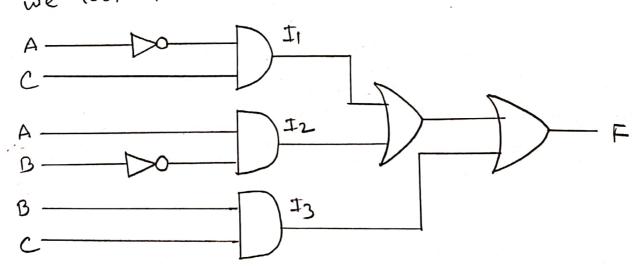
and we IC pin 14 will be connected to the Vec(tsv)

and IC pin 7 will be connected to GND. We connected without wives as input on 1,2. Then we connected this 2 wires with some switch 14,13 and for out second gate we took the output wire from 3 and connect 4 and pin 5 we connect wire switch 12. Thus our 3 input AND gate is complete. For final output we took pin 6 and a wire connected to a random LED. We did the same connected to a random LED. We did the same this for OR gate because the configuration for 12. 7408 and 10. 7432 is some.

1			4	
Α	B	c	F=ABC	FZA+B+C
0	D	0	O	- O ,
0	0	1	0	1
0	1	0	0.	1
0	1	١	0	1.
1	0	0	0	
1	0	7	0	
i	1	0	0	• 1 2 2
١	1	١	1 - \$7	1.
				1

3-input AND and OR

Experiment 3; In this third experiment we were given a digram, a truth table of boolean expression. So, to prove that, we could find that we need one IC 7408 AND gate, one IC 7432 OR gate and one IC 7404 NOT gate. In this experiment we have to use three logic AT AND gate, two Logic OR gate and also two Logic NOT gate. First of all, II, we took one input A and connect with NOT IC pin 1, and another input e directly connected to II (AND Grate). For Iz, we took A and another input B, we connect it IC 7909 pin 3 and output pin 4 connect to Iz gate. NOW IC 7408 pin 3 and pin 6 output wire, we connect it to IC PH 7432 pln 1 and 2. for I3 we took input Band c and connet it to the other Side of Il 7408 geste pin 10 and 9. Now IC7432 pin 3 and IC7408 pin 8 are conveted to IC7432 pin 9 and 5 and thus for the final output ou we took pin 6 and connect to a random LED.



-0-9-10 4 M 4 15 0

Experimental Data Table:

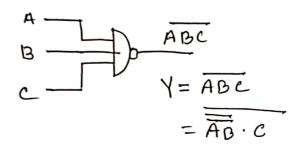
ABC	11 = 1/c	12: AB	To= BC	F=11+11+13
000	0	0	0	1-11-11-13
001	and the Salah decimal	0	0	
010	0	0	0	
011	1	0	A STATE OF THE PARTY OF THE PAR	
100	0		0	
101	0		0	
110	0	0	0	0
1 11	0	0		
				,
-				

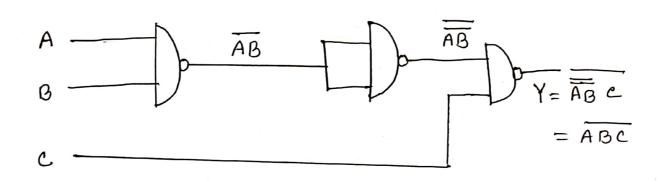
Question: 1

Is it possible to make a 3-input NAND or PIDR gate with 2-input NAND or NOR gate?

Yes, it is possible. We can justify the answere Using boolean logic expression and conficult diagram.

3-input NAND Gate:





3-input NOR Gate:

$$A = A + G + C$$

$$C = (A+B) + C$$

A
$$B$$

$$A+B$$

$$Y = A+B+C$$

$$C$$

Discussion: In this whole lab-01, we were introduced to fundamental logic gates , their Propertise, truth table and how to work with Ic. Every Ic has their own configuration to work with. IC 7400, IC 7408, IC 7432 and, FC 7486 are some with their configuration. But Ic 7404 which is Logic NOT gote has a little bit different. The NOR Logic gate which is IC 7402 has a configuration with pin I output and pin 2,3 input, similarly 9 output and 5,6 input. Experiment 1 we funadamental logic circuit and their truth table. Experiment 2, we were shown Binput AND and OR gate , tinalyon in the experiment 3, we build a discircuit using three different Ic and our lab instructor told us to complete this circuit. To build this circuit we tried several time but failed became Of the IC. Despite of changing several IC's of NOT gate , we still coundit find the good IC. Finally we informed our lab instructor and then giave us a fc that could totally work . Then We were able to finish the final task.