North South University

Department of Electrical and Computer Engineering

CSE 231L: Digital Logic Design Lab

Lab 05: Binary Arithmetic

A. Objectives

- · Minimize combinational logic circuits using Karnaugh maps.
- · Learn various numerical representation systems.
- Implement circuits using 1st and 2nd canonical minimal forms.
- · Implement circuits using universal logic

B.Theory

Topics covered: Binary adder using IC, Ripple through carry 8-bit adder, Binary adder-subtractor, BCD adder

C. Experiment 1: Binary Adder-Subtractor

C.1 Apparatus

- · Trainer board
- 1 x IC 7483 4-bit binary adder
- 1 x IC 7486 quadruple 2-Input XOR gates

C.2 Procedure

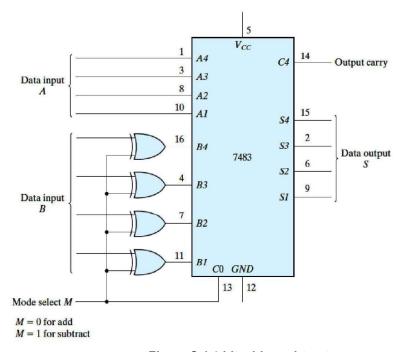


Figure C.1 4-bit adder-subtractor

- 1. Construct the 4-bit adder-subtractor circuit of Figure C.1.
- 2. Complete the operations in Table C.1.
 - i. For each operation, convert the first operand to binary as A, and the second operand as B.
 - ii. Write down the value of M required for the operation.
 - iii. Note down the values of the output carry C4 and data output S4-S1. Verify the results.

7 + 5 4 + 6 9 + 11	Operation	М	A	В	C4	S4 S3 S2 S1
	7 + 5					
9+11	4 + 6					
	9 + 11					

15 + 15			
7 – 5			
4-6			
11 – 2			
15 – 15			

Table C.1

C.3 Report

- 1. Comment on the use of the XOR gates and the M bit of the 4-bit adder-subtractor.
- 2. Write down your observations of the results from the addition and subtraction operations performed.

D Experiment 2: Ripple-Through-Carry Adder

D.1 Apparatus

- Trainer board
- 2 x IC 7483 4-bit binary adder

D.2 Procedure

- 1. Deduce the circuit diagram of an 8-bit ripple-through-carry binary adder using two 4-bit adders, clearly showing the pin numbers.
- 2. Construct the 8-bit adder.
- 3. Complete the operations in Table D.1.

Operation	A	В	Overflow Carry	Sum
7 + 5				
18 + 19				
72 + 83				
129 + 255				

Table D.1

D.3 Report

1. Comment on your observations of the results.

E Experiment 3: BCD Adder

E.1 Apparatus

- Trainer board
- 2 x IC 7483 4-bit binary adder
- 1 x IC 7408 quadruple 2-Input AND gates
- 1 x IC 7432 quadruple 2-Input OR gates

E.2 Procedure

1. Complete Table E.1 for the BCD sum.

	Binary Sum				BCD Sum				
K	Z8	Z4	Z 2	Z1	C	S8	S4	S2	S1
0	0	0	0	0					
0	0	0	0	1					
0	0	0	1	0					
0	0	0	1	1					
0	0	1	0	0					
0	0	1	0	1					
0	0	1	1	0					
0	0	1	1	1					
0	1	0	0	0					
0	1	0	0	1					
0	1	0	1	0					
0	1	0	1	1					
0	1	1	0	0					
0	1	1	0	1					
0	1	1	1	0					
0	1	1	1	1					
1	0	0	0	0					
1	0	0	0	1					
1	0	0	1	0					
1	0	0	1	1					

2. Construct the circuit of Figure E.1

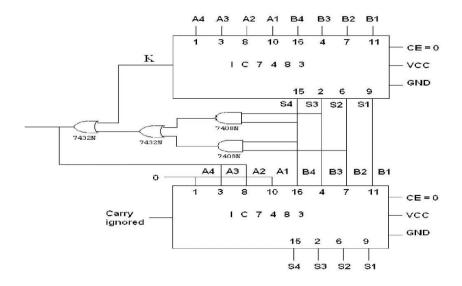


Figure E.1

3. Verify the outputs in Table E.2

Operation	А	В	Overflow Carry	Sum
9 + 0				
9 + 1				
9 + 2				
9 + 3				
9 + 4				
9 + 5				
9 + 6				
9 + 7				
9 + 8				
9 + 9				

Table E.2

E.3 Report

1. Derive the circuit for the BCD adder.