North South University
Department of Electrical & Computer Engineering
LAB REPORT- 03

Course Code: **CSE231L**

Course Title: **Digital Logic Design Lab**

Section: **09**

Lab Number: **03**

Experiment Name:

Universal Gates

Experiment Date: 20.03.2024

Date of Submission: 27.03.2024

Submitted by Group Number: 02

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Experiment name : Universal Gates

objectives :

① Becoming familiar with Universal gates, such; NAND gate and NOR gate.

② Implementation of the Basic Gates using Universal gates (NAND gate and NOR gate)

③ Understanding Boolean Functions from Basic Gates and implementing it into Universal Gate. Moreover, we learning ~~simplify~~ simplifying form of Boolean Algebra.

④ Using minimum universal gates to get our desired boolean function.

Apparatus :

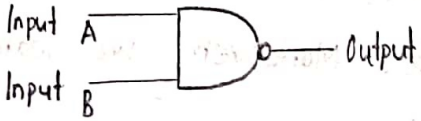
① Trainer Board
② 2 x IC 7400 Quadruple 2-input NAND gates
③ 1 x IC 7402 Quadruple 2-input NOR gate

Theory :

Universal gates are special types of logic gates in digital circuits. The key thing about universal gate is that they can be used to build any other logic gate. This means we can create complex digital circuits using just these Universal gates. Such as, NAND and NOR. So this two

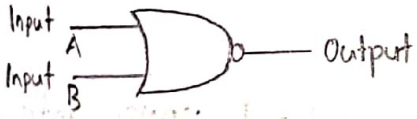
types of universal gates : NAND (NOT AND) and NOR (NOT OR) can be used in digital logic design for minimalization of the circuit. By combining these gates in different ways, we can implement any boolean logic function. This makes them very versatile building blocks for digital circuits.

NAND Gate



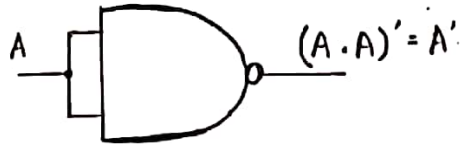
A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

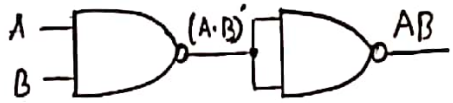


A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

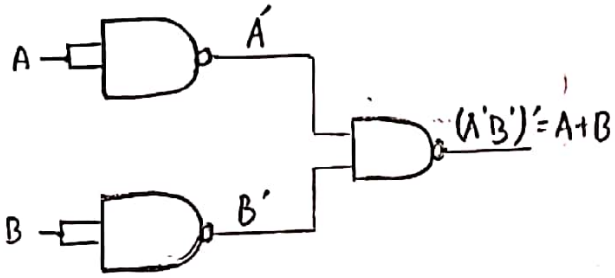
Circuit Diagram :



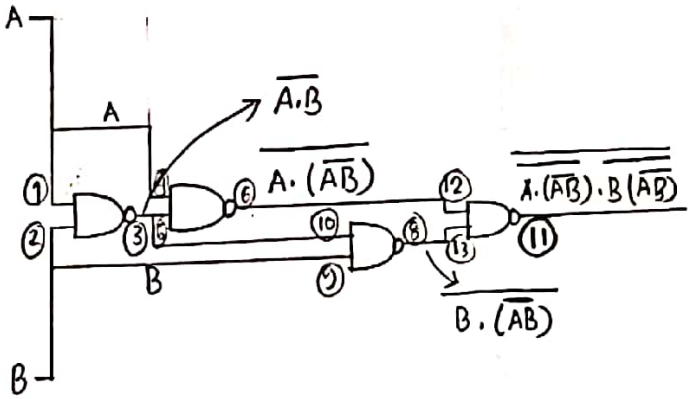
implementation of NOT gate using NAND gate



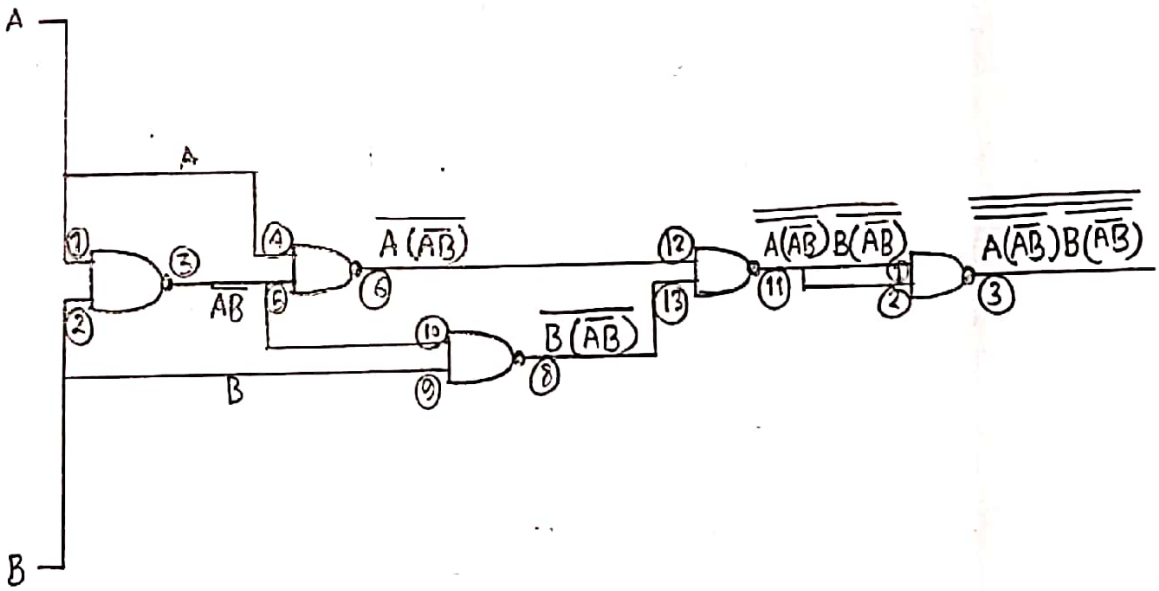
implementation of AND gate using NAND gate



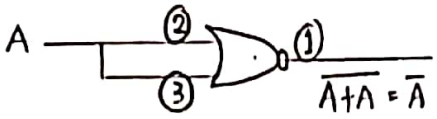
implementation of OR gate using NAND gate



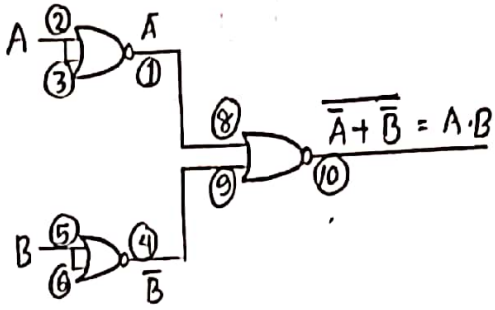
implementation of XOR gate using NAND gate



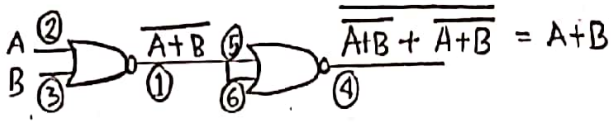
implementation of XNOR gate using NAND gate



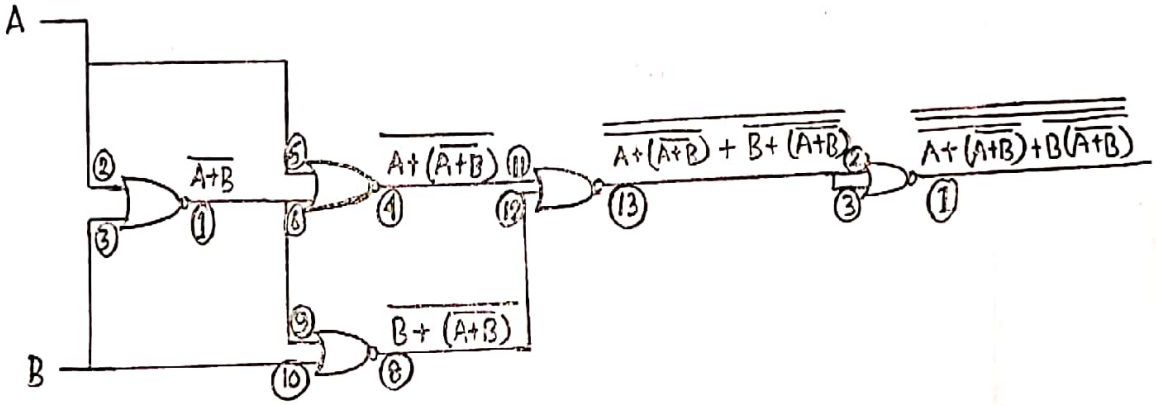
implementation of NOT gate using NOR gate



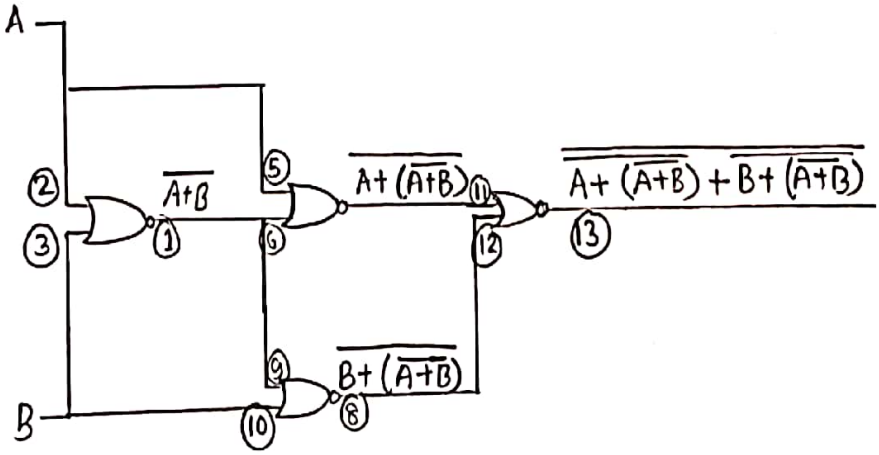
implementation of AND gate using NAND gate



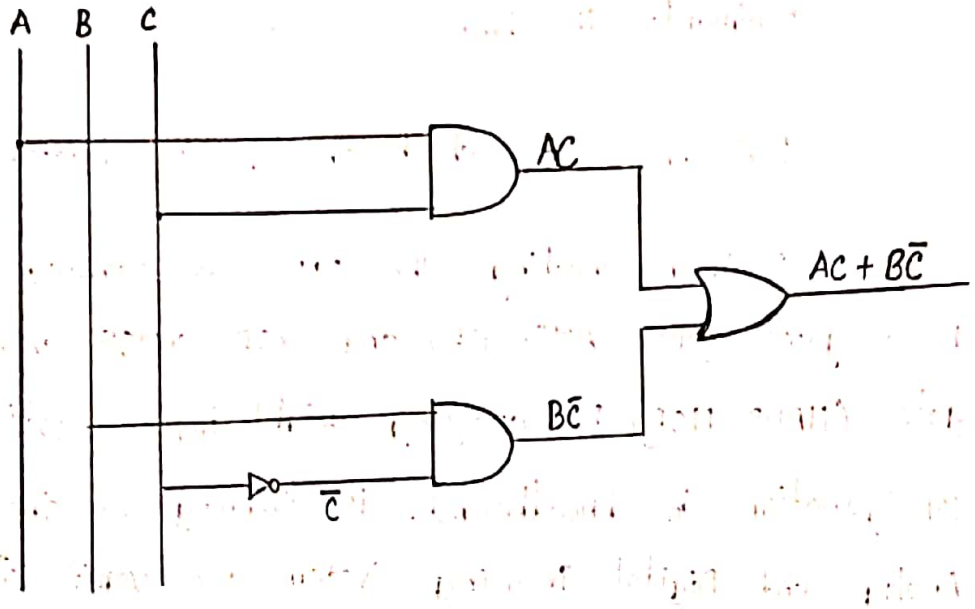
implementation of OR gate using NOR gate



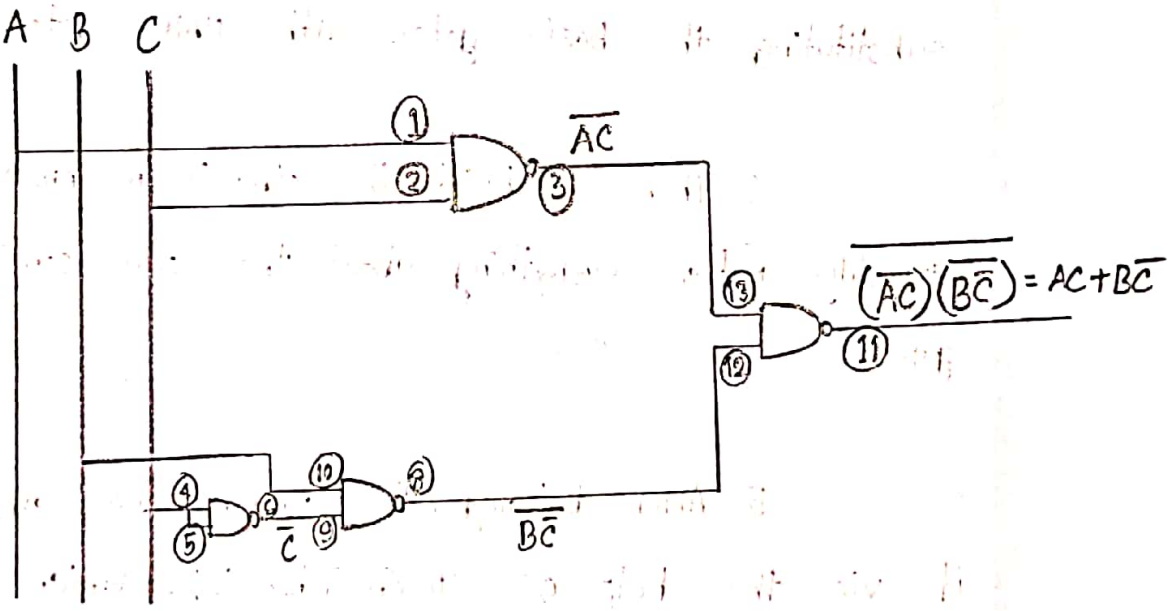
implementation of XOR gate using NOR gate



implementation of XNOR gate using NOR gate



A combinational Circuit



Universal (NAND) gate implementation of the previous circuit

Experimental Procedure :

1. At first we check the IC of related gates.

2. After checking the IC's we started implementing basic gates (NOT, AND, OR) and XOR, XNOR using universal gates (NAND, NOR) by applying right implementation of pin configuration in breadboard. By turning on the switch in Analog and Digital Training System we verify the result of each gate with the help of "Truth Table".

3. We ~~data~~ draw the logic gate one by one by substituting the basic gates with NAND gate.

4. Then we build the circuit in breadboard. Here, we carefully notice everything about the pin configuration of NAND gate.

5. After building the combinational circuit, we tested it via the help of Truth Table DI. Which we have to fill up using boolean logic.

Experimental Data Table :

A	B
0	1
1	0

NOT Truth Table

A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

AND Truth Table

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

OR Truth Table

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

XOR Truth Table

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

XNOR Truth Table

A	B	C	$I_1 = AC$	$I_2 = BC'$	$F = I_1 + I_2$
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	1	1	0	1

Truth table of Combination circuit

Results :

We got the outputs according to the truth table.

Discussion :

In this lab, we learned about Universal Gates such as the NAND and NOR gates. Using these universal gates, we have formed a combinational circuit and the basic gates such as the NOT gate, AND gate, OR gate, XOR gate, and XNOR gate.

In our lab, we have faced the problem of more than one faulty IC that needed to be changed. So, we had to change one IC 7400 Quadruple 2-input NAND gate and another IC 7402 Quadruple 2-input NOR gate. While building the combinational circuit, we also faced some problems with loose wires and some defective switches in the Analog and Digital Training System. We have solved this problem by changing the wires and changing them into other switches in the Analog and Digital Training System.

We got our desired outputs for logic gates and the combinational logic circuit according to the truth table D1.

In a nutshell, this lab has helped us get to know Universal Gates practically and enriched our knowledge of Digital Logic Design.

North South University

Department of Electrical and Computer Engineering

CSE 231L: Digital Logic Design Lab

Lab 03: Universal Gates

A. Equipments

- Trainer Board
- IC 7400 Quadruple 2-input NAND gates
- IC 7402 Quadruple 2-input NOR gates

B. Procedure

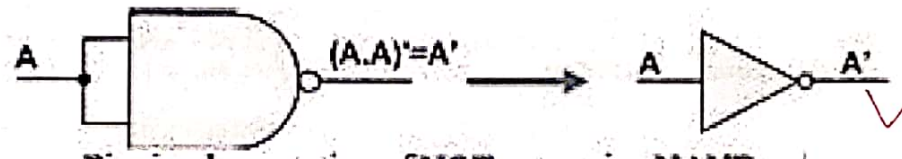


Fig: implementation of NOT gate using NAND gate

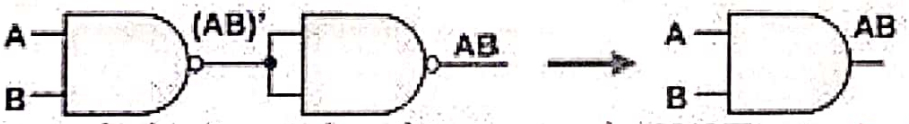


Fig: implementation of AND gate using NAND gate

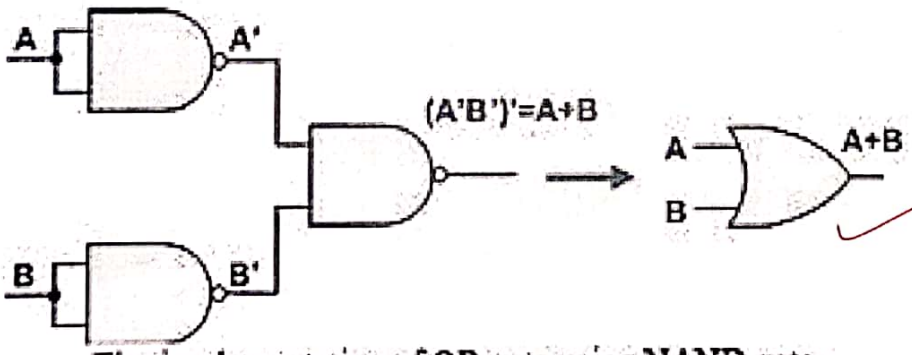


Fig: implementation of OR gate using NAND gate

Figure B1: NAND as a universal gate

1. Verify each of the NAND gate equivalent circuits in Figure B1 to perform the same operations of the basic gates.
2. Design, construct and test the implementations of XOR and XNOR gates using NAND gates only. Show the circuits in Figure D1 (Section D), clearly labeling the pin numbers.
3. Design, construct and test the implementations of NOT, AND, OR, XOR and XNOR gates using NOR gates only. Show the circuits in Figure D2 (Section D), clearly labeling the pin numbers.

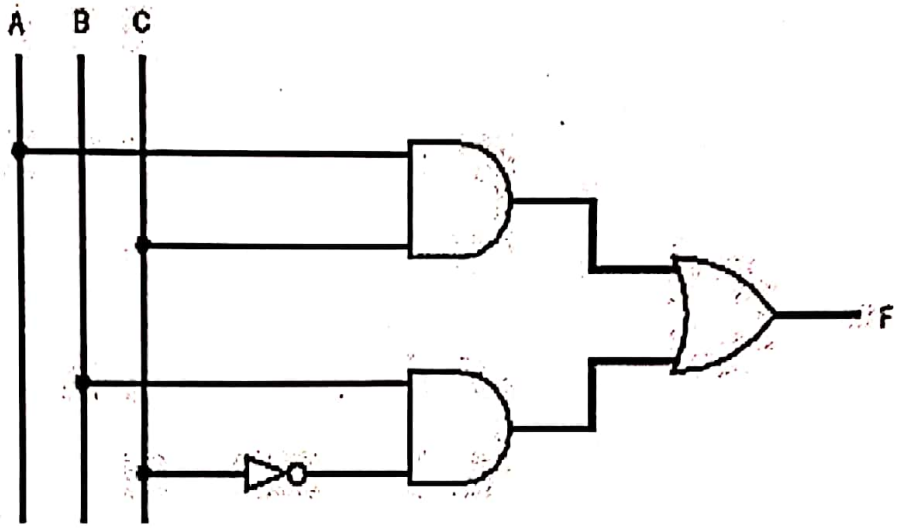


Figure B2: A combinational circuit

4. Complete the truth table for the circuit in Figure B2 in table D1 (Section D)
5. Convert the circuit in Figure B2 to a NAND gate equivalent circuit, showing the steps involved and clearly labeling the pin numbers in the final circuit design. Show your work in Figure D3 (Section D).
   (i) Replace each of the gates with its NAND gate equivalent in step 1.
   (ii) Identify any inversions that are compensated (i.e. one inverter followed by another) in step 1 and redraw the final circuit in step 2.
6. Validate the operation of the universal gate circuit from the truth table.

C. Report

2. Convert the combinational circuit of Figure B2 to a universal gate circuit using NOR gates only and simulate it using Logisim. You will need to convert the circuit to 2nd Canonical form and then minimize it before performing this conversion. Provide the Logisim circuit schematic with your report.

D. Experimental Data

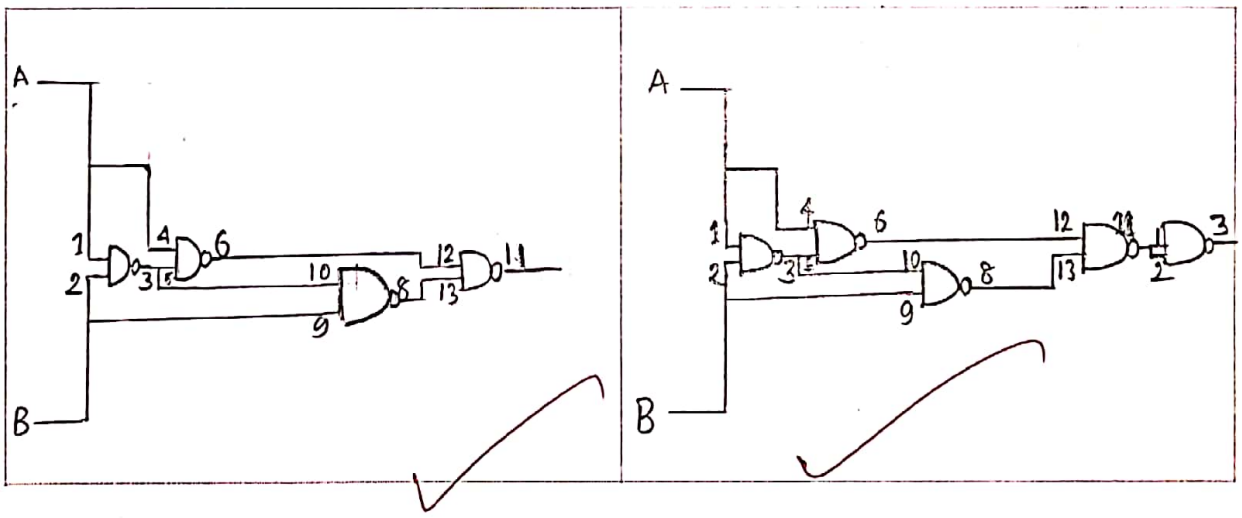


Figure D1: Implementation of XOR and XNOR using NAND gates

$\overline{A \cdot (\overline{A \cdot B})} \cdot \overline{B (\overline{A \cdot B})}$

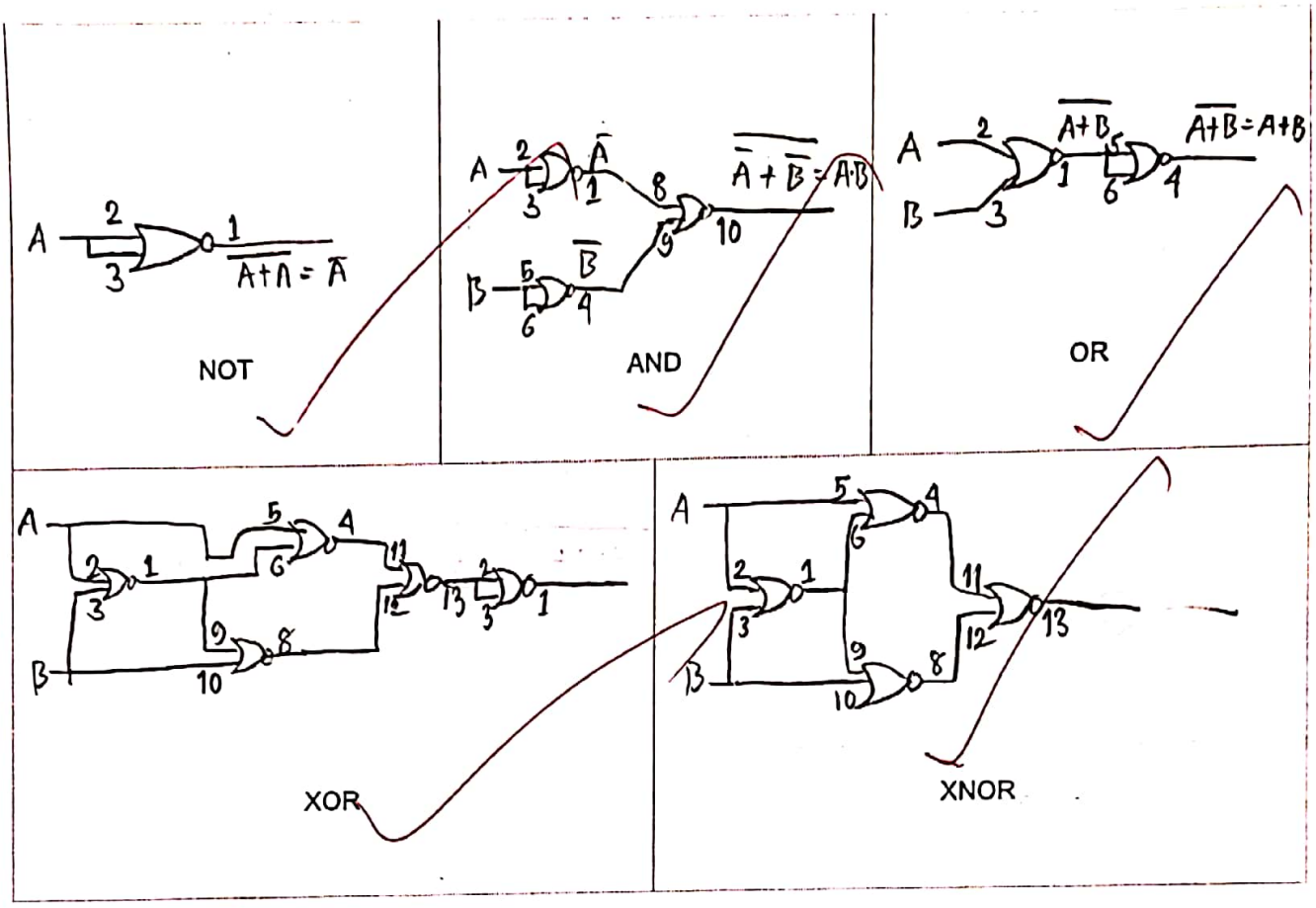


Figure D2: Implementation of NOT, AND, OR, XOR and XNOR using NOR gates

A B C	$I_1 = A\ C$	$I_2 = B\ C'$	$F = I_1 + I_2$
0 0 0	0	0	0
0 0 1	0	0	0
0 1 0	0	1	1
0 1 1	0	0	0
1 0 0	0	0	0
1 0 1	1	0	1
1 1 0	0	1	1
1 1 1	1	0	1

Table D1: Truth table of combinational circuit in Figure B2

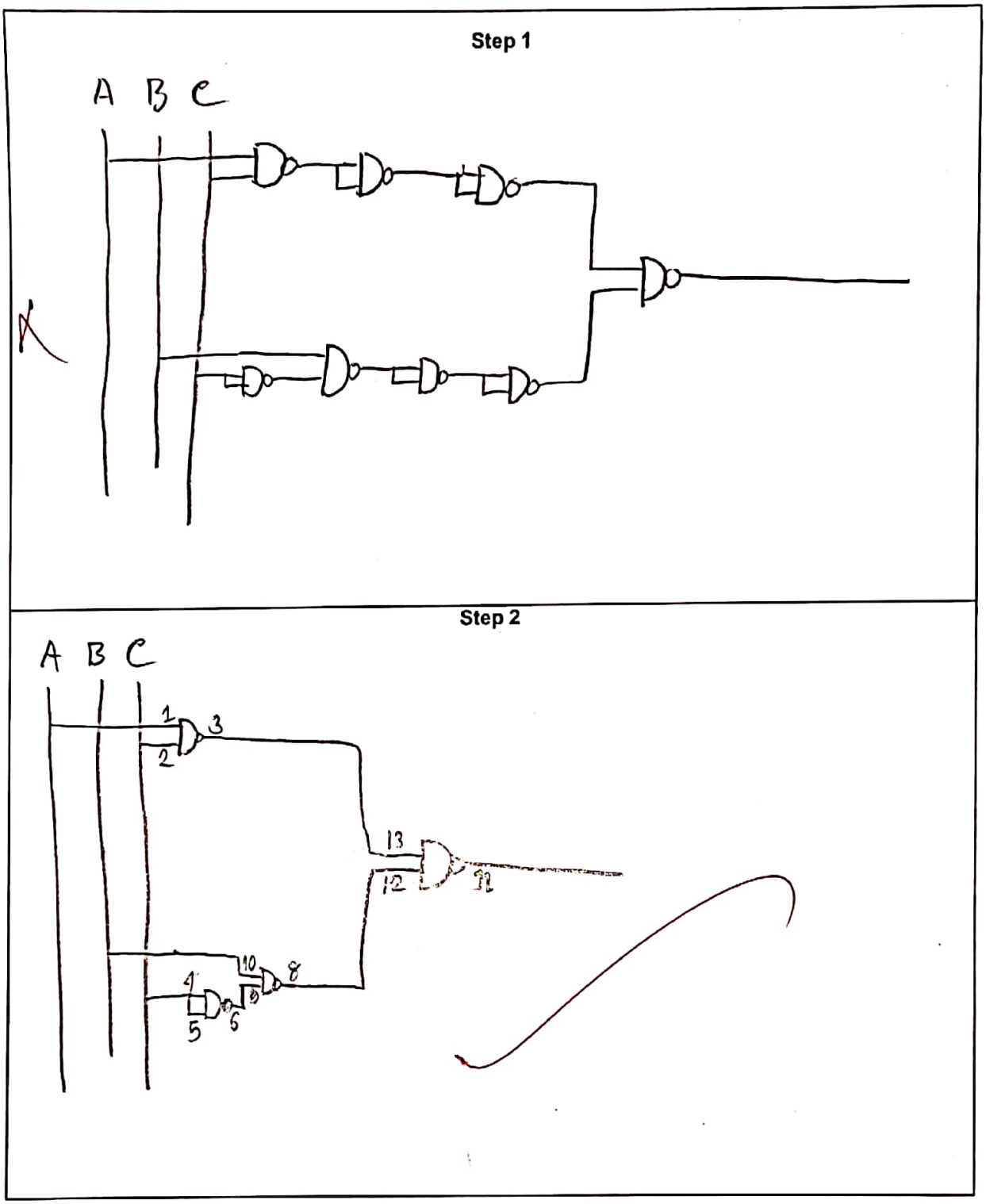


Figure D.3 Universal (NAND) gate implementation of the circuit of Figure B2

Prathika
20/3/24