North South University
Department of Electrical & Computer Engineering

LAB REPORT

Subject Name: Digital logic Design Lab

Experiment Number: 04

Experiment Name: Combinational logic design

Experiment Date: 26, 03, 24

Report Submission Date: 17, 04, 24

Section: 09

Group Number: 02

Student Name & ID:	Score:
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Objectives:

(i) Design a complete minimal combinational logic system from specification to implementation.

(ii) Minimize combinational logic circuits using Karnaugh maps.

(iii) Learn various numerical representation system.

(iv) Implement circuits using 1st and 2nd canonical forms.

List of Equipments:

- Trainer Board
- Logic gate ICs: 2 and 3 input AND, OR, NAN

Theory:

Karnaugh map or K-Map is a map method which is straightforward procedure for minimizing boolean functions. It is a pictorial form of truth table. K-map diagram is made up of squares with each square represents one minterm of the function that is minimized.

Don't care conditions are used on a map to provide further simplification of the boolean function. To distinguished they don't care condition x is used.

K-map of the table E-1:-

0	0	0	0
0	1	1	1
x	x	x	x
1	1	x	x

W = A + BD + BC

0	1	1	1
1	0	0	0
x	x	x	x
0	1	x	x

X = B'C + B'D + BC'D'

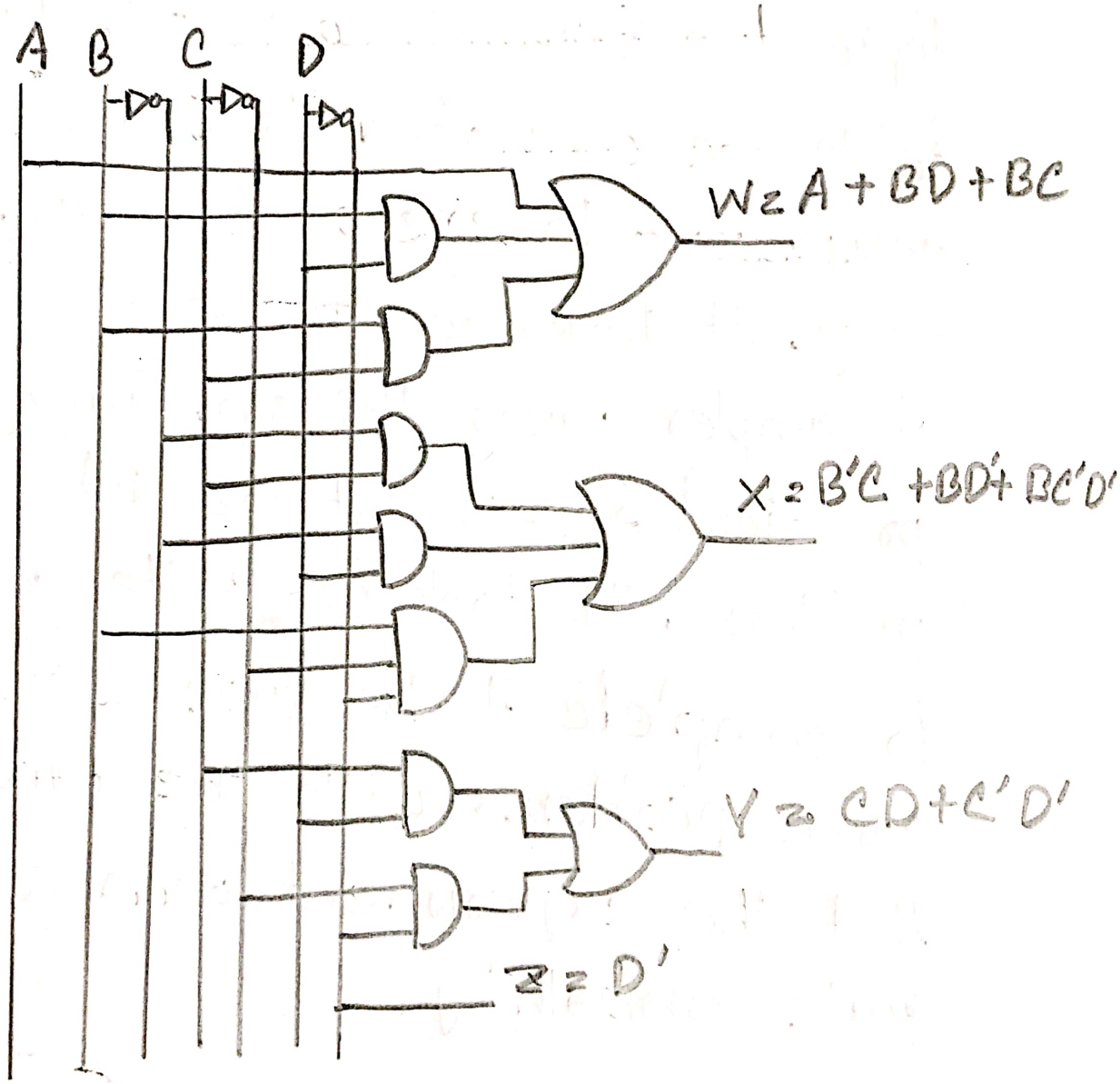
1	0	1	0
1	0	1	0
x	x	x	x
1	0	x	x

$Y = CD + C'D'$

1	0	0	1
1	0	0	1
x	x	x	x
1	0	x	x

$Z = D'$

Circuit Diagram:



Truth Table:

Binary Coded Decimal (BCD)				Excess-3			
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x

Discussion:

In this experiment we get to learn a new topic the Excess-3 converter. Using truth table we converted BCD codes to it's equivalent to excess-3 codes which was easy. It tooks us some time make it simpler using K-Map. During the practical experiment we did face some problems. It took us quite a while to complete it because we were facing some problems with the wire. Except that the experiment was completed quite smoothly.

Reference:

Class lecture
Google
Book

North South University
Department of Electrical and Computer Engineering
CSE 231L: Digital Logic Design Lab
Lab 04: Combinational Logic Design

A. Objectives

- Design a complete minimal combinational logic system from specification to implementation.
- Minimize combinational logic circuits using Karnaugh maps.
- Learn various numerical representation systems.
- Implement circuits using 1st and 2nd canonical minimal forms.

B. Apparatus

- Trainer board
- Logic gate ICs: 2- and 3-input AND, OR, NAND

C. Procedure

Design of BCD to Excess-3 converter: Design, minimize and implement a digital logic system where an input in binary coded decimal (BCD) in converted and displayed in Excess-3.

1. Complete the truth table (Table E1, Section E) for the BCD to Excess-3 converter.
2. Identify the inputs and outputs from the truth table and complete the system analysis (Table E2, Section E).
3. Complete the K-maps (Figure E1, Section E) to find the minimal 1st canonical functions of each output variable.
4. Draw the minimal circuit showing the pin configurations (Figure E2, Section E).
5. Implement and test the circuit on the trainer board.
   Connect the 4 inputs to the BCD inputs on the trainer board to display the input digits on the seven-segment display.
6. Convert, implement and test the circuit in the suitable universal gate format. Show the circuit with pin configurations (Figure E3, Section E).

D. Report

1. Design and simulate the minimal NOR logic implementation of Excess-3 to BCD converter.

E. Experimental Data

Binary Coded Decimal (BCD)				Excess-3			
A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Table E1: Truth table - BCD to Excess-3

Number of inputs bits:		**Input variables:**	
Number of outputs bits:		**Output variables:**	

Table E2: System analysis

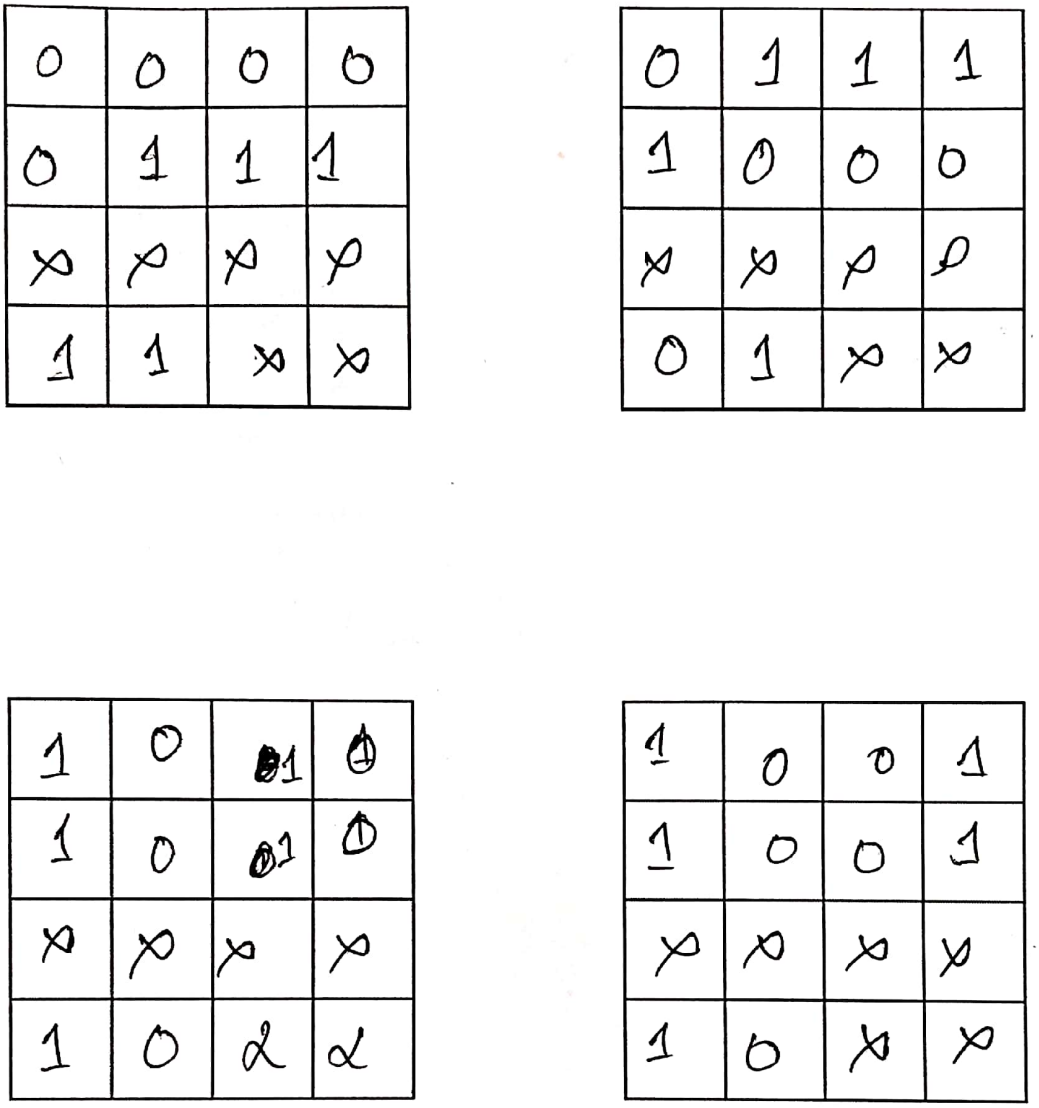


Figure E1: K-M

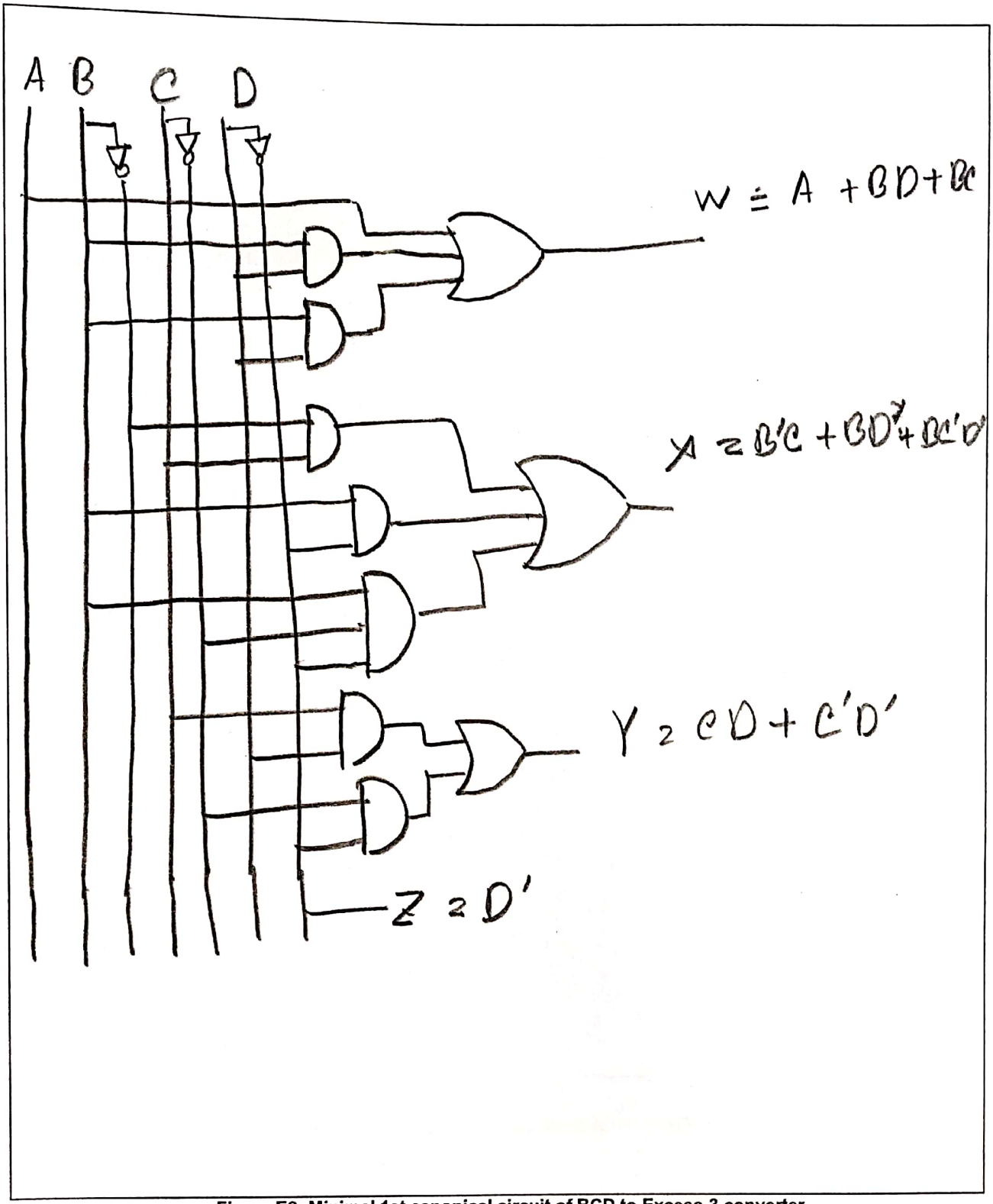


Figure E2: Minimal 1st canonical circuit of BCD to Excess-3 converter

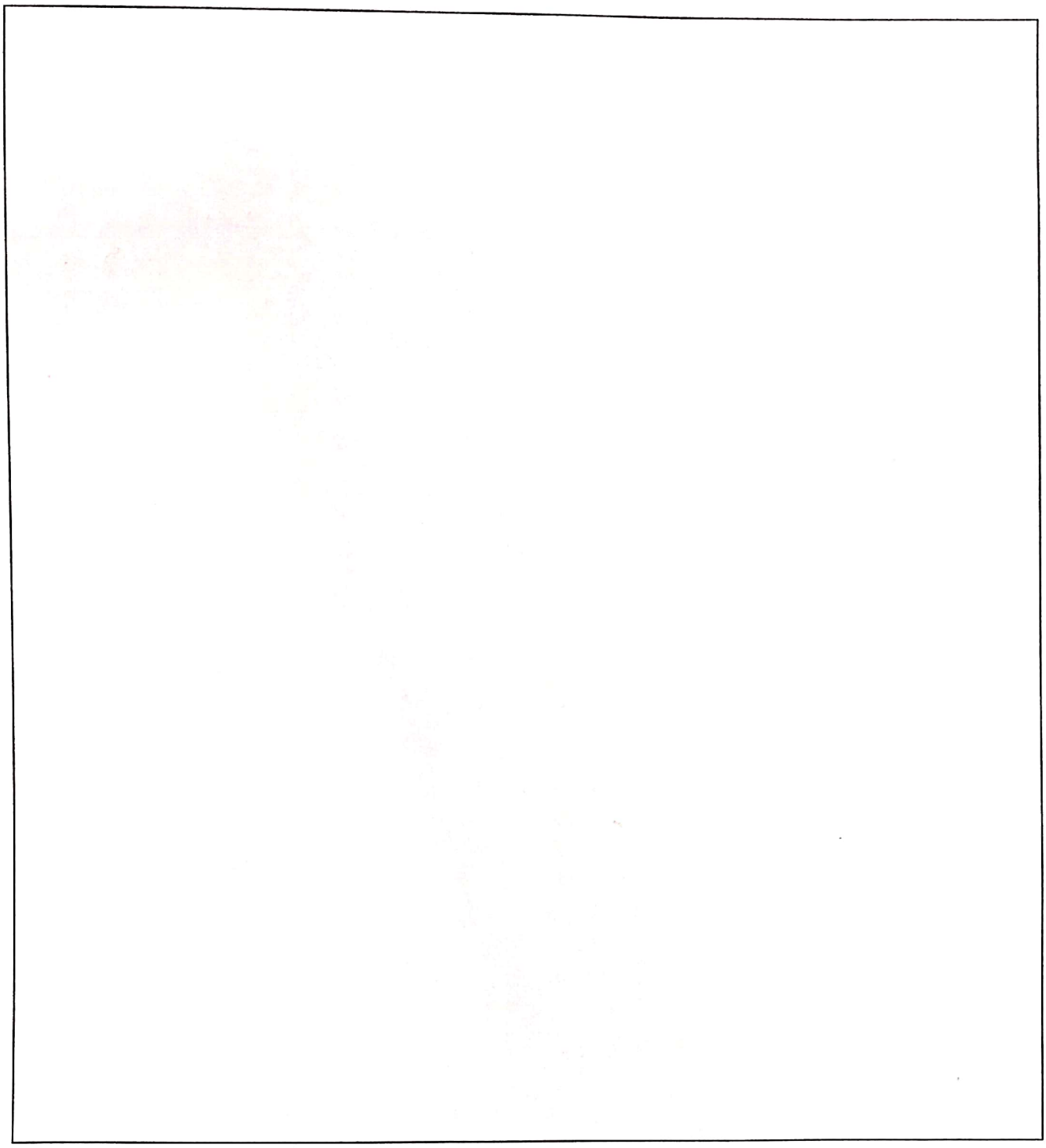


Figure E3: Minimal universal gate implementation of BCD to Excess-3 converter