North South University
Department of Electrical & Computer Engineering
LAB REPORT- 06

Course Code: CSE231L

Course Title: Digital Logic Design Lab

Section: 09

Lab Number: 03

Experiment Name:

Introduction to Multiplexers & 3 to 8 line Decoder

Experiment Date: 17th April, 2024

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Submitted by Group Number: *02*

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Experiment Name : Introduction to Multiplexers and 3 to 8 line Decoder.

Objectives :

① Recognize the multiplexing concept in relation to digital logic circuits
② Use multiplexers to implement digital logic functions
③ Acquire ~~knowd~~ knowledge of digital multiplexer's internal logic.
④ Examine and evaluate the 3 to 8 Line Decoder's functioning.

Apparatus :

① Trainer Board
② 1 x IC 7404 Hex Inverter
③ 2 x IC 4073 3-input AND gates
④ 1 x IC 7432 2-input OR gates
⑤ 1 x IC 74151 (8:1 Multiplexer)
⑥ 1 x IC 74138 (3:8 Line Decoder)
⑦ Connecting wires

Theory :

□ Multiplexer : A multiplexer (often abbreviated as MUX) is a combinational circuit that selects one of several data inputs and forwards it to the output.

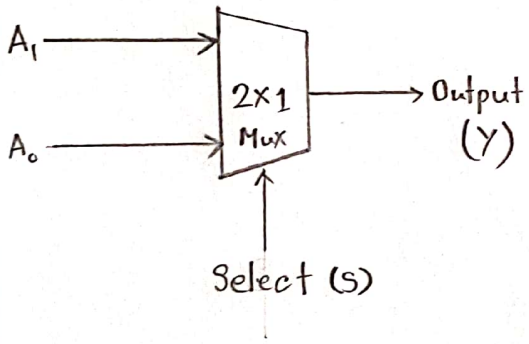
Multiplexer has 2^n input lines and a single output line. And multiplexer consists of 'n' selection lines.

Example : 8 x 1 Multiplexer
16 x 1 Multiplexer etc

2 x 1 Multiplexer

In 2x1 multiplexer, there are two inputs, i.e., A_0 and A_1, one selection line i.e., S_0 and a single output, i.e., Y.

Block Diagram :

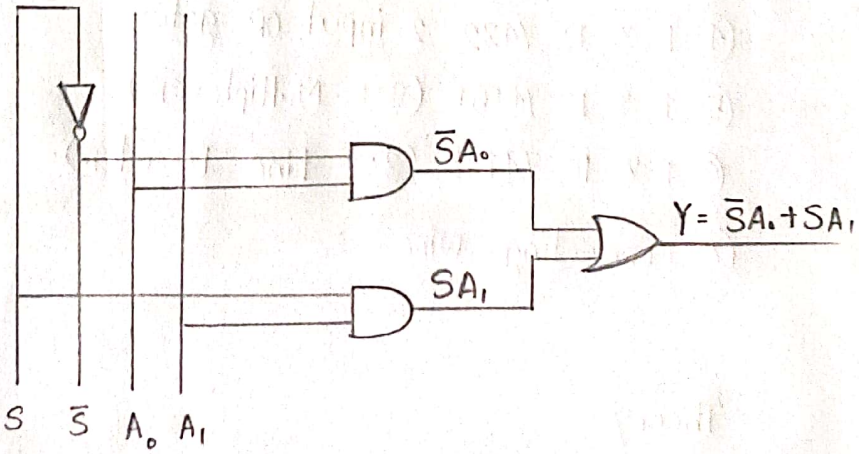


Truth Table :

Select (S)	Output (Y)
0	A_0
1	A_1

Here, $Y = \bar{S}A_0 + SA_1$

Logic Circuit :



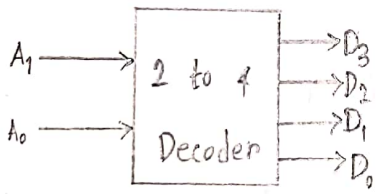
☐ Decoder: Decoder is a combinational circuit that has 'n' input lines and maximum of 2^n output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. This means decoder detects a particular code.

Example : 2 to 4 Decoder
3 to 8 Decoder etc.

2 to 4 Decoder:

In 2 to 4 decoder, there are two inputs A_1 and A_0 and four outputs Y_3, Y_2, Y_1 and Y_0.

Block Diagram:



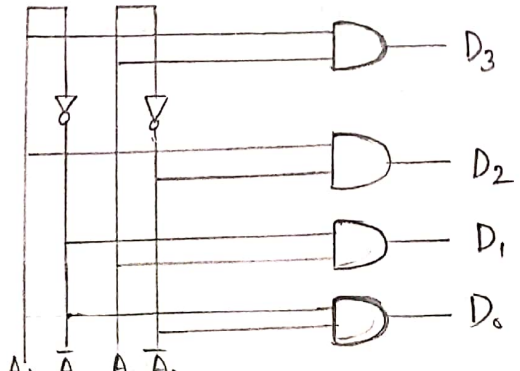
Truth Table:

Inputs		Outputs			
A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

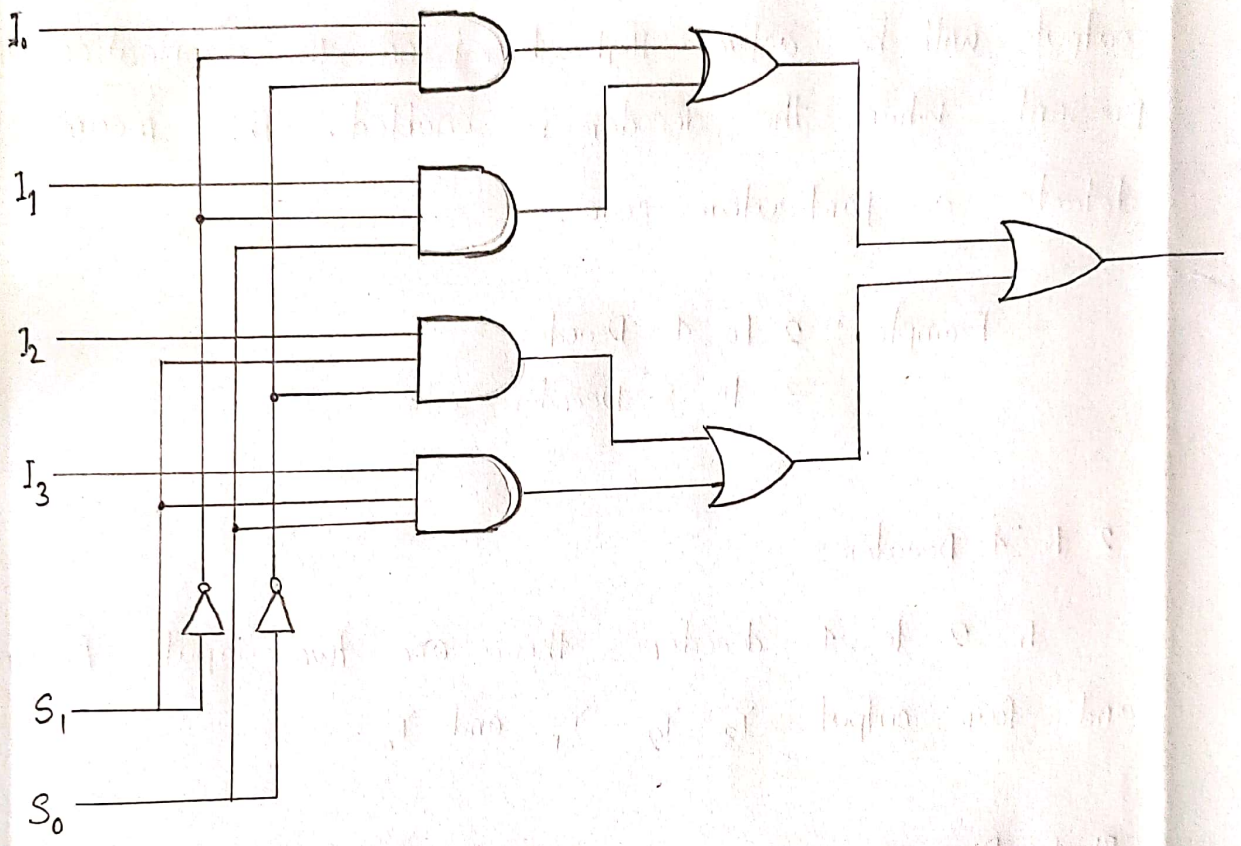
Here, $D_3 = A_1 A_0$ $\quad D_1 = \overline{A}_1 A_0$

$D_2 = A_1 \overline{A}_0$ $\quad D_0 = \overline{A}_1 \overline{A}_0$

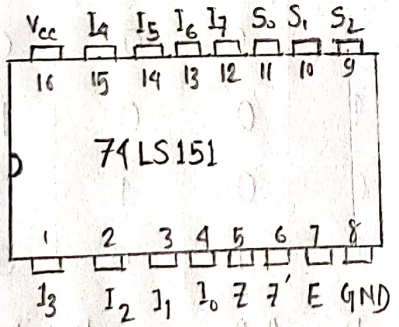
Logic Circuit:



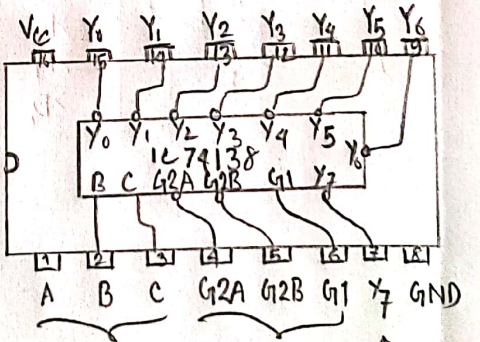
Circuit Diagram :



Logic circuit for JOB-1



Pinout of IC74151



Pinout of IC74138

Experimental Procedure :

JOB 1

① Our task is to implement this function using 4:1 MUX circuit diagram of

$$F(A,B,C) = \Sigma(0,1,5,7)$$

$$= m_0 + m_1 + m_5 + m_7$$

② First we have to find out which MUX to use.

In function, number of variables = 3

$\therefore n$ = variable - 1

= 3 - 1 = 2

Here, 2 is the number of select lines.

$\therefore$ For, Mux = $2^n = 2^2 = 4$

So, we will ~~used~~ use 4:1 mux.

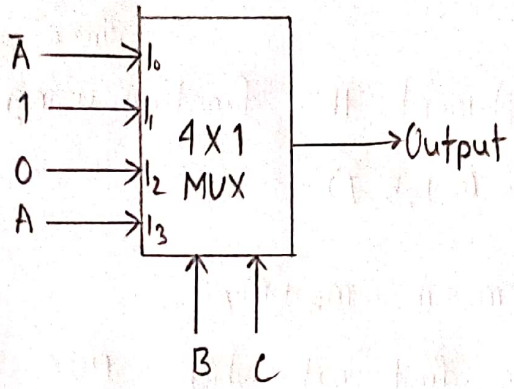
③ Then we ~~will~~ made table - 01 for all combinations.

④ Since A is given as input bit, our next step -

	I_0	I_1	I_2	I_3
$\bar{A}$	(0)	(1)	2	3
A	4	(5)	6	(7)
	$\bar{A}$	1	0	A

We filled this data inputs in table -1. And we are considering B and C as select bit.

Block Diagram :



necessary gates and circuit diagram of

⑤ Then we implemented the circuit using 4:1 MUX. And checked all the possible inputs using data table - 01.

JOB 2

① Our task was to implement following function using 8:1 MUX.

$$F(A,B,C,D) = \Sigma(0,1,3,5,8,9,14,15)$$
$$= m_0 + m_1 + m_3 + m_5 + m_8 + m_9 + m_{14} + m_{15}$$

② First we have to find out which MUX to use.

In this function, number of variable = 4

$$\therefore n = \text{variable} - 1$$
$$= 4 - 1$$
$$= 3$$

Here, 3 means the number of the select line.

$$\therefore \text{For Mux}, 2^n = 2^3 = 8$$

So, we will use 8:1 MUX.

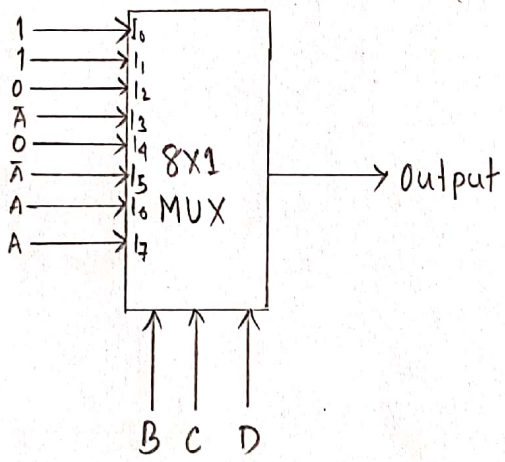
③ Then we made table - 02 for all combinations.

④ Since we have to keep A as input bit, our next step -

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	(0)	(1)	2	(3)	4	(5)	6	7
A	(8)	(9)	10	11	12	13	(14)	(15)
	1	1	0	$\bar{A}$	0	$\bar{A}$	A	A

We filled this data inputs in table - 2. And we are considering B, C and D as select bit.

Block Diagram :



⑤ Then we implemented the circuit using 8:1 MUX. And checked all the possible inputs using data table - 02.

JOB 3

By using necessary guides, we wired up the IC 74138 to start our task-03, 3 to 8 line decoder. Then set the necessary values for the Enable inputs. Both G2A and G2B should be set to low, while G1 should be set to high. Then, we wired up three inputs (C B A) to three binary switches, and the eight outputs to individual LEDs. Then, we tested our circuit using Function Table from lab manual.

Experimental Data Table :

A	B	C	F (Theoritical)	Data Inputs	F (Practical)
0	0	0	1	$I_0 = \bar{A}$	1
0	0	1	1		1
0	1	0	0	$I_1 = 1$	0
0	1	1	0		0
1	0	0	0	$I_2 = 0$	0
1	0	1	1		1
1	1	0	0	$I_3 = A$	0
1	1	1	1		1

Table 01 : Truth Table for 4:1 Multiplexer

A	B	C	D	F (Theoritical)	Data Inputs	F (Practical)
0	0	0	0	1	$I_0 = 1$	1
0	0	0	1	1		1
0	0	1	0	0	$I_1 = 1$	0
0	0	1	1	1		1
0	1	0	0	0	$I_2 = 0$	0
0	1	0	1	1		1
0	1	1	0	0	$I_3 = \bar{A}$	0
0	1	1	1	0		0
1	0	0	0	1	$I_4 = 0$	1
1	0	0	1	1		1
1	0	1	0	0	$I_5 = \bar{A}$	0
1	0	1	1	0		0
1	1	0	0	0	$I_6 = A$	0
1	1	0	1	0		0
1	1	1	0	1	$I_7 = A$	1
1	1	1	1	1		1

Table 02 : Truth Table for 8:1 Multiplexer

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Results:

We got the outputs according to the Truth Table/ Function Table.

Dissecussion : We learned about multiplexers and decoders in this lab. Any circuit can be converted to a multiplexer - implemented circuit. A multiplexer is a device that accepts numerous inputs but produces only one output. And decoder is a multiple - input, multiple - output logic circuit that converts coded inputs into coded outputs.

Our task - 01 was to build a 4:1 multiplexer. We implemented function, $F(A,B,C) = \Sigma(0,1,5,7)$ using 4:1 MUX. Using data table we also verified the experiment. All the outputs was accurate. In our task - 02, we built, $F(A,B,C,D) = \Sigma(0,1,3,5,8,9,14,15)$ using 8:1 MUX. And we also checked the outputs using data table - 02. In task - 03 we implemented 3 to 8 line decoder by using IC 74138. We checked the outputs using the given function table in Lab Manual.

In this lab, we didn't faced any kind of faultness in IC. All IC worked well. Sometimes we faced problem during applying inputs because of the bad behaviour of input switches in the Analog and Digital Training System.

Moreover, this lab has helped us get to know Multiplexers and Decoders practically and enriched our knowledge of digital logic design.