North South University
Department of Electrical & Computer Engineering
LAB REPORT-

Course Code: CSE 2311

Course Title: Digital Logic Lab

Section: 9

Lab Number: 8

Experiment Name:

Flip-Flops and Shift Registers

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Experiments Name: Introduction to Flip-Flops and Shift Registers.

Objective : • Learn the concepts of states in digital logic and how flip-flop circuit can be used to store state information.

• Understand the relation between J-K Flip-Flops, T and D Flip-Flops and observe the characteristics of all three.

• Implement a shift register using D Flip-Flops and analyze its appt operation

Apparatus; 1 x IC 7402 2-Input NOR gate.
1 x IC 4073 3 Input AND gates
1 x IC 7404 Hex Inverter
2 x IC 7474 (D Flip-Flop)
Trainer Board
Wires

Theory: Flip-Flops are essential componets for storing data in digital circuit. Flip-Flop has input, output and a clock input. Clock signal determines when its state based inputs are updated. There are D, T, JK Flip-Flops. These have two states 'set' and 'reset'. Flip-Flop used in sequential circuits like registers, counter, memory elements. They are reqired in applications such as computer processor, control, communication system, where data is synchorized and manupulation is required

In JK flipflop the combination $J=1, k=0$, is a command to set the flip-flop. And $J=0, k=1$ is a command to reset the flipflop ($Q=0$); The command $J=1, k=1$ is a command to toggle the flip-flop. like change val output to the logical complement of its current value. Setting $J=0, k=0$ maintains current state.

Characteristic Table		
J	k	Q_{next}
0	0	Q
0	1	0
1	0	1
1	1	$\bar{Q}$

Excitation Table			
Q	Q_{next}	J	k
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

JK Flip-Flop characteristic & Excitation Table

T Flip Flop changes states ("toggles") whenever the input T is high and clock input is stored. If the T input is low, the flip-flop holds the previous value when given a clock pulse.

characteristic		Excitation		
T	Q_{next}	Q	Q_{next}	T
0	Q	0	0	0
		0	1	1
1	$\bar{Q}$	1	0	1
		1	1	0

T flip flop characteristic and Excitation Table

The D flip-flop captures the value of the D-input at a definite portion of the clock. That capture value becomes the Q output. At other time output Q does not change.

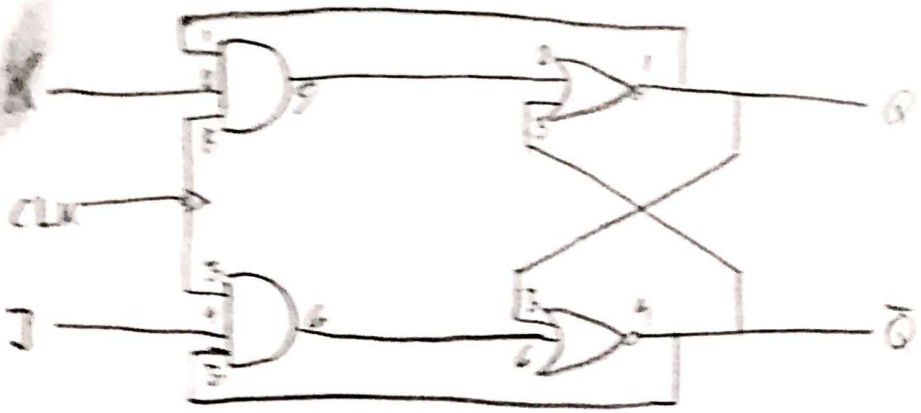
characteristic			Excitation		
D	Q_{next}		Q	Q_{next}	D
0	0		0	0	0
			0	1	1
1	1		1	0	0
			1	1	1

D flip-flop characteristic and excitation Table

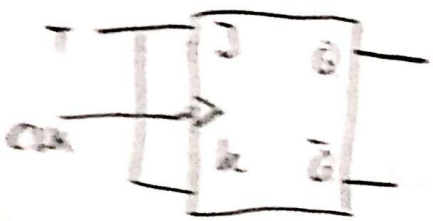
Register:

Register is a component of digital circuit used to store and manipulate binary data. It consists of multiple flip-flops connected. It can store multiple bits of data simultaneously and retain their values until updated. They are commonly used for temporary storage, data transfer between different parts of a digital system. A register that can shift right or left its binary information is called a shift register. All flip flop receive a common pulse causes the shift from one stage to the next

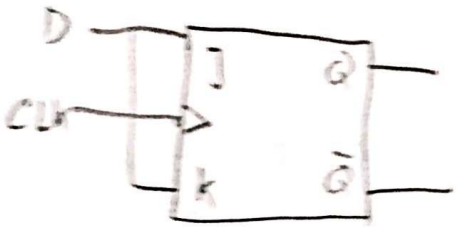
Circuit Diagram:



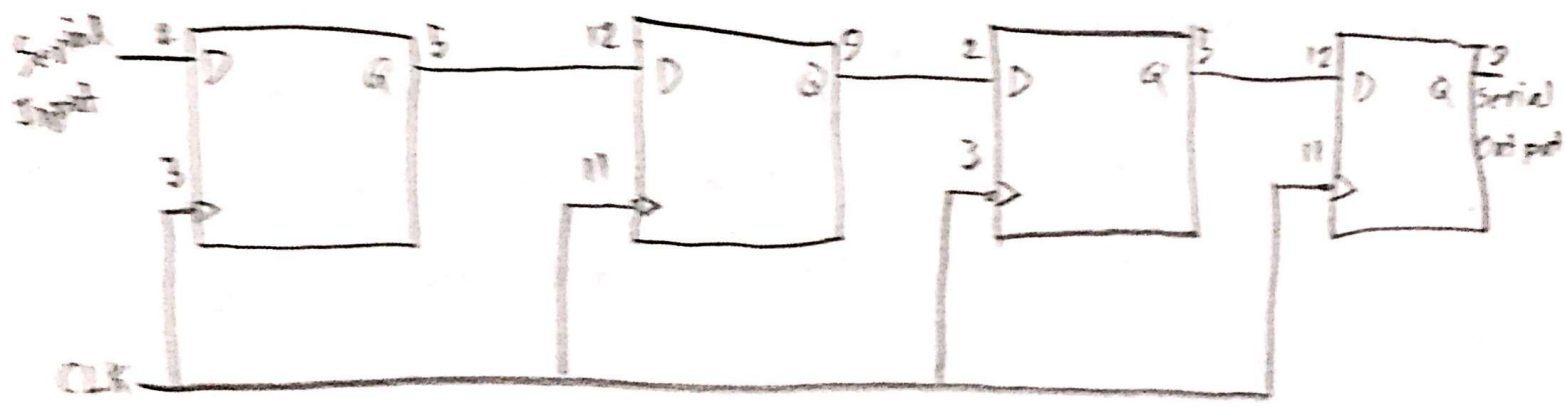
JK Flip Flop using AND & NOR gate



T flip-flop using JK



D flip-flop using JK



Right Shift Register

Experimental Procedure:

Experiment 1:

i. First we build the circuit for th J-k flipflop a the p diagram shown in the circuit Diagram Section.

ii. Complete the truth table according to the characteristic of J-K Flip-Flop.

iii. After that we set both J and K to 0, set J to 1., again set J and K to 0. Finally set both J and K to 1.

Experiment 2:

i. For this we need some minor change to our previously buiH circuit J-K.

ii. The we set the inputs and clock pulse as the truth table to T flip flop.

iii. Then we connect T flip flop into D flipflop by adding a Not gate between the connection from J to K.

iv. After that set the input values as D flip flop table.

Experiment 3:

i. First we complete the truth table for Right shift register.

ii. we Construct the truth table as the pin diagram shown in the circuit. We initial all the se and reset pin by giving a constant input of 1.

iii. After implementing we give input values as the of truth table

Experiment Data table:

J	K	Q	$\bar{Q}$
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	1	0
1	0	1	0
1	0	1	0
1	1	0	1

JK Flip-flop using AND and NOR gates

T	Q
0	0
1	1

D	Q
0	0
1	1

T and D Flip-Flops

Status	Input	Output
Initial state	X	X X X X
T_1	1	1 X X X
T_2	0	0 1 X X
T_3	1	1 0 1 X
T_4	0	0 1 0 1

Result: A our every truth table and output data matched with characteristic table and excitation table of JK, D, T Flipfop, we can assume that we have successfull completed the experiment.

Discussion:

From this experiment we learned a lot abot the characteristics and excitation for JK, T and D flipflop. As we observe the behaviour we learn we need these Flip Flop is digital logic. We learn to construct using D Flip Flop. We also built JK flip flop using basic gate. we know basic relation between and difference between these three flip flop. In this experiment we didn't faice a litte problem due to faulty wires and compronent, but we completed this experiment