North South University
Department of Electrical & Computer Engineering
LAB REPORT-

Course Code: CSE 231

Course Title: Digital Logic Lab

Section: 9

Lab Number: 5

Experiment Name:

Binary Arithmetic

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Submitted by Group Number: 02

Group members

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1: LAB 5 : Binary Arithmetic

2A. Objectives

- Minimize combinational logic circuits using Karnugh map.
- Learn various numerical representation system.
- Implement circuits using 1st and 2nd canonical minimal forms.
- Implement circuits using universal logic.

3. Theory : Binary adder performs binary addition on the A and B input and the carry output CO. It generates a 4 bit sum and a carry out C4. It can be Half Adder which is a fundamental building block of a binary adder. It adds two single digit binary numbers and produces two output. The sum (S) and the carry (C). ICs like the 7400 seris often contain integrated half adder circuits. Another one is full adder, while a half adder can add two bits, it cannot contain account for a carry from a previous addition. A full adder, built using multiple half adder and additional logic gates, can handle three inputs: two bits to be added and a carry from the previous lower significant bit addition.

Two 7483 ICs can be cascaded to form an 8-bit

ripple through - carry adder. The lower 4-bits of each number is used as input for the first 7483 and the output carry is connected to the input carry of the next 7483. The higher 4 bits of the sum and the second one provides the upper 4-bits.

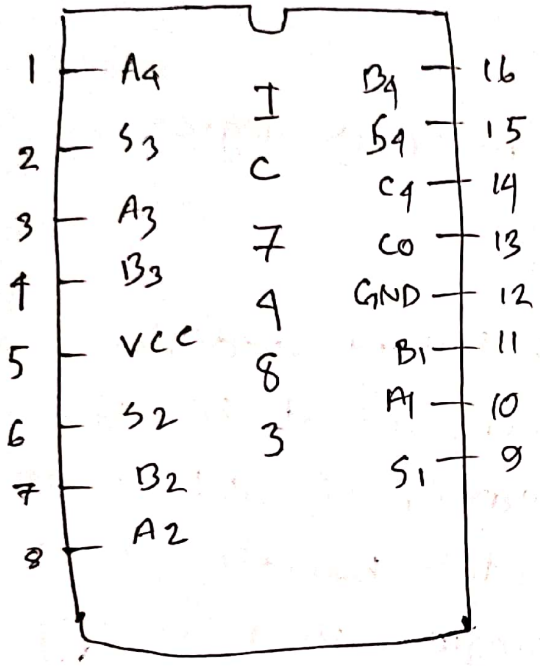


Figure: Pinout of IC7483

Apparatus:

Experiment 1: Binary Adder – Subtractor

- Traine Board
- 1X IC7483 4-bit binary Adder
- 1X IC 7486 quadruple 2-input x-OR gates

Experiment-2: Ripple-Through-Carry Adder

- Traine Board
- 2 XIC 7483 4-bit binary Adder

Experiment-3: BCD Adder

- Trainer Board
- 2X IC 7483 4 bit binary adder
- 1X IC 7408 quadruple 2-input AND gate
- 1XIC 7432 quadruple 2-input OR gate.

Experimental Data: Binary Adder - subtractor

Operation	M	A	B	C_4	S_4 S_3 S_2 S_1
7+5	0	0111	0101	0	1 1 0 0
4+6	0	0100	0110	0	1 0 1 0
9+11	0	1001	1011	1	0 1 0 0
15+15	0	1111	1111	1	1 1 1 0
7-5	1	0111	0101	0	0 0 1 0
4-6	1	0100	0110	1	1 1 1 0
11-2	1	1011	0010	0	1 0 0 1
15-15	1	1111	1111	0	0 0 0 0

table: E.1.1

Experimental Data (Ripple - Through - Carry - Adder) :

Operation	A	B	overflow carry	Sum
7+5	00000111	0000 0101	0	00001100
18 +19	0001 0010	0001 0011	0	0010 0101
72+83	0100 1000	0101 0011	0	1001 1011
129+255	10000001	1111 1111	1	1000 0000

Experimental Data (BCD sum)

Binary Sum						BCD Sum			
K	Z_8	Z_4	Z_2	Z_1	C	S_8	S_4	S_2	S_1
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	1	0	0	0	0
0	1	0	1	1	1	0	0	0	1
0	1	1	0	0	1	0	0	1	0
0	1	1	0	1	1	0	0	1	1
0	1	1	1	0	1	0	1	0	0
0	1	1	1	1	1	0	1	0	1
1	0	0	0	0	1	0	1	1	0
1	0	0	0	1	1	0	1	1	1
1	0	0	1	0	1	1	0	0	0
1	0	0	1	1	1	1	0	0	1

Experimental Procedure:

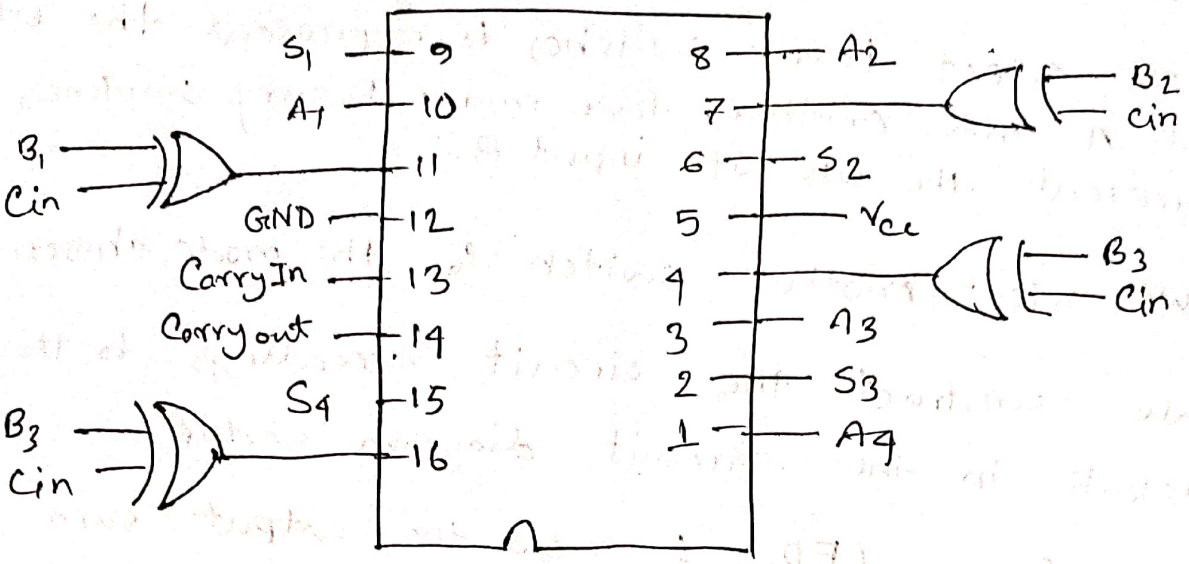
Binary Adder Subtractor:

1. First we select four switches to represent the bits of input A and Another four more binary switches to represent the bits of input B.
2. Then we select another switch for the mode chosen.
3. Then we construct the circuit accordings to the pin details in the circuit diagram section.
4. we chose foure LEDs, to view the output sum and another LED for the output carry.
5. we Test the circuit with the data in table for the BCD Sum.

BCD Adder:

1. Fisrst we complete tabe F.2.1. and F2.2 for the BCD sum.
2. Then we construct the circuit.
3. we use the first adder output as the input of the second adder.
4. we built the circuit according to the pin details shown In circuit D.2.2.
5. Then we test the circuit with data In table: F.2.2

Circuit Diagram :



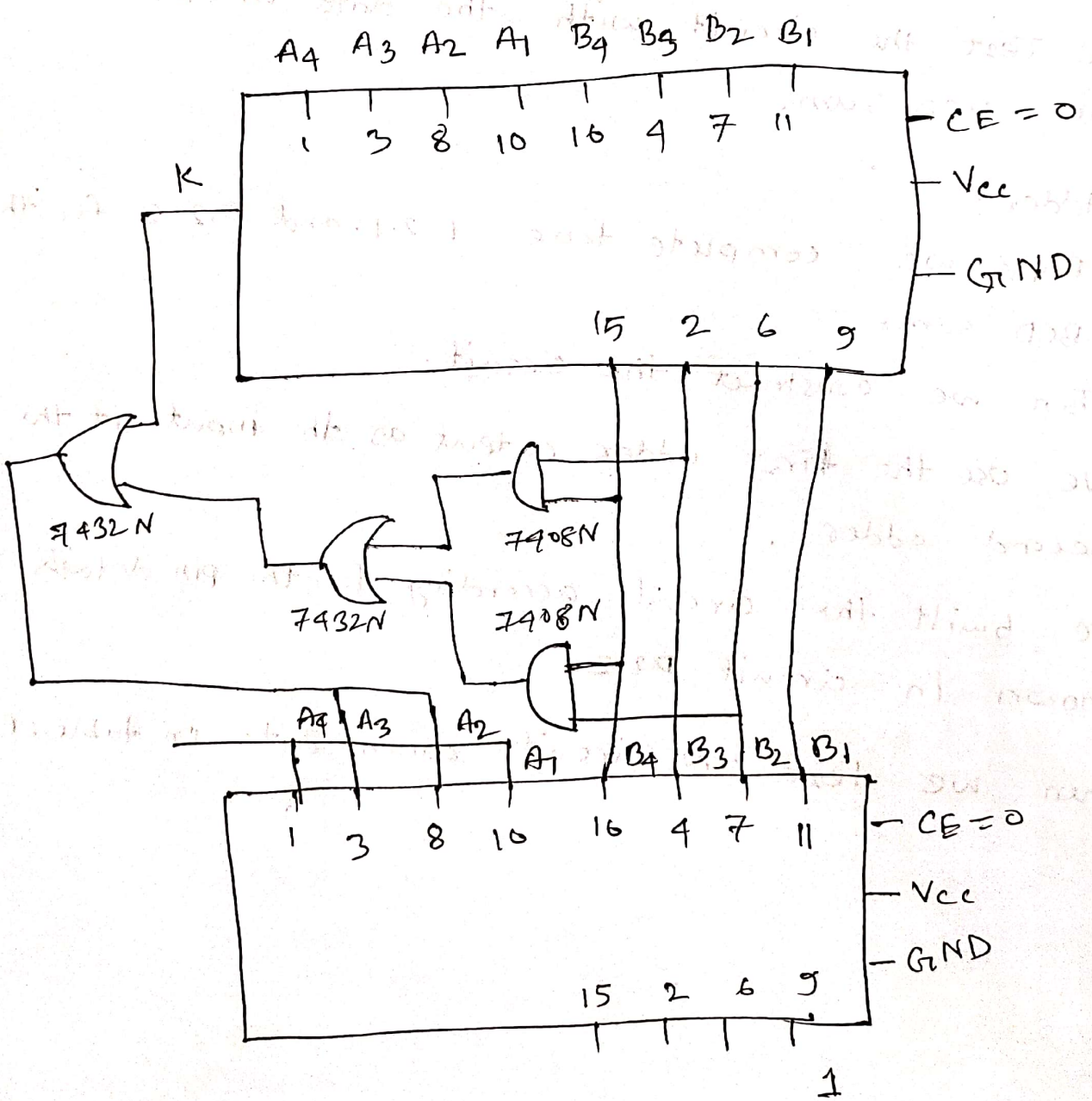


Figure : D.2.1 ; BCD Adder Circuit

Operation	A	B	Overflow Carry	Sum
9+0	1001	0000	0	1001
9+1	1001	0001	1	0000
9+2	1001	0010	1	0001
9+3	1001	0011	1	0010
9+4	1001	0100	1	0011
9+5	1001	0101	1	0100
9+6	1001	0110	1	0101
9+7	1001	0111	1	0110
9+8	1001	1000	1	0111
9+9	1001	1001	1	1000

table : F.2.2

Result:

After implementation of our circuits, we test it with the data table F.1.1, F.2.1 ; and we get the exact output as the table.

Question and Answere:

01. In this exeperiment, we use XOR gates for the input of B to converted in the first complements and then we use the M bit as carryin, to convert the B to the seconds complements.

According the truth table, when M bit is 0, the inputs of B will not change. And when the M bit is 1, inputs of B will convert. We know that for the subtractor, we need to convert the negative number to second compliments then we can add and get the final result.

input		output
A	B	
0	0	0
0	1	1
1	0	1
1	1	0

X-OR Gate

Discussion: Through this experiment, we understand the concept of binary addition and subtraction. We can use half and Full Binary Adders. We can do addition and subtraction by using this adder. We also learn the concept of BCD sum. In the first part, our circuit was unable to do subtractor, But then we identify that the adder IC was damaged. Then we replace it and get the accurate result. In the second part we didn't ~~get~~ face any problem and complete within time. In short we learned about the adder and subtractor circuits.