

# North South University

### Department of Electrical & Computer Engineering

#### Lab Report

**Experiment No:** 

04

**Experiment Title:** 

Design of a 3-bit Binary Up-Down counter

Course Code:

CSE332L

Section:

07

Course Name:

Computer Organization & Architecture Lab

Lab Group #:

02

Written By:

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Date of Experiment:

27.02.2025

Date of Submission:

13.03.2025

| <b>Group Members ID:</b>      | Group Members Name: |  |  |
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### Objective:

1) To build and understand the behaviour of an up-down counter.

## Equipments List:

- · Trainer Board
- IC 7404 (Not Grate), IC 7408 (AND Grate), IC 7432 (OR Gate)
  IC 7486 (XOR gate), IC 7474 (D-tlipflop)
- · wires
- · Power supply.

# Block Diagram:

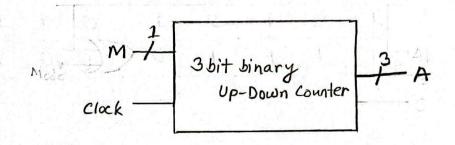


Fig: Block Diagram of 3-bit Up-Down Counter

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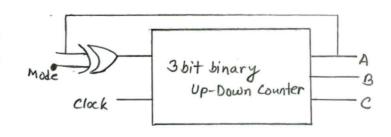


Fig: Block Diagram of 3-bit Up-Down Counter

Truth table:

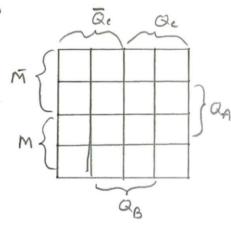
| Μ | O.c | Q <sub>B</sub> | QA | Qt   | Qi | Q+ | Te | To | TA |
|---|-----|----------------|----|------|----|----|----|----|----|
| 0 | 0   | 0              | 0  | 0    | 0  | 1  | 0  | O  | 7  |
| 0 | 0   | 0              | 1  | 6    | 1  | 0  | O  | 1  | 3  |
| 0 | 0   | 4              | 0  | 0    | ٦  | _1 | 0  | O  | 1  |
| 0 | 0   | 1              | 1  | 1    | 0  | 0  | 1  | 1  | 1  |
| 0 | 1   | 6              | ٥  | 1    | 0  | 1  | 0  | 0  | 7  |
| 0 | 1   | 0              | 1  | _1 . | ١  | 6  | 0  | 1  | 1  |
| 0 | 1   | 1              | 0  | 1    | 1  | J  | 0  | 0  | 1  |
| 0 | 1   | 1              | J  | 0    | 0  | 0  | 1  | 1  | 1  |
| 1 | 0   | 0              | 6  | _1   | 1  | 1  | _1 | 1  | 1  |
| 1 | 0   | 0              | 1  | 0    | g  | 0  | 0  | 0  | נ  |
| 1 | 0   | 1              | 0  | 0    | 0  | 1  | ಲ  | 1  | 1  |
| 1 | 0   | 1              | 4  | O    | 1  | 0  | 0  | 0  | J  |
| 1 | 1   | 0              | 0  | 6    | 1  | 2  | 1  | 1  | J  |
| 1 | 1   | 0              | 4  | 1    | 9  | 0  | O  | 0  | 1  |
| 1 | 1   | 1              | Ø  | 1    | 0  | 1  | O  | 1  | 1  |
| 1 | 1   | 1              | 1  | 1    | 1  | D  | 0  | ð  | 1  |

#### K-Map:

| /   | 00 | 01 | 11 | 10 |   |
|-----|----|----|----|----|---|
| 00  | 0  | 1  | 1  | 0  |   |
| 01  | 0  | 1  | 1  | 0  |   |
| 11- | 1  | 0  | 0  | 1  | - |
| 10  | 1  | 0  | 0  | 1  | _ |

$$T_B = M\overline{Q}_B + \overline{M}Q_B$$
  
=  $M \oplus Q_B$ 

| /  | 00  | 01 | . 11 | 10 |
|----|-----|----|------|----|
| 00 | 0   | 0  | 1    | 0  |
| 01 | 0   | 0  |      | 0  |
| П  | (1) | 0  | 0    | 0  |
| 10 |     | 0  | 0    | 0  |



#### Boolean Expression :

#### Circuit Diagram:

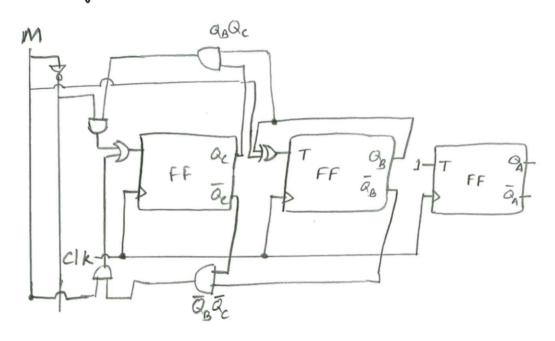
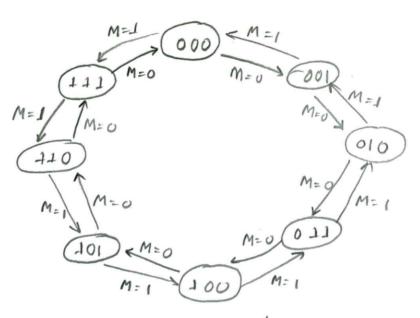


Fig. 3-bit up-down counter

# State Diagram:



Mode, M=0; + up count Mode, M=1; + down Count